1201 MPP

Understanding the PIC® MCU Product Portfolio

Class Objectives

- Learn the fundamental characteristics about Microchip's different 8, 16 and 32-bit architectures
- Describe the different levels of peripheral and product offerings for each specific architecture
- Describe the hardware and software tools available for use with all of Microchip's PIC® microcontrollers

Class Agenda

- 8-bit overview
- 16-bit overview
- 32-bit overview

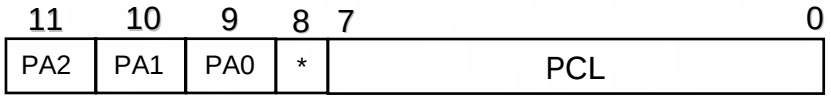
Baseline

PIC10F	PIC12F	PIC16F
PIC10F2XX	***PIC12F5XX***	***PIC16F5XX***
	PIC12F6XX	PIC16FXXX
	PIC12F1XXX	PIC16F1XXX
6-pin PIC® MCU	8-pin PIC MCU	≥14-pin PIC MCU
2.0-5.5V 4/8 MHz	2.0-5.5V 4/8 MHz	2.0-5.5V Up to 20 MHz

Baseline Architecture

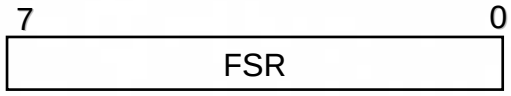
- **Harvard Architecture**
  - 12-bit wide instruction word
  - 8-bit wide data byte
- **Instruction Set Features**
  - 33 instructions
    - 4 clocks per instruction cycle
    - Most instructions are one cycle
  - 20 MHz maximum clock rate (5 MIPS maximum)
- **1 8-bit Working (W) Register**
  - Data use only
- **Hardware Stack**
  - 2 levels deep
- **Interrupts**
  - Does not support interrupts – uses resets and polling

Baseline Programmer's Model



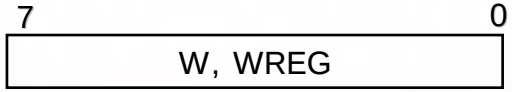
Program Counter (12-bit)

*** - Determined by type of opcode**
No direct access to the entire PC

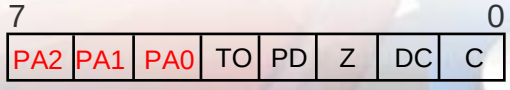


File Select Register

Indirect File Addressing Register



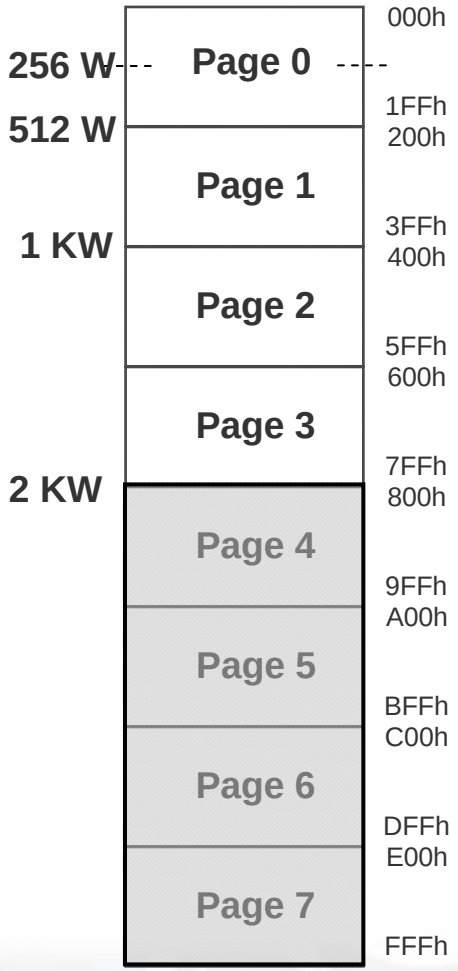
Working Register



STATUS Register

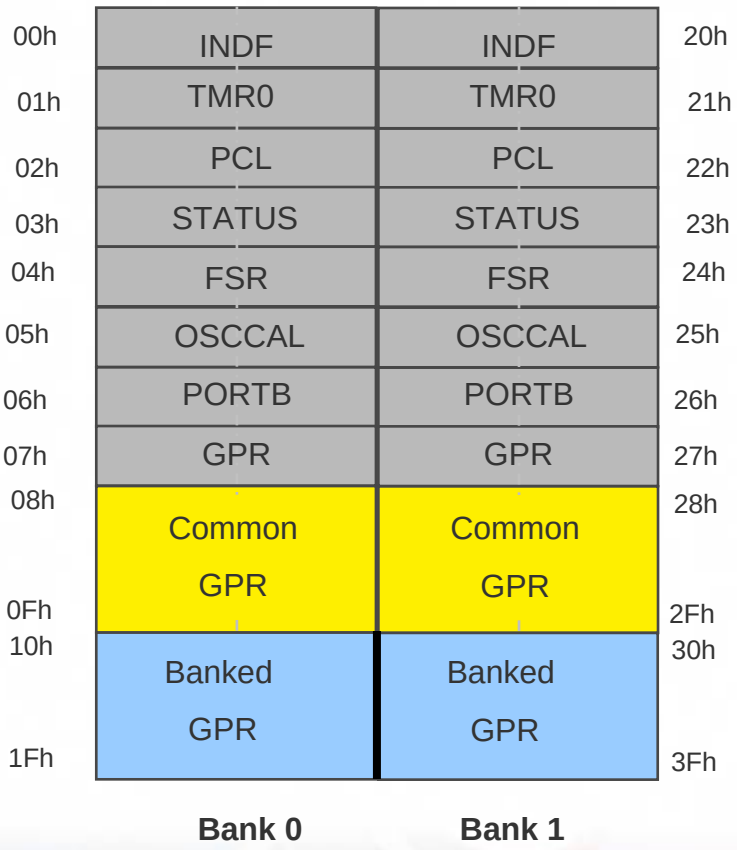
Baseline Program Memory

- Maximum of 4 KW of Program Memory
  - Program memory is divided into 512 W “pages”
- 12-bit Program Counter
  - Only the lower 8 bits are mapped into the data space (PCL register)
- Hardware Stack
  - 2 levels deep
  - Circular stack pointer
  - No overflow or underflow detection



Baseline Data Space

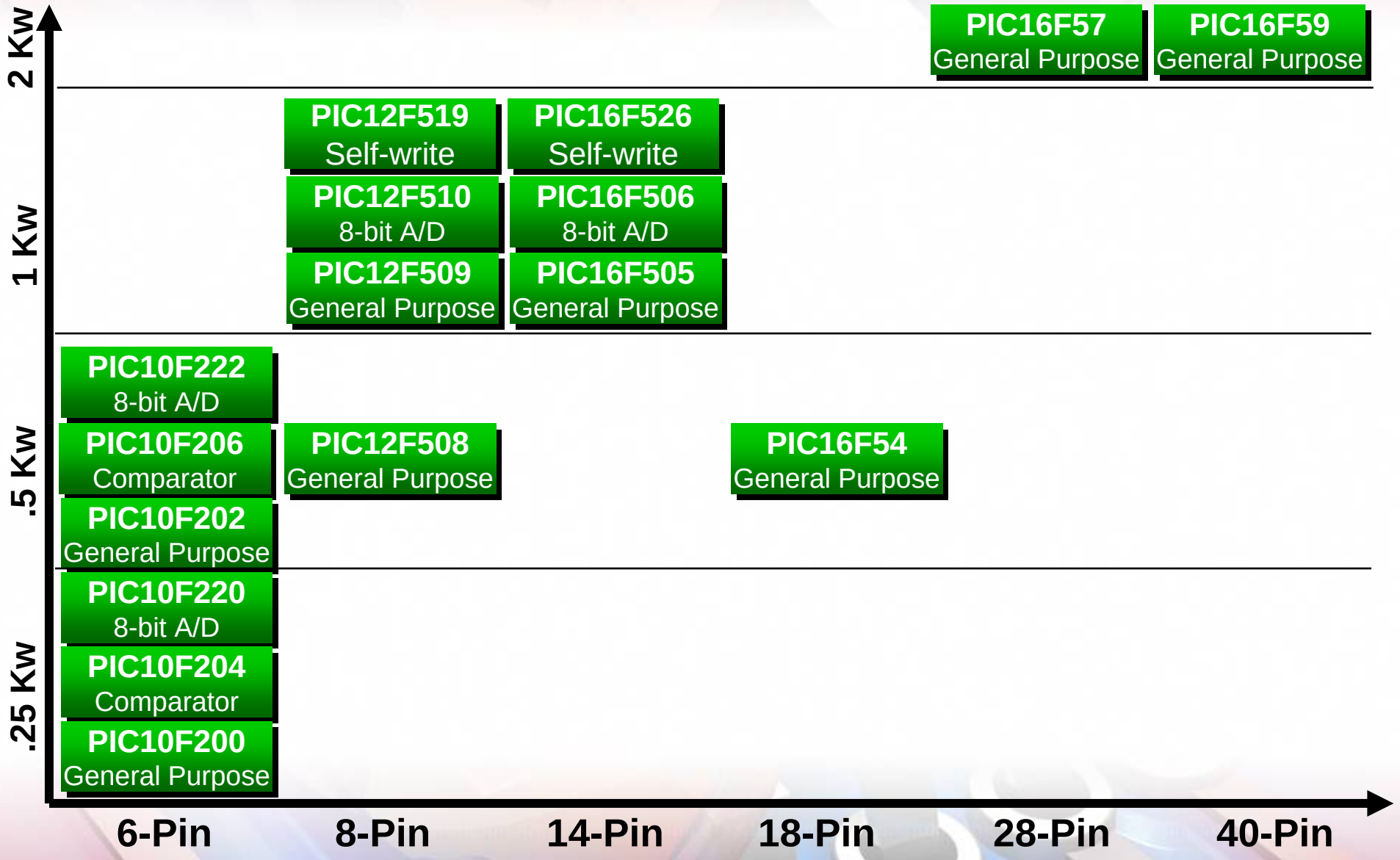
- Maximum of 256 Bytes of Data Memory
  - Data space is divided into 32 Byte “Banks”
  - Banks are selected via the 3 MSbs of the File Select Register (FSR)
- Direct Addressing
  - Can address 32 bytes in a specific bank
- Indirect Addressing
  - Can address all 256 Bytes in the data space



Baseline Peripherals

- **8-bit Timer Timer0**
- **Comparators**
- **ADC**
- **High Frequency Internal Oscillator**
  - 4 or 8 MHz
  - Crystal/resonator oscillator
- **Flash Data Memory**
  - 64 Bytes of nonvolatile memory storage
- **Supervisory Peripherals**
- **High Drive Strength I/Os**

Baseline Flash Family



Standard Mid-Range

PIC12F

PIC16F

PIC12F5XX

PIC16F5XX

PIC12F6XX

PIC16FXXX

PIC12F1XXX

PIC16F1XXX

8-pin PIC® MCU

≥14-pin PIC MCU

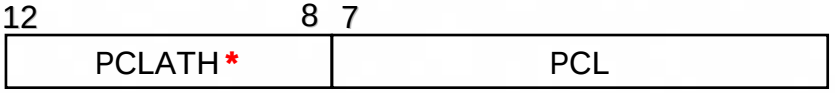
2.0-5.5V
Up to 20 MHz

2.0-5.5V
Up to 20 MHz

Mid-Range Architecture

- **Harvard Architecture**
  - 14-bit wide instruction word
  - 8-bit wide data byte
- **Instruction Set Features**
  - 35 instructions
    - 4 clocks per instruction cycle
    - Most instructions are one cycle
  - 20 MHz maximum clock rate (5 MIPS maximum)
- **8-bit Working (W) Registers**
  - Data use only
- **Hardware Stack**
  - 8 levels deep
- **Interrupts**
  - Single priority interrupt

Mid-Range Programmer's Model

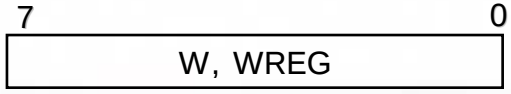


Program Counter (13-bit)

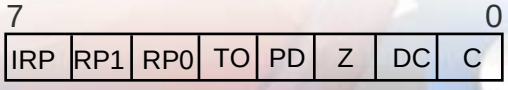
***There is no direct access to the upper 5 bits of the PC**

File Select Register

Indirect File Addressing Register



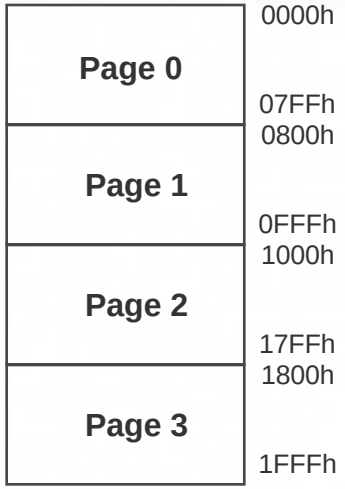
Working Register



STATUS Register

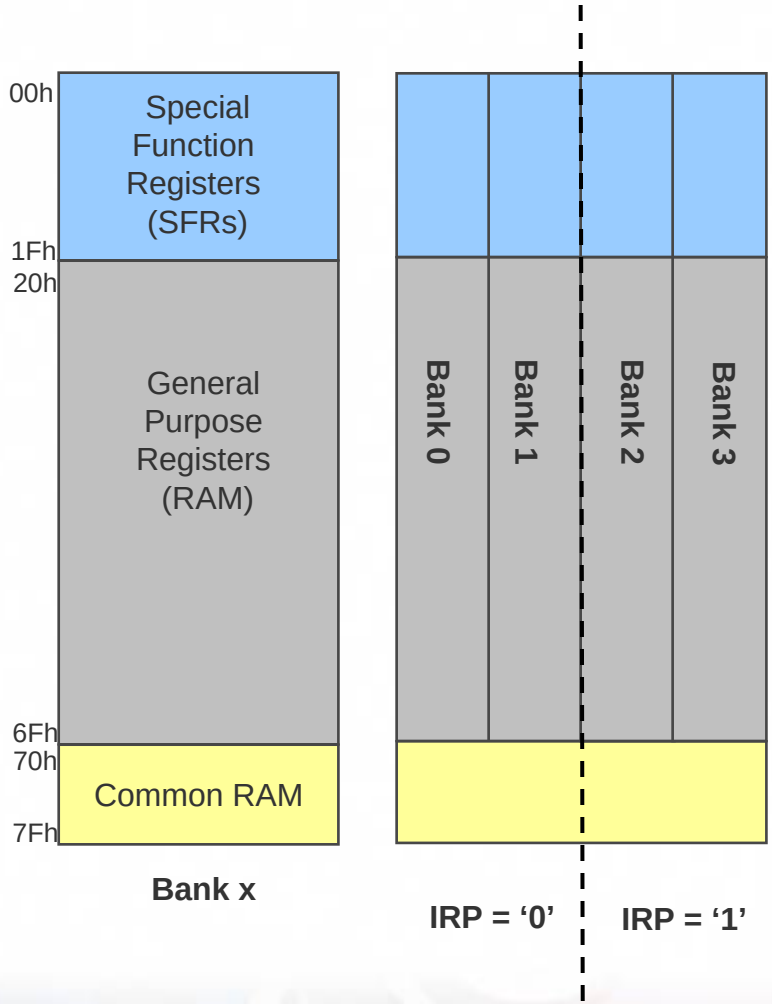
Mid-Range Program Space

- Maximum of 8 KW of Program Memory
  - Program memory is divided into 2 KW “pages”
- 13-bit Program Counter
  - Lower 8 bits are mapped into the data space (PCL register)
  - Upper 5 bits are accessed via the PCLATH register
- Hardware Stack
  - 8 levels deep
  - Circular stack pointer
  - No overflow or underflow detection



Mid-Range Data Space

- Maximum of 512 Bytes of Data Memory
  - Data space is divided into 128 Byte “Banks”
  - 16 Bytes of Common RAM
- Direct Addressing
  - Can address 128 bytes in a specific bank
  - Banks are selected via the RP<1:0> bits of the STATUS register
- Indirect Addressing
  - Can address a 256 byte range
  - Selecting the lower or upper 256 bytes requires the use of the IRP bit



Mid-Range Interrupts

- Single priority level
- Single interrupt vector (0004h)
- Individual interrupt enable and flags for each source
- Context saving is required in software
- Hardware latency
  - 3 or 4 cycles for asynchronous interrupts
  - 3 cycles for synchronous interrupts
- Two modes of interrupt operation in Sleep
  - In-line interrupt
  - Vectored interrupt

1XXX Mid-Range

PIC12F

PIC12F5XX

PIC12F6XX

PIC12F1XXX

8-pin PIC® MCU

1.8-3.6V/5.5V
Up to 32 MHz

PIC16F

PIC16F5XX

PIC16FXXX

PIC16F1XXX

≥14-pin PIC MCU

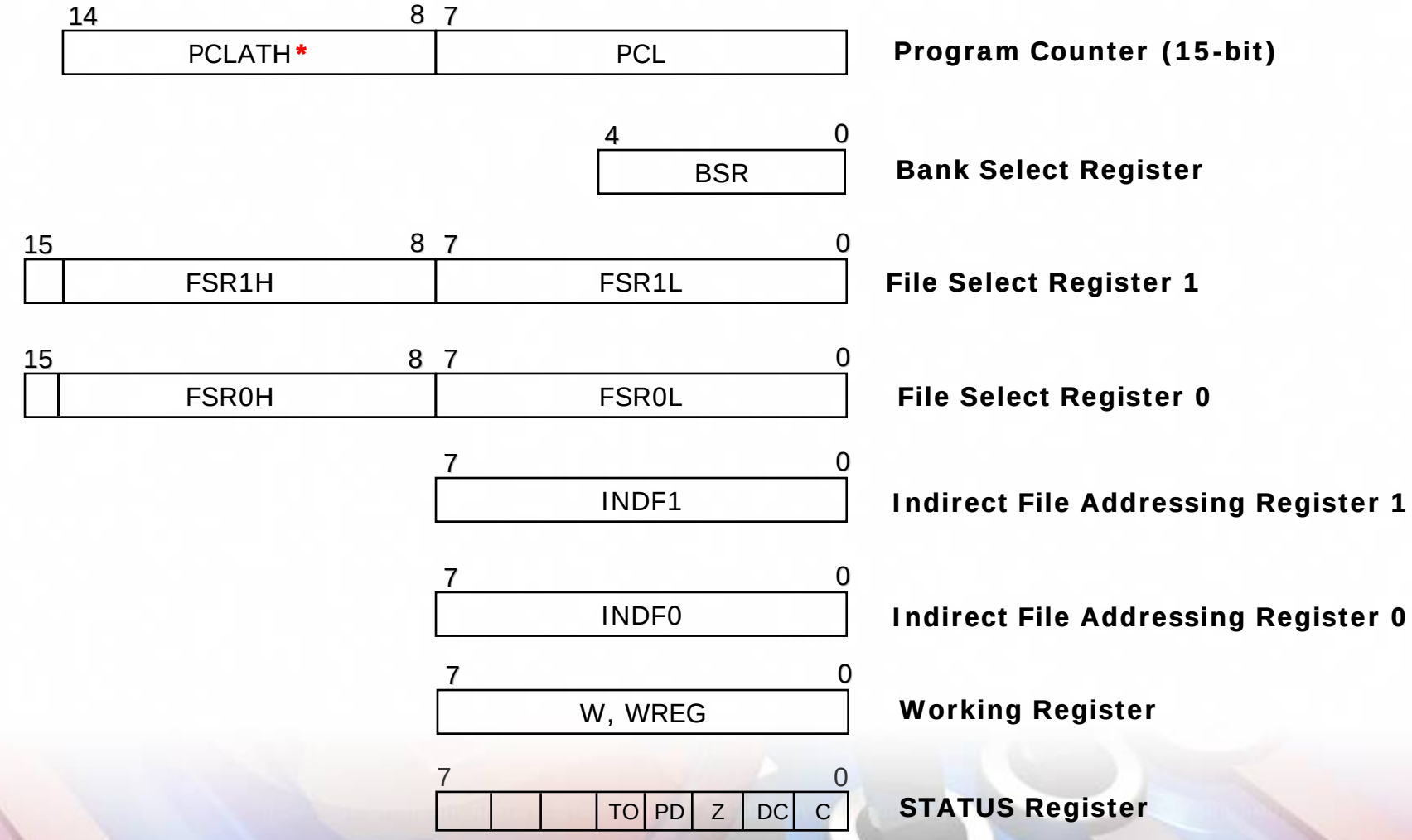
1.8-3.6V/5.5V
Up to 32 MHz

Mid-Range 1XXX Architecture

- **Harvard Architecture**
  - 14-bit wide instruction word
  - 8-bit wide data byte
- **Instruction Set Features**
  - 48 instructions
    - Same 35 instructions as standard mid-range
    - 13 new instructions to improve overall device performance
  - 32 MHz maximum clock rate (8 MIPS maximum)
- **1 8-bit Working (W) Register**
  - Data use only
- **Hardware Stack**
  - 16 levels deep
- **Interrupts**
  - Hardware context saving

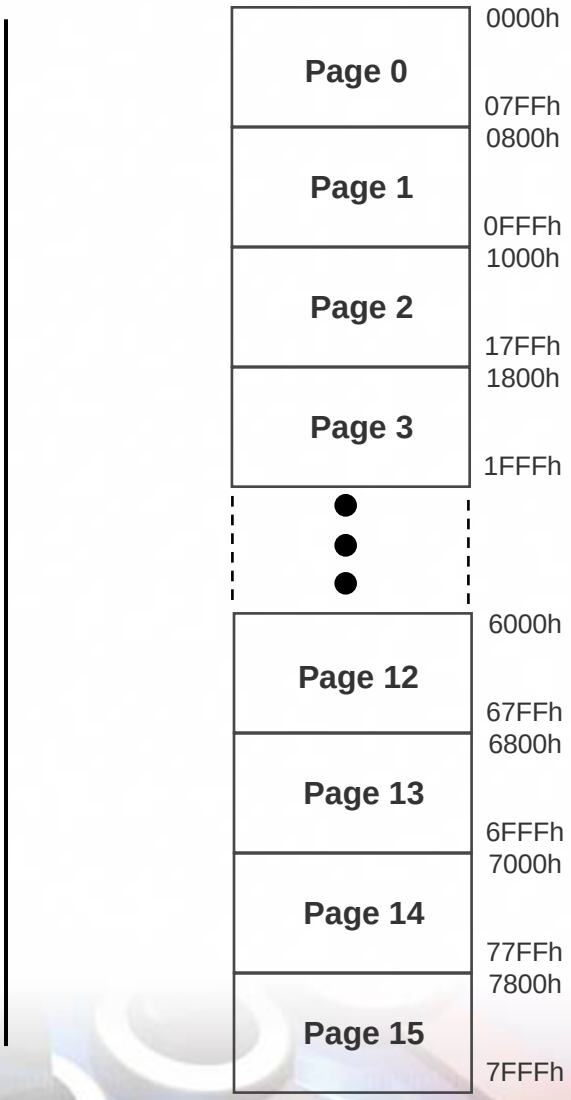
Mid-Range 1XXX Programmer's Model

***There is no direct access to the upper 7 bits of the PC**



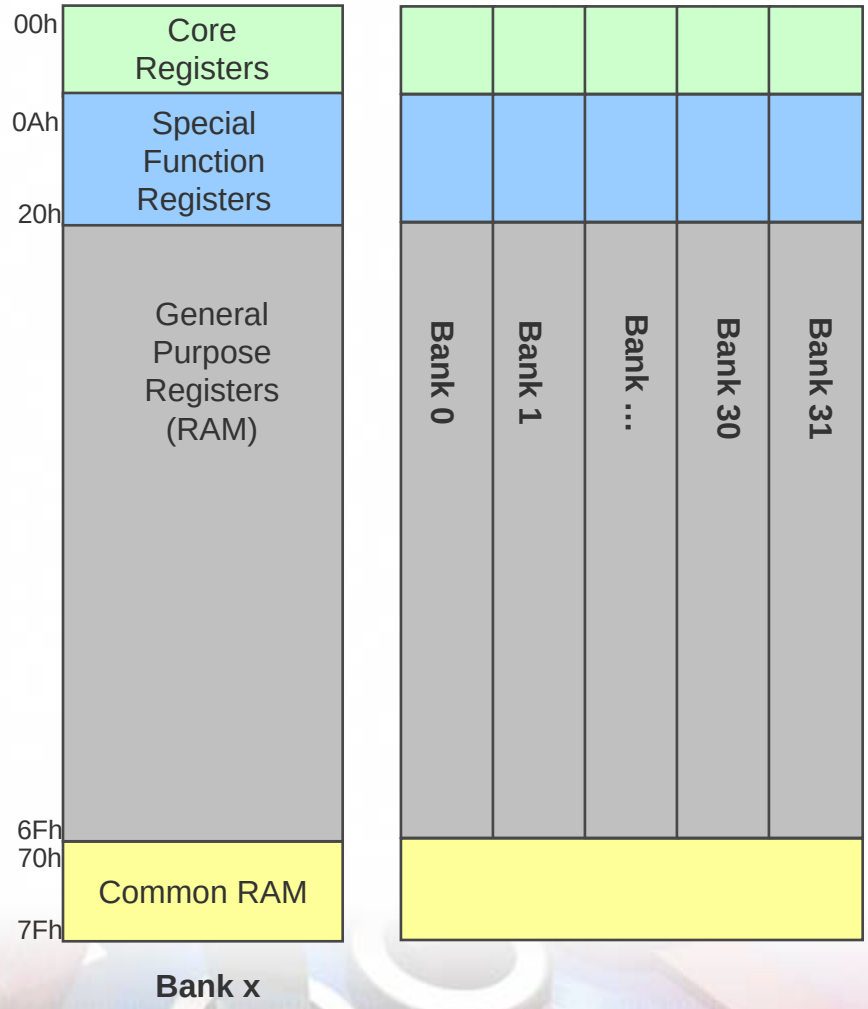
Mid-Range 1XXX Program Space

- Maximum of 32 KW of Program Memory
  - Program memory is still divided into 2 KW “pages”
  - New MOVLP instruction makes all paging instructions 1 cycle
- 15-bit Program Counter
  - Lower 8 bits are still mapped into the data space via PCL
  - Upper 7 bits are still accessed via the PCLATH register
- Hardware Stack
  - 16 levels deep
  - Non-circular stack pointer
  - Overflow/Underflow reset



Mid-Range 1XXX Data Space

- Maximum of 4 KB of Data Memory
  - Banks remain unchanged
- Direct Addressing
  - Banks now selected via the BSR register
  - MOVLB instruction makes all banking instructions 1 cycle
- Indirect Addressing
  - 2 full FSRs can address the entire 4 KB data space
  - FSRs can also address program space



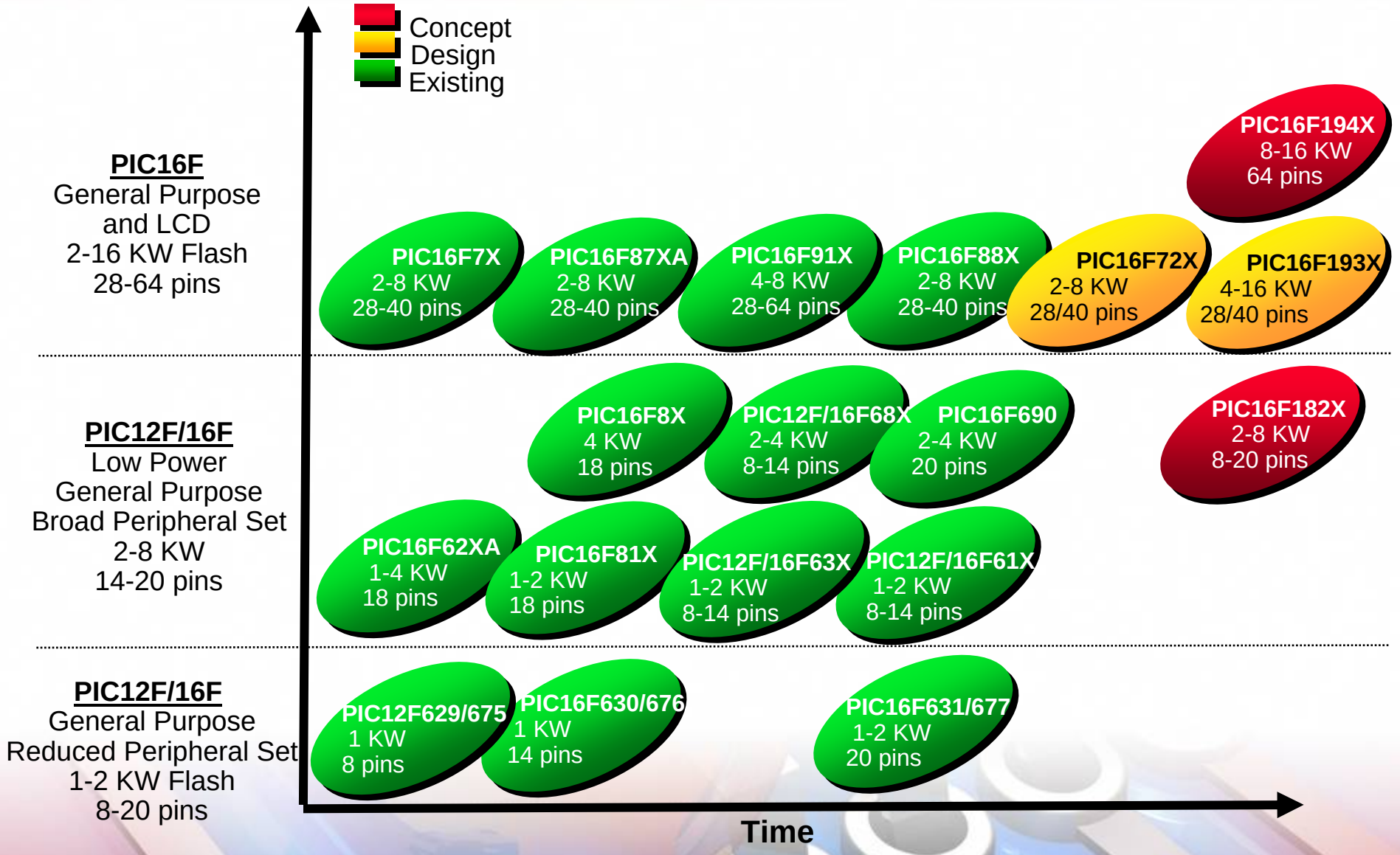
Mid-Range 1XXX Interrupts

- Single priority level
- Single interrupt vector (0004h)
- Individual interrupt enable and flags for each source
- Hardware latency
  - 3 or 4 cycles for asynchronous interrupts
  - 3 cycles for synchronous interrupts
- Two modes of interrupt operation in Sleep
  - In-line interrupt
  - Vectored interrupt
- Context saving done in hardware
  - WREG, PCLATH, BSR and STATUS are all saved on Vectored Interrupt entry

Mid-Range Peripherals

- Analog-to-Digital Converters
- Comparators
- Supervisory Peripherals
- Oscillators
  - Internal Oscillators
  - Clock Switching
  - Fail-Safe Clock Monitor
  - Two-Speed Start-Up
- Pins
  - High Drive Strength I/O
- 8 and 16-bit timers
- Capture/Compare/PWM
  - 16-bit Input Capture
  - 16-bit Output Compare
  - 10-bit PWM
- Synchronous Serial Port (SSP)
  - SPI
  - I^2C™
- UARTs
- Data EEPROM
- Self-Readable/Writeable Flash

Mid-Range Families



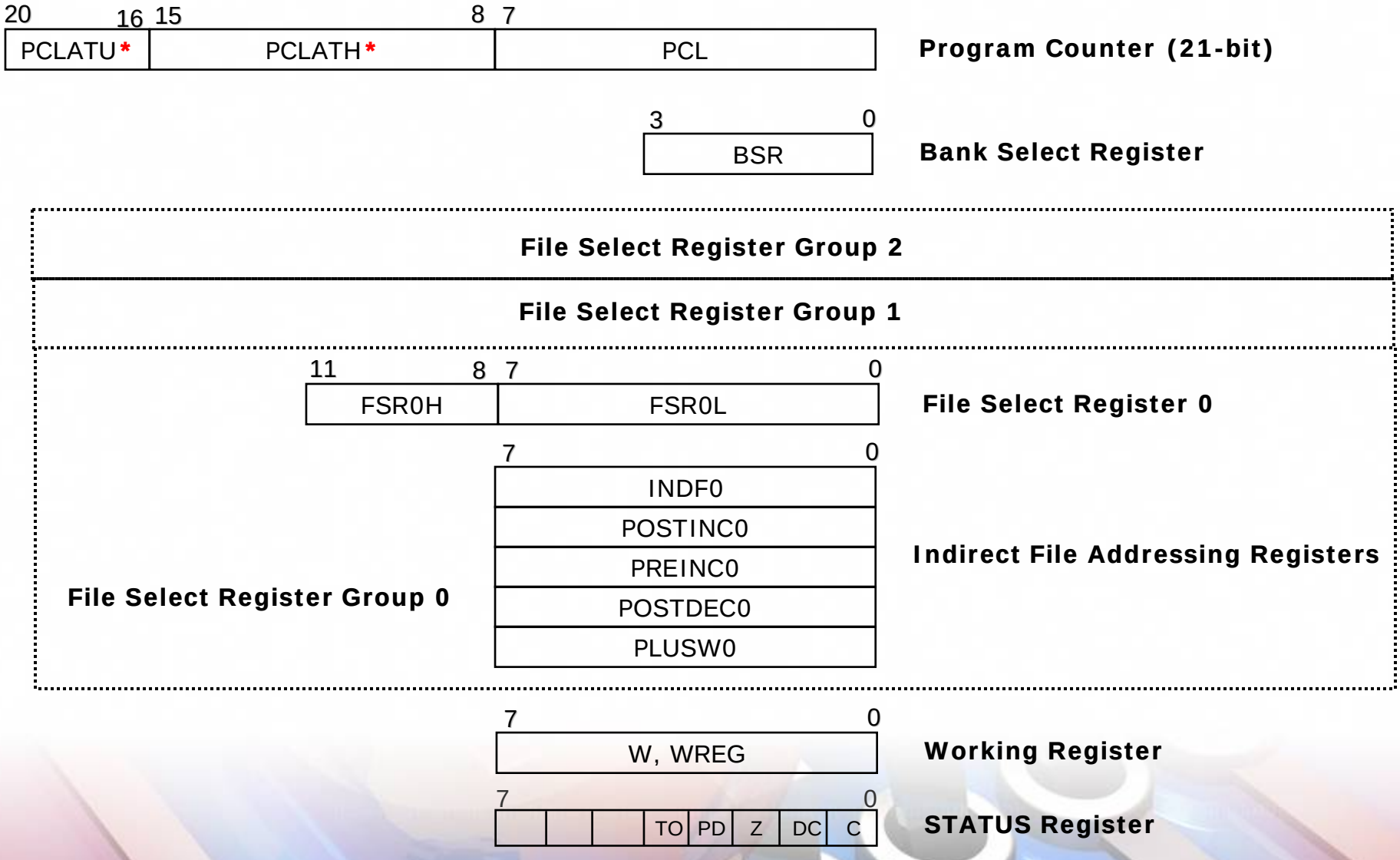
Enhanced 8-bit

PIC18F	PIC18FJ	PIC18FK
All pin count PIC18 MCU		
2.0-5.5V Up to 40 MHz	2.0-3.6V Up to 40/48 MHz	1.8-3.6V/5.5V Up to 64 MHz

Enhanced PIC18 Architecture

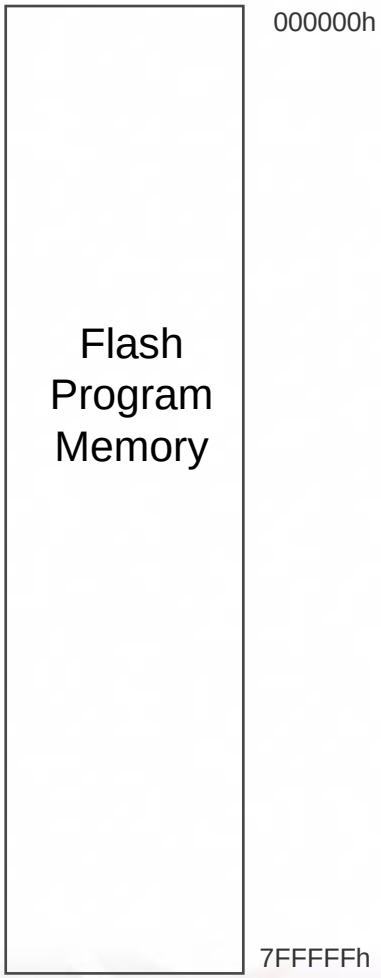
- **Harvard Architecture**
  - 16-bit wide instruction word
  - 8-bit wide data byte
- **Instruction Set Features**
  - 75/83 instructions
    - Backward compatible with the mid-range architecture
  - 4 clocks per instruction cycle
  - 64 MHz maximum clock rate
- **1 8-bit Working (W) Register**
  - Data use only
- **Hardware Stack**
  - 31 levels deep
  - Software Access to Stack
- **Interrupts**
  - Adds interrupt priorities
- **Hardware Multiplier**

PIC18 Programmer's Model



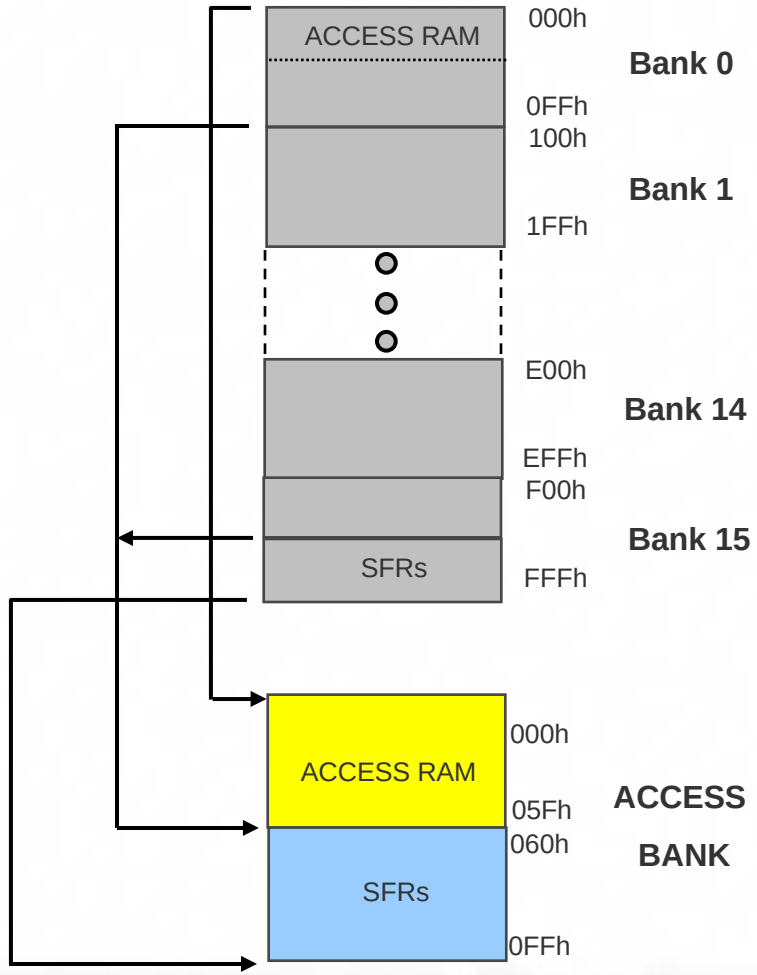
PIC18 Program Space

- Maximum of 1 MW of program memory
  - Program memory is linear
  - NO PAGING
- 21-bit Program Counter
  - Lower 8-bits are still mapped into the data space via PCL
  - Upper 13-bits are still accessed via the PCLATH and PCLATU registers
- Hardware Stack
  - 31 levels deep
  - Non-circular stack pointer
  - Overflow/Underflow reset



PIC18 Data Space

- Maximum of 4 KB of data memory
  - Data space is divided into 256 Byte “Banks”
  - Special “Access RAM’ functionality for improved
- Direct Addressing
  - Can address all of the 256 Bytes in a specific bank
  - Banks are selected via the BSR register
- Indirect Addressing
  - 3 full FSRs can address the entire 4 KB data space



PIC18 Interrupts

- Two priority levels
  - High (Vector 0008h)
  - Low (Vector 0018h)
- Individual interrupt enable and flags for each source
- Hardware latency
  - 3 or 4 cycles for asynchronous interrupts
  - 3 cycles for synchronous interrupts
- High priority interrupt with fast context saving
  - WREG, BSR and STATUS are all saved on High Priority Vectored Interrupt entry
- Two modes of interrupt operation in Sleep
  - In-line interrupt
  - Vectored interrupt

PIC18 Peripherals

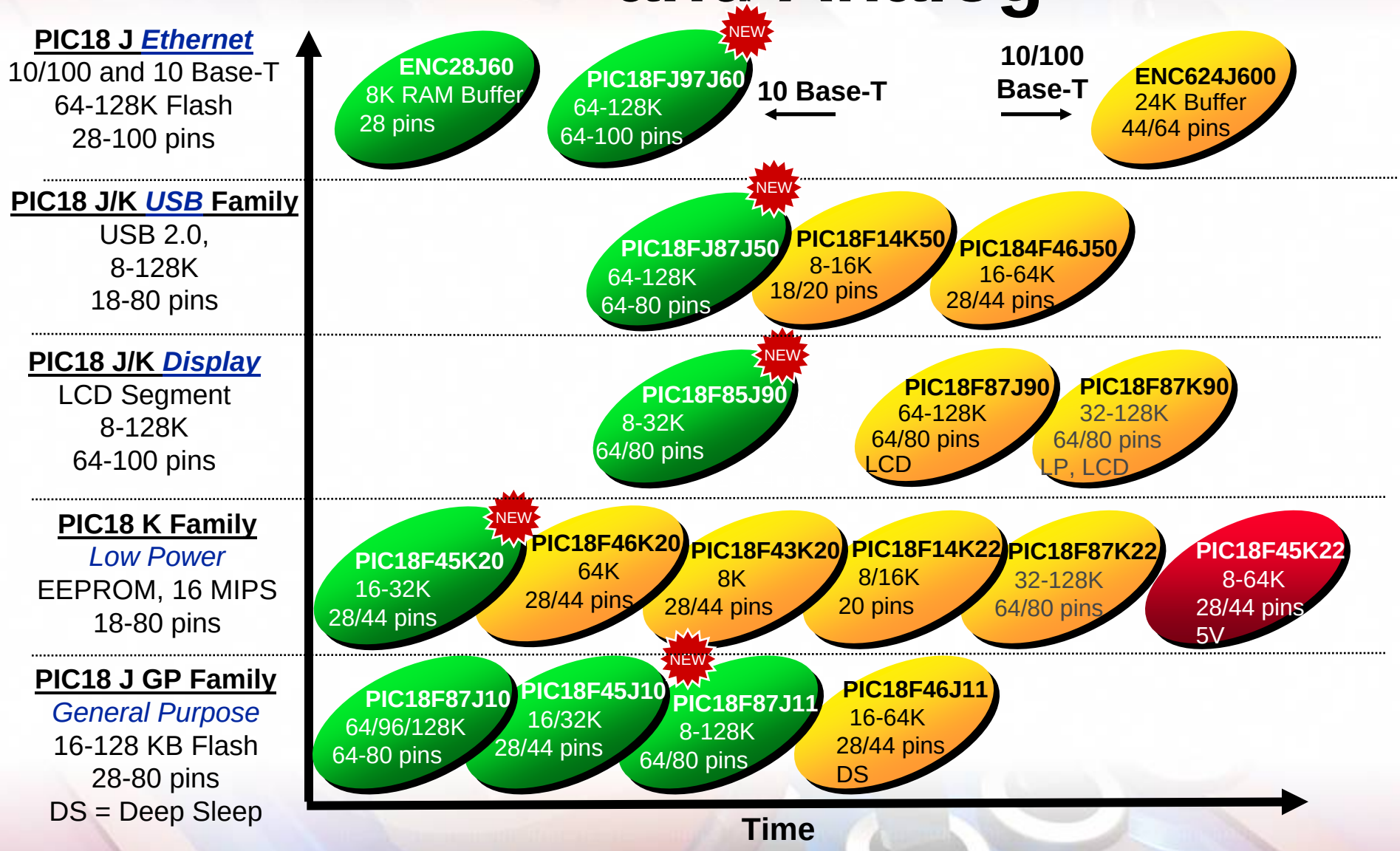
- Analog-to-Digital Converters
- Comparators
- Supervisory Peripherals
- Oscillators
  - Internal Oscillators
  - Clock Switching
  - Fail-Safe Clock Monitor
  - Two-Speed Start-Up
- Pins
  - High Drive Strength I/O
- 8 and 16-bit timers
- Capture/Compare/PWM
  - 16-bit Input Capture
  - 16-bit Output Compare
  - 10-bit PWM
- Synchronous Serial Port (SSP)
  - SPI
  - I^2C™
- UARTs
- Data EEPROM
- Self-Readable/Writeable Flash

Same peripherals as Mid-Range

PIC18 Peripherals

- Programmable Low-Voltage Detect (PLVD)
- Peripheral Pin Select (PPS)
  - Allows user to select the pinout of digital peripherals
- Capacitive Time Measurement Unit (CTMU)
  - Absolute capacitive sensor (mTouch™ sensing solution peripheral)
- Real-Time Clock Calendar (RTCC)
  - Clock provides: hours, minutes and seconds
  - Calendar provides: day, month, year and day of week
  - Alarm with interval mask
- Parallel Master Port (PMP)
  - Supports QVGA displays

PIC18F General Purpose and Analog



8-bit Software Tools

- **MPLAB® IDE**
  - Supports all 8-bit architectures
- **Compilers**
  - C compiler is available for each architecture
    - C18 compiler
    - HI-TECH (3rd party)
    - CCS (3rd party)
- **Code Module Library**
- **RTOS**
- **Software Stacks**
  - USB
  - ZigBee
  - mTouch™ Sensing Solution

8-bit Hardware Tools

- **Programmers and Debuggers**
  - MPLAB® REAL ICE™ in-circuit emulator
  - MPLAB ICD 2
  - PICkit™ 2
- **Programmers Only**
  - PM3
- **Demo Boards**
  - System Management
  - Mechatronics
  - Full Speed USB
  - PICDEM.net™
- **PICkit Serial Analyzer**
- **PICtail™ Daughter Boards**

PIC24

PIC24F

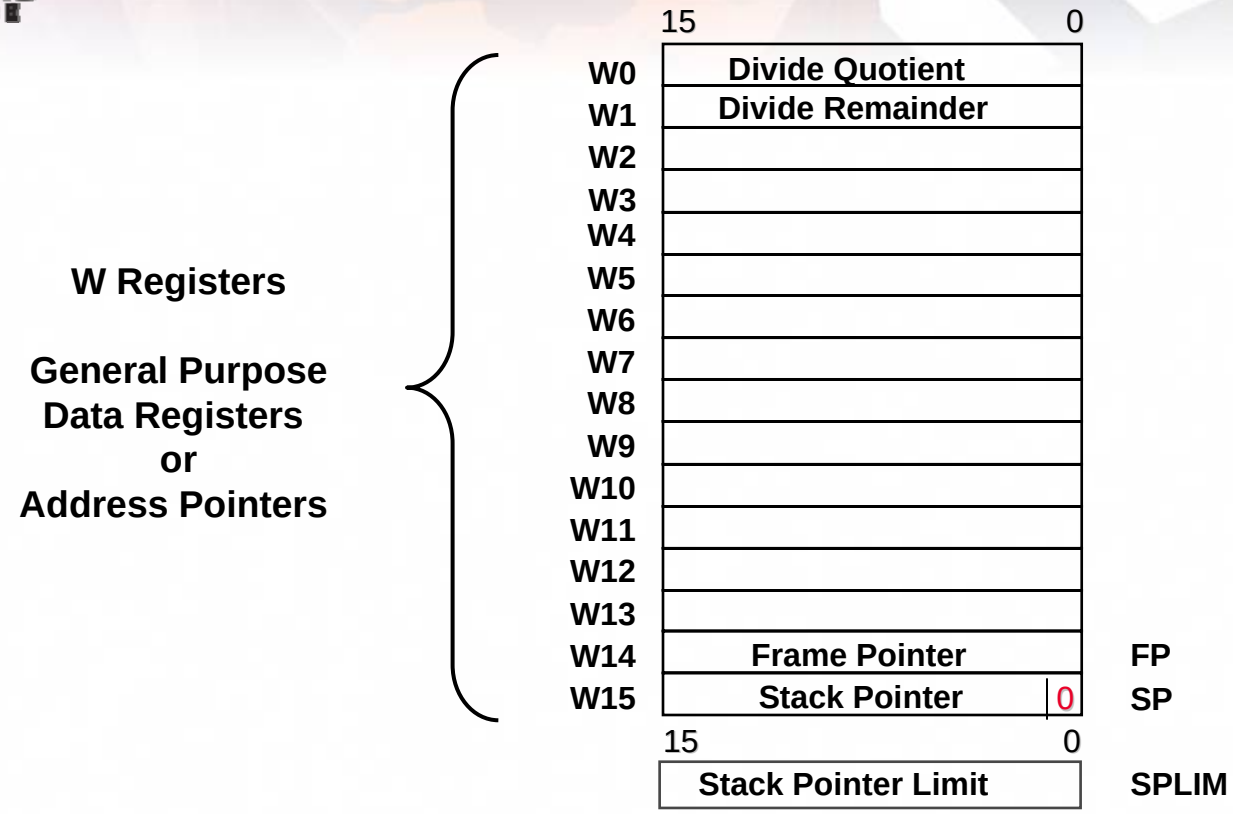
PIC24H

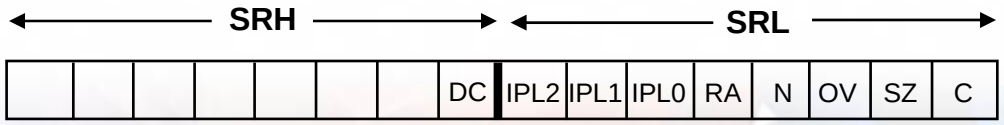
All pin count PIC24 MCU

PIC24 Architecture

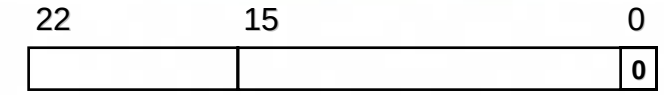
- **Harvard Architecture**
  - 24-bit wide instruction word
  - 16-bit wide data byte
- **Instruction Set Features**
  - 76 instructions
    - Most instructions are one cycle
    - Most instructions are one word
  - 2 clocks per instruction cycle
  - 32 MHz (16 MIPS) performance
- **16 x 16-bit Working (W) Registers**
- **Software Stack**
- **Program Space Visibility**
- **Hardware Multiplier and Divider**

PIC24 Programmer's Model





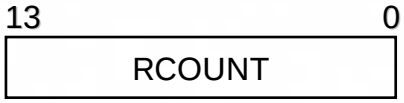
PIC24 Programmer's Model (cont.)



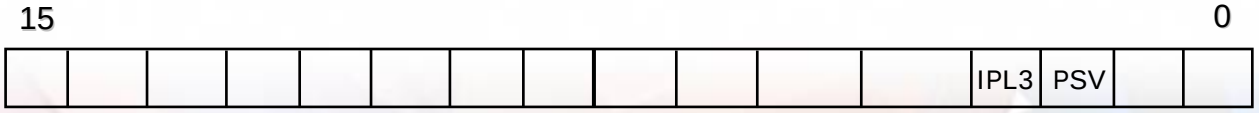
Program Counter (23-bit)

TABLE Data Read Page Address

PSV Page Address



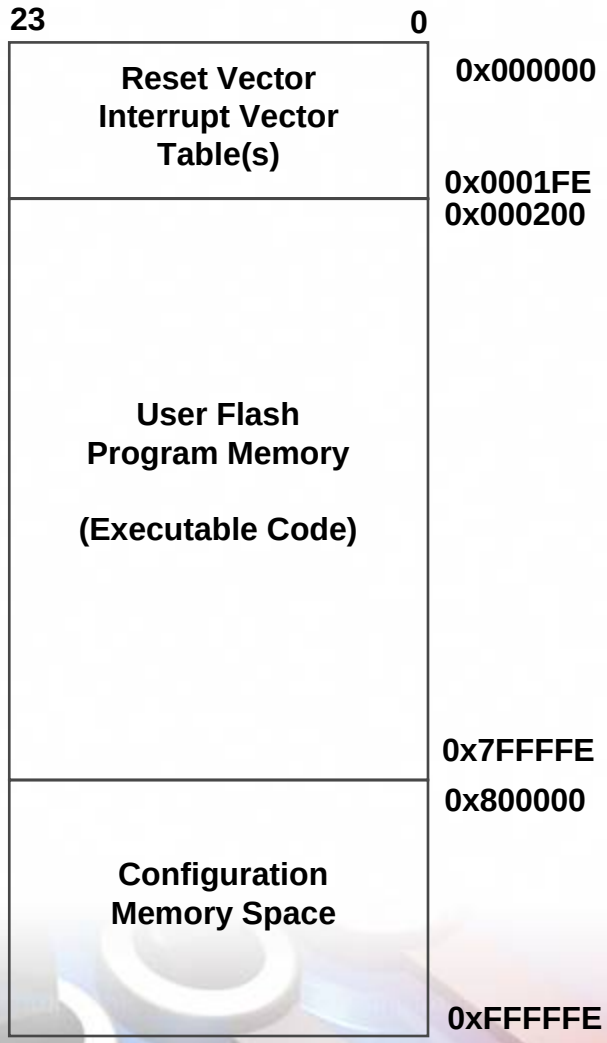
REPEAT Loop Counter



Core Control Register (CORCON)

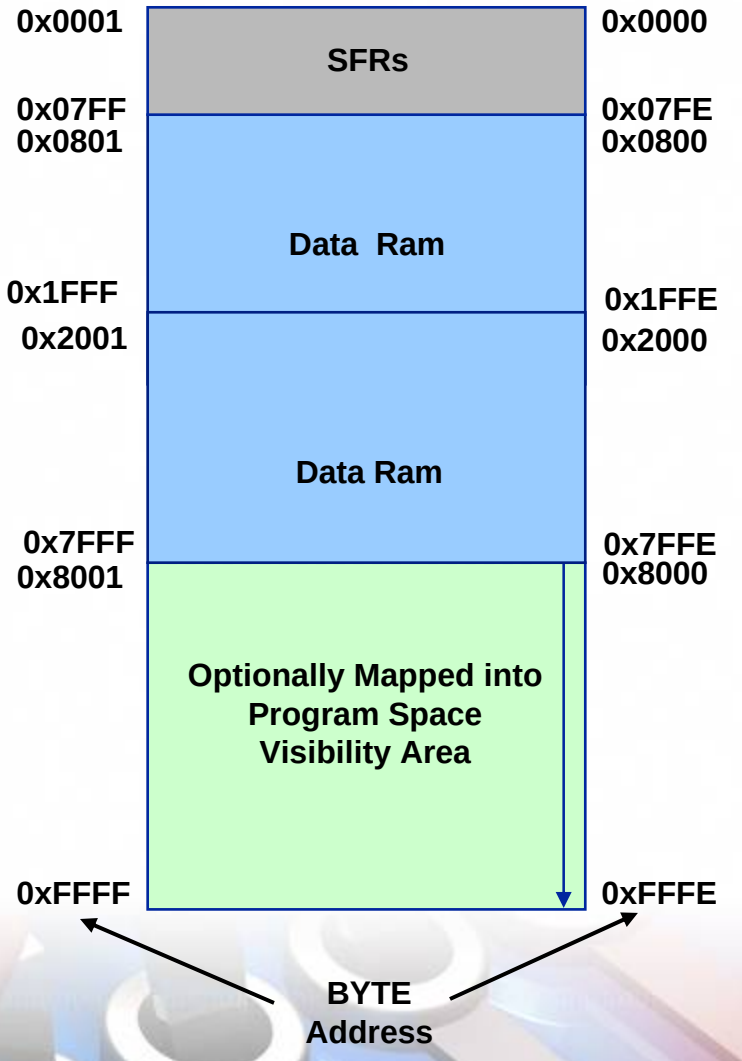
PIC24 Program Space

- Maximum of 4 MB of Program Memory
  - Program memory is linear – NO PAGING
- 23-bit Program Counter
  - All 23 bits are mapped into the data space
- Software Stack
  - W14 is the frame pointer
  - W15 is stack pointer
    - SPLIM register used to set the size of the stack
    - Will generate an overflow if W15 > SPLIM
    - Will generate an underflow if W15 < 0800h



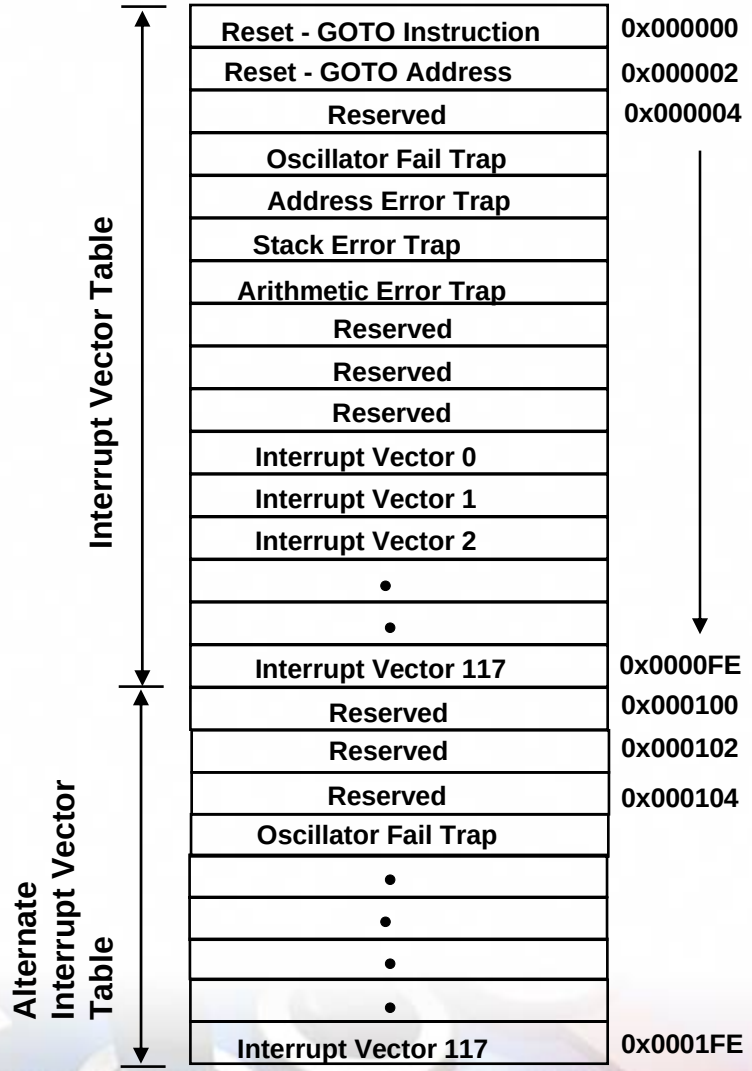
PIC24 Data Memory

- Linear Data Memory
  - Up to 64 KB data memory
- DS features 8 KB of “Near” RAM Space
  - Directly addressable
  - Includes Special Function Register (SFR)
- Entire Data Space is Indirectly Addressable
  - 7 addressing modes for flexibility in indirect operations



PIC24 Interrupts

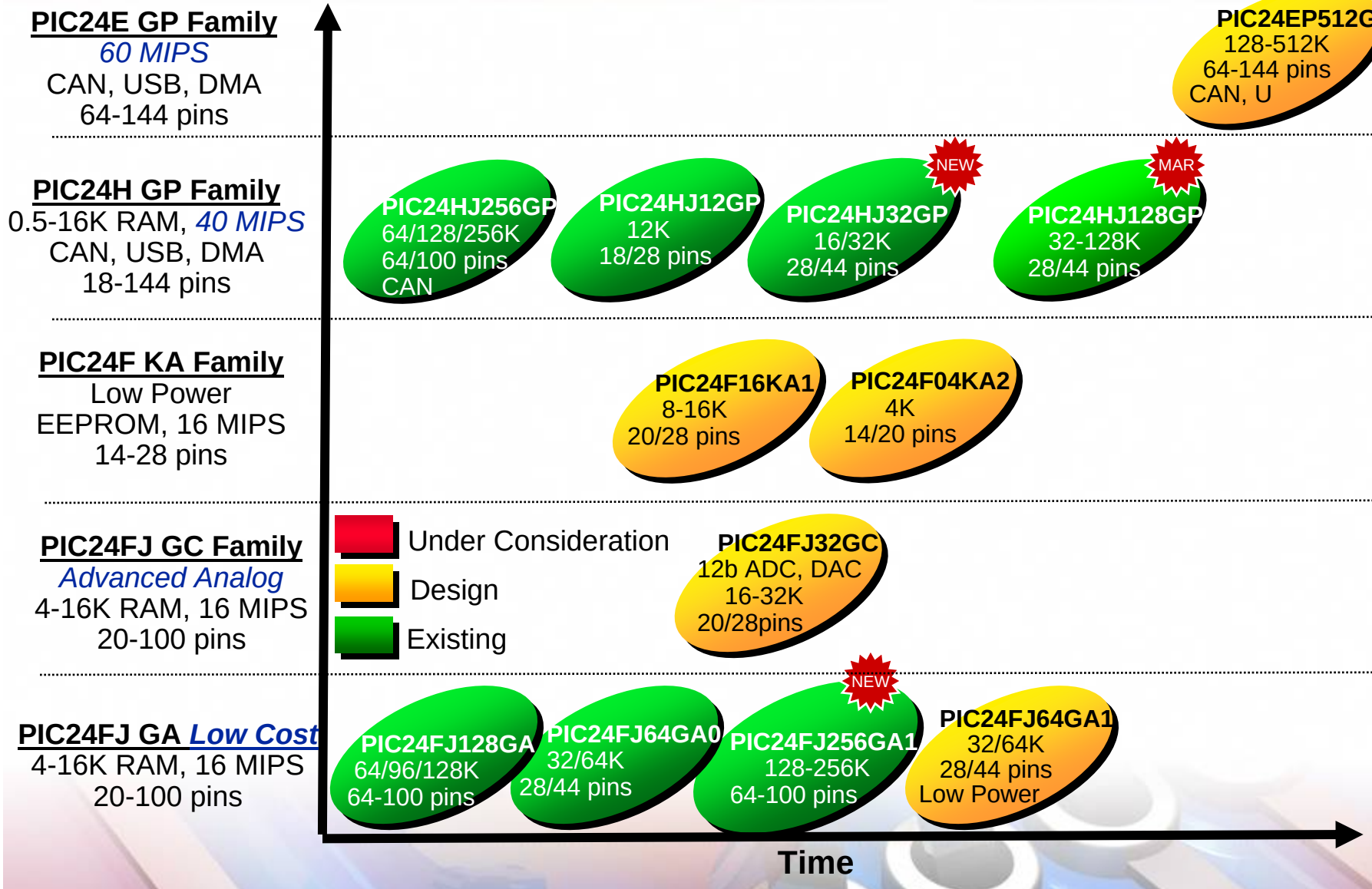
- CPU has 16 Priority Levels
  - Level 8-15 for traps
  - Level 0-7 allocated for interrupt sources
- Each user interrupt source has 7 levels of priority
- Interrupt Vector Table (IVT) has a unique vector for each source
- Alternate IVT for diagnostics
- Consistent ISR latency
  - 5 cycle latency for entry
  - 3 cycle latency for exit
- Context Saving



PIC24 Peripherals

- 16 and 32-bit timers
- Input capture
- Output compare/PWM
- SPI with deep buffer
- I^2C™ with address masking
- UART
- Real-Time Clock and Calendar (RTCC)
- Parallel Master Port (PMP)
- Capacitive Time Measurement Unit (CTMU)
- Analog-to-Digital Converter
  - 10-bit, 500 ksps (PIC24F)
  - 10-bit, 1.1 Msps or 12-bit, 500 ksps (PIC24H)
- Comparators
- Programmable Cyclic Redundancy Checker (CRC)
- DMA (PIC24H only)
  - CPU independent data transfers
- Enhanced CAN (PIC24H only)
  - CAN 1.2, 2.0A and 2.0B

PIC24 General Purpose and Analog Families



PIC24 Communication and Display Families

PIC24 *CAN* Family
8-32K RAM,
40-60 MIPS
CAN, USB, DMA
28-144 pins

PIC24HJ256GP
64/128/256K
64/100 pins
CAN

MAR
PIC24HJ128GP
32-128K
28/44 pins
CAN

PIC24EP512G
128-512K
64-144 pins
CAN, USB

***Ethernet* Family**
10/100T Ethernet
16-24K RAM, 16 MIPS
28-100 pins

NEW
ENC28J60
8K RAM Buffer
28 pins

10 Base-T

10/100 Base-T

ENC624J600
24K Buffer
44/64 pins

PIC24FJ *Display*
Graphics, LCD
4-96K RAM, 16 MIPS
28-100 pins

PIC24FJ256DA1
128-256K
24K RAM
Graphics

PIC24FJ256DA2
128-256K
96K RAM
Graphics

PIC24FJ *USB*
USB OTG
8-24K RAM, 16 MIPS
28-100 pins

PIC24FJ256GB1
64-256K
64-100 pins

PIC24FJ64GB
32/64K
28/44 pins

PIC24EP512G
128-512K
64-144 pins
CAN, USB

Time

dsPIC® DSCs

dsPIC30F

dsPIC33F

All pin count dsPIC DSCs

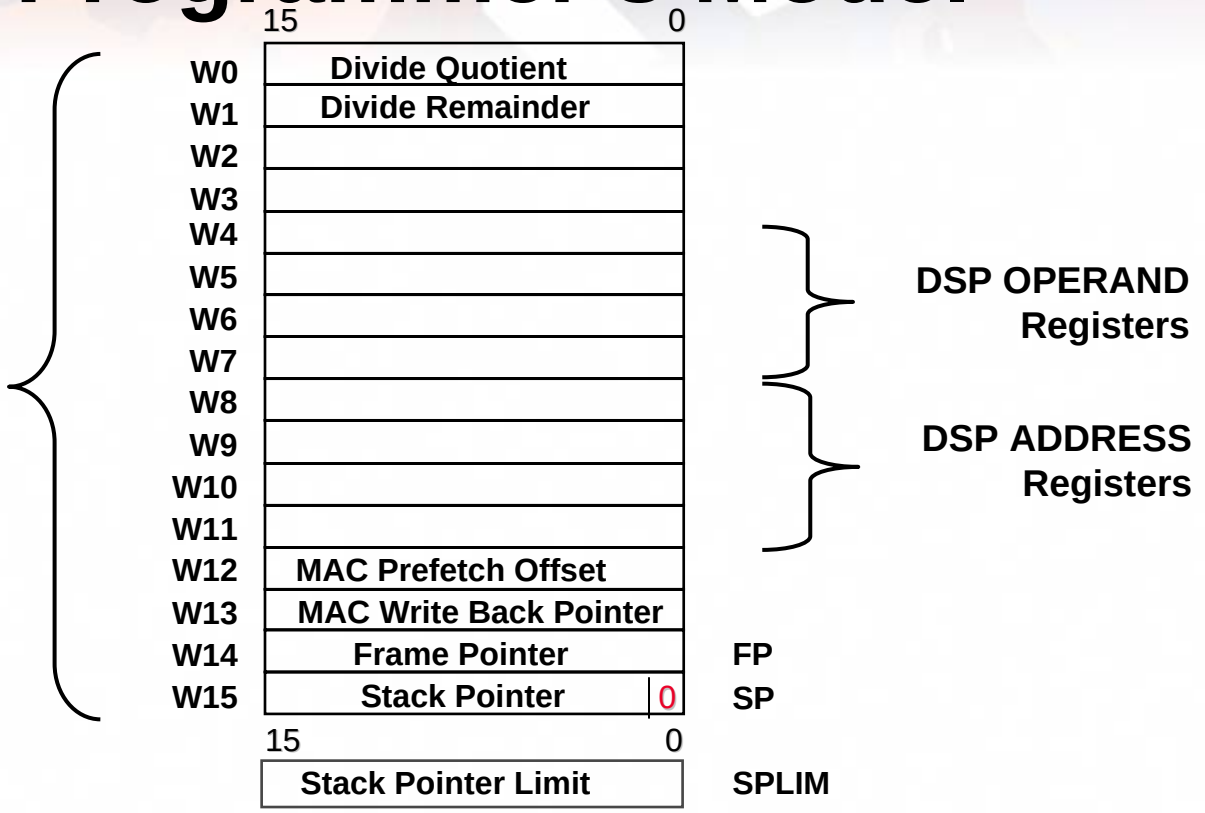
2.X-5.5V
Up to 30 MIPS

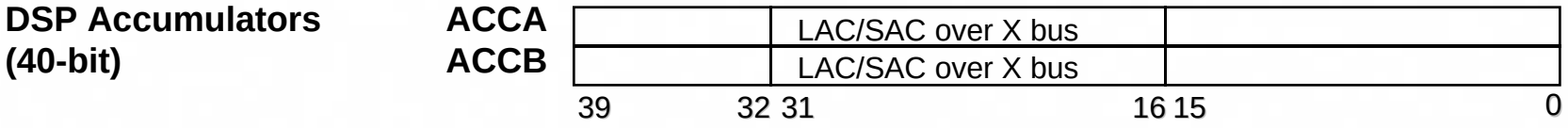
3.0-3.6V
Up to 40 MIPS

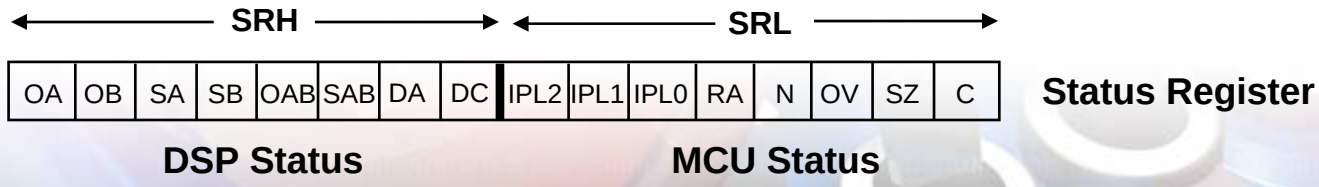
dsPIC® DSC Architecture

- **Same architectural features as the PIC24**
- **dsPIC DSC has a DSP Engine, which includes:**
  - 7 additional DSP specific instructions
  - 17x17-bit I/F Multiplier
  - 40-bit Barrel Shifter
  - 40-bit Adder/Subtracter
  - Two 40-bit Accumulators
  - Sign Extend and Zero Backfill logic
  - Rounding and Saturation Logic
  - X Y address generation logic

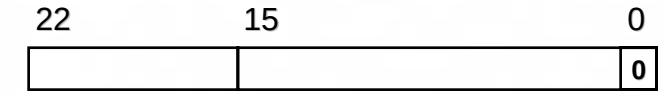
dsPIC® DSC Programmer's Model







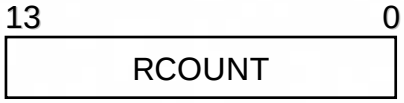
dsPIC® DSC Programmer's Model (cont.)



Program Counter (23-bit)

TABLE Data Read Page Address

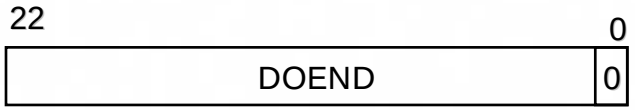
PSV Page Address



REPEAT Loop Counter

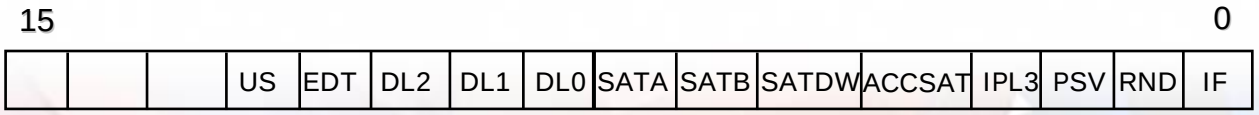
DO Loop Counter

DO Loop Start Address



DO Loop End Address

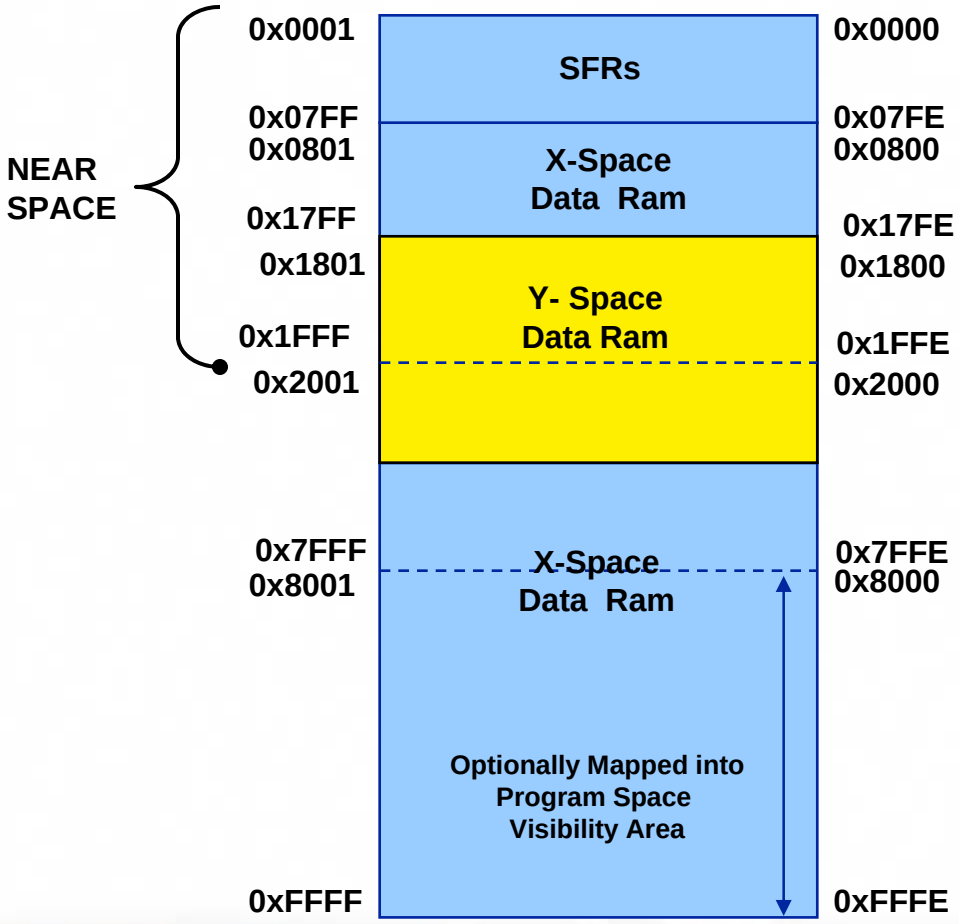
DO SFRs



Core Control Register (CORCON)

dsPIC® DSC Data Space

- Memory space is the same as PIC24
  - 64 KB Data Memory
  - 8 KB of “Near” RAM space
  - Entire Data Space is indirectly addressable
- Adds separate data spaces (X and Y) for MAC class of DSP instructions
  - Enables single-cycle simultaneous dual operand fetch from DS



DSP Hardware

- **Two Independent 40-bit Accumulators**
  - 32 result bits + 8 guard bits (for large dynamic range)
  - Overflow detection, flags and associated branch instructions for each Accumulator
  - Two saturation modes
  - Accumulator store mechanism is 16 bits wide

- **40-bit Wide Barrel Shifter**
  - Shift ACCA, ACCB, W registers or memory
  - Maximum shift range is 16 bits to the left or right
  - Overflow recognition and range limit detection
  - Integral part of DSP engine so permits shifting concurrent with other DSP operations

dsPIC® DSC Peripherals

- 16-bit timers
- Input capture
- Output compare/PWM
- SPI
- I²C™ with address masking
- UART
- Real-Time Clock and Calendar
- Parallel Master Port (PMP)
- Comparators with voltage references
- CTMU
- Programmable Cyclic Redundancy Checker (CRC)
- DMA
- ECAN™
- High-Speed Analog-to-Digital Converter
- Data Converter Interface (DCI)
- Quadrature Encoder Interface
- Motor control PWM
- SMPS PWM

PIC24 Peripheral Set

dsPIC® DSC Roadmap

GP : General Purpose Control
SMPS : Switch Mode Power Supply
MC : Motor Control
SN : Sensor

Under Consideration
Design
Existing

dsPIC33E 60 MIPS
GP, MC, SMPS
128-512 KB Flash
64-144 pins

3.3V
0.18u

+ USB
+ Ethernet
+ Advance Emulation

dsPIC33F 40 MIPS
GP, MC, PC
64-256 KB Flash
64-100 pins

dsPIC33F 40 MIPS
GP, MC, SMPS
12-128 KB Flash
28-44 pins

3.3V
0.25u

+ Comparator
+ 16-bit Speech DAC

dsPIC30F 30 MIPS
GP, MC, SN
12-144 KB Flash
18-80 pins

dsPIC30F 30 MIPS
SMPS
6-12 KB Flash
28-44 pins

5V, 0.4u
Data EE

10-bit ADC	CAN
12-bit ADC	UART
MC PWM	SPI
QEI	I²C™
SMPS	I2S/AC97

dsPIC33F 16 MIPS
GP, MC
12-32 KB Flash
20-28 pins

3.0-3.6V
0.25u

+ Low Power
+ Low Cost
+ 12-Bit ADC
+ 10-Bit DAC

16-bit Software Tools

- **MPLAB® IDE**
  - Has the same functionality as for the 8-bit microcontrollers
- **Compilers**
  - PIC24
  - dsPIC30/33
  - PIC24 and dsPIC30/33
  - 3rd party compilers
    - HI-TECH
    - CCS
- **RTOS**
- **Software Stacks**
  - USB
  - TCP/IP
  - ZigBee
- **Software Libraries**
  - DSP functions
  - Echo cancellation
  - Speech Encoding
  - Speech Recognition
  - Graphics
  - mTouch™ Sensing Solution

16-bit Hardware Tools

- **Programmers and Debuggers**
  - MPLAB® REAL ICE™ in-circuit emulator
  - MPLAB ICD 2
  - PICkit™ 2
- **Programmers only**
  - PM3
- **Starter Kits**
  - PIC24F Starter Kit
  - dsPIC® DSC Starter Kit
- **Demo Boards**
  - Explorer 16
  - dsPICDEM™
- **PICtail™ Daughter Boards**

Same Hardware Tools that are used by the 8-bit PIC® microcontrollers

PIC32

All pin count PIC32 MCU

2.3-3.6V
Up to 80 MHz
-40C→85C

PIC32 Architecture

- MIPS® M4K® 32-bit Core
- BUS Matrix
- DMA Controller
- Hardware Assisted Bit Manipulation
- Interrupts

PIC32 Programmer's Model

General Purpose Registers

R0	Always 0
R1	Assembler Temporary
R2-R3	Function Return Values
R4-R7	Function Arguments
R8-R15	Temporary
R16-R23	Saved Temporary
R24-R25	Temporary
R26-R27	Kernel temporary
R28	Global Pointer
R29	Stack Pointer
R30	Frame Pointer
R31	Return Address

Special Purpose Registers

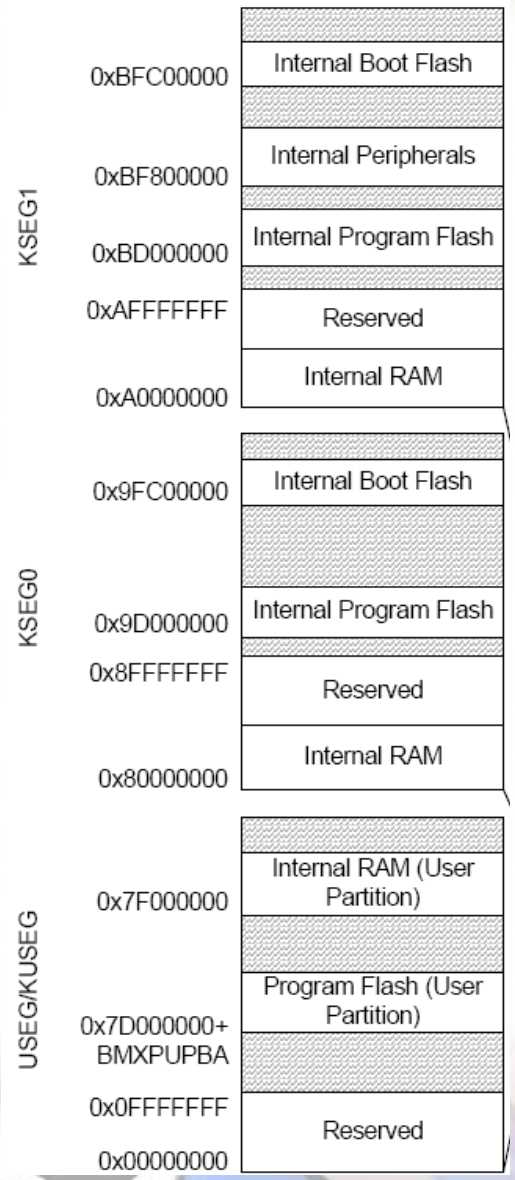
HI
LO
Program Counter

CoProcessor0 Registers

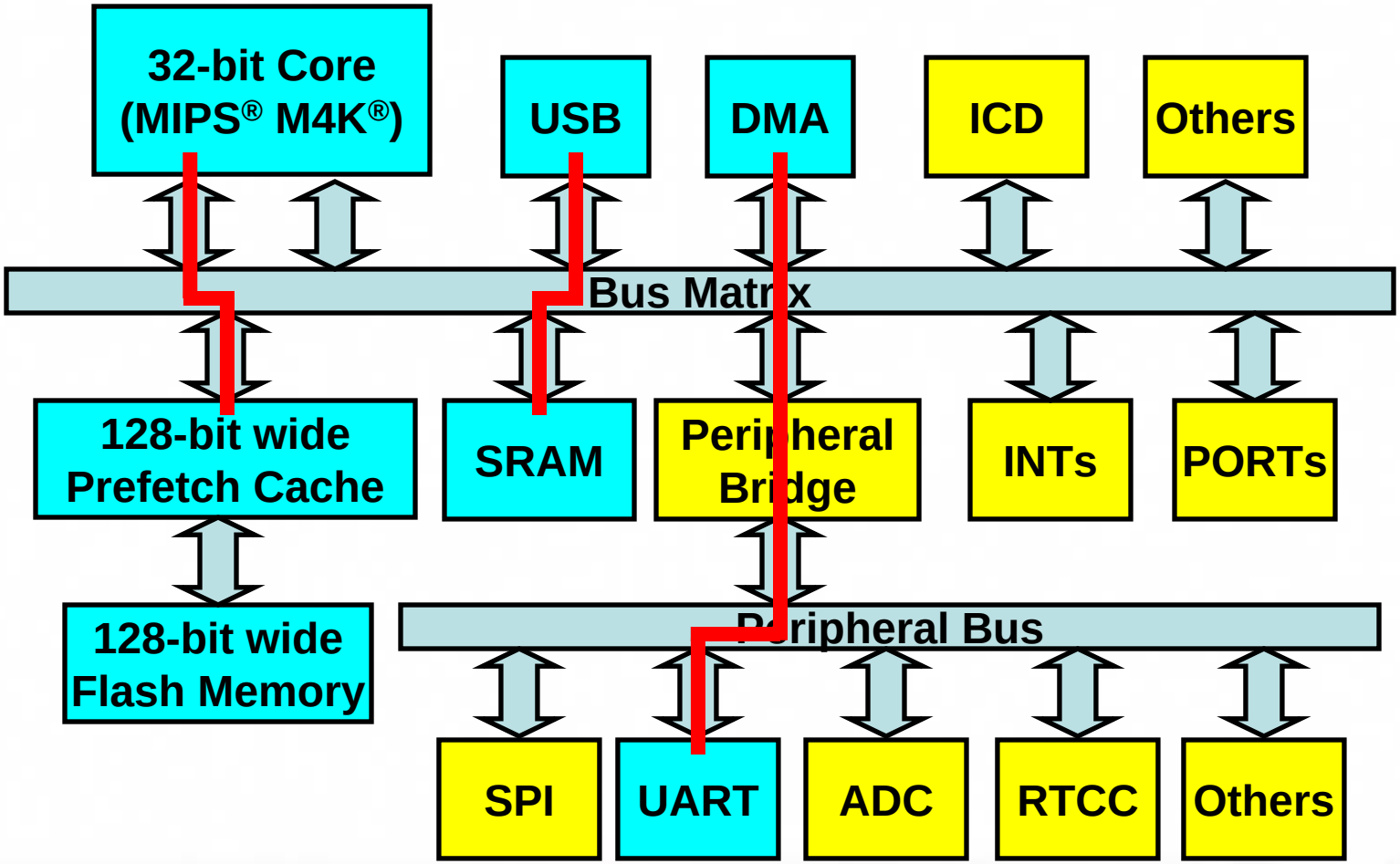
0-6	Reserved
7	HWREna
8	BadVAddr
9	Count
10	Reserved
11	Compare
12	Status/IntCtl/Shadow
13	Cause
14	EPC
15	PRId/EBASE
16	ConfigX
17-22	Reserved
23	Debug
24	DEPC
25-29	Reserved
30	ErrorEPC
31	DeSAVE

PIC32 Unified Memory Space

- Maximum of 4 GB of Memory Space
  - Lower 2 GB for user/kernel segment
  - Upper 2 GB for kernel only segment
  - Each segment includes Flash and RAM
  - Fixed Memory Translation Unit

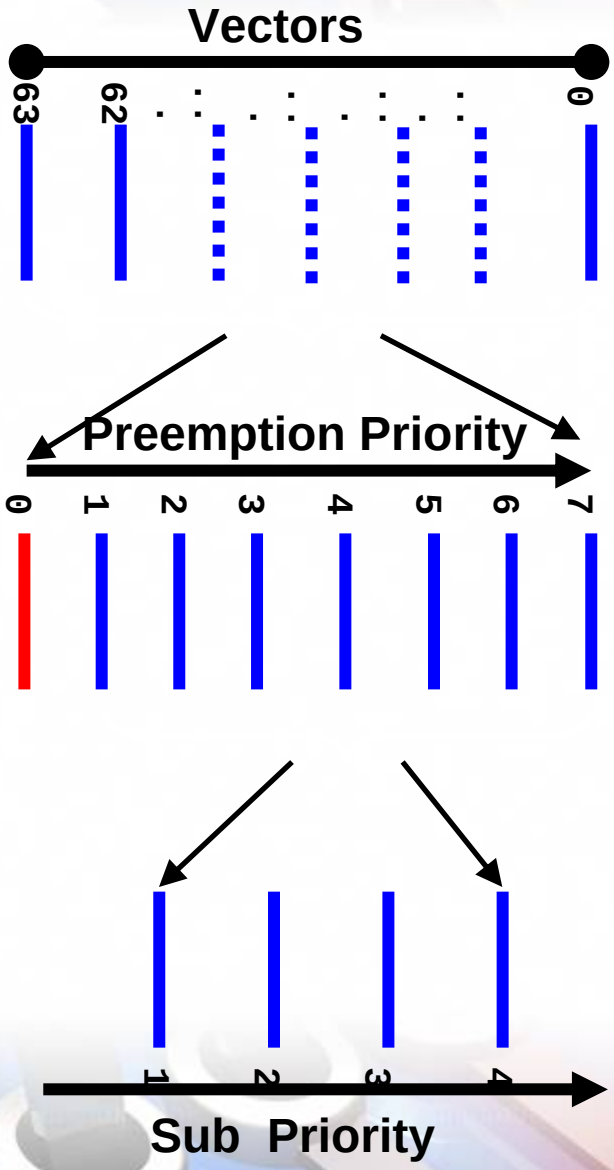


PIC32 BUS Matrix



PIC32 Interrupts

- Up to 96 interrupt source
- Up to 64 interrupt vectors
- Single or multi-vector option
- With multi-vector, each vector has 7 priority operating levels
  - Each priority has 4 sub-priorities
- User selectable location of Interrupt Service Routine
  - Flash execution
  - RAM execution
- Level 7 interrupt uses a shadow register set

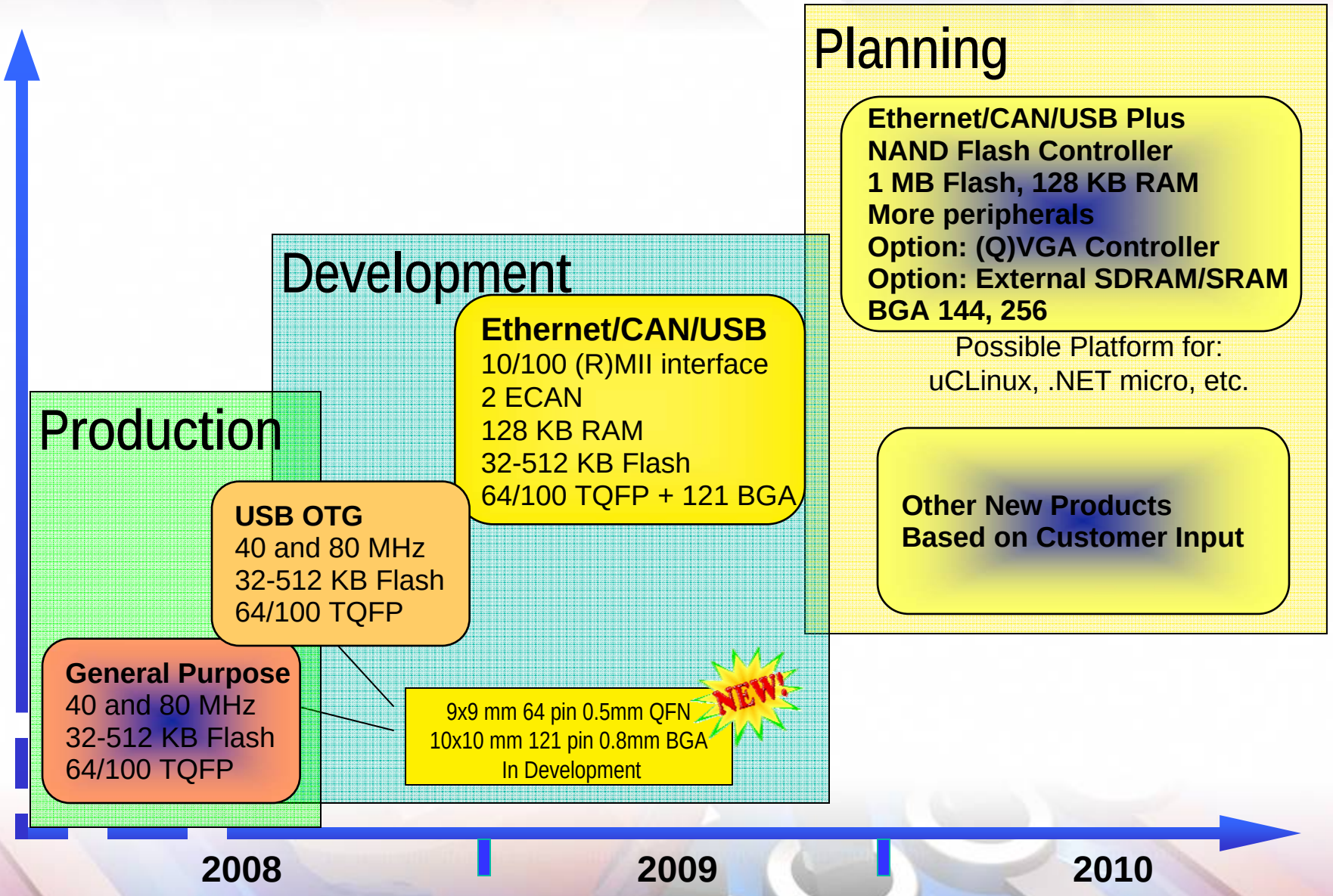


PIC32 Peripherals

- 16-bit timers
- Input capture
- Output compare/PWM
- SPI
- I^2C™ with address masking
- UART
- Real-Time Clock and Calendar
- Programmable Cyclic Redundancy Checker (CRC)
- DMA
- Analog-to-Digital Converter
  - 10-bit, 500 ksps
- Comparators with voltage references

PIC24/dsPIC® DSC Peripheral Set

PIC32 Roadmap



32-bit Software Tools

- **MPLAB® IDE**
  - Same functionality as for the 8-bit, 16-bit and now 32-bit microcontrollers
- **Compilers**
  - PIC32
  - 3rd party compilers
    - HI-TECH
    - Green Hills
    - Ashling
- **RTOS**
  - Thread-X
  - embOS
  - CMX
- **Software Stacks**
  - USB
  - TCP/IP
- **Software Libaries**
  - Speech Encoding
  - Graphics
  - GoFast

32-bit Hardware Tools

- **Programmers & Debuggers**
  - MPLAB® REAL ICE™ in-circuit emulator
  - MPLAB ICD 2
  - PICkit™ 2
- **Programmers only**
  - PM3
- **Starter Kits**
  - PIC32F Starter Kit
- **Demo boards**
  - Explorer 16
- **PICtail™ Plus Daughter Boards**

Same Hardware Tools used by the 8-bit and 16-bit PIC® microcontrollers

Questions

Thank You

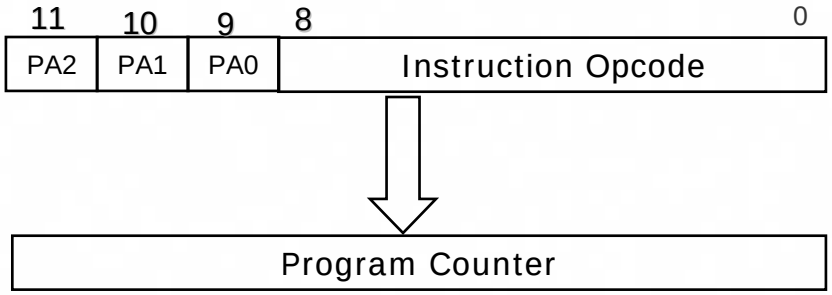
Supplemental Material

Program Counter Modification on 8-bit Architectures

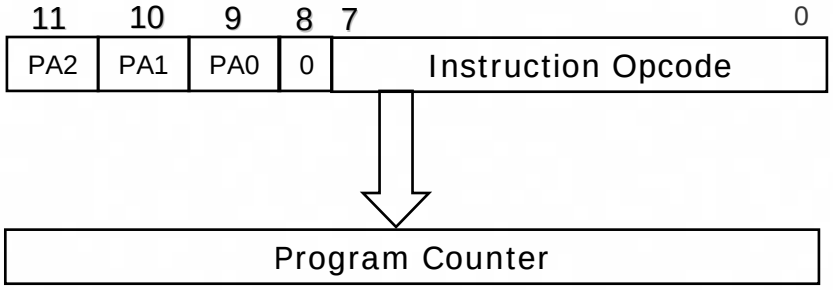
Baseline PS – Modifying the PC

- Normal instruction execution increments by 1
  - PC = PC + 1
  - Normal execution is not paging dependant
- GOTO instruction
  - PC<8:0> are derived from the instruction
  - PC<11:9> are derived from the banking bits in the STATUS register
- CALL or Modify PCL
  - PC<7:0> are derived from the instruction
  - PC<8> is set to '0'
  - PC<11:9> are derived from the banking bits in the STATUS register
- RETLW
  - PC<11:0> is restored (no paging issues on return)

GOTO Instruction



CALL Instruction

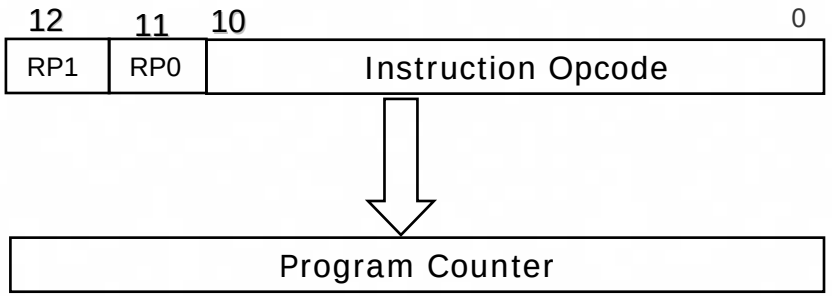


Limits CALL to the first 256 words of each page

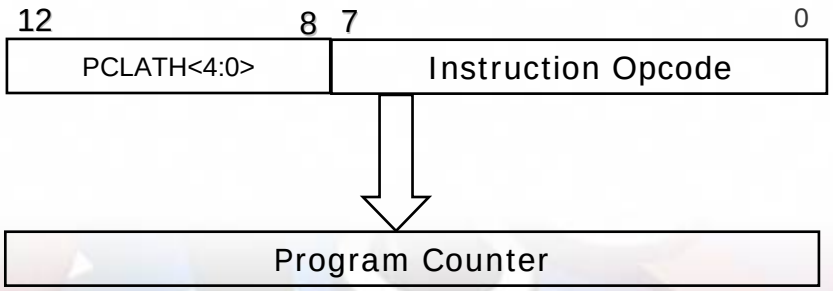
Mid-Range Program Memory - New

- Normal instruction execution increments by 1
  - PC = PC + 1
  - Normal execution is not paging dependant
- GOTO and CALL instructions
  - PC<10:0> are derived from the instruction
  - PC<12:11> are derived from the PCLATH<4:3> register bits
- Modify PCL
  - PC<7:0> are derived from the instruction
  - PC<12:8> are derived from the PCLATH<4:0> register bits
- RETURN, RETLW, RETFIE
  - PC<11:0> is restored on any of these instruction (no paging issues)

GOTO and CALL Instructions



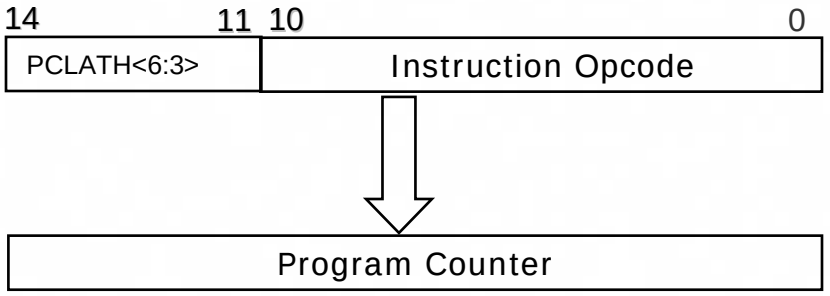
Modify PCL Instruction



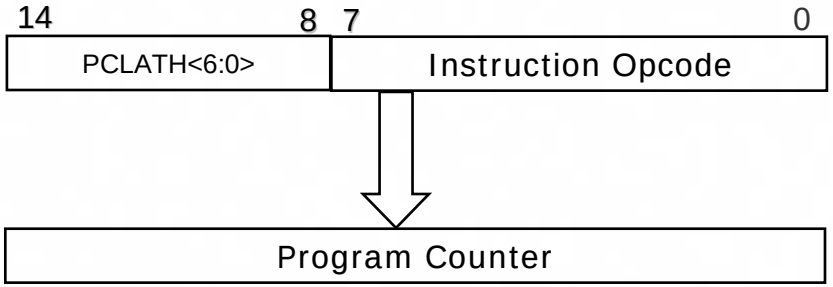
Mid-Range - 1XXX Program Memory - New

- Normal instruction execution increments by 1
  - PC = PC + 1
- GOTO and CALL instructions
  - PC<10:0> are derived from the instruction
  - PC<14:11> are derived from the PCLATH<6:3> register bits
- Modify PCL
  - PC<7:0> are derived from the instruction
  - PC<14:8> are derived from the PCLATH<6:0> register bits
- RETURN, RETLW, RETFIE instructions
  - No paging or banking issues

GOTO and CALL Instructions



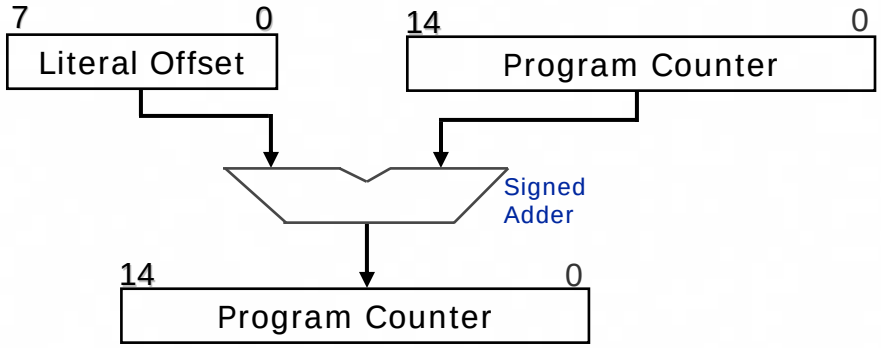
Modify PCL Instruction



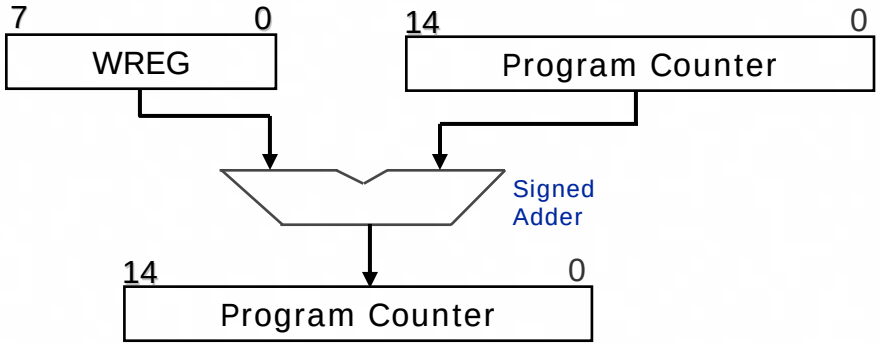
Mid-Range – 1XXX Program

- BRA N
  - Always branch to PC + N
  - Range is -256 < N < 256
  - No paging issues
- BRW
  - Always branch to PC + W (unsigned)
  - Fast lookup tables/State Machines
  - No paging issues
- CALLW
  - Call to PCLATH: W
  - Fast Lookup Tables/State Machines

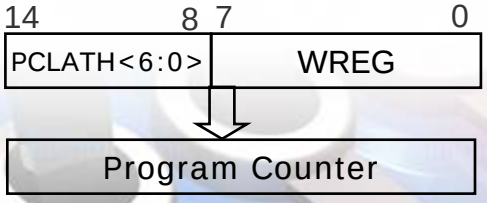
BRA Instruction



BRA W Instruction



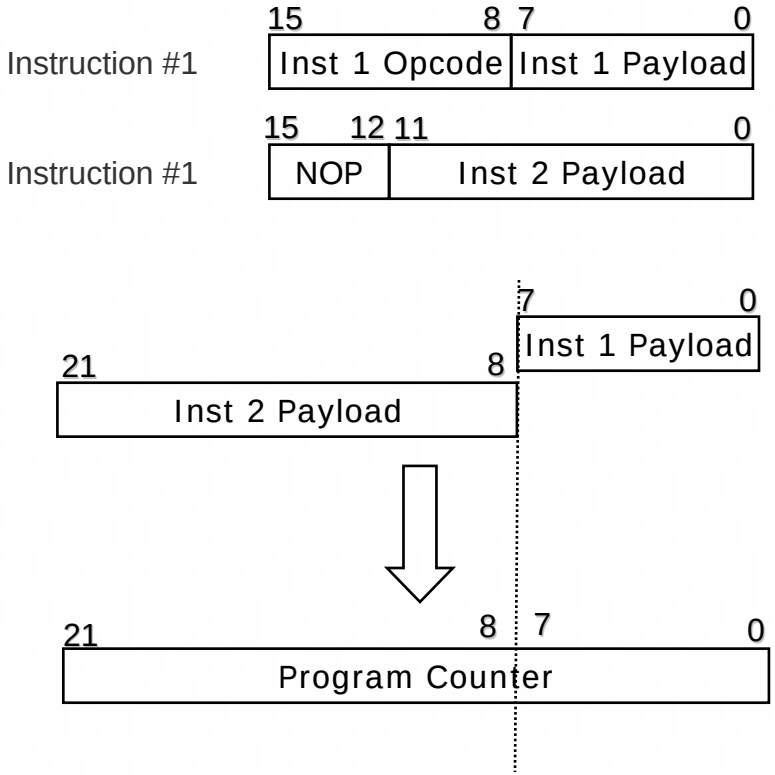
CALLW Instruction



Enhanced PIC18 Program Memory - New

- Normal instruction execution increments by 2
  - PC = PC + 2
  - PC is now byte aligned
- GOTO and CALL instructions
  - 2 word instructions
  - Entire destination PC is contained in the opcode
  - 1st instruction contains opcode and lower 8 bits of destination
  - 2nd instruction contains a 4-bit header and upper 12 bits of destination
- Modify PCL
  - PC<7:0> are derived from the instruction
  - PC<14:8> are derived from the PCLATH<6:0> register bits

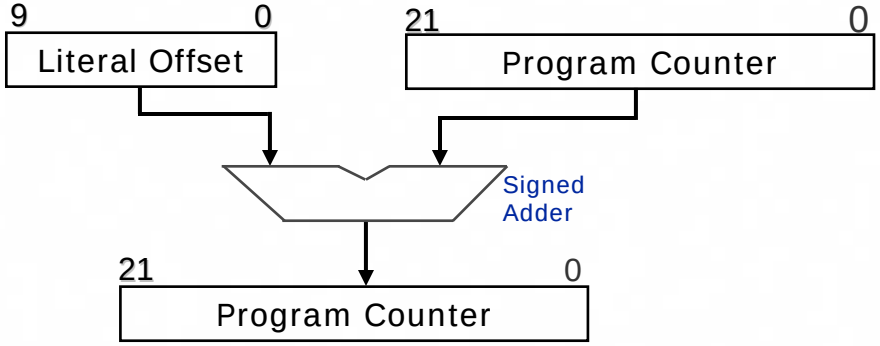
GOTO and CALL Instructions



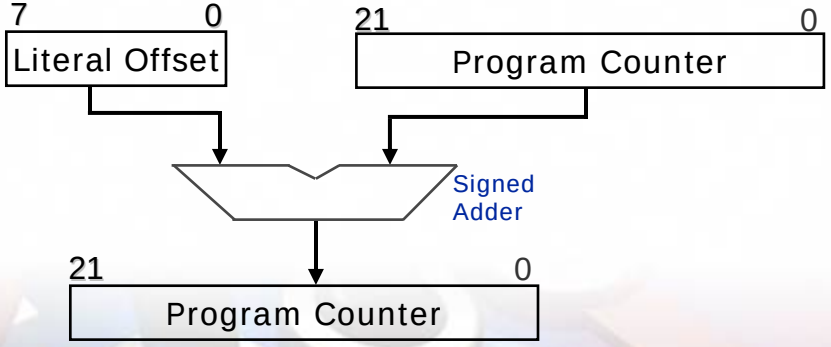
Enhanced PIC18 Program Memory - New

- BRANCH instructions
  - Always branch to PC + N
  - Multiple branch conditions;
    - IF CARRY
    - IF NOT CARRY
    - IF NEGATIVE
    - IF NOT NEGATIVE
    - IF OVERFLOW
    - IF NOT OVERFLOW
    - IF ZERO
    - IF NOT ZERO
    - UNCONDITIONAL
- RCALL
  - Always branch to PC + N
  - Range is -1024 < N < 1023
  - No paging issues
  - Stack is updated

Unconditional BRANCH Instruction



Conditional BRANCH & RCALL Instructions



Trademarks