INTRODUCTION

CMOS devices have been used for many years in applications where the primary concerns were low power consumption, wide power–supply range, and high noise immunity. However, metal–gate CMOS (MC14000 series) is too slow for many applications. Applications requiring high–speed devices, such as microprocessor memory decoding, had to go to the faster families such as LSTTL. This meant sacrificing the best qualities of CMOS. The next step in the logic evolution was to introduce a family of devices that were fast enough for such applications, while retaining the advantages of CMOS. The results of this change can be seen in Table 1 where HSCMOS devices are compared to standard (metal–gate) CMOS, LSTTL, and ALS.

The Motorola CMOS evolutionary process shown in Figure 1 indicates that one advantage of the silicon–gate process is device size. The High–Speed CMOS (HSCMOS) device is about half the size of the metal–gate predecessor, yielding significant chip area savings. The silicon–gate process allows smaller gate or channel lengths due to the self–aligning gate feature. This process uses the gate to define the channel during processing, eliminating registration errors and, therefore, the need for gate overlaps. The elimination of the gate overlap significantly lowers the gate capacitance, resulting in higher speed capability. The smaller gate length also results in higher drive capability per unit gate width, ensuring more efficient use of chip area. Immunity enhancements to electrostatic discharge (ESD) damage and latch up are ongoing. Precautions should still be taken, however, to guard against electrostatic discharge and latch up.

Motorola's High–Speed CMOS family has a broad range of functions from basic gates, flip–flops, and counters to bus–compatible devices. The family is made up of devices that are identical in pinout and are functionally equivalent to LSTTL devices, as well as the most popular metal–gate devices not available in TTL. Thus, the designer has an excellent alternative to existing families without having to become familiar with a new set of device numbers.

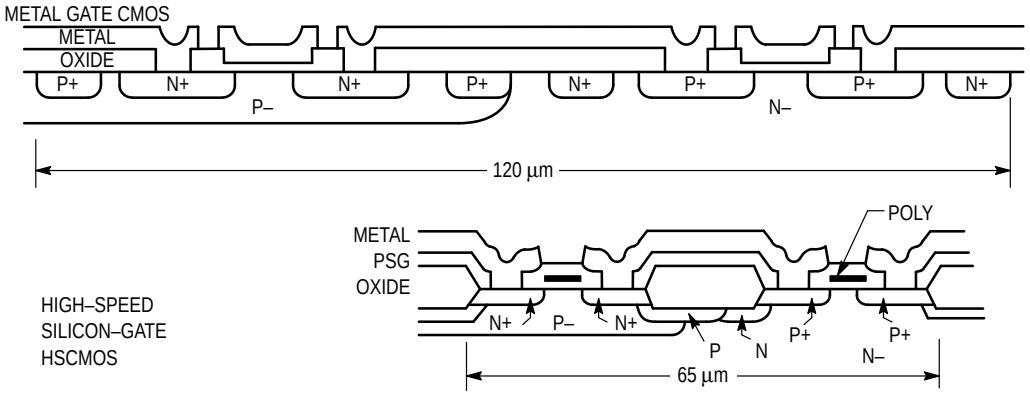


Figure 1. CMOS Evolution

HANDLING PRECAUTIONS

High–Speed CMOS devices, like all MOS devices, have an insulated gate that is subject to voltage breakdown. The gate oxide for HSCMOS devices breaks down at a gate–source potential of about 100 volts. Some device inputs are protected by a resistor–diode network (Figure 2). New input protection structure deletes the poly resistor (Figure 3) Using the test setup shown in Figure 4, the inputs typically withstand a > 2 kV discharge.

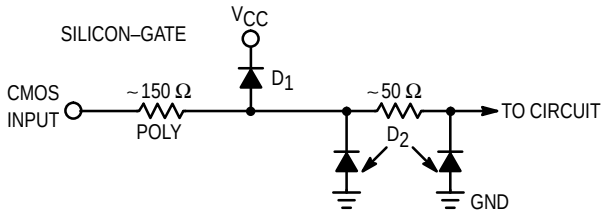


Figure 2. Input Protection Network

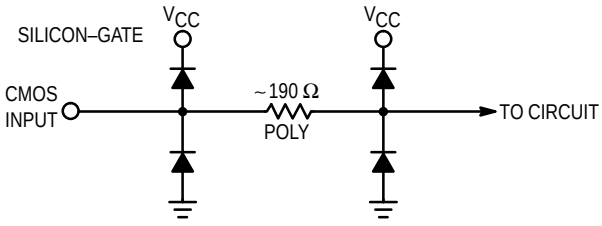


Figure 3. New Input Protection Network

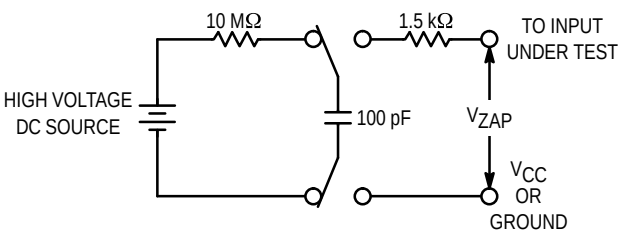


Figure 4. Electrostatic Discharge Test Circuit

Table 1. Logic Family Comparisons

General Characteristics (1) (All Maximum Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Operating Voltage Range	$V_{CC/EE/DD}$	5 ± 5%	5 ± 5%	3.0 to 18	2.0 to 6.0	V
Operating Temperature Range	T_A	0 to + 70	0 to + 70	– 40 to + 85	– 55 to + 125	°C
Input Voltage (limits)	V_{IH} min	2.0	2.0	3.5[4]	3.5[4]	V
	V_{IL} max	0.8	0.8	1.5[4]	1.0[4]	V
Output Voltage (limits)	V_{OH} min	2.7	2.7	V_{DD} – 0.05	V_{CC} – 0.1	V
	V_{OL} max	0.5	0.5	0.05	0.1	V
Input Current	I_{INH}	20	20	± 0.3	± 1.0	µA
	I_{INL}	– 400	– 200			
Output Current @ V_O (limit) unless otherwise specified	I_{OH}	– 0.4	– 0.4	– 2.1 @ 2.5 V	– 4.0 @ V_{CC} – 0.8 V	mA
	I_{OL}	8.0	8.0	0.44 @ 0.4 V	4.0 @ 0.4 V	mA
DC Noise Margin Low/High	DCM	0.3/0.7	0.3/0.7	1.45[4]	0.90/1.35[4]	V
DC Fanout	—	20	20	50(1)[2]	50(10)[2]	—

Speed/Power Characteristics (1) (All Typical Ratings)

Characteristic	Symbol	TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Quiescent Supply Current/Gate	I_G	0.4	0.2	0.0001	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.0	0.0006	0.001	mW
Propagation Delay	t_p	9.0	7.0	125	8.0	ns
Speed Power Product	—	18	7.0	0.075	0.01	pJ
Clock Frequency (D–F/F)	f_{max}	33	35	4.0	40	MHz
Clock Frequency (Counter)	f_{max}	40	45	5.0	40	MHz

Propagation Delay (1)

Characteristic		TTL		CMOS		Unit
		LS	ALS	MC14000	Hi–Speed	
Gate, NOR or NAND:	**Product No.**	SN74LS00	SN74ALS00	MC14001B	74HC00	—
t_{PLH}/t_{PHL}[(5)]	Typical	(10)[3]	(5)[3]	25	(8)[3] 10	ns
	Maximum	(15)[3]	10	250	(15)[3] 20	
Flip–Flop, D–type:	**Product No.**	SN74LS74	SN74ALS74	MC14013B	74HC74	—
t_{PLH}/t_{PHL}[(5)] (Clock to Q)	Typical	(25)[3]	(12)[3]	175	(23)[2] 25	ns
	Maximum	(40)[3]	20	350	(30)[3] 32	
Counter:	**Product No.**	SN74LS163	SN74ALS163	MC14163B	74HC163	—
t_{PLH}/t_{PHL}[(5)] (Clock to Q)	Typical	(18)[3]	(10)[3]	350	(20)[3] 22	ns
	Maximum	(27)[3]	24	700	(27)[3] 29	

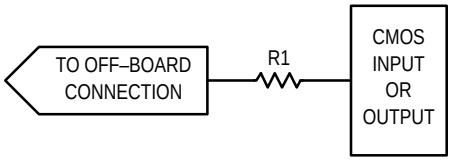
NOTES:
1. Specifications are shown for the following conditions:
   a) V_{DD} (CMOS) = 5.0 V ± 10% for dc tests, 5.0 V for ac tests; V_{CC} (TTL) = 5.0 V ± 5% for dc tests, 5.0 V for ac tests
   b) Basic Gates: LS00 or equivalent
   c) T_A = 25°C
   d) C_L = 50 pF (ALS, HC), 15 pF (LS, 14000 and Hi–Speed)
   e) Commercial grade product
2. ( ) fanout to LSTTL
3. ( ) C_L = 15 pF
4. DC input voltage specifications are proportional to supply voltage over operating range.
5. The number specified is the larger of t_{PLH} and t_{PHL} for each device.

The input protection network uses a polysilicon resistor in series with the input and before the protection diodes. This series resistor slows down the slew rate of static discharge spikes to allow the protection diodes time to turn on. Outputs have a similar ESD protection network except for the series resistor. Although the on–chip protection circuitry guards against ESD damage, additional protection may be necessary once the chip is placed in circuit. Both an external series resistor and ground and V_{CC} diodes, similar to the input protection structure, are recommended if there is a potential of ESD, voltage transients, etc. Several monolithic diode arrays are available from Motorola, such as the MAD130 (dual 10 diode array) or the MAD1104 (dual 8 diode array). These diodes, in chip form, not only provide the necessary protection, but also save board space as opposed to using discrete diodes.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged pins are the easiest to detect. An ESD–damaged pin that has been completely destroyed may exhibit a low–impedance path to V_{CC} or GND. Another common failure mode is a fused or open circuit. The effect of both failure modes is that the device no longer properly responds to input signals. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Generally, another effect of static damage is increased chip leakage currents (I_{CC}).

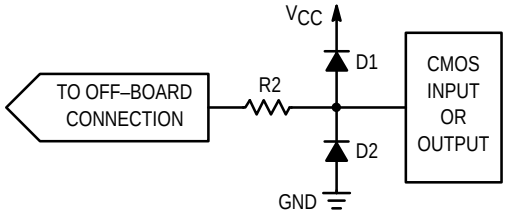
Although the input network does offer significant protection, these devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

1. Wrist straps and equipment logs should be maintained and audited on a regular basis. Wrist straps malfunction and may go unnoticed. Also, equipment gets moved from time to time and grounds may not be reconnected properly.
2. Do not exceed the Maximum Ratings specified by the data sheet.
3. All unused device inputs should be connected to V_{CC} or GND.
4. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
5. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connectors to a PC board are connected to an input or output of a CMOS device, a resistor should be used in series with the input or output. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. The delay is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 5, two possible networks are shown using a series resistor to reduce ESD damage. For convenience, an equation is given for added propagation delay and rise time effects due to series resistance size.



Advantage: Requires minimal area

Disadvantage: R1 > R2 for the same level of protection; therefore, rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:
A digital inputs and outputs
B analog inputs and outputs
C 3–state outputs
D bidirectional (I/O) ports

Propagation Delay and Rise Time vs. Series Resistance

$$R \approx \frac{t}{C \cdot k}$$

where:
R=the maximum allowable series resistance in ohms
t= the maximum tolerable propagation delay or rise time in seconds
C= the board capacitance plus the driven input capacitance in farads
k= 0.7 for propagation delay calculations
k= 2.3 for rise time calculations

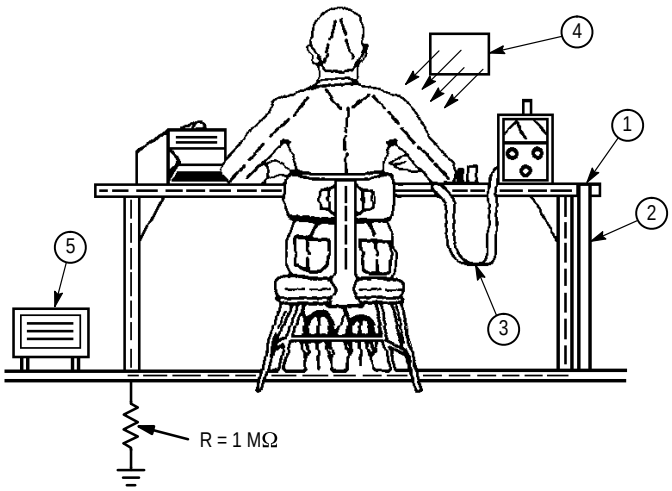
Figure 5. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility

6. All CMOS devices should be stored or transported in materials that are antistatic or conductive. CMOS devices must not be inserted into conventional plastic “snow”, Styrofoam, or plastic trays, but should be left in their original container until ready for use.
7. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, because a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are essential and should be tested daily. See Figure 6 for an example of a typical work station.
8. Nylon or other static generating materials should not come in contact with CMOS devices.
9. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static buildup by using ionized air blowers, anti–static sprays, and room humidifiers. All conductive parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to earth ground.
10. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
11. When lead straightening or hand soldering is necessary, provide ground straps for the apparatus used and be sure that soldering iron tips are grounded.
12. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to earth ground.
    b. The loading and unloading work benches should have conductive tops grounded to earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic or conductive containers prior to being moved to subsequent stations.
13. The following steps should be observed during board–cleaning operations:
    a. Vapor degreasers and baskets must be grounded to earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic or conductive container.
    d. Cleaned assemblies should be placed in antistatic or conductive containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when a static eliminator using ionized air is directed at the printed circuit board.
14. The use of static detection meters for production line surveillance is highly recommended.
15. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
16. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
17. Double check test equipment setup for proper polarity of V_{CC} and GND before conducting parametric or functional testing.
18. Do not recycle shipping rails. Repeated use causes deterioration of their antistatic coating. Exception: carbon rails (black color) may be recycled to some extent. This type of rail is conductive and antistatic.

RECOMMENDED READING

“Requirements for Handling Electrostatic–Discharge Sensitive (ESDS) Devices” EIA Standard EIA–625
Available by writing to:
Global Engineering Documents
15 Inverness Way East
Englewood, Colorado 80112
Or by calling:
1–800–854–7179 in the USA or CANADA or
(303) 397–7956 International

S. Cherniak, “A Review of Transients and Their Means of Suppression”, Application Note–843, Motorola Semiconductor Products Inc., 1982.



NOTES:
1. 1/16 inch conductive sheet stock covering bench-top work area.
2. Ground strap.
3. Wrist strap In contact with skin.
4. Static neutralizer. (ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside a building to be less than outside humidity.

Figure 6. Typical Manufacturing Work Station

POWER SUPPLY SIZING

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive power supplies without cooling fans. In addition, batteries may be used as either a primary power source or as a backup.

The maximum recommended power supply voltage for HC devices is 6.0 V and 5.5 V for HCT devices. Figure 7 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current for the latch–up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided. The low–current junction avalanche region is between 10 and 14 volts at T_A = 25°C.

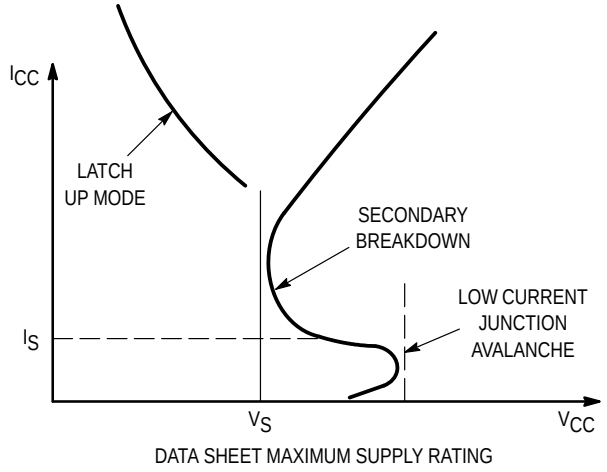


Figure 7. Secondary Breakdown Characteristics

In an ideal system design, the power supply should be designed to deliver only enough current to ensure proper operation of all devices. The obvious benefit of this type of design is cost savings.

BATTERY SYSTEMS

HSCMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery–operated systems.

1. The recommended power supply voltages should be observed. For battery backup systems such as the one in Figure 8, the battery voltage must be at least 2.7 volts (2 volts for the minimum power supply voltage and 0.7 volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should use the HC4049 or HC4050 buffers (Figure 8). If line power is interrupted, CMOS System A and Buffer A lose power. However, CMOS System B and Buffer B remain active due to the battery backup. Buffer A protects System A from System B by blocking active inputs while the circuit is not powered up. Also, if the power supply voltage drops below the battery voltage, Buffer A acts as a level translator for the outputs from System B. Buffer B acts to protect System B from any overvoltages which might exist. Both buffers may be replaced with current–limiting resistors, however power consumption is increased and propagation delays are lengthened.
3. Outputs that are subject to voltage levels above V_{CC} or below GND should be protected with a series resistor and/or clamping diodes to limit the current to an acceptable level.

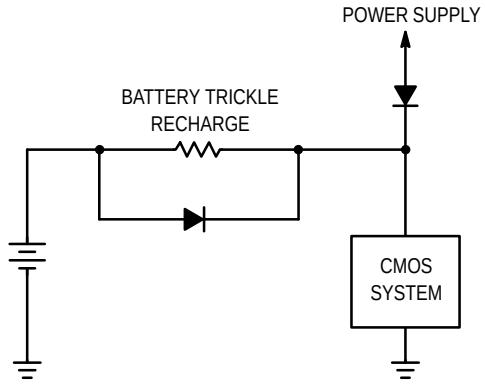


Figure 8. Battery Backup System

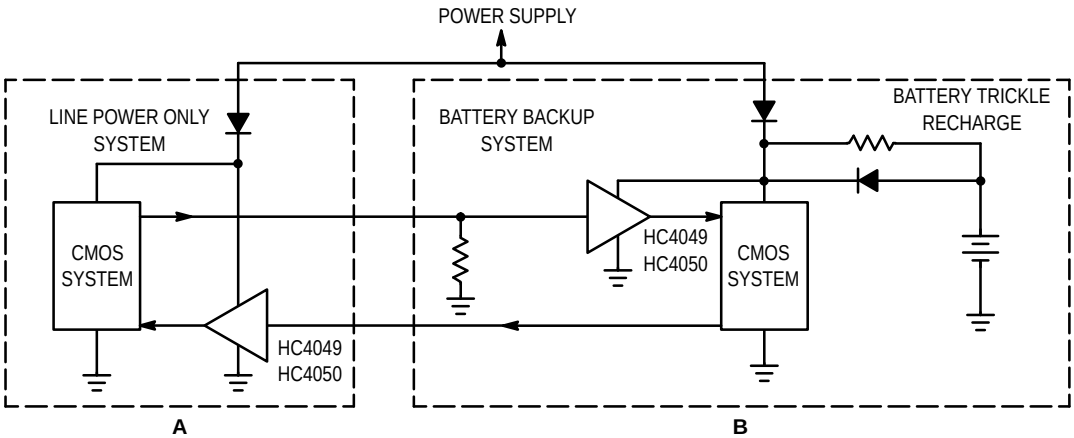


Figure 9. Battery Backup Interface

C_{PD} POWER CALCULATION

Power consumption for HSCMOS is dependent on the power–supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC} \bullet V_{CC}$, and the switching power required by each device within the package. For large systems, the most timely method is to bread–board the circuit and measure the current required under a variety of conditions.

The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD}) V_{CC}^2 f$$

where: P_D = power dissipated in μW

C_L = total load capacitance present at the output in pF

C_{PD} = a measure of internal capacitances, called power dissipation capacitance, given in pF

V_{CC} = supply voltage in volts

f = frequency in MHz

If the devices are tested at a sufficiently high frequency, the dc supply current contributes a negligible amount to the overall power consumption and can therefore be ignored. For this reason, the power consumption is measured at 1 MHz and the following formula is used to determine the device's C_{PD} value:

$$C_{PD} = \frac{I_{CC}\ (\text{dynamic})}{V_{CC} \bullet f} - C_L$$

The resulting power dissipation is calculated using C_{PD} as follows under no–load conditions.

(HC) $P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC}$

(HCT) $P_D = C_{PD} V_{CC}^2 f + V_{CC} I_{CC} + \Delta I_{CC} V_{CC} (\delta_1 + \delta_2 + \ldots + \delta_n)$

where the previously undefined variable, δ_n is the duty cycle of each input applied at TTL/NMOS levels.

The power dissipation for analog switches switching digital signals is the following:

(HC) $P_D = C_{PD} V_{CC}^2 f_{in} + (C_S + C_L) V_{CC}^2 f_{out} + V_{CC} I_{CC}$

where: C_S = digital switch capacitance, and

f_{out} = output frequency

In order to determine the C_{PD} of a single section of a device (i.e., one of four gates, or one of two flip–flops in a package), Motorola uses the following procedures as defined by JEDEC. Note: "biased" as used below means "tied to V_{CC} or GND."

Gates:	Switch one input while the remaining input(s) are biased so that the output(s) switch.
Latches:	Switch the enable and data inputs such that the latch toggles.
Flip–Flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Decoders/ Demultiplexers:	Switch one address pin which changes two outputs.
Data Selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.
Analog Switches:	Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance.
Counters:	Switch the clock pin with the other inputs biased so that the device counts.
Shift Registers:	Switch the clock while alternating the input so that the device shifts alternating 1s and 0s through the register.
Transceivers:	Switch only one data input. Place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Encoders:	Switch the lowest priority output.
Display Drivers:	Switch one input so that approximately one–half of the outputs change state.
ALUs/Adders:	Switch the least significant bit. The remaining inputs are biased so that the device is alternately adding 0000 (binary) or 0001 (binary) to 1111 (binary).

On HSCMOS data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip–flops, etc.) within the package. An example of calculating the package power requirement is given using the 74HC00, as shown in Figure 10.

From the data sheet:

I_{CC} = 2 μA at room temperature (per package)

C_{PD} = 22 pF per gate

$P_D = (C_{PD} + C_L) V_{CC}^2 f + V_{CC} I_{CC}$

$P_{D1} = (22\ \text{pF} + 50\ \text{pF})(5\ \text{V})^2 (1\ \text{kHz})$ 1.8 μW

$P_{D2} = (22\ \text{pF} + 50\ \text{pF})(5\ \text{V})^2 (1\ \text{MHz})$ 1800 μW

$P_{D3} = (22\ \text{pF})\ (5\ \text{V})^2 (0\ \text{Hz}) = 0$ μW

$P_{D4} = (22\ \text{pF})(5\ \text{V})^2 (0\ \text{Hz}) = 0$ μW

$P_D(\text{total}) = V_{CC} I_{CC} + PD1 + PD2 + PD3 + PD4$

= 10 μW + 1.8 μW + 1800 μW + 0 μW

= 1812 μW

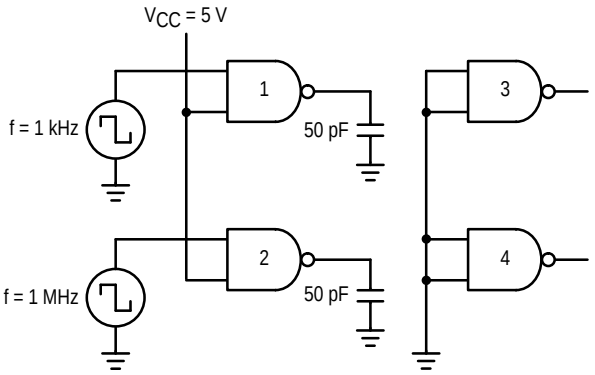


Figure 10. Power Consumption Calculation Example

As seen by this example, the power dissipated by CMOS devices is dependent on frequency. When operating at very high frequencies, HSCMOS devices can consume as much power as LSTTL devices, as shown in Figure 11. The power savings of HSCMOS is realized when used in a system where only a few of the devices are actually switching at the system frequency. The power consumption savings comes from the fact that for CMOS, only the devices that are switching consume significant power.

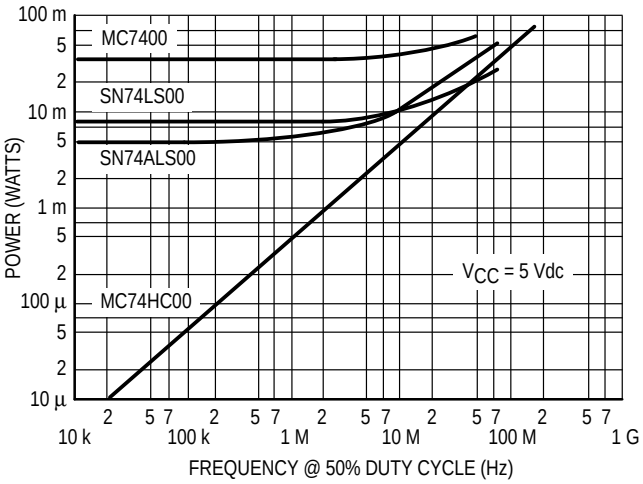


Figure 11. Power Consumption Vs. Input Frequency for TTL, LSTTL, ALs, and HSCMOS

INPUTS

A basic knowledge of input and output structures is essential to the HSCMOS designer. This section deals with the various input characteristics and application rules regarding their use. Output characteristics are discussed in the section titled **Outputs**.

All standard HC, HCU and HCT inputs, while in the recommended operating range (GND ≤ V_{in} ≤ V_{CC}), can be modeled as shown in Figure 12. For input voltages in this range, diodes D1 and D2 are modeled as resistors representing the high–impedance of reverse biased diodes. The maximum input current is 1 µA, worst case over temperature, when the inputs are at V_{CC} or GND, and V_{CC} = 6 V.

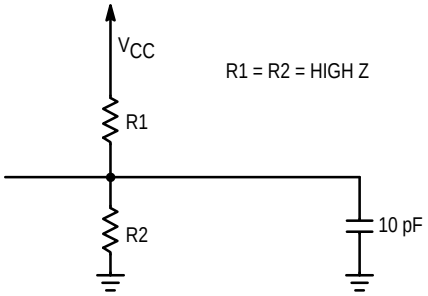


Figure 12. Input Model for GND ≤ V_{in} ≤ V_{CC}

When CMOS inputs are left open–circuited, the inputs may be biased at or near the typical CMOS switchpoint of 0.45 V_{CC} for HC devices or 1.3 V for HCT devices. At this switchpoint, both the P–channel and the N–channel transistors are conducting, causing excess current drain. Due to the high gain of the buffered devices (see Figure 13), the device can go into oscillation from any noise in the system, resulting in even higher current drain.

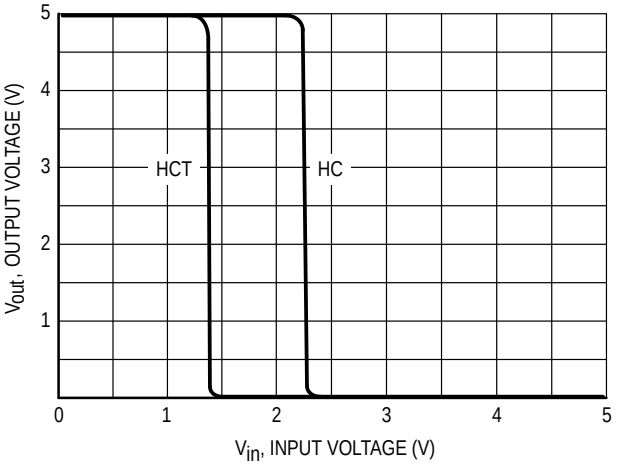


Figure 13. Typical Transfer Characteristics for Buffered Devices

For these reasons, all unused HC/HCT inputs should be connected either to V_{CC} or GND. For applications with inputs going to edge connectors, a 100 kΩ resistor to GND should be used, as well as a series resistor (R_S) for static protection and current limiting (see **Handling Precautions**, this chapter, for series resistor consideration). The resistors should be configured as in Figure 14.

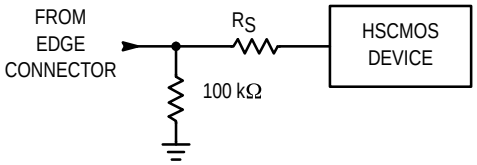


Figure 14. External Protection

For inputs outside of the recommended operating range, the CMOS input is modeled as in Figure 15 and Figure 16.

Current flows through diode D1 or D2 whenever the input voltage exceeds V_{CC} or drops below GND enough to forward bias either D1 or D2. The device inputs are guaranteed to withstand from GND – 1.5 V to V_{CC} + 1.5 V and a maximum current of 20 mA. If this maximum rating is exceeded, the device could go into a latch–up condition. (See **CMOS Latch Up**, this chapter.) Voltage should never be applied to any input or output pin before power has been applied to the device's power pins. Bias on input or output pins should be removed before removing the power. However, if the input current is limited to less than 20 mA, and this current only lasts for a brief period of time (< 100 ms), no damage to the device occurs.

Another specification that should be noted is the maximum input rise (t_r) and fall (t_f) times. Figure 17 shows the results of exceeding the maximum rise and fall times recommended by Motorola or contained in JEDEC Standard No. 7A. The reason for the oscillation on the output is that as the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input line is amplified, and is passed through to the output. This oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed the maximum specified rise or fall times, Schmitt–triggered devices such as Motorola's HC14 and HC132 are recommended.

OUTPUTS

All HSCMOS outputs, with the exception of the HCU04, are buffered to ensure consistent output voltage and current specifications across the family. All buffered outputs have guaranteed output voltages of V_{OL} = 0.1 V and V_{OH} = V_{CC} – 0.1 V for $|I_{out}| \leq$ 20 μA ($\leq$ 20 HSCMOS loads). The output drives for standard drive devices are such that 54HC/HCT and 74HC/HCT devices can drive ten LSTTL loads and maintain a $V_{OL} \leq$ 0.4 V and $V_{OH} \geq V_{CC}$ – 0.8 V across the full temperature range; bus–driver devices can drive fifteen LSTTL loads under the same conditions.

The outputs of all HSCMOS devices are limited to externally forced output voltages of $-0.5 \leq V_{out} \leq V_{CC} + 0.5$ V. For externally forced voltages outside this range a latch up condition could be triggered. (See **CMOS Latch Up**, this chapter.)

The maximum rated output current given on the individual data sheets is 25 mA for standard outputs and 35 mA for bus drivers. The output short circuit currents of these devices typically exceed these limits. The outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dissipation is not violated. (See individual data sheets for maximum power dissipation ratings.)

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETS), devices within the same package may be paralleled. Paralleling devices in different packages may result in devices switching at different points on the input voltage waveform, creating output short circuits and yielding undesirable output voltage waveforms.

As a design aid, output characteristic curves are given for both P–channel source and N–channel sink currents. The curves given include expected minimum curves for T_A = 25°C, 85°C, and 125°C, as well as typical values for T_A = 25°C. For temperatures < 25°C, use the 25°C curves. These curves, Figure 18 through Figure 29, are intended as design aids, not as guarantees. Unused output pins should be open–circuited (floating).

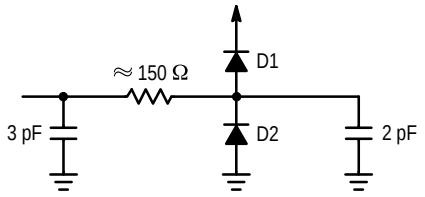


Figure 15. Input Model for $V_{in} > V_{CC}$ or $V_{in} < GND$

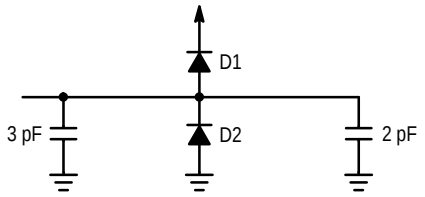


Figure 16. Input Model for New ESD Enhanced Circuits

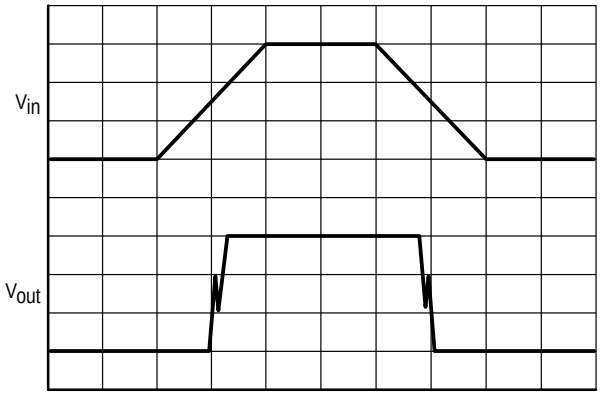


Figure 17. Maximum Rise Time Violation

STANDARD OUTPUT CHARACTERISTICS

N–CHANNEL SINK CURRENT

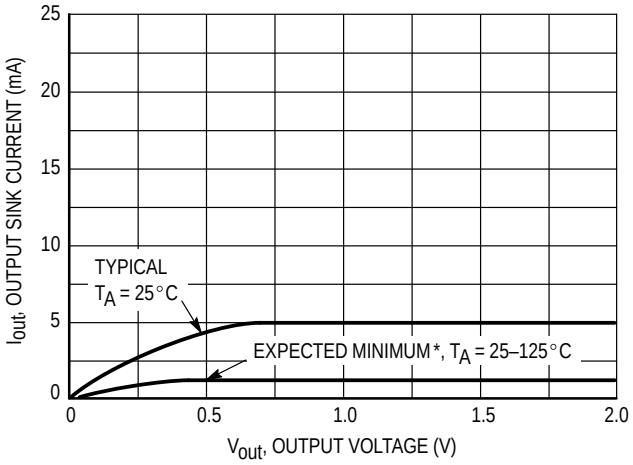


Figure 18. V_{GS} = 2.0 V

P–CHANNEL SOURCE CURRENT

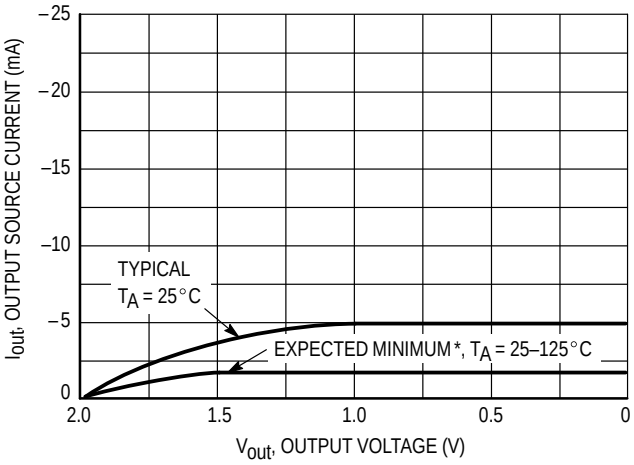


Figure 19. V_{GS} = – 2.0 V

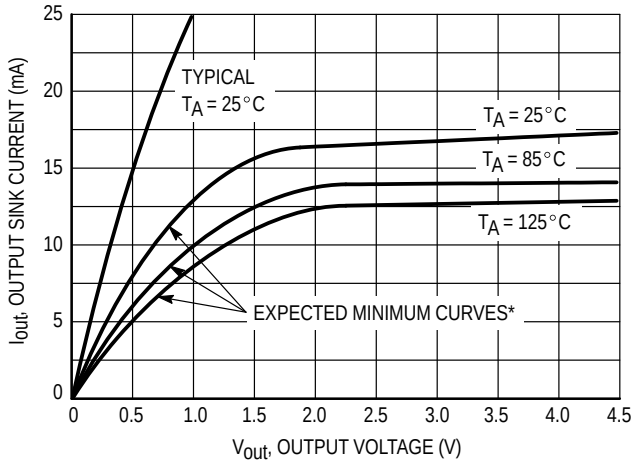


Figure 20. V_{GS} = 4.5 V

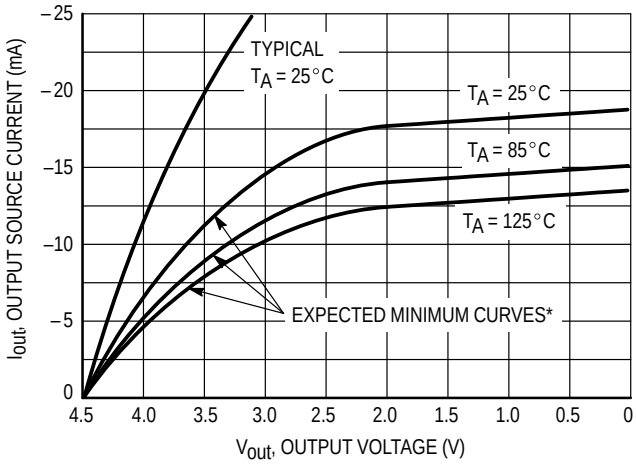


Figure 21. V_{GS} = – 4.5 V

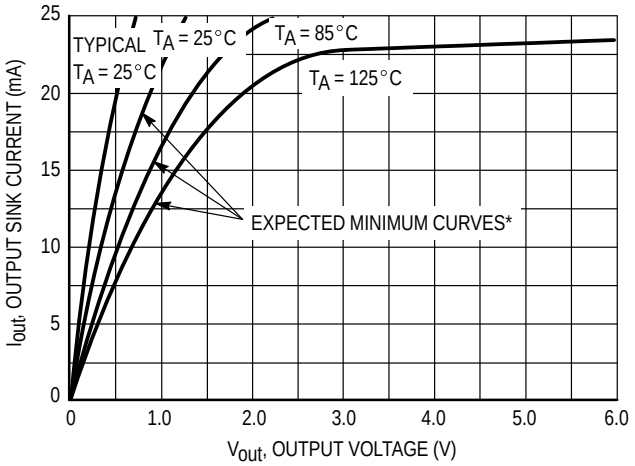


Figure 22. V_{GS} = 6.0 V

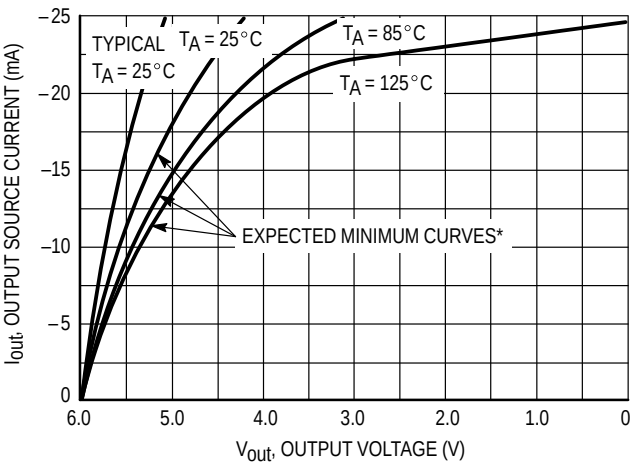


Figure 23. V_{GS} = – 6.0 V

*The expected minimum curves are not guarantees, but are design aids.

BUS–DRIVER OUTPUT CHARACTERISTICS

N–CHANNEL SINK CURRENT

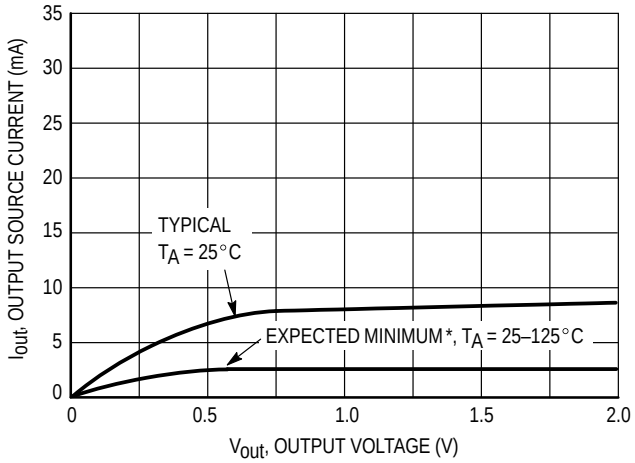


Figure 24. V_{GS} = 2.0 V

P–CHANNEL SOURCE CURRENT

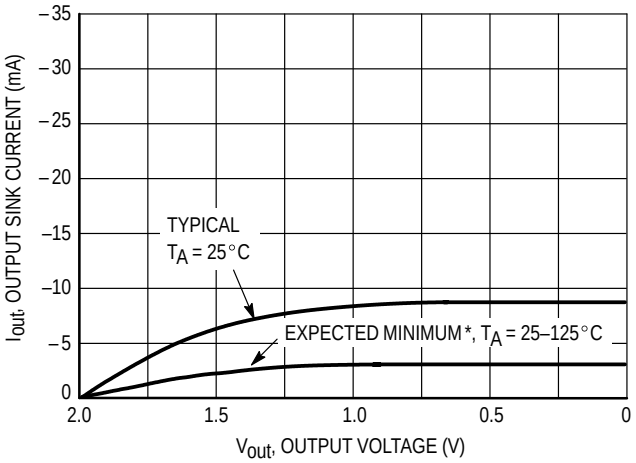


Figure 25. V_{GS} = – 2.0 V

2

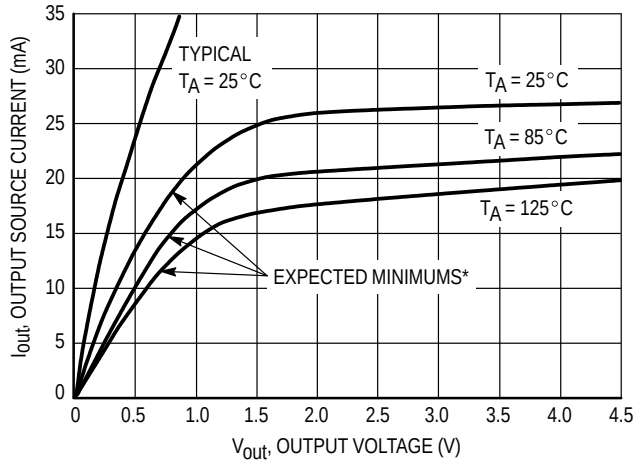


Figure 26. V_{GS} = 4.5 V

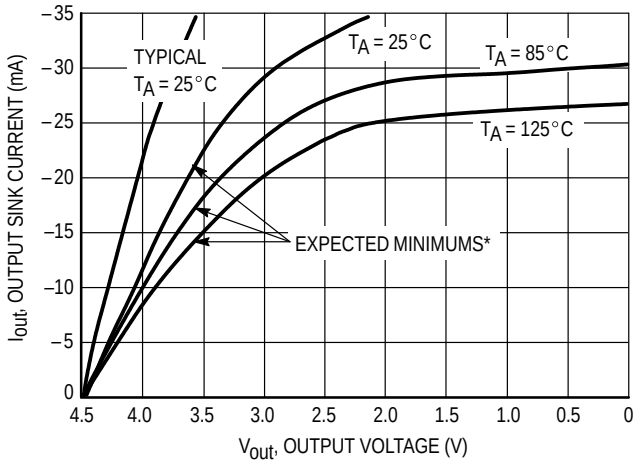


Figure 27. V_{GS} = – 4.5 V

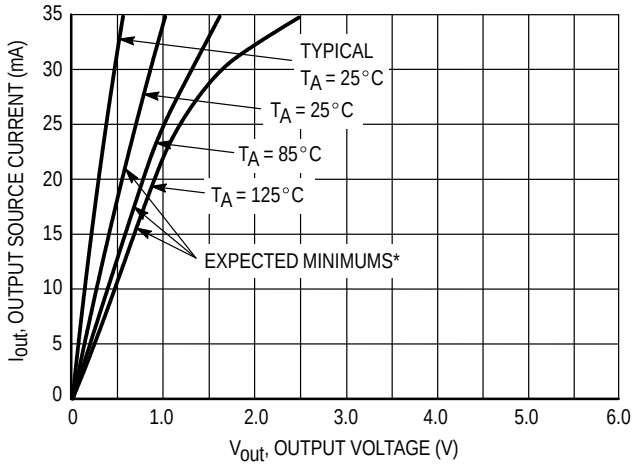


Figure 28. V_{GS} = 6.0 V

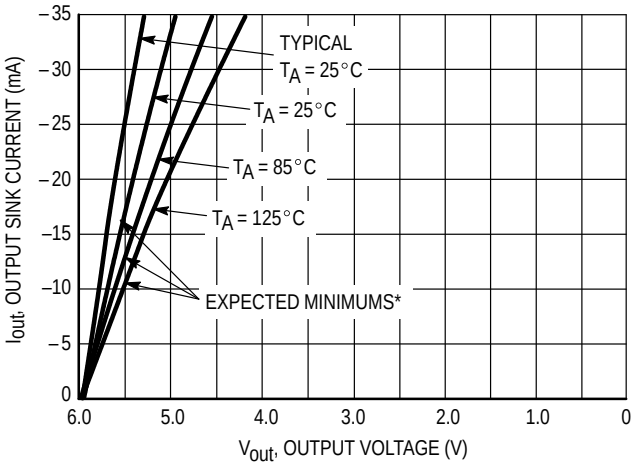


Figure 29. V_{GS} = – 6.0 V

*The expected minimum curves are not guarantees, but are design aids.

3–STATE OUTPUTS

Some HC/HCT devices have outputs that can be placed into a high–impedance state. These 3–state output devices are very useful for gang connecting to a common line or bus. When enabled, these output pins can be considered as ordinary output pins; as such, all specifications and precautions of standard output pins should be followed. When disabled (high–impedance state), these outputs can be modeled as in Figure 30. Output leakage current (10 μA worst case over temperature) as well as 3–state output capacitance must be considered in any bus design.

When power is interrupted to a 3–state device, the bus voltage is forced to between GND and V_{CC} + 0.7 V regardless of the previous output state.

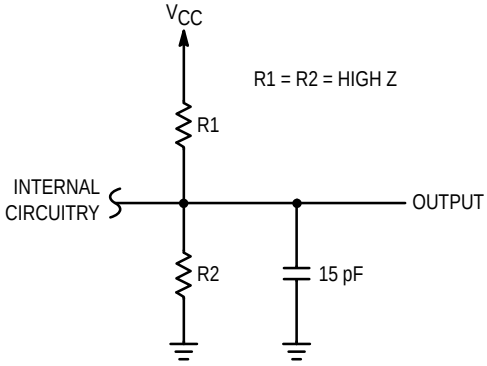


Figure 30. Model for Disabled Outputs

OPEN–DRAIN OUTPUTS

Motorola provides several devices that are designed only to sink current to GND. These open–drain output devices are fabricated using only an N–channel transistor and a diode to V_{CC} (Figure 31). The purpose of the diode is to provide ESD protection. Open–drain outputs can be modeled as shown in Figure 32.

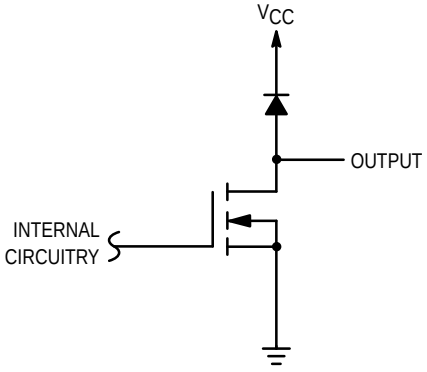


Figure 31. Open–Drain Output

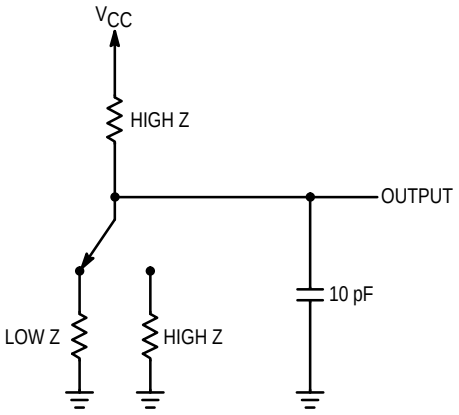


Figure 32. Model of Open–Drain Output

INPUT/OUTPUT PINS

Some HC/HCT devices contain pins that serve both as inputs and outputs of digital logic. These pins are referred to as digital I/O pins. The logic level applied to a control pin determines whether these I/O pins are selected as inputs or outputs.

When I/O pins are selected as outputs, these pins may be considered as standard CMOS outputs. When selected as inputs, except for an increase in input leakage current and input capacitance, these pins should be considered as standard CMOS inputs. These increases come from the fact that a digital I/O pin is actually a combination of an input and a 3–state output tied together (see Figure 33).

As stated earlier, all HC/HCT inputs must be connected to an appropriate logic level. This could pose a problem if an I/O pin is selected as an input while connected to an improperly terminated bus.

Motorola recommends terminating HC/HCT–type buses with resistors to V_{CC} or GND of between 1 kΩ to 1 MΩ in value. The choice of resistor value is a trade–off between speed and power consumption (see **Bus Termination**, this chapter).

Some Motorola devices have analog I/O pins. These analog I/O pins should not be confused with digital I/O pins. Analog I/O pins may be modeled as in Figure 34. These devices can be used to pass analog signals, as well as digital signals, in the same manner as mechanical switches.

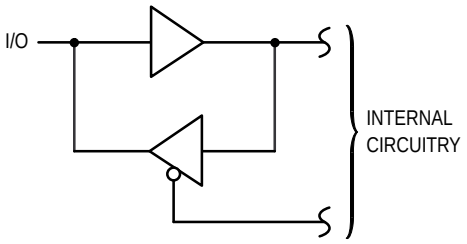


Figure 33. Typical Digital I/O Pin

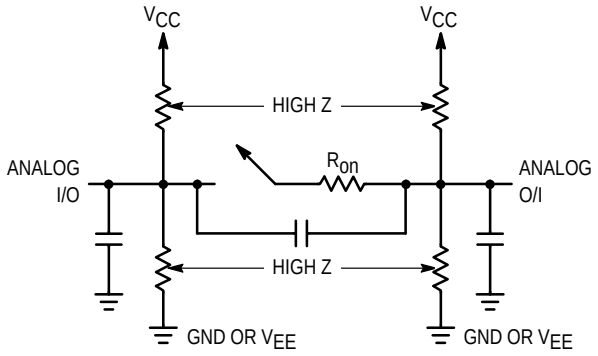


Figure 34. Analog I/O Pin

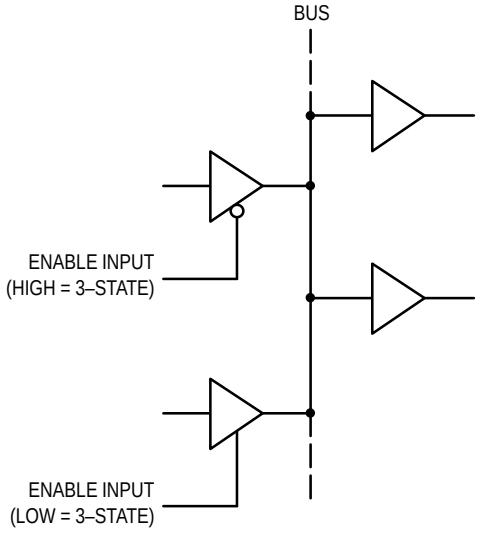


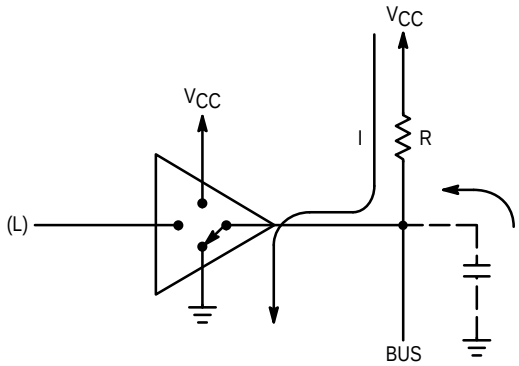
Figure 35. Typical Bus Line with 3–State Bus Drivers

BUS TERMINATION

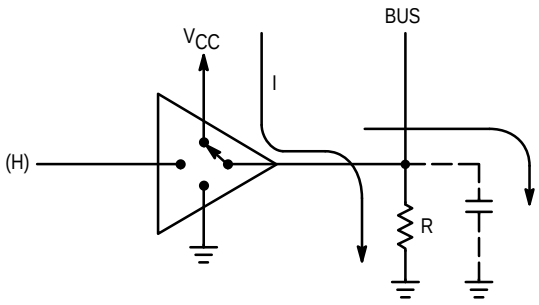
Because buses tend to operate in harsh, noisy environments, most bus lines are terminated via a resistor to V_{CC} or ground. This low impedance to V_{CC} or ground (depending on preference of a pull–up or pull–down logic level) reduces bus noise pickup. In certain cases a bus line may be released (put in a high–impedance state) by disabling all the 3–state bus drivers (see Figure 35). In this condition all HC/HCT inputs on the bus would be allowed to float. A CMOS input or 1/0 pin (when selected as an input) should never be allowed to float. (This is one reason why an HCT device may not be a drop–in replacement of an LSTTL device.) A floating CMOS input can put the device into the linear region of operation. In this region excessive current can flow and the possibility of logic errors due to oscillation may occur (see **Inputs**, this chapter). Note that when a bus is properly terminated with pull–up resistors, HC devices, instead of HCT devices, can be driven by an NMOS or LSTTL bus driver. HC devices are preferred over HCT devices in bus applications because of their higher low level input noise margin. (With a 5 V supply the typical HC switch point is 2.3 V while the switch point of HCT is only 1.3 V.)

Some popular LSTTL bus termination designs may not work for HSCMOS devices. The outputs of HSCMOS may not be able to drive the low value of termination used by some buses. (This is another reason why an HCT device may not be a drop in replacement for an LSTTL device.) However, because low power operation is one of the main reasons for using CMOS, an optimized CMOS bus termination is usually advantageous.

The choice of termination resistances is a trade–off between speed and power consumption. The speed of the bus is a function of the RC time constant of the termination resistor and the parasitic capacitance associated with the bus. Power consumption is a function of whether a pull–up or pull–down resistor is used and the output state of the device that has control of the bus (see Figure 36). The lower the termination resistor the faster the bus operates, but more power is consumed. A large value resistor wastes less power, but slows the bus down. Motorola recommends a termination resistor value between 1 kΩ and 1 MΩ. An alternative to a passive resistor termination would be an active–type termination (see Figure 37). This type termination holds the last logic level on the bus until a driver can once again take control of the bus. An active termination has the advantage of consuming a minimal amount of power. Most HC/HCT bus drivers do not have built–in hysteresis. Therefore, heavily loaded buses can slow down rise and fall signals and exceed the input rise/fall time defined in JEDEC Standard No. 7A. In this event, devices with Schmitt–triggered inputs should be used to condition these slow signals.



(a) USING A PULL-UP RESISTOR



(b) USING A PULL-DOWN RESISTOR

Figure 36.

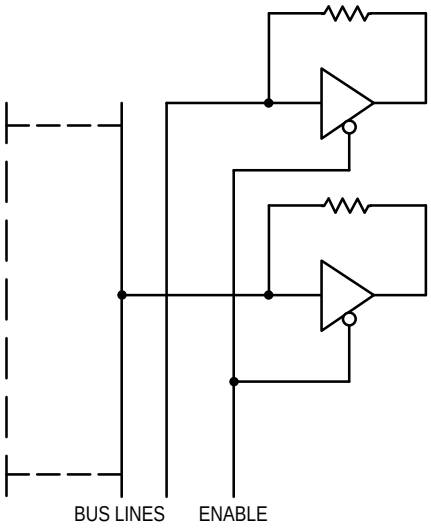


Figure 37. Using Active Termination (HC125)

TRANSMISSION LINE TERMINATION

When data is transmitted over long distances, the line on which the data travels can be considered a transmission line. (Long distance is relative to the data rate being transmitted.) Examples of transmission lines include high–speed buses, long PCB lines, coaxial and ribbon cables. All transmission lines should be properly terminated into a low–impedance termination. A low–impedance termination helps eliminate noise, ringing, overshoot, and crosstalk problems. Also a low–impedance termination reduces signal degradation because the small values of parasitic line capacitance and inductance have lesser effect on a low–impedance line.

The value of the termination resistor becomes a trade–off between power consumption, data rate speeds, and transmission line distance. The lower the resistor value, the faster data can be presented to the receiving device, but the more power the resistor consumes. The higher the resistor value, the longer it will take to charge and discharge the transmission line through the termination resistor ($T = R \bullet C$).

Transmission line distance becomes more critical as data rates increase. As data rates increase, incident (and reflective) waves begin to resemble that of RF transmission line theory. However, due to the nonlinearity of CMOS digital logic, conventional RF transmission theory is not applicable.

HC devices are preferred over HCT devices due to the fact that HC devices have higher switch points than HCT devices. This higher switch point allows HC devices to achieve better incident wave switching on lower impedance lines.

HC/HCT may not have enough drive capability to interface with some of the more popular LSTTL transmission lines. (Possible reason why an HCT device may not be a drop–in replacement of an equivalent TTL device.) This does not pose a major problem since having larger value termination resistors is desirable for CMOS type transmission lines.

By increasing the termination resistance value, the CMOS advantage of low power consumption can be realized. Motorola recommends a minimum termination resistor value as shown in Figure 38. The termination resistor should be as close to the receiving unit as possible. Another method of terminating the line driver, as well as the receiving unit, is shown in Figure 39. Note that the resistor values in Figure 39 are twice the resistor value of Figure 38; this gives a net equivalent termination value of Figure 38. Even higher values of resistors may be used for either termination method. This reduces power consumption, but at the expense of speed and possible signal degradation.

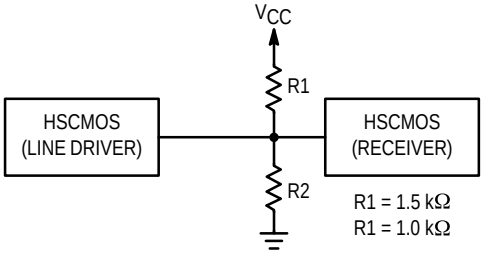


Figure 38. Termination Resistors at the Receiver

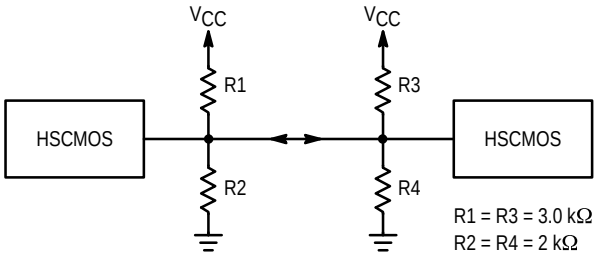


Figure 39. Termination Resistors at Both the Line Driver and Receiver

CMOS LATCH UP

Typically, HSCMOS devices do not latch up with currents of 75 mA forced into or out of the inputs or 300 mA for the outputs under worst case conditions ($T_A = 125°C$ and $V_{CC} = 6$ V). Under dc conditions for the inputs, the input protection network typically fails, due to grossly exceeding the maximum input voltage rating of $– 1.5$ to $V_{CC} + 1.5$ V before latch–up currents are reached. For most designs, latch up will not be a problem, but the designer should be aware of it, what causes it, and how it can be prevented.

Figure 40 shows the layout of a typical CMOS inverter and Figure 41 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch–up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the device on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than $V_{CC} + 0.5$ V or less than $– 0.5$ V and have sufficient current to trigger the SCR. The latch–up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device can be destroyed or its reliability can be degraded. Ways to prevent such an occurrence are listed below.

1. Industrial controllers driving relays or motors is an environment in which latch up is a potential problem. Also, the ringing due to inductance of long transmission lines in an industrial setting could provide enough energy to latch up CMOS devices. Opto–isolators, such as Motorola's MOC3011, are recommended to reduce chances of latch up. See the Motorola Semiconductor Master Selection Guide for a complete listing of Motorola opto–isolators.
2. Ensure that inputs and outputs are limited to the maximum rated values.

   $-1.5 \le V_{in} \le V_{CC} +1.5$ V referenced to GND or
   $-0.5 \le V_{in} \le V_{CC} +0.5$ V referenced to GND

   $-0.5 \le V_{out} \le V_{CC} +0.5$ V referenced to GND

   $|I_{in}| \le 20$ mA

   $|I_{out}| \le 25$ mA for standard outputs

   $|I_{out}| \le 35$ mA for bus–driver outputs
3. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum ratings value. See **Handling Precautions** for other possible protection circuits and a discussion of ESD prevention.
4. Sequence power supplies so that the inputs or outputs of HSCMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug–in board applications).
5. Voltage regulating and filtering should be used in board design and layout to ensure that power supply lines are free of excessive noise.
6. Limit the available power supply current to the devices that are subject to latch–up conditions. This can be accomplished with the power–supply filtering network or with a current–limiting regulator.

RECOMMENDED READING

Paul Mannone, "Careful Design Methods Prevent CMOS Latch–Up", EDN, January 26, 1984.

2

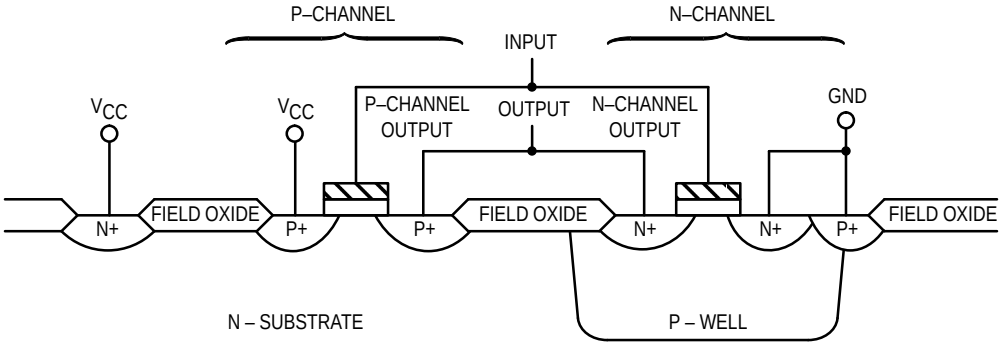


Figure 40. CMOS Wafer Cross Section

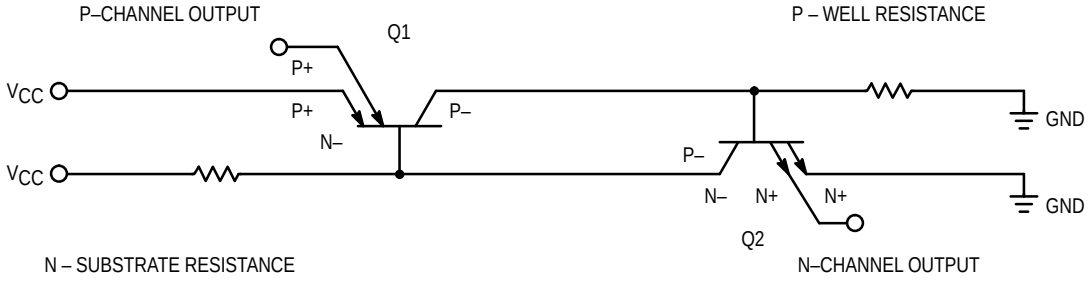


Figure 41. Latch–Up Circuit Schematic

MAXIMUM POWER DISSIPATION

The maximum power dissipation for Motorola HSCMOS packages is 750 mW for both ceramic and plastic DIPs and 500 mW for SOIC packages. The deratings are – 10 mW/°C from 65°C for plastic DIPs, – 10 mW/°C from 100°C for ceramic packages, and – 7 mW/°C from 65°C for SOIC packages. This is illustrated in Figure 42.

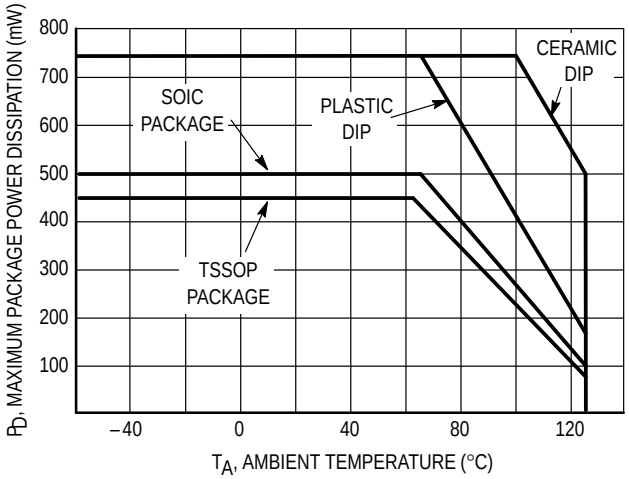


Figure 42. Maximum Package Power Dissipation versus Temperature

Internal heat generation in HSCMOS devices comes from two sources, namely, the quiescent power and dynamic power consumption.

In the quiescent state, either the P–channel or N–channel transistor in each complementary pair is off except for small source–to–drain leakage due to the inputs being either at V_{CC} or ground. Also, there are the small leakage currents flowing in the reverse–biased input protection diodes and the parasitic diodes on the chip. The specification which takes all leakage into account is called Maximum Quiescent Supply Current (per package), or I_{CC}, and is shown on all data sheets.

The three factors which directly affect the value of quiescent power dissipation are supply voltage, device complexity, and temperature. On the data sheets, I_{CC} is specified only at V_{CC} = 6.0 V because this is the worst–case supply voltage condition. Also, larger or more complex devices consume more quiescent power because these devices contain a proportionally greater reverse–biased diode junction area and more off (leaky) FETs.

Finally, as can be seen from the data sheets, temperature increases cause I_{CC} increases. This is because at higher temperatures, leakage currents increase.

HC QUIESCENT POWER DISSIPATION

When HC device inputs are virtually at V_{CC} or GND potential (as in a totally CMOS system), quiescent power dissipation is minimized. The equation for HC quiescent power dissipation is given by:

$$P_D = V_{CC}I_{CC}$$

Worst–case I_{CC} occurs at V_{CC} = 6.0 V. The value of I_{CC} at V_{CC} = 6.0 V, as specified in the data sheets, is used for all power supply voltages from 2 to 6 V.

HCT QUIESCENT POWER DISSIPATION

Although HCT devices belong to the CMOS family, their input voltage specifications are identical to those of LSTTL. HCT parts can therefore be either judiciously substituted for or mixed with LS devices in a system.

TTL output voltages are V_{OL} = 0.4 V (max) and V_{OH} = 2.4 to 2.7 V (min).

Slightly higher I_{CC} current exists when an HCT device is driven with V_{OL} = 0.4 V (max) because this voltage is high enough to partially turn on the N–channel transistor. However, when being driven with a TTL V_{OH}, HCT devices exhibit large additional current flow (ΔI_{CC}) as specified on HCT device data sheets. ΔI_{CC} current is caused by the off–rail input voltage turning on both the P and N channels of the input buffer. This condition offers a relatively low impedance path from V_{CC} to GND. Therefore, the HCT quiescent power dissipation is dependent on the number of inputs applied at the TTL V_{IH} logic voltage level.

The equation for HCT quiescent power dissipation is given by:

$$P_D = I_{CC}V_{CC} + \eta\Delta I_{CC}V_{CC}$$

where η = the number of inputs at the TTL V_{IH} level.

HC AND HCT DYNAMIC POWER DISSIPATION

Dynamic power dissipation is calculated in the same way for both HC and HCT devices. The three major factors which directly affect the magnitude of dynamic power dissipation are load capacitance, internal capacitance, and switching transient currents.

The dynamic power dissipation due to capacitive loads is given by the following equation:

$$P_D = C_L V_{CC}^2 f$$

where P_D = power in μW, C_L = capacitive load in pF, V_{CC} = supply voltage in volts, and f = output frequency driving the load capacitor in MHz.

All CMOS devices have internal parasitic capacitances that have the same effect as external load capacitors. The magnitude of this internal no–load power dissipation capacitance, C_{PD}, is specified as a typical value.

Finally, switching transient currents affect the dynamic power dissipation. As each gate switches, there is a short period of time in which both N– and P–channel transistors are partially on, creating a low–impedance path from V_{CC} to ground. As switching frequency increases, the power dissipation due to this effect also increases.

The dynamic power dissipation due to C_{PD} and switching transient currents is given by the following equation:

$$P_D = C_{PD}V_{CC}^2 f$$

Therefore, the total dynamic power dissipation is given by:

$$P_D = (C_L + C_{PD})V_{CC}^2 f$$

Total power dissipation for HC and HCT devices is merely a summation of the dynamic and quiescent power dissipation elements. When being driven by CMOS logic voltage levels (rail to rail), the total power dissipation for both HC and HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + (C_L + C_{PD})V_{CC}^2f$$

When being driven by LSTTL logic voltage levels, the total power dissipation for HCT devices is given by the equation:

$$P_D = V_{CC}I_{CC} + V_{CC}\Delta I_{CC}(\delta, + \delta_2 + \ldots + \delta_n) + (C_L + C_{PD})V_{CC}^2f$$

where δ_n = duty cycle of LSTTL output applied to each input of an HCT device.

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. See page 2–6 for the calculation of CMOS power consumption.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit — from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \qquad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \qquad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation on page 2–15).

$\overline{\theta}_{JC}$ = average thermal resistance, junction to case

$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient

$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) devices.

Only two terms on the right side of equation (1) can be varied by the user — the ambient temperature, and the device case-to-ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can also be controlled, but under recommended use the V_{CC} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\overline{\theta}_{JC}) \qquad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average $\overline{\theta}_{JC}$ resistance values for standard IC packages are given in Table 2.

Table 2. Thermal Resistance Values for Standard I/C Packages

Thermal Resistance In Still Air								
Package Description								
No. Leads	Body Style	Body Material	Body W × L	Die Bonds	Die Area (Sq. Mils)	Flag Area (Sg. Mils)	θ_{JC} (°C/Watt)	
							Avg.	Max.
14	DIL	Epoxy	1/4″ × 3/4″	Epoxy	4096	6,400	38	61
16	DIL	Epoxy	1/4″ × 3/4″	Epoxy	4096	12,100	34	54
20	DIL	Epoxy	0.35″ × 0.35″	Epoxy	4096	14,400	N/A	N/A

NOTES:
1. All plastic packages use copper lead frames.
2. Body style DIL is "Dual-In-Line."
3. Standard Mounting Method: Dual-In-Line Socket or P/C board with no contact between bottom of package and socket or P/C board.

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) reduces the temperature rise of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 3 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Table 3. Thermal Gradient of Junction Temperature (16-Pin Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing of 0.5″.
Air flow is 500 lfpm along the Z axis.

Table 4 is graphically illustrated in Figure 43 which shows that the reliability for plastic and ceramic devices is the same until elevated junction temperatures induce intermetallic failures in plastic devices. Early and mid-life failure rates of plastic devices are not effected by this intermetallic mechanism.

PROCEDURE

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 4 or Equation (1) on page 2–16 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 43.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\overline{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

Table 4. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

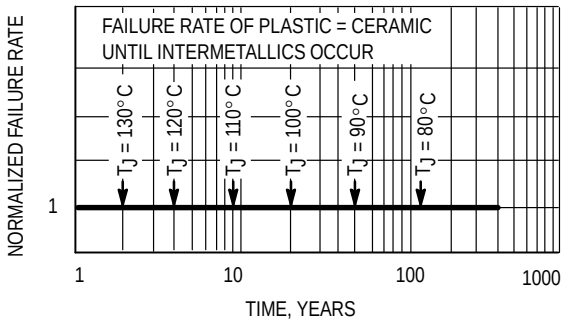


Figure 43. Failure Rate versus Time Junction Temperature

CAPACITIVE LOADING EFFECTS ON PROPAGATION DELAY

In addition to temperature and power–supply effects, capacitive loading effects should be taken into account. The additional propagation delay may be calculated if the short circuit current for the device is known. Expected minimum numbers may be determined from Table 5.

From the equation

$$i = \frac{Cdv_C}{dt}$$

this approximation follows:

$$I = \frac{C\Delta V}{\Delta t}$$

so

$$\Delta t = \frac{C\Delta V}{I}$$

or

$$\Delta t = \frac{C(0.5\ V_{CC})}{I}$$

because the propagation delay is measured to the 50% point of the output waveform (typically 0.5 V_{CC}).

This equation gives the general form of the additional propagation delay. To calculate the propagation delay of a device for a particular load capacitance, C_L, the following equation may be used.

$$t_{PT} = t_P + 0.5\ V_{CC}\ (C_L - 50\ pF)/I_{OS}$$

where t_{PT} = total propagation delay

t_P = specified propagation delay with 50 pF load

C_L = actual load capacitance

I_{OS} = short circuit current (Table 5)

An example is given here for t_{PHL} of the 74HC00 driving a 150 pF load.

$$V_{CC} = 4.5\ V$$

$$t_{PHL}\ (50\ pF) = 18\ ns$$

$$C_L = 150\ pF$$

$$I_{OS} = 17.3\ mA$$

$$t_{PHL}\ (150\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(150\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + 13\ ns$$

$$= 31\ ns$$

Another example for C_L = 0 pF and all other parameters the same.

$$t_{PHL}\ (0\ pF) = 18\ ns + \frac{(0.5)(4.5\ V)(0\ pF - 50\ pF)}{17.3\ mA}$$

$$= 18\ ns + (-6.5\ ns)$$

$$t_{PHL} = 11.5\ ns$$

This method gives the expected propagation delay and is intended as a design aid, not as a guarantee.

Table 5. Expected Minimum Short Circuit Currents*

Parameter	V_{CC}	Standard Drivers			Bus Drivers			Unit
		25°C	85°C	125°C	25°C	85°C	125°C	
Output Short Circuit Source Current	2.0	1.89	1.83	1.80	3.75	3.64	3.60	mA
	4.5	18.5	15.0	13.4	37.0	30.0	26.6	
	6.0	35.2	28.0	24.6	70.6	56.1	49.2	
Output Short Circuit Sink Current	2.0	1.55	1.55	1.55	2.45	2.45	2.43	mA
	4.5	17.3	14.0	12.5	27.2	22.1	19.6	
	6.0	33.4	26.5	23.2	52.6	41.7	36.5	

* These values are intended as design aids, not as guarantees.

TEMPERATURE EFFECTS ON DC AND AC PARAMETERS

One of the inherent advantages of CMOS devices is that characteristics of the N– and P–channel transistors, such as drive current, channel resistance, propagation delay, and output transition time, track each other over a wide temperature range. Figure 44 shows the temperature relationships for these parameters. To illustrate the effects of temperature on noise margin, Figure 45 shows the typical transfer characteristics for devices with buffered inputs and outputs. Note that the typical switch point is at 45% of the supply voltage and is minimally affected by temperature.

The graphs in this section are intended to be design aids, not guarantees.

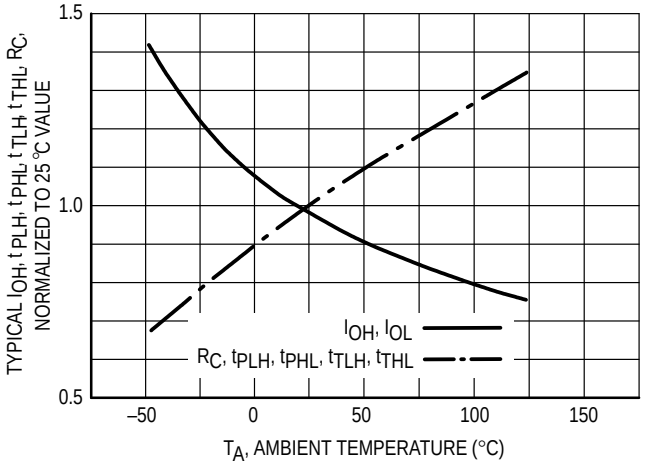


Figure 44. Characteristics of Drive Current, Channel Resistance, and AC Parameters Over Temperature

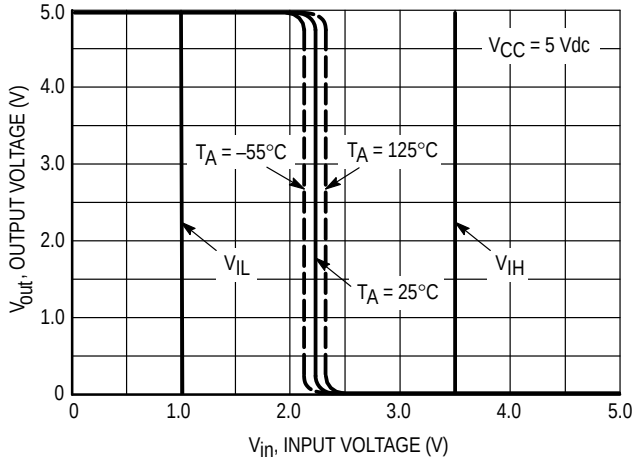


Figure 45. Temperature Effects on the HC Transfer Characteristics

SUPPLY VOLTAGE EFFECTS ON DRIVE CURRENT AND PROPAGATION DELAY

The transconductive gain, I_{out}/V_{in}, of MOSFETs is proportional to the gate voltage minus the threshold voltage, $V_G - V_T$. The gate voltage at the input of the final stage of buffered devices is approximately the power supply voltage, V_{CC} or GND. Because $V_G = V_{CC}$ or GND, the output drive current is proportional to the supply voltage. Propagation delays for CMOS devices are also affected by the power supply voltage, because most of the delay is due to charging and discharging internal capacitances. Figure 46 and Figure 47 show the typical variation of current drive and propagation delay, normalized to V_{CC} = 4.5 V for 2.0 ≤ V_{CC} ≤ 6.0 V. These curves may be used with the tables on each data sheet to arrive at parametric values over the voltage range.

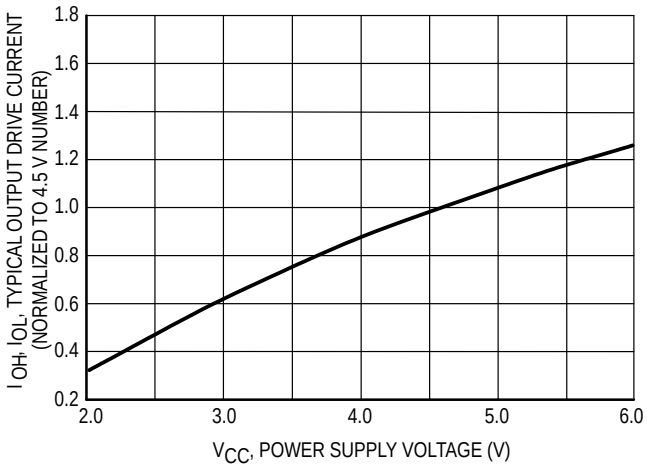


Figure 46. Drive Current versus V_{CC}

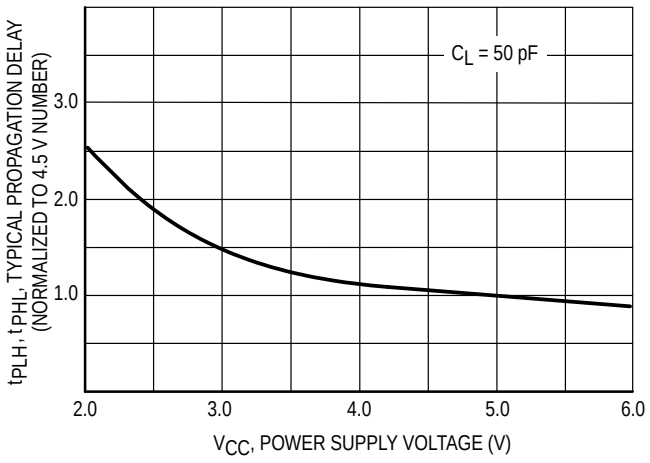


Figure 47. Propagation Delay versus V_{CC}

DECOUPLING CAPACITORS

The switching waveforms shown in Figure 48 and Figure 49 show the current spikes introduced to the power supply and ground lines. This effect is shown for a load capacitance of less than 5 pF and for 50 pF. For ideal power supply lines with no series impedance, the spikes would pose no problem. However, actual power supply and ground lines do possess series impedance, giving rise to noise problems. For this reason, care should be taken in board layouts, ensuring low impedance paths to and from logic devices.

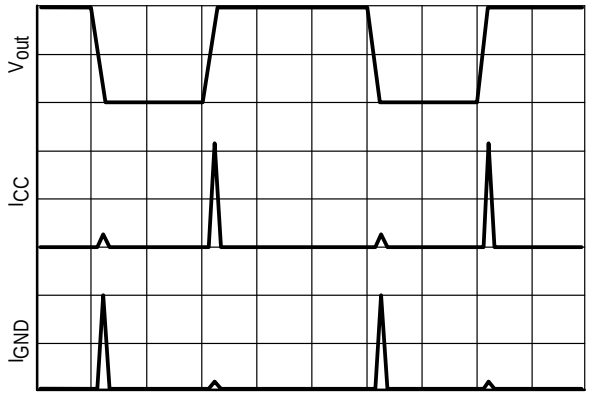
To absorb switching spikes, the following HSCMOS devices should be bypassed with good quality 0.022 μF to 0.1 μF decoupling capacitors:

1. Bypass every device driving a bus with all outputs switching simultaneously.
2. Bypass all synchronous counters.
3. Bypass devices used as oscillator elements.
4. Bypass Schmitt–trigger devices with slow input rise and fall times. The slower the rise and fall time, the larger the bypass capacitor. Lab experimentation is suggested.

Bypass capacitors should be distributed over the circuit board. In addition, boards could be decoupled with a 1 μF capacitor.

BUFFERED DEVICE: INPUT t_r, $t_f \leq 500$ ns, $C_L < 5$ pF

Figure 48. Switching Currents for $C_L < 5$ pF



BUFFERED DEVICE: INPUT t_r, $t_f \leq 500$ ns, $C_L < 5$ pF

Figure 49. Switching Currents for $C_L = 50$ pF

INTERFACING

HSCMOS devices have a wide operating voltage range (V_{CC} = 2 to 6 V) and sufficient current drive to interface with most other logic families available today. In this section, various interface schemes are given to aid the designer (see Figure 50 through Figure 55). The various types of CMOS devices with their input/output levels and comments are given in Table 6.

Motorola presently has available several CMOS memories and microprocessors (see Table 7) which are designed to directly interface with High–Speed CMOS. With these devices now available, the designer has an attractive alternative to LSTTL/NMOS, and a total HSCMOS system is now possible. (See SG102, CMOS System IC Selection Guide, for more information.)

Device designators are as follows:

HC This is a high–speed CMOS device with CMOS input switching levels and buffered CMOS outputs. The numbering of devices with this designator follows the LSTTL numbering sequence. These devices are functional and pinout equivalents of LSTTL devices (e.g., HC00, HC688, etc.). Exceptions to this are devices that are functional and pinout equivalents to metal–gate CMOS devices (e.g., HC4002, HC4538A, etc.).

HCU This is an unbuffered high–speed CMOS device with only one stage between the input and output. Because this is an unbuffered device, input and output levels may differ from buffered devices. At present, the family contains only one unbuffered device, the HCU04A.

HCT This is a high–speed CMOS device with an LSTTL–to–CMOS input buffer stage. These devices are designed to interface with LSTTL outputs operating at V_{CC} = 5 V ± 10%. HCT devices have fully buffered CMOS outputs that directly drive HSCMOS or LSTTL devices.

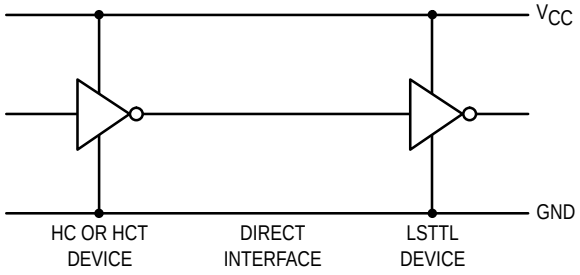


Figure 50. HC to LSTTL Interfacing

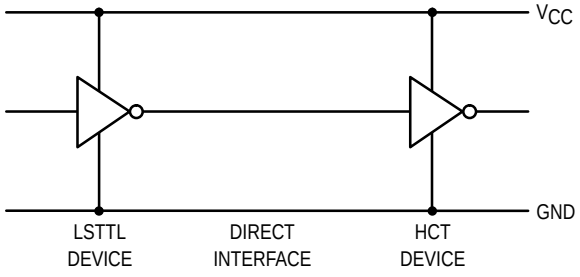


Figure 51. LSTTL to HCT Interfacing

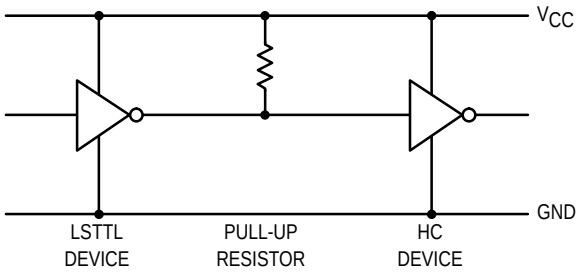


Figure 52. LSTTL to HC Interfacing

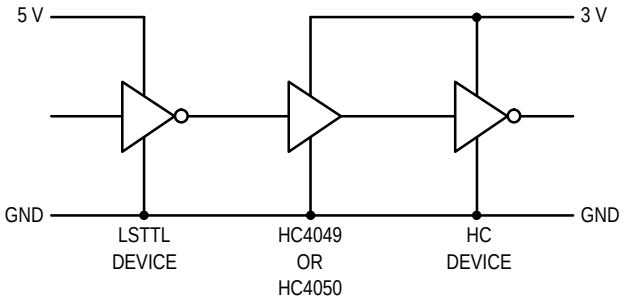
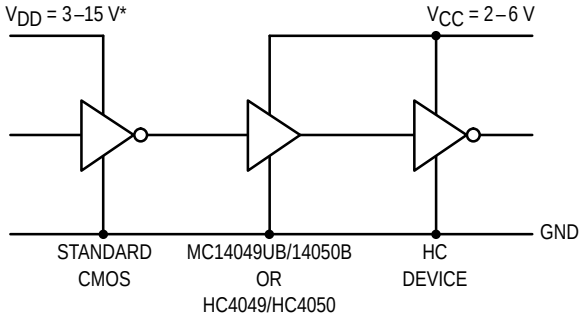


Figure 53. LSTTL to Low–Voltage HSCMOS



*V_{OH} must be greater than V_{IH} of low voltage Device;
V_{DD} = 3–18 V may be used if interfacing to 14049UB/14050B.

Figure 54. High Voltage CMOS to HSCMOS

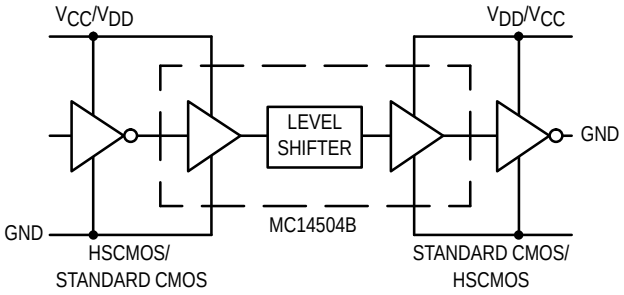


Figure 55. Up/Down Level Shifting Using the MC14504B

Table 6. Interfacing Guide

Device	Input Level	Output Level	Comments
HCXXX	CMOS	CMOS	LSTTL Functional and Pinout Equivalent Devices
HC4XXX	CMOS	CMOS	CMOS Functional and Pinout Equivalent Devices
HCUXX	CMOS	CMOS	Used in Linear Applications
HCTXXX	TTL	CMOS	HSCMOS Device with TTL–to–CMOS Input Buffering
HC4049, HC4050	$-0.5 \le V_{in} \le 15$ V	CMOS	High–to–Low Level Translators, CMOS Switching Levels
MC14049UB MC14050B	$-0.5 \le V_{in} \le 18$ V	CMOS	Metal–Gate CMOS High–to–Low Level Translators, CMOS Switching Levels
MC14504B	CMOS or TTL	CMOS	Metal–Gate CMOS High–to–Low or Low–to–High Level Translator

Table 7. CMOS Memories and Microprocessors

CMOS Memories	CMOS Microprocessors	
MCM6147	MC68HC01	MC146805G2
MCM61L47	MC68HC03	MC146805H2
MCM68HC34	MC68HC11A8	MC1468705F2
	MC68HC11D4	MC1468705G2
	MC68HC811A2	MC68HC05C4
	MC68HC811D4	MC68HSC05C4
	MC68HC04P3	MC68HC05C8
	MC146805E2	MC68HC805C4
	MC146805F2	MC68HC000

RECOMMENDED READING

S. Craig, “Using High–Speed CMOS Logic for Microprocessor Interfacing”, Application Note–868, Motorola Semiconductor Products Inc., 1982.

TYPICAL PARAMETRIC VALUES

Given a fixed voltage and temperature, the electrical characteristics of High–Speed CMOS devices depend primarily on design, layout, and processing variations inherent in semiconductor fabrication.

A preliminary evaluation of each device type essentially guarantees that the design and layout of the device conforms to the criteria and standards set forth in the design goals. With very few exceptions, device electrical parameters, once established, do not vary due to design and layout.

Of much more concern is processing variation. A digital processing line is allowed to deviate over a fairly broad processing range. This allows the manufacturer to incur reduced processing costs. These reduced processing costs are passed on to the consumer in the form of lower device prices.

Processing variation is the range from worst case to best case processing and is defined as the process window. This window is established with the aid of statistical process control (SPC). With SPC, when a processing parameter approaches the process window limit, that parameter is adjusted toward the middle of the window. This keeps process variations within a predetermined tolerance.

Motorola characterizes each device type over this process window. Each device type is characterized by allowing experimental lots to be processed using worst case and best case processing. The worst case processed lots usually determine the minimum or maximum guaranteed limit. (Whether the limit is a guaranteed minimum or maximum depends on the particular parameter being measured.)

In production, these limits are guaranteed by probe and final test and therefore appear independent of process variation to the end user. However, this does not hold true for the mean value of the total devices processed. The mean value, commonly referred to as a typical value, shifts over processing and therefore varies from lot to lot or even wafer to wafer within a lot.

As with all processing or manufacturing, the total devices being produced fit the normal distribution or bell curve of Figure 56. In order to guarantee a valid typical value, a typical number plus a tolerance, would have to be specified and tested (see Figure 57). However, this would greatly increase processing costs which would have to be absorbed by the consumer.

In some cases, the device's actual values are so small that the resolution of the automatic test equipment determines the guaranteed limit. An example of this is quiescent supply current and input leakage current.

Most manufacturers provide typical numbers by one of two methods. The first method is to simply double or halve, depending on the parameter, the guaranteed limit to determine a typical number. This would theoretically put all processed lots in the middle of the process window. Another approach to typical numbers is to use a typical value that is derived from the aforementioned experimental lots. However, neither method accurately reflects the mean value of devices any one consumer can expect to receive.

Therefore, the use of typical parametric numbers for design purposes does not constitute sound engineering design practice. Worst case analysis dictates the use of guaranteed minimum or maximum values. The only possible exception would be when no guaranteed value is given. In this case a typical value may be used as a ballpark figure.

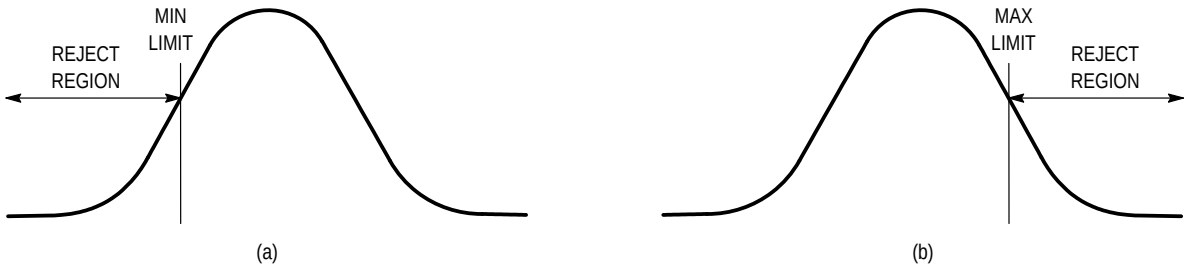


Figure 56.

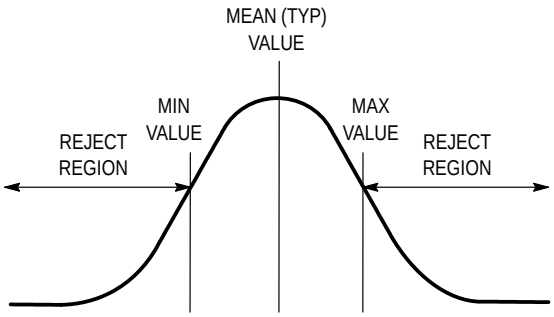


Figure 57.

REDUCTION OF ELECTROMAGNETIC INTERFERENCE (EMI)

Electromagnetic interference (EMI) and radio frequency interference (RFI) are phenomena inherent in all electrical systems covering the entire frequency spectrum. Although the characteristics have been well documented, EMI remains difficult to deal with due to numerous variables. EMI should be considered at the beginning of a design, and taken into account during all stages, including production and beyond.

These entities must be present for EMI to be a factor: (1) a source of EMI, (2) a transmission medium for EMI, and (3) a receiver of EMI. Several sources include relays, FM transmitters, local oscillators in receivers, power lines, engine ignitions, arc welders, and lighting. EMI transmission paths include ground connections, cables, and the space between conductors. Some receivers of EMI are radar receivers, computers, and television receivers.

For microprocessor based equipment, the source of emissions is usually a current loop on a PC board. The chips and their associated loop areas also function as receivers of EMI. The fact is that PC boards which radiate high levels of EMI are also more likely to act as receivers of EMI.

All logic gates are potential transmitters and receivers of emissions. Noise immunity and noise margin are two criterion which measure a gate's immunity to noise which could be caused by EMI. CMOS technology, as opposed to the other commonly used logic families, offers the best value for noise margin, and is therefore an excellent choice when considering EMI.

The electric and magnetic fields associated with ICs are proportional to the current used, the current loop area, and the switching transition times. CMOS technology is preferred due to smaller currents. Also, the current loop area can be reduced by the use of surface mount packages.

In a system where several pieces of equipment are connected by cables, at least five coupling paths should be taken into account to reduce EMI. They are: (1) common ground impedance coupling (a common impedance is shared between an EMI source and receiver), (2) common–mode, field–to–cable coupling (electromagnetic fields enter the loop found by two pieces of equipment, the cable connecting them, and the ground plane), (3) differential–mode, field–to–cable coupling (electromagnetic fields enter the loop formed by two pieces of equipment and the cable connecting them), (4) crosstalk coupling (signals in one transmission line are coupled into another transmission line), and (5) a conductive path through power lines.

Shielding is a means of reducing EMI. Some of the more commonly used shields against EMI and RFI contain stainless steel fiber–filled polycarbonate, aluminum flake–filled polycarbonate/ABS coated with nickel and copper electrolysis plating or cathode sputtering, nickel coated graphite fiber, and polyester SMC with carbon–fiber veil. Several manufacturers who make conductive compounds and additives are listed below.

SHIELDING MANUFACTURERS

General Electric Co., Plastics Group, Pittsfield, MA

Mobay Chemical Corp., Pittsburgh, PA

Wilson–Fiberfil International, Evansville, IN

American Cyanamid Co., Wayne, NJ

Fillite U.S.A., Inc., Huntington, WV

Transnet Corp., Columbus, OH

Motorola does not recommend, or in any way warrant the manufacturers listed here. Additionally, no claim is made that this list is by any means complete.

RECOMMENDED READING

D. White, K. Atkinson, and J. Osburn, "Taming EMI in Microprocessor Systems", *IEEE Spectrum*, Vol. 22, Number 12, Dec. 1985.

D. White and M. Mardiguian, *EMI Control Methodology and Procedures*, 1985.

H. Denny, *Grounding for the Control of EMI*.

M. Mardiguian, *How to Control Electrical Noise*.

D. White, *Shielding Design Methodology and Procedures*.

For more information on this subject, contact:

Interference Control Technologies
Don White Consultants, Inc., Subsidiary
State Route 625
P.O. Box D
Gainesville, VA 22065

HYBRID CIRCUIT GUIDELINES

High–Speed CMOS devices, when purchased in chip (die) form, are useful in hybrid circuits. Most high–speed devices are fabricated with P wells and N substrates. Therefore, the substrates should be tied to V_{CC} (+ supply).

Several devices however, are fabricated with N wells and P substrates. In this case, the substrates should be tied to GND. The best solution to alleviate confusion about the substrate is the use of nonconductive or insulative substrates. This averts the necessity of tying the substrate off to either V_{CC} or GND.

For more information on hybrid technology, contact:

International Society for Hybrid Microelectronics
P.O. Box 3255
Montgomery, AL 36109

SCHMITT–TRIGGER DEVICES

Schmitt–trigger devices exhibit the effect of hysteresis. Hysteresis is characterized by two different switching threshold levels, one for positive–going input transitions and the other for negative–going input transitions.

Schmitt triggers offer superior noise immunity when compared to standard gates and inverters. Applications for Schmitt triggers include line receivers, sine to square wave converters, noise filters, and oscillators. Motorola offers six versatile Schmitt–trigger devices in the High–Speed CMOS logic family (see Table 8).

The typical voltage transfer characteristics of a standard CMOS inverter and a CMOS Schmitt–trigger inverter are compared in Figure 58 and Figure 59. The singular transfer threshold of the standard inverter is replaced by two distinct thresholds in a Schmitt–trigger inverter. During a positive–going transition of V_{in}, the output begins to go low after the V_{T+} threshold is reached. During a negative–going V_{in} transition, V_{out} begins to go high after the V_{T-} threshold is reached. The difference between V_{T+} and V_{T-} is defined as V_H, the hysteresis voltage.

As a direct result of hysteresis, Schmitt–trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times. Positive–going input noise excursions must rise above the V_{T+} threshold before they affect the output. Similarly, negative–going input noise excursions must drop below the V_{T-} threshold before they affect the output.

The HC132A can be used as a direct replacement for the HC00A NAND gate, which does not have Schmitt–trigger capability. The HC132A has the same pin assignment as the HC00A. Schmitt–trigger logic elements act as standard logic elements in the absence of noise or slow rise and fall times, making direct substitution possible.

Versatility and low cost are attractive features of CMOS Schmitt triggers. With six Schmitt triggers per HC14A package, one trigger can be used for a noise elimination application while the other five function as standard inverters. Similarly, each of the four triggers in the HC132A can be used as either Schmitt triggers or NAND gates or some combination of both.

Table 8. Schmitt–Trigger Devices

HC14A	Hex Schmitt–Trigger Inverter
HCT14A	Hex Schmitt–Trigger Inverter with LSTTL Inputs
HC132A	Quad 2–Input NAND Gate with Schmitt–Trigger Inputs

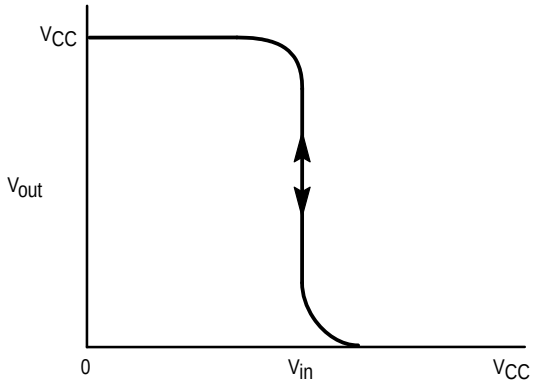


Figure 58. Standard Inverter Transfer Characteristic

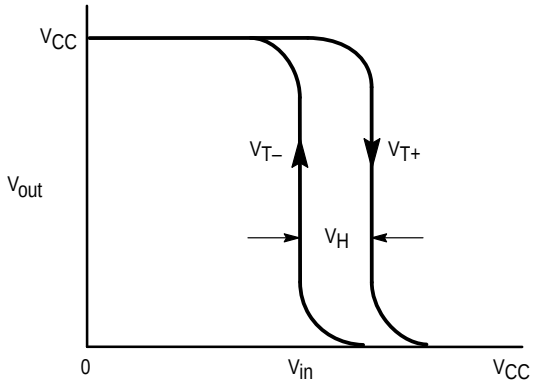


Figure 59. Schmitt–Trigger Inverter Transfer Characteristic

OSCILLATOR DESIGN WITH HIGH–SPEED CMOS

Oscillator design is a fundamental requirement of many systems and several types are discussed in this section. In general, an oscillator is comprised of two parts: an active network and a feedback network. The active network is usually in the form of an amplifier, or an unbuffered inverter, such as the HCU04. The feedback network is mainly comprised of resistors, capacitors, and depending upon the application, a quartz crystal or ceramic resonator.

Buffered inverters are never recommended in oscillator applications due to their high gain and added propagation delay. For this reason Motorola manufactures the HCU04, which is an unbuffered hex inverter.

Oscillators for use in digital systems fall into two general categories, RC oscillators and crystal or ceramic resonator oscillators. Crystal oscillators have the best performance, but are more costly, especially for nonstandard frequencies. RC oscillators are more useful in applications where stability and accuracy are not of prime importance. Where high performance at low frequencies is desired, ceramic resonators are sometimes used.

RC OSCILLATORS

The circuit in Figure 60 shows a basic RC oscillator using the HCU04. When the input voltage of the first inverter reaches the threshold voltage, the outputs of the two inverters change state, and the charging current of the capacitor changes direction. The frequency at which this circuit oscillates depends upon R1 and C. The equation to calculate these component values is given in Figure 60.

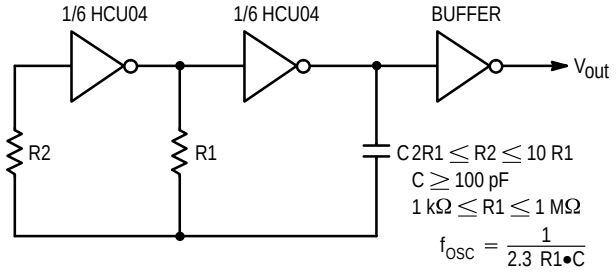


Figure 60. RC Oscillator

Certain constraints must be met while designing this type of oscillator. Stray capacitance and inductance must be kept to a minimum by placing the passive components as close to the chip as possible. Also, at higher frequencies, the HCU04's propagation delay becomes a dominant effect and affects the cycle time. A polystyrene capacitor is recommended for optimum performance.

CRYSTAL OSCILLATORS

Crystal oscillators provide the required stability and accuracy which is necessary in many applications. The crystal can be modeled as shown in Figure 62.

The power dissipated in a crystal is referred to as the drive level and is specified in mW. At low drive levels, the resonant resistance of the crystal can be so large as to cause start–up problems. To overcome this problem, the amplifier (inverter) should provide enough amplification, but not too much as to overdrive the crystal.

Figure 61 shows a Pierce crystal oscillator circuit, which is a popular configuration with CMOS.

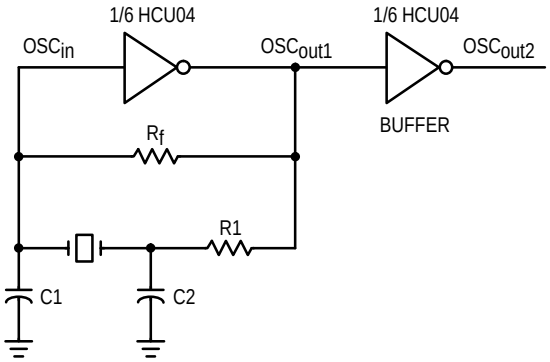
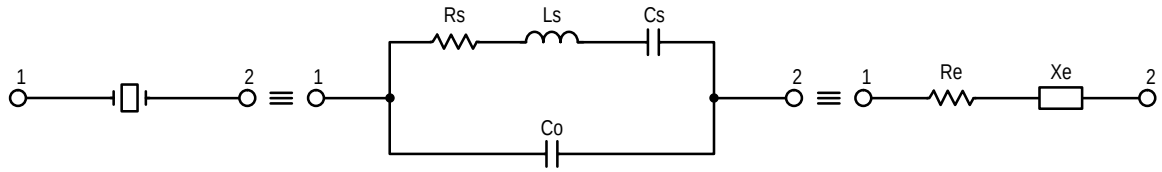


Figure 61. Pierce Crystal Oscillator Circuit

Choosing R1

Power is dissipated in the effective series resistance of the crystal. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 limits the drive level.



Values are supplied by the crystal manufacturer
(parallel resonant crystal)

Figure 62. Equivalent Crystal Networks

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency at OSC Out 2. The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or RI must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Selecting R_f

The feedback resistor (R_f) typically ranges up to 20 MD. R_f determines the gain and bandwidth of the amplifier. Proper bandwidth ensures oscillation at the correct frequency plus roll–off to minimize gain at undesirable frequencies, such as the first overtone. R_f must be large enough so as not to affect the phase of the feedback network in an appreciable manner.

RECOMMENDED READING

D. Babin, “Designing Crystal Oscillators”, Machine Design, March 7, 1985.
D. Babin, “Guidelines for Crystal Oscillator Design”, Machine Design, April 25, 1985.

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PRINTED CIRCUIT BOARD LAYOUT

Noise generators on the power supply lines should be decoupled. The two major sources of noise on the power supply lines are peak current in output stages during switching and the charging and discharging of parasitic capacitances.

A good power distribution network is essential before decoupling can provide any noise reduction. Avoid using jumpers for ground and power connections; the inductance they introduce into the lines permits coupling between outputs. Therefore, use of PC boards with premanufactured ground connections is advised to connect the device pins to ground.

However, the optimum solution is to use multi–layer PC boards where different layers are used for the supply rails and interconnections. Even with double–sided boards, placing the power and ground lines on opposite sides of the board whenever possible is recommended. The multi–wire board is a less expensive approach than the multi–layer PC board, while retaining the same noise reduction characteristics. As a rule of thumb, there should be several ground pins per connector to give good ground distribution.

The precautions for ground lines also apply to V_{CC} lines: 1) separate power stabilization for each board; 2) isolate noise sources; and 3) avoid the use of large, single voltage regulators.

After all of these precautions, decoupling is an added measure to reduce supply noise. See the **Decoupling Capacitors** section.

Definitions and Glossary of Terms

HC vs. HCT

Motorola's High–Speed CMOS is intended to give the designer an alternative to LSTTL. HSCMOS, with the faster speed advantage over metal–gate CMOS (MC14000 series) and the lower power consumption advantage over LSTTL, is an optimum choice for new midrange designs. With the advent of high–speed CMOS microprocessors and memories, the ability to design a 100% CMOS system is now possible.

HCT devices offer a short–term solution to the TTL/NMOS–to–CMOS interface problem. To achieve this interface capability, some CMOS advantages had to be compromised. These compromises include power consumption, operating voltage range, and noise immunity.

In most cases HCT devices are drop–in replacements of TTL devices with significant advantages over the TTL devices. However, in some cases, an equivalent HCT device may not replace a TTL device without some form of circuit modification.

The wise designer uses HCT devices to perform logic level conversions only. In new designs, the designer wants all the advantages of a true CMOS system and designs using only HC devices.

"A" versus "Non–A"

"A" Versus "Non–A" — Motorola has an on–going device performance enhancement program for the Hi–Speed CMOS family. This is indicated by the "A" suffix of the device identification. Some of the characteristics of this "A" enhancement program are improved design, a better quality process, faster performing AC propagation delays and enhancements to various DC characteristics.

The old "Non–A" process was a 5 micron process that was modified to run a 3.5 micron family. The new "A" process is a true 3 micron process and gives better process control, with improved performance and quality.

GLOSSARY OF TERMS

C_{in} Input Capacitance — The parasitic capacitance associated with a given input pin.

C_L Load Capacitance — The capacitor value which loads each output during testing and/or evaluation. This capacitance is assumed to be attached to each output in a system. This includes all wiring and stray capacitance.

C_{out} Output Capacitance — The capacitance associated with a three–state output in the high–impedance state.

C_{PD} Power Dissipation Capacitance — Used to determine device dynamic power dissipation, i.e., $P_D = C_{PD}V_{CC}^2f + V_{CC}I_{CC}$. See **POWER SUPPLY SIZING** for a discussion of C_{PD}.

f_{max} Maximum Clock Frequency — The maximum clocking frequency attainable with the following input and output conditions being met:

Input Conditions — (HC) $t_r = t_f = 6$ ns, voltage swing from GND to V_{CC} with 50% duty cycle. **(HCT)** $t_r = t_f = 6$ ns, voltage swing from GND to 3.0 V with 50% duty cycle.

Output Conditions — (HC and HCT) waveform must swing from 10% of ($V_{OH} - V_{OL}$) to 90% of ($V_{OH} - V_{OL}$) and be functionally correct under the given load condition: C_L = 50 pF, all outputs.

V_{CC} Positive Supply Voltage — + dc supply voltage (referenced to GND). The voltage range over which ICs are functional.

V_{in} Input Voltage — DC input voltage (referenced to GND).

V_{out} Output Voltage — DC output voltage (referenced to GND).

V_{IH} Minimum High Level Input Voltage — The worst case voltage that is recognized by a device as the HIGH state.

V_{IL} Maximum Low Level Input Voltage — The worst case voltage that is recognized by a device as the LOW state.

V_{OH} Minimum High Level Output Voltage — The worst case high–level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{OL} Maximum Low Level Output Voltage — The worst case low–level voltage at an output for a given output current (I_{out}) and supply voltage (V_{CC}).

V_{T+} Positive–Going Input Threshold Voltage — The minimum input voltage of a device with hysteresis which is recognized as a high level. (Assumes ramp up from previous low level.)

V_{T-} Negative–Going Input Threshold Voltage — The maximum input voltage of a device with hysteresis which is recognized as a low level. (Assumes ramp down from previous high level).

V_H Hysteresis Voltage — The difference between V_{T+} and V_{T-} of a given device with hysteresis. A measure of noise rejection.

I_{CC} IC Quiescent Supply Current — The current into the V_{CC} pin when the device inputs are static at V_{CC} or GND and outputs are not connected.

ΔI_{CC} Additional Quiescent Supply Current — The current into the V_{CC} pin when one of the device inputs is at 2.4 V with respect to GND and the other inputs are static at V_{CC} or GND. The outputs are not connected.

I_{in} Input Current — The current into an input pin with the respective input forced to V_{CC} or GND. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{out} Output Current — The current out of an output pin. A negative sign indicates current is flowing out of the pin (source). A positive sign or no sign indicates current is flowing into the pin (sink).

I_{IH} Input Current (High) — The input current when the input voltage is forced to a high level.

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I_{IL} **Input Current (Low) —** The input current when the input voltage is forced to a low level.

I_{OH} **Output Current (High) —** The output current when the output voltage is at a high level.

I_{OL} **Output Current (Low) —** The output current when the output voltage is at a low level.

I_{OZ} **Three–State Leakage Current —** The current into or out of a three–state output in the high–impedance state with that respective output forced to V_{CC} or GND.

t_{PLH} **Low–to–High Propagation Delay (HC) —** The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from low level to high level. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from low level to high level.

t_{PHL} **High–to–Low Propagation Delay (HC) —** The time interval between the 0.5 V_{CC} level of the controlling input waveform and the 50% level of the output waveform, with the output changing from high level to low level. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the controlling input waveform and the 1.3 V level (with respect to GND) of the output waveform, with the output changing from high level to low level.

t_{PLZ} **Low–Level to High–Impedance Propagation Delay (Disable Time) —** The time interval between the 0.5 V_{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 10% level of the output waveform, with the output changing from the low level to high–impedance (off) state.

t_{PHZ} **High–Level to High–impedance Propagation Delay (Disable Time) —** The time interval between the 0.5 V_{CC} level for HC devices (1.3 V with respect to GND for HCT devices) of the controlling input waveform and the 90% level of the output waveform, with the output changing from the high level to high–impedance (off) state.

t_{PZL} **High–Impedance to Low–Level Propagation Delay (Enable Time) —** The time interval between 0.5 V_{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high–impedance (off) state to a low level.

t_{PZH} **High–Impedance to High–Level Propagation Delay (Enable Time) —** The time interval between the 0.5 V_{CC} level (HC) or 1.3 V level with respect to GND (HCT) of the controlling input waveform and the 50% level (HC) or 1.3 V level with respect to GND (HCT) of the output waveform, with the output changing from the high–impedance (off) state to a high level.

t_{TLH} **Output Low–to–High Transition Time —** The time interval between the 10% and 90% voltage levels of the rising edge of a switching output.

t_{THL} **Output High–to–Low Transition Time —** The time interval between the 90% and 10% voltage levels of the falling edge of a switching output.

t_{su} **Setup Time —** The time interval immediately preceeding the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative setup time indicates that the data at the input may be applied sometime after the active clock or latch transition and still be recognized. For HC devices, the setup time is measured from the 50% level of the data waveform to the 50% level of the clock or latch input waveform. For HCT devices, the setup time is measured from the 1.3 V level (with respect to GND) of the data waveform to the 1.3 V level (with respect to GND) of the clock or latch input waveform.

t_h **Hold Time —** The time interval immediately following the active transition of a clock or latch enable input, during which the data to be recognized must be maintained (valid) at the input to ensure proper recognition. A negative hold time indicates that the data at the input may be changed prior to the active clock or latch transition and still be recognized. For HC devices, the hold time is measured from the 50% level of the clock or latch input waveform to the 50% level of the data waveform. For HCT devices, the hold time is measured from the 1.3 V level (with respect to GND) of the clock or latch input waveform to the 1.3 V level (with respect to GND) of the data waveform.

t_{rec} **Recovery Time (HC) —** The time interval between the 50% level of the transition from active to inactive state of an asynchronous control input and the 50% level of the active clock or latch enable edge required to guarantee proper operation of a device. **(HCT) —** The time interval between the 1.3 V level (with respect to GND) of the transition from active to inactive state of an asynchronous control input and the 1.3 V level (with respect to GND) of the active clock or latch edge required to guarantee proper operation of a logic device.

t_w **Pulse Width (HC) —** The time interval between 50% levels of an input pulse required to guarantee proper operation of a logic device. **(HCT) —** The time interval between 1.3 V levels (with respect to GND) of an input pulse required to guarantee proper operation of a logic device.

t_r **Input Rise Time (HC) —** The time interval between the 10% and 90% voltage levels on the rising edge of an input signal. **(HCT) —** The time interval between the 0.3 V level and 2.7 V level (with respect to GND) on the rising edge of an input signal.

t_f **Input Fall Time (HC) —** The time interval between the 90% and 10% voltage levels on the falling edge of an input signal. **(HCT) —** The time interval between the 2.7 V level and 0.3 V level (with respect to GND) on the falling edge of an input signal.