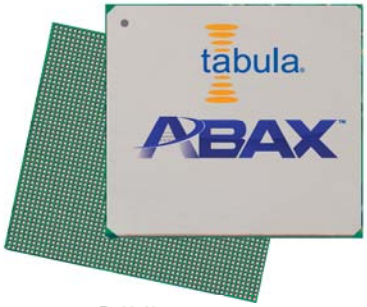
tabula

ABAX™

PRODUCT FAMILY OVERVIEW



Enabled by: SPACETIME™

Electronic systems manufacturers have always wanted to bring innovative, large-scale designs to market quickly while keeping unit costs low. Addressing this daunting, unmet need requires a scalable, programmable platform: one that can be used from the first explorations of a new idea all the way through volume production. Current programmable devices, such as FPGAs, fail to meet this need because they are simply too large to be cost-effective in most production settings.

Tabula's ABAX™ family of 3D Programmable Logic Devices (3PLD) represents a new category of general-purpose chips. Leveraging Tabula's breakthrough Spacetime™ architecture, ABAX delivers programmability with unprecedented capabilities at volume price points. Setting new marks in density and performance for logic, memory, and signal processing, ABAX extends the benefits of programmability to many applications that previously required ASICs or ASSPs. In addition, ABAX devices have a rich mixture of fully configurable, high-performance I/Os, including 920 general-purpose I/Os and 48 6.5Gbps SerDes. The design flow is similar to FPGA and ASIC flows; using synthesis, placement, and routing to compile designs from RTL into silicon automatically. To increase designers' productivity, ABAX also supports a broad portfolio of soft IP cores. ABAX products are manufactured using TSMC's 40 nm process.

FEATURE SUMMARY

SPACETIME FABRIC - HIGH DENSITY, CAPACITY, PERFORMANCE AND THROUGHPUT

- Logic: 0.22 MegaLUT to 0.63 MegaLUT (4-input LUT equivalent), operating at up to 1.6 GHz
- Memory: 5.5 MBYTES of high-performance 1.6 GHz RAM, consisting of three different block sizes. Featuring 8 and 16 ports and built-in ECC and FIFO controller
- DSP blocks: up to 1280 1.6 GHz, configurable, 18x18 multiplier/ accumulators (MAC)
- High-performance clock network supporting 1.6 GHz operations

CONFIGURABLE PARALLEL I/O

- 920 high-performance, parallel I/O supporting a wide range of single-ended and differential I/O standards
- Dedicated hardware to support the latest memory standards
- Designed in conjunction with the ABAX device package for best SSN performance

CONFIGURABLE SERDES

- Each ABAX device has 48 SerDes channels supporting data rates between 55 Mbps and 6.5 Gbps
- Built-in fully programmable PCS and PMA circuitry with dedicated support for networking, communications, and video protocols

SPACETIME COMPILER

- Integrated design system including synthesis, placement and routing, timing analysis, and configuration generation, using VHDL/Verilog inputs
- Intuitive GUI front-end with integrated Tcl scripting
- Broad portfolio of design library building blocks and 3rd party soft IP cores

DEVICE CONFIGURATION

- Flexible and simple-to-use configuration modes including SPI flash, CPU, and JTAG
- Built-in multi-image support

SPACETIME™ ARCHITECTURE

Spacetime is a groundbreaking programmable logic architecture that uses time as a third dimension to deliver unmatched capability and affordability. Tabula achieves this breakthrough by combining the Spacetime hardware that dynamically reconfigures logic, memory, and interconnect at multi-GHz rates with the Spacetime compiler that manages ultra-rapid reconfiguration transparently. Tabula leverages Spacetime to deliver 3D devices that have significant density advantages and dramatically shorter interconnects when compared to FPGAs that use 2D architectures. In addition, Tabula delivers these benefits while preserving a traditional design methodology. As a result, Spacetime enables a new class of programmable devices that combines the capability of an ASIC with the ease of use of an FPGA at price points suitable for volume production.

- All the advantages of FPGAs
  - Re-programmability at the desktop and in the field
  - Familiar design flow
- Plus the benefits of 3D
  - Highest logic density
  - Highest memory density
  - Highest memory port count
  - Highest DSP performance

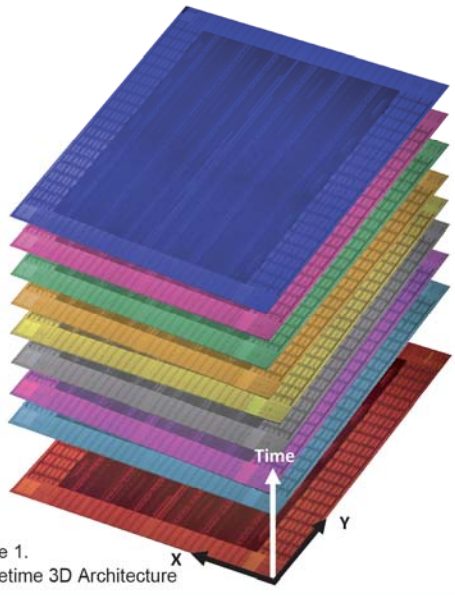


Figure 1.
Spacetime 3D Architecture

CONFIGURABLE I/O

- To enable greater flexibility and ease of system design, ABAX devices' parallel I/O and SerDes are fully programmable and support a broad range of standards

PARALLEL I/O

- Each ABAX device has 920 fully featured General Purpose I/O (GPIO)
  - Fully configurable to support a broad range of standards
  - Per bit de-skew
  - Built-in hardware for clock control between Spacetime fabric and I/O
  - Dedicated support for DDR standards
    - Hardware-assisted read/write leveling

SERDES

- Each ABAX device has 48 SerDes
  - 55 Mbps - 6.5 Gbps operation
  - Built-in PMA and PCS per SerDes channel
  - Fully programmable PMA and PCS
  - Independent clocking per channel
  - Channel bond: 2-24 channels

PARALLEL I/O CLASS	STANDARD	PERFORMANCE (MHz)	DDR (Mb/s) PERFORMANCE
3.0V, 2.5V, 1.8V, 1.5V LVTTL/LVCMOS	General purpose	200	400
SSTL-2 Class I, II	DDRSDRAM	200	400
SSTL-18 Class I, II	DDR2 SDRAM	400	800
SSTL-15	DDR3 SDRAM	400	800
HSTL-18 Class I, II	QDRII/QDRII+/RLDRAM II	400	800
HSTL-15 Class I, II	QDRII/QDRII+/RLDRAM II	400	800
Diff SSTL-2 Class I, II	DDR SDRAM	200	400
Diff SSTL-18 Class I, II	DDR2 SDRAM	400	800
Diff SSTL-15	DDR3 SDRAM	400	800
Diff HSTL-18 Class I, II	Clock interfaces	400	800
Diff HSTL-15 Class I, II	Clock interfaces	400	800
LVDS	High-speed comm.	600	1200
RSDS & Mini-LVDS	Flat panel display	85	170
HyperTransport	µP bus/router/switch	600	1200
LVPECL	Clock interfaces	450	900
Open Drain	General purpose	–	–

SERDES STANDARDS	DATA RATE (Gbps)
PCI Express Gen1 and Gen2	2.5, 5
GbE/SGMII	1.25
XAUI/RXAUI	3.125, 6.25
Interlaken	3.125-6.375
GPON	1.244, 2.488
Serial RapidIO	1.25, 2.5, 3.125, 6.25
CPRI LV	0.614, 1.228, 2.457, 3.072, 6.144
OBSAI	0.768, 1.536, 3.072, 6.144
Sonet	0.155, 0.622, 2.488
SMPTE SD/HD	0.270, 1.485, 2.97
DisplayPort	1.62, 2.7, 5.4
Fibre Channel	1.06, 2.12, 4.25
SATA/SAS	1.5, 3.0, 6.0
DVB-ASI	0.270
JC-16	0.3125-3.125
OIF SPI-S/SFI-5	3.125

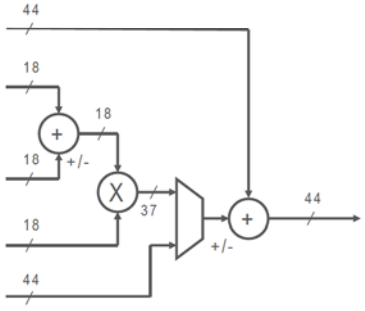
EMBEDDED MEMORY

- ABAX products integrate 5.5 MBYTES of 8- and 16-port configurable user RAM
- RAM blocks come in three sizes to support various use models. They are configurable in width and depth to accommodate different data sizes
- 8- and 16-ported memories
  - Ultra high memory bandwidth
  - High utilization of memory resources, even when data size and RAM block size do not match
- Memory mapping and multi-port memory generation are automatically managed by the Spacetime compiler
  - Simple to use; no additional user logic required

	LRAM (Large RAM)	MRAM (Medium RAM)	RegFILE
Block Size	72Kb	36Kb	576b
Ports	Up to 8	Up to 16	Up to 16
Configuration	36Kx2/ 18Kx4/ 9Kx8/ 4Kx16/ 9Kx9/ 4Kx18	18Kx2 /9Kx4/ 4Kx8/ 2Kx16/ 4Kx9/ 2Kx18	9 x 64
Access	Synchronous	Synchronous	Synchronous Write/ Asynchronous Read
Features	ECC	ECC, Built-in FIFO controller with programmable watermark	Usable as a 6-LUT

DSP BLOCK

- The ABAX devices include up to 1280 DSP blocks optimized for data processing-intensive applications such as LTE base-stations and video processing
  - 1.6 GHz operations, matched to fabric performance
  - 18-bit pre-add/sub
  - 18x18 multiplier
  - 44-bit accumulator
  - Multi-context accumulator storage
  - 44-bit result with optional post-processing
  - Cascadable



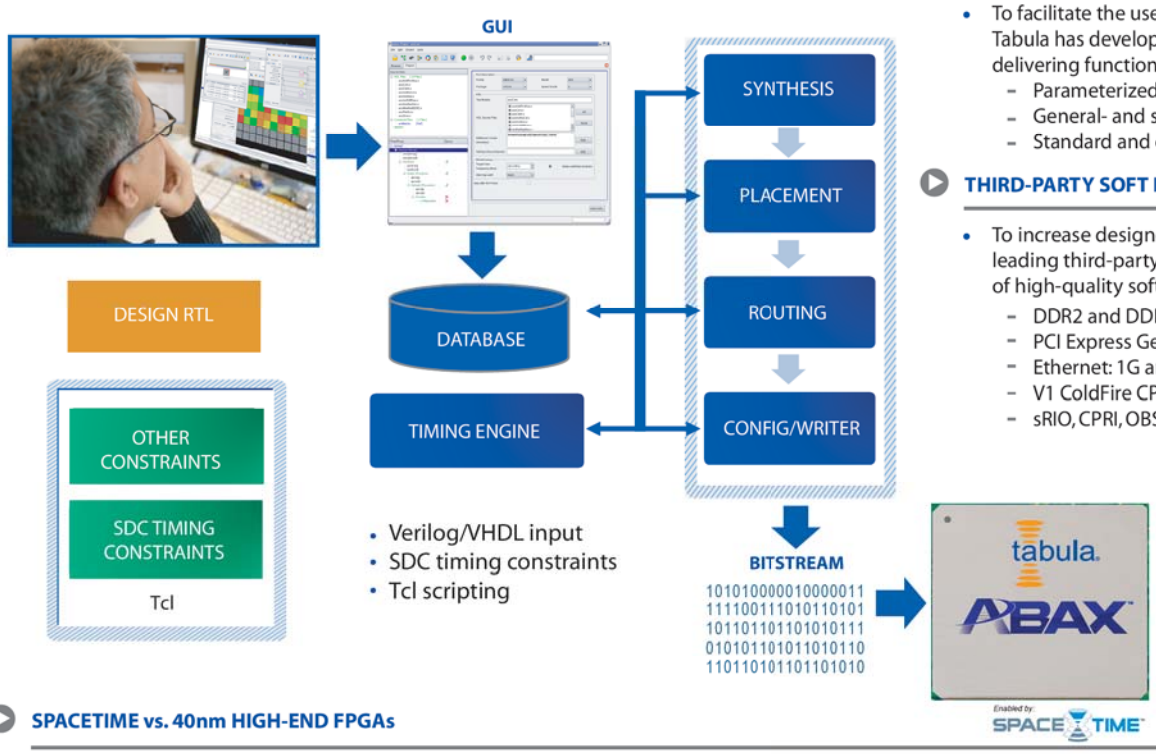
CLOCK RESOURCES

- To facilitate implementation of high-performance designs, a rich set of clocking resources has been built into each ABAX family member
  - Fabric clocks from I/O PLL
    - Up to 44 clock PLL providing regional and global clock reach
  - Fabric clock regions
    - Up to 5 per device

SPACETIME COMPILER

- The Spacetime architecture is designed to work with your existing design methodology. Therefore, there is no need to change or adapt your design environment to accommodate its 3D nature
- The Spacetime compiler automatically maps, places, and routes your design into an ABAX device using standard design inputs and flows
  - Verilog/VHDL input
  - An intuitive GUI to manage design inputs, projects, and design flows
  - SDC timing constraints and Tcl-based pin and placement constraints
- All control of the hardware reconfiguration is automatically and invisibly managed by the Spacetime compiler

STANDARD DESIGN TOOLS AND FLOW



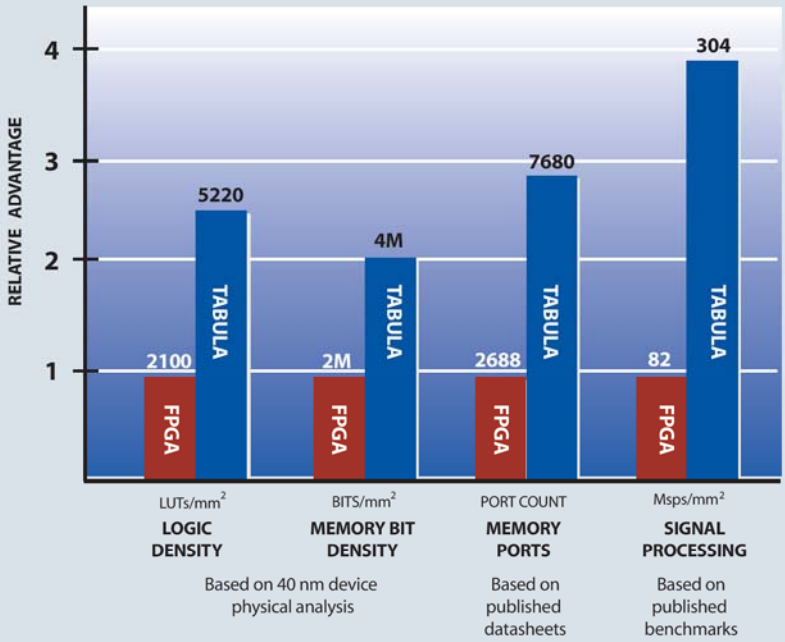
MACRO LIBRARY

- To facilitate the use of ABAX devices' rich on-chip resources, Tabula has developed a library of fully validated macros delivering functionality for:
  - Parameterized multi-port memories
  - General- and special-purpose I/O interfaces
  - Standard and custom SerDes protocols

THIRD-PARTY SOFT IP

- To increase designers' productivity, Tabula is working with leading third-party soft IP suppliers to offer a broad portfolio of high-quality soft IP solutions, including:
  - DDR2 and DDR3 Memory Controllers
  - PCI Express Gen 1 and Gen 2
  - Ethernet: 1G and 10G
  - V1 ColdFire CPU
  - sRIO, CPRI, OBSAI

SPACETIME vs. 40nm HIGH-END FPGAs



2.5x LOGIC DENSITY VS. FPGA

Unlike FPGAs, Spacetime devices are capable of dynamically changing configurations at multi-GHz frequency. As a result, logic, memory and routing resources are all re-used multiple times per user cycle, enabling much higher density and shorter interconnect than FPGAs.

2.0x MEMORY DENSITY VS. FPGA

FPGAs use large dual-port memory cells for their embedded memory blocks to support the multi-port functionality required in most communications and data-processing applications. Spacetime memories provide greater multi-port flexibility while using twice denser single-port memory cells.

2.9x MEMORY PORTS VS. FPGA

FPGA memories have 2 ports, whereas Spacetime memories have 8 or 16 ports. Many communications and data-processing applications can take advantage of such multi-ported memories which enable functions such as broadcast, muxing, de-muxing multiple channels of data, and 2-read/1-write register files.

3.7x DSP PERFORMANCE VS. FPGA

The logic fabric on FPGA runs much more slowly than the hard multipliers, which limits practical DSP throughput to that of the slow fabric, rather than that of the fast multiplier. In contrast, with Spacetime, the logic fabric, memories, and DSP blocks can all run at 1.6 GHz, which eliminates this bottleneck. The resulting high-speed pipelines in Spacetime are setting new standards for signal-processing performance.

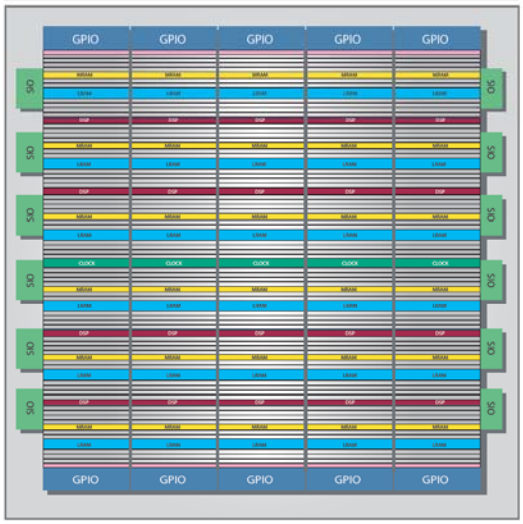
PACKAGING AND SIGNAL INTEGRITY

- ABAX devices are available in 1936-pin and 1156-pin, high-performance, flip-chip packages
- Ten-layered, high-performance, flip-chip package (4-2-4) with two primary signal layers and eight layers for power and ground planes
- All differential signals are skew-matched to <10 ps and are isolated from each other with crosstalk < 2%

ABAX PRODUCT FAMILY

FEATURES	A1EC02	A1EC03	A1EC04	A1EC06
MegaLUT	0.22	0.30	0.39	0.63
MegaBYTEs RAM	5.5	5.5	5.5	5.5
RegFile Blocks	960	960	960	960
LRAM (Large RAM) Blocks	480	480	480	480
MRAM (Medium RAM) Blocks	240	240	240	240
Multiplier/Accumulators (18x18)	–	–	–	1280
Parallel I/Os	920	920	920	920
SerDes (55 Mb/s - 6.5 Gb/s)	48	48	48	48
PLLs	44	44	44	44

A1EC06 FLOOR PLAN



ABAX PRODUCT FAMILY OPTIONS AND I/O PIN COUNTS

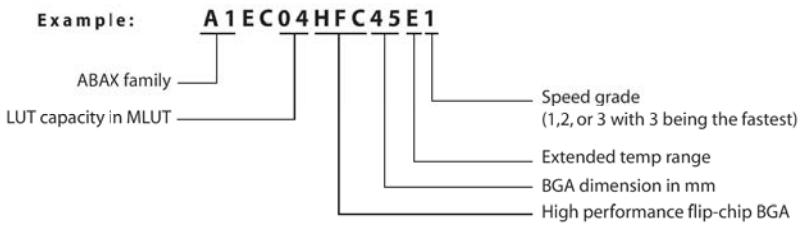
Pins/GPIOs/6.5Gbps SerDes	A1EC02	A1EC03	A1EC04	A1EC06
45mm FCBGA	1936/920/48	1936/920/48	1936/920/48	1936/920/48
35mm FCBGA	1156/496/24	1156/496/24	1156/496/24	1156/496/24

- Vertical Migration
  - To simplify system design evolution and upgrade, all the devices in a package share a common footprint and pinout, enabling vertical migration

SPEED GRADE OPTIONS

SPEED GRADE	DESCRIPTION
1	Base
2	Medium
3	Fast

ABAX ORDERING INFORMATION



EXTENDED TEMPERATURE RANGE

- The maximum junction temperature range for all ABAX devices is -40°C to +125°C

ABOUT TABULA, INC.

Tabula is a privately held, fabless semiconductor company developing 3D Programmable Logic Devices (3PLD). The Company's ABAX family of general-purpose 3PLDs, based on Tabula's patented Spacetime architecture, sets a new benchmark for the capability of programmable devices at volume price points, enabling re-programmability not only in FPGA applications but also in those historically served only by ASICs or ASSPs. Based on Tabula's patented Spacetime architecture, ABAX uses time as a third dimension to advance logic density, memory capability and signal processing performance while still preserving a traditional design flow. Headquartered in Santa Clara, California, Tabula has over 100 employees and has assembled a leadership team consisting of industry veterans and successful entrepreneurs. Tabula is backed by top-tier investors with a long-term view toward enduring market leadership.

3250 Olcott St. Santa Clara, CA 95054 Phone: 408.986.9140 Fax: 408.986.9146 For more information on Tabula, please contact us at sales@tabula.com