AM335x ARM Cortex-A8 Microprocessors (MPUs)
Silicon Revision 1.0

Silicon Errata

Literature Number: SPRZ360
October 2011

Contents

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1 Introduction

This document describes the known exceptions to the functional specifications for the AM335x ARM Cortex-A8 Microprocessors (MPUs). [See the *AM335x ARM Cortex-A8 Microprocessors (MPUs)* data manual (literature number SPRS717).]

For additional information, see the latest version of the *AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical Reference Manual* (literature number SPRUH73).

1.1 AM335x Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (e.g., XAM3358ZCE). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X — Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P — Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null — Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX — Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS — Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

1.2 Revision Identification

The device revision can be determined by the symbols marked on the top of the package. Figure 1 provides an example of the AM335x device markings.

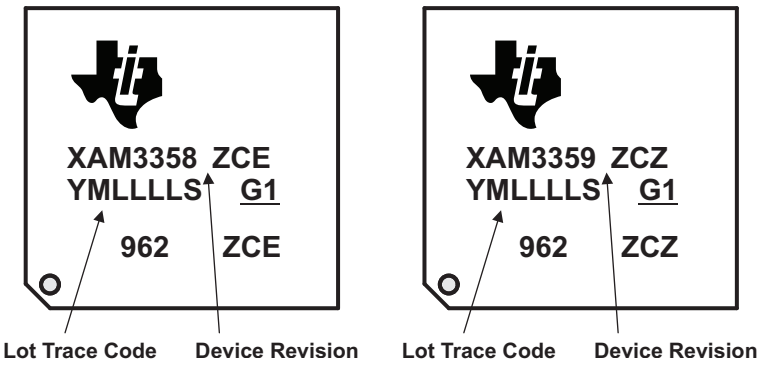

Figure 1. Example of Device Revision Codes for the AM335x Microprocessor

NOTES:

(A) Non-qualified devices are marked with the letters "X" or "P" at the beginning of the device name, while qualified devices have a "blank" at the beginning of the device name.

(B) The AM3358 and AM3359 devices shown in this device marking example are two of several valid part numbers for the AM335x family of devices.

(C) The device revision code is the device revision (A, B, etc.).

(D) YM denotes year/month.

(E) LLLL denotes Lot Trace Code.

(F) 962 is a generic family marking ID.

(G) G1 denotes green, lead-free.

(H) ZCE or ZCZ is the package designator.

(I) S denotes Assembly Site Code.

(J) On some "X" devices, the device speed may not be shown.

Silicon revision is identified by a code marked on the package. The code is of the format AM3358x, where "x" denotes the silicon revision. Table 1 lists the information associated with each silicon revision for each device type. For more details on device nomenclature, see the device-specific data manual.

Table 1. AM335x Production Device Revision Codes

DEVICE REVISION CODE (x)	SILICON REVISION	COMMENTS
(blank)	1.0	Silicon revision is new

Each silicon revision uses a specific revision of TI's ARM® Cortex™-A8 processor. The ARM Cortex-A8 processor variant and revision can be read from the Main ID Register. The ROM code revision can be read from address 2BFFCh. The ROM code version consists of two decimal numbers: major and minor. The major number is always 22, minor number counts ROM code version. The ROM code version is coded as hexadecimal readable values; e.g., ROM version 22.02 will be coded as 0000 2202h. Table 2 shows the ROM code revision for each silicon revision of the device.

Table 2. Silicon Revision Variables

SILICON REVISION	ARM CORTEX-A8 VARIANT/REVISION	ROM REVISION
1.0	r3p2	22.02

2 All Errata Listed With Silicon Revision Number

Table 3. All Design Exceptions to Functional Specifications

Type/Number	Title	Revision Affected
		1.0
Advisory 1.0.1	DDR2/3/mDDR PHY: Control/Status Registers Configured for Write Only	X
Advisory 1.0.2	Debug Subsystem: EMU[4:2] Signals Are Not Available by Default After Reset	X
Advisory 1.0.3	Debug Subsystem: Internal Inputs Tied-off to the Wrong Value	X
Advisory 1.0.4	PRU Subsystem: Clock Domain Crossing (CDC) Issue	X
Advisory 1.0.5	RTC: 32.768-kHZ Clock is Gating Off	X
Advisory 1.0.6	EXTINTn: Input Function of the EXTINTn Terminal is Inverted	X
Advisory 1.0.7	Boot: Ethernet Boot ROM Code PHY Link Speed Detection	X

3 Revision 1.0 Usage Notes and Known Design Exceptions to Functional Specifications

3.1 Revision 1.0 Usage Notes

This document contains Usage Notes. Usage Notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes may be incorporated into future documentation updates for the device (such as the device-specific data manual), and the behaviors they describe may or may not be altered in future device revisions.

3.1.1 LCD: Color Assignments of LCD_DATA Terminals

The blue and red color assignments to the LCD data pins are reversed when operating in RGB888 (24bpp) mode compared to RGB565 (16bpp) mode. In order to correctly display RGB888 data from the SGX, or any source formatted as RGB in memory, it is necessary to connect the LCD panel as shown in Figure 2. Using the LCD Controller with this connection scheme limits the use of RGB565 mode. Any data generated for the RGB565 mode requires the red and blue color data values be swapped in order to display the correct color.

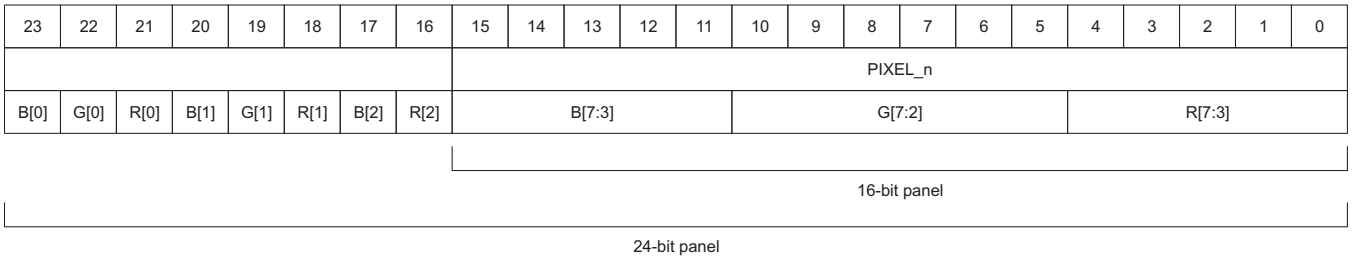

Figure 2. RGB888 Mode LCD Controller Output Pin Mapping (LCD_DATA[23:0])

When operating the LCD Controller in RGB565 mode the LCD panel should be connected as shown in Figure 3. Using the LCD Controller with this connection scheme limits the use of RGB888 mode. Any data generated for the RGB888 mode requires the red and blue color data values be swapped in order to display the correct color.

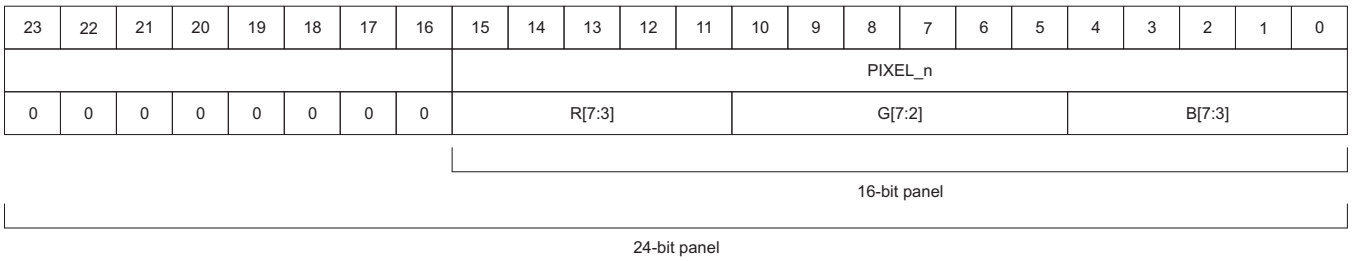

Figure 3. RGB565 Mode LCD Controller Output Pin Mapping (LCD_DATA[23:0])

3.1.2 DDR3: JEDEC Compliance for Maximum Self-Refresh Command Limit

When using DDR3 EMIF Self-Refresh, it is possible to violate the maximum refresh command requirement specified in the JEDEC standard DDR3 SDRAM Specification (JESD79-3E, July 2010). This requirement states that the DDR3 EMIF controller should issue no more than 16 refresh commands within any 15.6-µs interval.

To avoid this requirement violation, when using the DDR3 EMIF and Self-Refresh (setting LP_MODE = 0x2 field in the PMCR), the SR_TIM value in the PMCR must to be programmed to a value greater than or equal to 0x9.

3.2 Revision 1.0 Known Design Exceptions to Functional Specifications

Table 4 lists known design exceptions to functional specifications for device revision 1.0. Advisories are numbered in the order in which they were added to this document. Some advisory numbers may be moved to the next revision and others may have been removed because the design exception was fixed or documented in the device-specific data manual or peripheral user's guide. When items are moved or deleted, the remaining numbers remain the same and are not re-sequenced.

Table 4. Revision 1.0 Advisory List

Advisory 1.0.1 *DDR2/3/mDDR PHY: Control/Status Registers Configured for Write Only*

Revision(s) Affected 1.0

Details The DDR2/3/mDDR PHY control/status registers mapped in address range 0x44e12000-0x44E123FF are configured for write-only operations, so the contents of these register cannot be read.

These registers must be configured by performing write-only operations.

Workaround(s) There is no workaround for this issue.

Advisory 1.0.2 *Debug Subsystem: EMU[4:2] Signals Are Not Available by Default After Reset*

Revision(s) Affected 1.0

Details All Debug subsystem components should remain unchanged when warm reset is asserted. For example, warm reset should not affect export of debug trace messages on the EMU[4:0] signals.

The AM335x EMU[4:2] signals can not be used to export trace messages from the Debug subsystem since AM335x does support warm reset and the EMU[4:2] signals are not assigned to pins after reset is asserted.

Workaround(s) Do not assert warm reset while performing trace functions.

Advisory 1.0.3 *Debug Subsystem: Internal Inputs Tied-off to the Wrong Value*

Revision(s) Affected 1.0

Details Internal inputs dbg_dpio_attr_dp_app_owner[4:0] and dbg_dpio_attr_dp_debug_only[4:0] to the Debug subsystem are used to report which EMU[4:0] signals can currently be used to export trace messages. These inputs were tied-off to the wrong value. The tie-off values used will always indicate EMU[4:2] signals are not available and EMU[1:0] signals are available to export trace messages.

This should not cause a problem for EMU[4:2] since these signals can not be used to export trace messages for the reason explained in advisory 1.3. However, the AM335x pins used for EMU[1:0] signals may be configured as GPIO. The Debug subsystem would not know these signals are not available for exporting trace messages when these pins are configured as GPIO.

Workaround(s) Do not configure the AM335x EMU[1:0] pins to operate as GPIO if you need to export trace messages.

Advisory 1.0.4 *PRU Subsystem: Clock Domain Crossing (CDC) Issue*

Revision(s) Affected 1.0

Details The PRU subsystem has a clock domain crossing issue when the MII receive multiplexer is configured to connect PR1_MII1 signals to PRU0 and PR1_MII0 signals to PRU1.

The multiplexer logic always uses the PR1_MII_MR0_CLK input to synchronize the PRU0 MII receive signals and the PR1_MII_MR1_CLK input to synchronize the PRU1 MII receive signals. This cause the wrong clock to be used when the MII receive multiplexer is configured to connect PR1_MII1 signals to PRU0 and PR1_MII0 signals to PRU1.

Workaround(s) There is no workaround for this issue.

Advisory 1.0.5 *RTC: 32.768-kHZ Clock is Gating Off*

Revision(s) Affected 1.0

Details The RTC has a clock gating issue that stops the internal 32.768-kHz clock when the VDD_CORE voltage domain drops below the recommended operating range or the PWRONRSTn input terminal is held low. This issue has the following side effects:

- The RTC counters stop incrementing when the 32.768-kHz clock is gated. This causes the RTC to lose time while the clock is gated.
- A wakeup event applied to the EXT_WAKEUP input terminal is masked if the EXT_WAKEUP_DB_EN bit in the RTC PMIC register (0x98) is set to 1 which enables the de-bounce function for the EXT_WAKEUP input. This occurs because the 32.768-kHz clock is being used to clock the de-bounce circuit.

Workaround(s) Do not turn off the VDD_CORE power source or source a logic low to the PWRONRSTn input while expecting RTC to keep an accurate time.

Do not enable the de-bounce circuit on the EXT_WAKEUP input if an external wakeup event needs to be detected while the 32.768-kHz clock is gated.

Advisory 1.0.6 *EXTINTn: Input Function of the EXTINTn Terminal is Inverted*

Revision(s) Affected 1.0

Details The EXTINTn input is active high.

Workaround(s) Use an active high interrupt source or use an external inverter to change the polarity of any active low interrupt source.

Advisory 1.0.7 *Boot: Ethernet Boot ROM Code PHY Link Speed Detection*

Revision(s) Affected 1.0

Details The device ROM code relies on the external PHY's Control Register (Register 0), specifically bits 0.6 [Speed Selection (MSB)] and 0.13 [Speed Selection (LSB)], to determine the operating speed of the link.

If the external PHY does not update its link speed selection bits to reflect the current operating speed, the ROM code will incorrectly assume the PHY is operating at the speed indicated by the link speed selection bits and configure the device Ethernet MAC to the wrong speed. For example, if the default value of the PHY link speed selection bits indicates 1 Gbps, when the PHY is actually operating at 100 Mbps, the ROM will incorrectly configure the device Ethernet MAC for 100 Mbps mode.

The IEEE 802.3 specification states: *When Auto-Negotiation Enable (bit 0.12) is enabled, bits 0.6 and 0.13 can be read or written to, but the state of bits 0.6 and 0.13 have no effect on the link configuration, and it is not necessary for bits 0.6 and 0.13 to reflect the operating speed of the link when it is read*. While some PHYs update the link speed in these bits to reflect the current operating speed, other PHYs do not update these bits because it is not mandatory according to the specification.

Workaround(s) When using Ethernet boot, an external PHY that updates the Register 0 link speed selection bits (0.6 and 0.13) to reflect the current operating speed is required.

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