LatticeECP4 Family Overview

Advance DS1037A Version 01.1, February 2012

LatticeECP4 Family Overview Introduction

February 2012 Advance Data Sheet DS1037A

Features

- **Higher Logic Density for Increased System Integration**
  - 33K to 241K LUTs
  - 224 to 512 I/Os and PCS
- **Embedded SERDES and PCS**
  - Data rates of 155 Mbps to 6.375 Gbps/channel
    - Wire-bond: 4G backplane and 6.375 Gbps chip-to-chip
    - Lidded Flip Chip: up to 6.375 Gbps backplane
  - Up to 16 channels per device:
    - PCI Express 2.1, SONET/SDH, GMII, Q/SGMII, R/XAUI, CPRI, SMPTE 3G, Serial RapidIO 2.1 (up to 6.25 Gbps), and more
  - Automatic Decision Feedback Equalizer (DFE) and Multiple Stage Linear Equalizer (LEQ)
- **sysDSP™**
  - Fully cascadable slice architecture with pre-adders
  - 500 MHz block performance based on double data rate conversion
  - 32 to 288 slices (64 to 576 18x18 multipliers and pre-adders) for high performance multiply and accumulate
  - Powerful 54-bit ALU operations
  - Time Division Multiplexing MAC Sharing
  - Rounding and truncation
  - 1D and 2D Symmetry support
  - Long FIR support (across multiple DSP rows)
  - Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources
  - Each slice supports
    - Half 36x36, two 18x18 or four 9x9 multipliers
    - Advanced 18x36 MAC and 18x18 Multiply-Multiply-Accumulate (MMAC) operations
- **Flexible Memory Resources**
  - Up to 10.6 Mbits Embedded Block RAM (EBR)
  - 18Kb blocks with up to 400MHz performance
  - Data width range from x1 up to x18 (and x36 for pseudo-dual port and single port)
  - Single port, Dual port, and Pseudo Dual Port operation
  - Built-in FIFO control logic
- **sysCLOCK PLLs**
  - Eight PLLs per device each with 4 outputs
  - Variable degree phase shifts per output
  - Input and output frequencies of up to 625 MHz
  - Outputs can be independently disabled and output clocks can be stopped
- **High-speed I/O**
  - DDR3 support of up to 1067 Mbps with dynamic ODT (on-die termination)
  - Hot socket and PCI clamp on all FPGA IO (excluding SERDES)
  - Source synchronous standards support
    - Max rate of 1.25Gbps (edge clock rate of 625MHz)
    - Dynamic phase alignment and CDR capability (using additional soft logic)
  - Optional Inter-Symbol Interference (ISI) correction on outputs
  - Eight DDRDLLs for phase-shifting on clock-forwarded applications
  - Up to 4 high speed edge clocks per side allow for multiple interfaces on each side
  - Input/Output Data Delay block with dynamic controls available on all I/O pins
- **Programmable sysI/O™ Buffer Supports Wide Range of Interfaces**
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 25/18/15 I, II
  - HSTL15 I, II and HSTL18 I, II
  - HSUL12 for Low Power DDR2
  - PCI and Differential HSTL, SSTL
  - LVDS, SLVDS, SUBLVDS, MIPI, TRLVDS, PPLVDS, MINILFVDS
  - Bus-LVDS, LVPECL, RSDS, MLVDS
- **Flexible Device Configuration**
  - Dedicated bank for configuration I/Os
  - SPI boot Flash interface
  - Dual-boot images supported
  - Slave SPI processor programming
  - TransFR™ I/O for simple field updates
  - Soft Error Detect embedded macro
  - Built-in encryption bit stream
- **MACO Communication Engines**
  - Largest variety of pre-engineered hard communication protocol processors
  - PCI Express 2.1 (up to 4x5 Gbps)
  - SRIO 2.1 (up to 4x6.25 Gbps)
  - 2 x 10 Gbps Ethernet MACs (including HiGig2™ option)
  - Up to 20 x Tri-speed (10/100/1000 Mbps) Ethernet MACs or up to 12 x 2.5G Ethernet MACs
  - 2500 Mbps Ethernet MACs
- **System-Level Support**
  - WISHBONE-based System Control Interface for easy configuration of register-based MACO Communication Engines and SerDes/PCS
  - IEEE 1149.1 and IEEE 1532 compliant
  - Reveal Logic Analyzer support
  - 1.2V core power supply

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LatticeECP4™ Family Selection Guide

Feature	ECP4-30	ECP4-50	ECP4-95	ECP4-130	ECP4-190	ECP4-250
LUT4s (K)	33K	47K	95K	128K	183K	241K
Embedded Memory (Mbits)	1.18	1.18	4.13	4.13	5.9	10.62
DSP Blocks/Multipliers (18x18)[2]	16/64	16/64	56/224	56/224	120/480	144/576
EBR Blocks (18k)	64	64	224	224	320	576
PLLs	8	8	8	8	8	8
DDRDLLs	8	8	8	8	8	8
MACO™ Blocks (250K Usable Gates)	1	1	2	2	3	4
Distributed RAM (Kbits)	263	378	762	1027	1465	1926
Edge Clocks per Bank (L, R, T)[1]	4	4	4	4	4	4
I/O Features						
Dedicated I/Os	11	11	11	11	11	11
I/O Banks	6	6	6	6	8	8
Maximum User I/Os	224	224	392	392	456	512
Maximum LVDS Input Pairs	112	112	196	196	228	256
Maximum LVDS Output Pairs	56	56	98	98	114	128
Maximum 6Gbps SERDES Channels	4	4	8	8	12	16
Maximum 1.25 Gbps CDRs	18	18	32	32	36	40
Packages and SERDES Channels / I/O Combinations at 6.375 GHz						
484-ball fpBGA (23x23 mm)	4/224	4/224	—	—	—	—
648-ball fpBGA (27x27 mm)	4/224	4/224	4/360	4/360	—	—
868-ball fpBGA (31x31 mm)	—	—	8/392	8/392	—	—
676-ball fcBGA (27x27 mm)	4/224	4/224	4/392	4/392	4/392	—
900-ball fcBGA (31x31 mm)	—	—	8/392	8/392	8/456	8/512
1152-ball fcBGA (35x35 mm)	—	—	—	—	12/456	16/512

1. L = Left, R = Right, T = Top.
2. The actual number of DSP Blocks/Multipliers can be twice the number when using the Double-Data-Rate feature. For more information regarding the LatticeECP4 DSP Double-Data-Rate feature, see TN1237, LatticeECP4 sysDSP Usage Guide.

Introduction

The LatticeECP4 (EConomy Plus, Fourth Generation) family of FPGA devices is optimized to deliver unprecedented high-performance features such as an enhanced DSP architecture, 6.375 Gbps SERDES, hard IP blocks and high-speed DDR3 and source synchronous interfaces in an economical FPGA fabric.

The LatticeECP4 device family expands look-up-table (LUT) capacity to 240K logic elements and supports up to 512 user I/Os. The LatticeECP4 device family also offers up to 576 18x18 multipliers and a wide range of parallel I/O standards.

The LatticeECP4 FPGA fabric is optimized with high performance and low cost in mind, supporting 6 Gbps serial protocols, while offering the lowest cost fabric.

The LatticeECP4 devices utilize re-configurable SRAM logic technology and provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, enhanced sysDSP slices and advanced configuration support, including encryption and multi-boot capabilities.

The pre-engineered source synchronous logic implemented in the LatticeECP4 device family supports a broad range of interface standards, including DDR3, XGMII, SPI4.2, and 7:1 LVDS. With additional logic, even serial interfaces like SGMII or Gigabit Ethernet can be supported in the general purpose I/O – an industry-leading capability.

The LatticeECP4 device family features high-speed SERDES with dedicated PCS functions. High jitter tolerance and low transmit jitter allow the SERDES and PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (R/XAUI, GbE, SGMII, and QSGMII) and CPRI for data rates up to 6.375 Gbps. Transmit Pre-emphasis and advanced Receive Equalization (including both Linear and Decision Feedback Equalization) settings make the SERDES suitable for transmission and reception over various forms of media.

The LatticeECP4 devices also provide flexible, reliable and secure configuration options, such as bitstream encryption and TransFR field upgrade features.

Lattice Diamond® design software allows large complex designs to be efficiently implemented using the LatticeECP4 FPGA family of devices. Synthesis library support for LatticeECP4 is available for popular logic synthesis tools. Diamond tools use the synthesis tool output along with the constraints from its floorplanning tools to place and route the design in the LatticeECP4 device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for the LatticeECP4 family. By using these configurable soft IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, thereby increasing their productivity.

LatticeECP4 Family Overview Architecture

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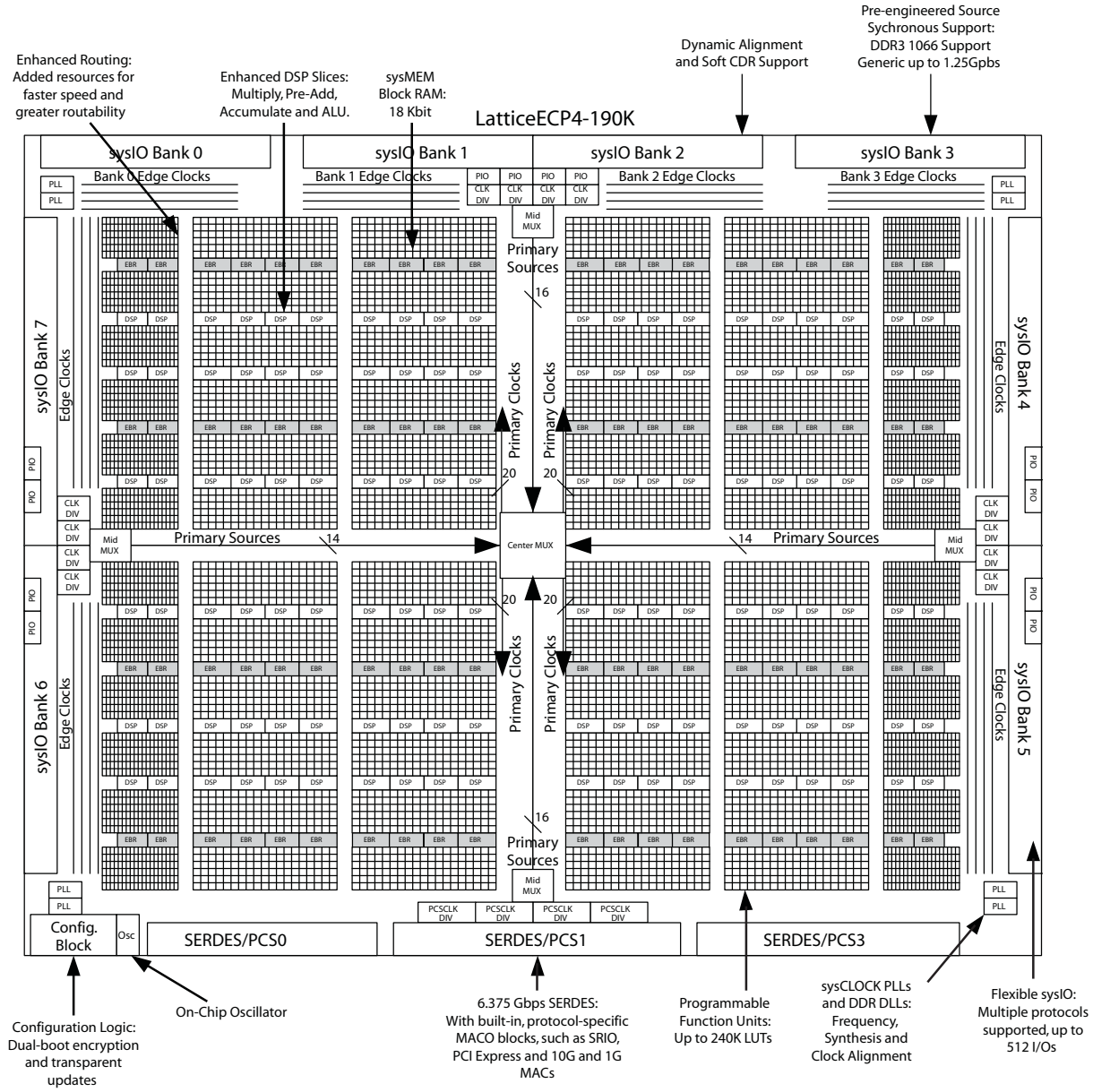
Overview

Each LatticeECP4 device contains an array of Programmable Function Units (PFUs) surrounded by Programmable I/O Cells (PICs). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP Digital Signal Processing slices. The PLLs are on both the left and right sides of the device. The SERDES/PCS quads, MACO, and configuration blocks are on the bottom side of the device. Dedicated I/Os are on the lower left side of the device. An example block diagram of the LatticeECP4-190 is shown in Figure 2-1.

Figure 2-1. Simplified Block Diagram, LatticeECP4-190 Device (Top Level)



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The Programmable Functional Unit (PFU) can be programmed to perform logic, arithmetic, distributed RAM functions and distributed ROM functions. The PFU also supports clock boosting where programmable delay is given to the clock path before it goes to the programmable registers or latches in the PFU. By introducing programmable delay stages to the clocks, longer data paths can be given more time to meet the system constraints without impacting the period of the distributed clock signals and therefore improving overall system performance.

LatticeECP4 devices contain two or more row(s) of embedded memory arranged in blocks called Embedded Block RAM (EBRs). Each EBR consists of 18,432 bits of RAM and includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers. There are numerous configurations and features for each block RAM.

The LatticeECP4 devices contain up to six rows of sysDSP slices. Each sysDSP slice has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

The number of rows of sysDSP slices, number of rows of EBRs, and number of PLLs for the LatticeECP4 devices are shown in Table 2-1.

Table 2-1. EBR Rows, DSP Rows, and PLLs Per Device

	ECP4-30	ECP4-50	ECP4-95	ECP4-130	ECP4-190	ECP4-250
EBR Rows	2	2	4	4	4	6
DSP Rows	2	2	4	4	6	6
PLLs	8	8	8	8	8	8

LatticeECP4 devices support up to 16 SERDES (Serializer/Deserializer) channels with data rates up to 6.375 Gbps. Protocols and rates are selectable per channel. Each SERDES/PCS quad can be configured as four single lanes, two pairs of two lanes, one pair of two lanes and two single lanes, or a group of four lanes.

Digital functions such as word alignment, encoding/decoding, multi-channel lane alignment, and clock tolerance compensation are handled by the Physical Coded Sublayer (PCS). The interface between the SERDES/PCS channel and the FPGA logic is handled by small FIFOs allowing flexible clocking into and out of the FPGA array.

The configuration for both the SERDES and PCS blocks and are set during FPGA configuration can be modified or accessed at runtime using the Embedded Feature Bus (EFB) with a Wishbone interface.

The LatticeECP4 sysIO interface consists of four sysIO blocks. The minimum building block is a quad of four GPIO and is the same on all three sides of the device (left, top, and right edges). Each quad is composed of two pairs of pads. The GPIO is designed to handle high-speed outputs on every pad with differential LVDS outputs on half of the I/O pad pairs. The true LVDS outputs are only available on the A/B pair of pads. Emulated differential outputs are available on every output pair. All GPIOs are hot-socketable.

The LatticeECP4-30, LatticeECP4-50, LatticeECP4-95, and LatticeECP4-130 have six general purpose I/O banks (two banks per left, top, and right sides). The LatticeECP4-190 and LatticeECP4-250 have eight banks (four banks on top and two banks on each of the left and right sides). Each of the I/O banks has its own VCCIO power supply. Every LatticeECP4 device has a TAP controller interface bank in the lower left corner of the device. The bank has four signal pins (TCK, TMS, TDI, and TDO) and is powered by VCCJ. Bank 6 is the bank with shared I/O for configuration. Bank 6 is located in the lower left side of the device. VCCIO5 is also used to power dedicated configuration pins (PROGRAMN, INITN, DONE, CCLK, CFG[2:0]).

Each of the LatticeECP4 devices provides eight Phase Locked Loops (PLLs) and four output clocks. Two PLL blocks are located in each of the upper left, upper right, lower left, and lower right sides of the LatticeECP4 device.

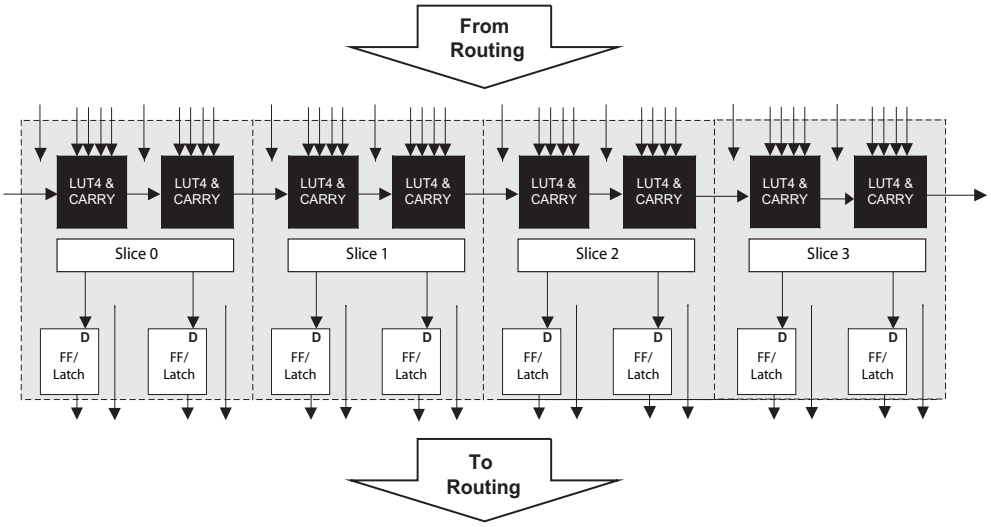
The configuration block that supports features such as configuration bitstream decryption, transparent updates and multi-boot support is located at the lower left side of the device.

PFU Blocks

The core of the LatticeECP4 device consists of PFU blocks which can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Each PFU block consists of four interconnected slices numbered 0 to 3, as shown in Figure 2-2. Each slice contains two LUTs and two registers. All the interconnections to and from PFU blocks are from routing. There are 49 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slices

Slices 0 to 3 contain two LUT4s feeding two registers. Slices 0 and 1 can be configured as distributed memory with the controls, data, and address of distributed memory coming from Slice 2. Table 2-2 shows the capability of the slices in the PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), programmable flip-flop/latch mode, clk/ce/lsr polarity control, clock boosting, clock select, chip-select, and wider RAM/ROM functions.

Table 2-2. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	Two LUT4s and two registers	Logic, Ripple, RAM, ROM
Slice 1	Two LUT4s and two registers	Logic, Ripple, RAM, ROM
Slice 2[1]	Two LUT4s and two registers	Logic, Ripple, RAM, ROM
Slice 3	Two LUT4s and two registers	Logic, Ripple, ROM

1. Slice 2 provides distributed RAM controls only; it cannot be configured as distributed memory.

Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 13 inputs from routing, two inputs (FXA and FXB) from hard-wired connections of the PFU OFX, and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Table 2-3 lists the signals associated with Slices 0 to 3.

Figure 2-3. Slice Diagram

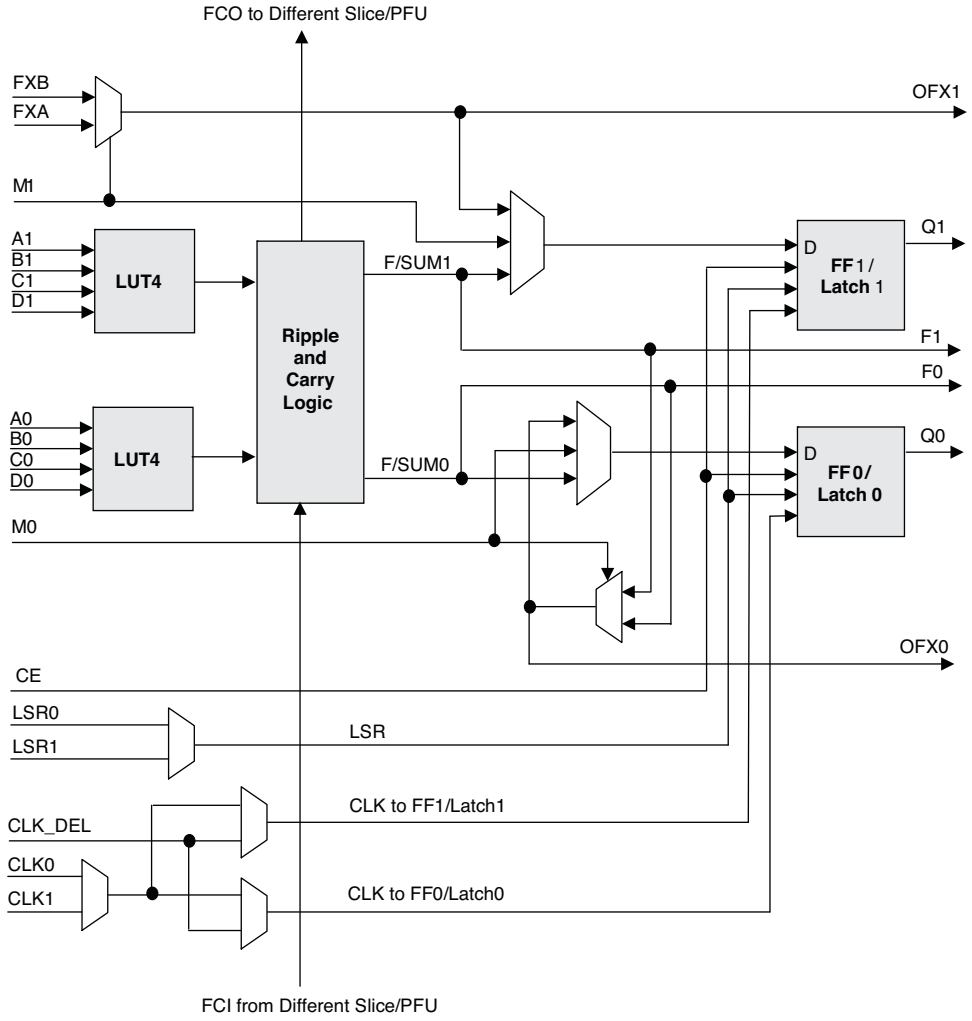


Table 2-3. Slice Signal Descriptions

Signal	Function	Type	Description
A0, B0, C0, D0	Input	Data signal	LUT4 inputs coming from routing
A1, B1, C1, D1	Input	Data signal	LUT4 inputs coming from routing
M0, M1	Input	Multi-purpose	Multi-purpose inputs and OFX mux select, from routing
CE	Input	Control signal	Clock Enable, from routing
CLK0, CLK1	Input	Control signal	System clocks, from routing
CLK_DEL	Input	Control signal	Delayed CLK0 or CLK1 from clock boosting circuit
LSR0, LSR1	Input	Control signal	Local set/reset, from routing
FCI	Input	Inter-PFU signal	Fast carry in, from previous slice or PFU
FXA, FXB	Input	Inter-slice signal	Intermediate signal to generate LUT6, LUT7, and LUT8
F0, F1	Output	Data signal	LUT4 output register bypass signals, to routing
Q0, Q1	Output	Data signal	Registered outputs, to routing
OFX0	Output	Data signal	Output of LUT5 MUX, to routing
OFX1	Output	Data signal	Output of LUT6, LUT7, or LUT8[1] MUX, to routing
FCO	Output	Inter-PFU signal	Fast carry out, to next slice or PFU

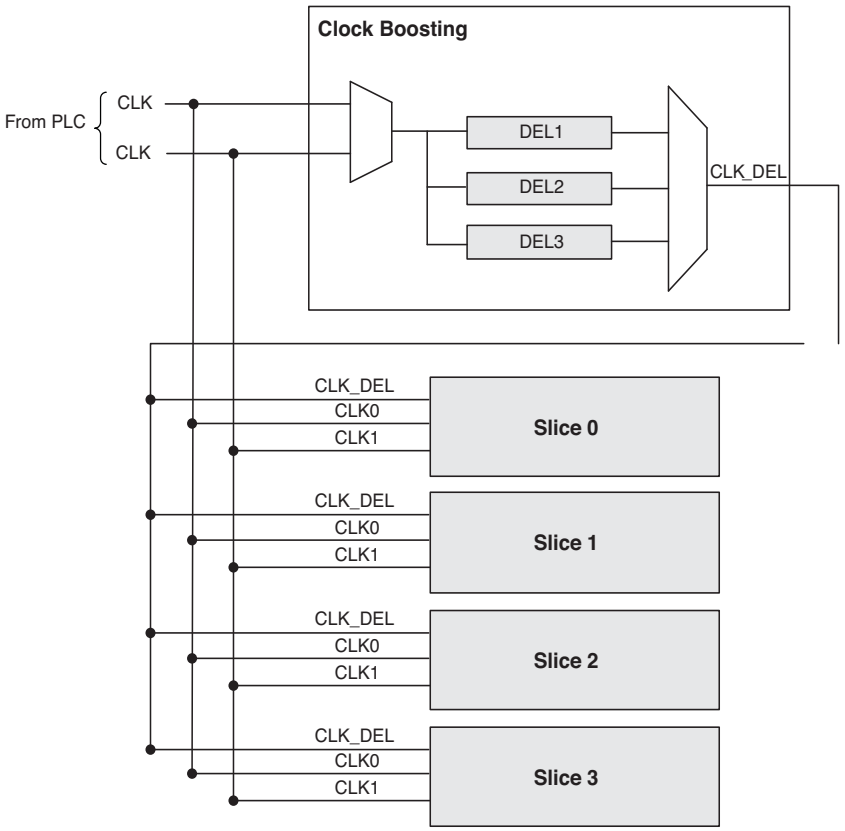
1. LUT6 in slice0 and slice2, LUT7 in slice 1, LUT8 in slice 3 and requires two PFUs

Clock Boosting in PFUs

LatticeECP4 registers feature clock boosting. This is the feature in which programmable delay is given to the clock path before it goes to the programmable registers or latches in the PFU. Any one of the two PFU clocks, which is CLK0 or CLK1 from the routing, can be chosen as a clock source for clock boosting. There are three delay settings in the clock boosting circuit (DEL1, DEL2, and DEL3). The user can choose a delay setting and generate a PFU. This is illustrated in Figure 2-4. The user can choose to apply CLK_DEL as the clock source to the slice registers on a per-register basis, as illustrated in Figure 2-3.

By introducing programmable delay stages to the clocks, longer data paths can be given more time to meet the system constraints without impacting the period of the distributed clock signals and therefore improving overall system performance.

Figure 2-4. Clock Boosting Feature in PFU



Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. *Note: LUT8 requires more than four slices.*

Ripple Mode
Ripple mode supports the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  – A greater-than-or-equal-to B
  – A not-equal-to B
  – A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode
In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address/data and control signals. The write address, write data, write clock, and write enable to the distributed RAM are brought in from A0/B0/C0/D0, A1/B1/C1/D1, CLK, and LSR of Slice 2, respectively. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one slice as the read port and the other companion slice as the write port.

LatticeECP4 devices support distributed memory initialization.

The Lattice Diamond design tool supports the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-4 shows the number of slices required to implement different distributed RAM primitives.

Table 2-4. Number of Slices Required to Implement Distributed RAM

	SPR 16x4	PDPR 16x4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode
ROM mode uses the LUT logic; therefore, Slices 0 through 3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeECP4 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: X1 (spans two PFUs), X2 (spans three PFUs) and X6 (spans seven PFUs). The X1, X2, and X6 connections provide fast and efficient connections in the horizontal and vertical directions; X1 also spans diagonally.

The Lattice Diamond design tool takes the output of the synthesis tool and places and routes the design. Typically, the place and route tool is completely automatic. An interactive routing editor is available to optimize the design.

Clock/Control Distribution Network

Primary Clocks

The LatticeECP4 provides low-skew, high fanout clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network. The primary clock network can be run at a maximum of 500 MHz.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 20 clocks that can be distributed to the fabric in the quadrant. Initially, the Lattice Diamond software automatically routes each clock to all 4 quadrants up to a maximum of 20 clocks. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific quadrants.

The LatticeECP4 provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network. Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA Fabric Entries
- SERDES/PCS clocks
- DQS clocks

These sources are routed to one of four clock switches called a Mid Mux. The outputs of the Mid MUX are routed to the center of the FPGA where another clock switch, called the Center MUX, is used to route the primary clock sources to primary clock distribution to the LatticeECP4 fabric. Since there is a maximum of 64 unique clock input sources to the clocking quadrants, there are potentially 64 unique clock domains that can be used in the LatticeECP4.

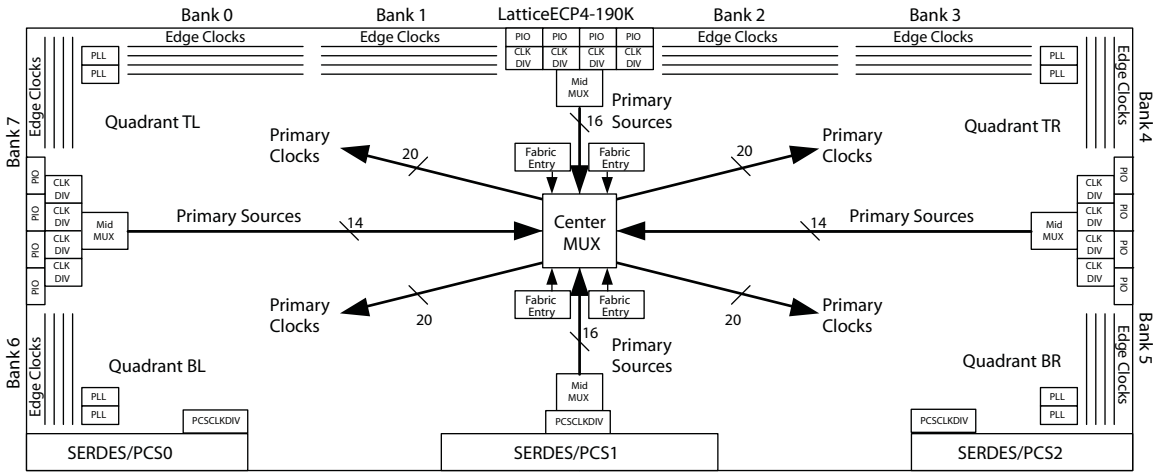
Edge Clocks

The LatticeECP4 also has dedicated high speed, low skew clock resources called Edge Clocks which are used to clock the I/O logic for DDR applications. There are four edge clocks per bank (left, right, and top sides). The maximum frequency these resources can run is 667 MHz. The sources of edge clocks are:

- Dedicated clock pins
- PLL outputs
- ECLK bridge
- Internal nodes

Figure 2-5 shows the clocks for the LatticeECP4-190 device. For detailed information about clocking, see TN1235, LatticeECP4 sysCLOCK PLL Design and Usage Guide.

Figure 2-5. LatticeECP4-190 Clocks



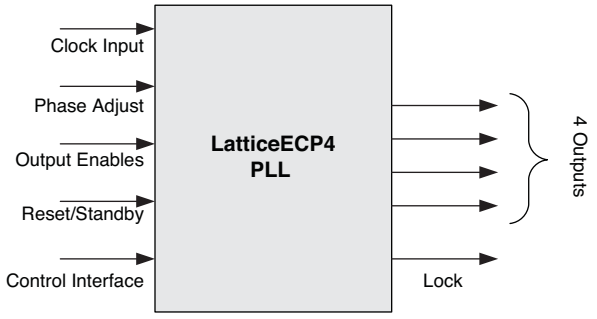
sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies, clock phase adjustment, clock duty cycle adjustment, and clock injection delay removal. All devices in the LatticeECP4 family support eight full-featured General Purpose PLLs (GPLL); two PLLs are in each corner of the device.

Table 2-5. PLLs, Clocks, Clock Dividers

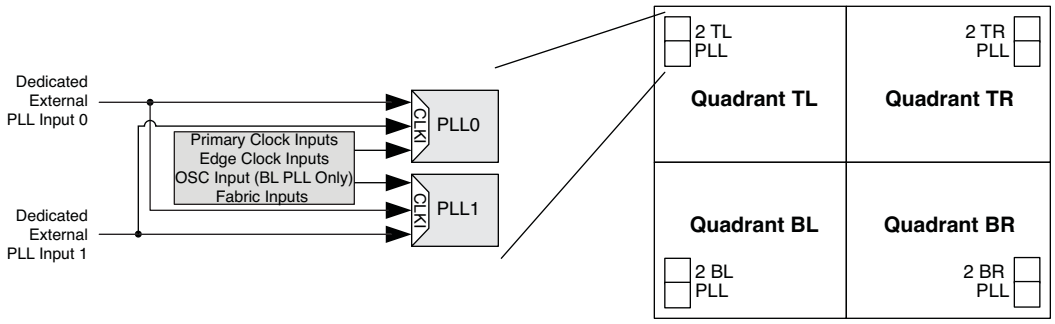
Description	ECP4-30	ECP4-50	ECP4-95	ECP4-130	ECP4-190	ECP4-250
Number of General Purpose PLLs	8	8	8	8	8	8
Number of Edge clocks for high speed applications	24	24	24	24	32	32
Number of Edge clock dividers for DDR applications	12	12	12	12	12	12
Number of PCS Clock dividers for domain crossing applications	1	1	2	2	3	4

Figure 2-6. sysCLOCK PLL Functional Block Diagram



The PLL output clocks (CLKOP, CLKOS, CLKOS2, and CLKOS3) can go to the primary clock network. Only CLKOP and CLKOS outputs can go to the edge clock network. Each PLL has dedicated input pins which are routed directly to the PLL input. Since there are two PLLs in a corner, there are two dedicated PLL inputs in each corner. Both dedicated inputs can route to both PLLs in a corner.

Figure 2-7. Dedicated PLL Inputs

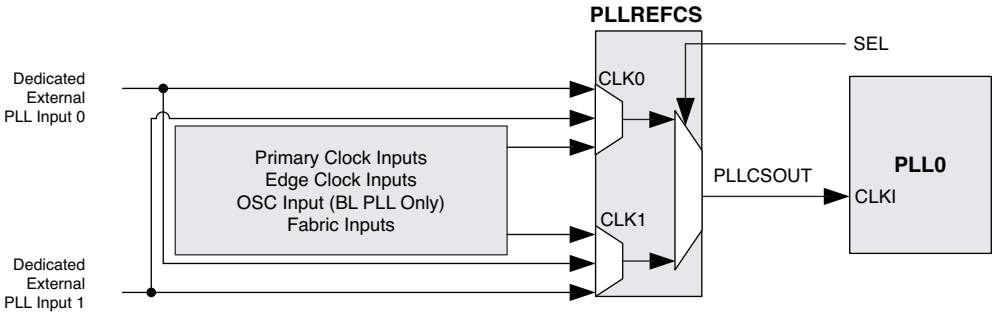


The LatticeECP4 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis which allows the user to generate an output clock which is a non-integer multiple of the input frequency. The PLL also has internal connections to cascade its output dividers, allowing for lower output frequencies.

The PLL output clocks can be individually dynamically stopped and re-started in order to save power. There is also a standby mode which can put an individual PLL into a low-power state.

A non-glitchless 2-to-1 input multiplexor is provided to dynamically select between two different reference clock sources. This feature is implemented by using the PLLREFCS primitive. This mux can also be used with the PLL in bypass mode to provide the ability to switch input clock sources without having to use clock synthesis. Both dedicated PLL inputs in each corner of the LatticeECP4 can route to both PLLREFCS components in a corner.

Figure 2-8. PLLREFCS Component



The PLL has a run-time programmable control interface to allow for dynamic changing of the PLL parameters. The SMI port connected to the Lattice ECP4 Embedded Function Block (EFB) is used to adjust this interface. An EFB should be instantiated to interface to the PLL register block. The PLL also has ports to allow for dynamically adjusting the phase without using the control interface.

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which will advance or delay the output clock with reference to the CLKOP output clock. The phase shift can be either programmed during configuration or can be adjusted dynamically.

For more information on the sysCLOCK PLLs, see TN1235, LatticeECP4 sysCLOCK PLL Design and Usage Guide.

sysMEM Embedded Block RAM Memory

LatticeECP4 devices consist of rows of embedded memory arranged in blocks called Embedded Block RAM (EBRs). Each sysMEM EBR includes memory input registers for synchronizing write operations and bypassable output registers for pipelining and high-performance designs. The sysMEM EBRs consists of 18,432 bits of RAM and includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and FIFO buffers. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks pro-

vide byte-enable support for configurations with18-bit and 36-bit data widths. Port A and Port B have independent and separate clocks. There are numerous configurations and features for each block RAM, and each sysMEM EBR supports the following features:

- 18Kbits RAM
- up to 400 MHz performance
- True dual-port memory
- Pseudo dual-port memory (one port read, and one port write)
- Parity bits
- Built-in FIFO control logic with optional First-Word-Fall-Through (FWFT) operation
- ROM
- Mixed clock mode
- Data width range from x1 up to x18 (and x36 for pseudo-dual port and single port)
- Mixed width mode
- Byte enables
- Asynchronous reset with optional synchronous release

Each EBR has the following:

- Registers
- Memory core
- Output registers (with separate enable)

For more information on the sysMEM Embedded Block Memory, see TN1234, LatticeECP4 On-Chip Memory Usage Guide.

sysMEM Memory Modes

Each sysMEM EBR can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
Dual-Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual-Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Single-Port Mode
In single-port mode, the EBR can either read from or write to a clock. During the write operation, data written to the RAM flows through to the RAM outputs. Both normal and write-through modes are supported.

True Dual-Port Mode
In true dual-port mode, 512x36 bit with parity configuration of the EBR is not available. True dual-port mode supports simultaneous read and write. Dual-port RAM has outputs on two ports; therefore the maximum width of the true dual-port RAM is half the total number of output drivers. The EBR supports true dual-port mode with any of the following combinations of two port operations:

- Two read operations
- Two write operations
- One read and one write operation at two different clock frequencies

Pseudo Dual-Port Mode
Pseudo dual-port mode supports simultaneous read and write. However, one port is used as a read port and the other port is used as a write port. None of the ports can operate as both read and write.

FIFO Mode
FIFO mode supports a special type of pseudo-dual-port operation where the addresses and flags are internally generated with FIFO logic. They are typically used for transferring wide packet data from one clock domain to another. The addresses are generated from current read pointers and write pointers for the next memory access. Port A becomes the write port. All write port controls use the Port A inputs. All read port controls use the Port B inputs. Several flags are generated for FIFO control. These flags are only to be used as data signals and should never be used to generate or interrupt clocks.

Shift Register Mode

The sysMEM EBR does not provide shift register mode but can be operated as a shift register with some additional logic implemented in the PLCs.

ROM Emulation

The sysMEM EBR can be configured as ROM by using a memory initialization file through software.

sysMEM EBR Memory Writes

The EBR memory supports two forms of memory write behavior for single-port or dual-port operation:

- **Write-through** - A copy of the input data appears at the output of the same port.
- **Read-Before-Write** - When new data is being written, the old contents of the address appears at the output.

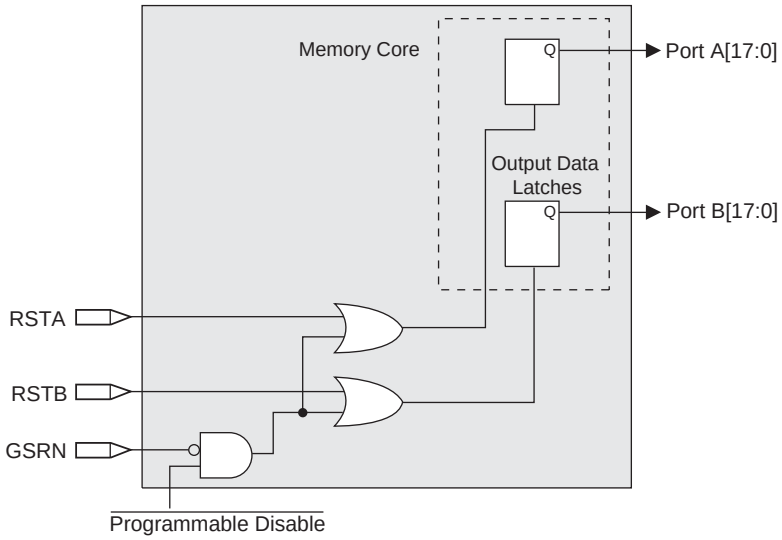
sysMEM EBR Asynchronous Reset

The EBR outputs can be programmed to do either a synchronous or an asynchronous reset. A single configuration bit controls the programming; therefore, both ports must have the same setting. Asynchronous reset implies the reset is applied without a clock and should commence from the asserted edge of the reset signal. Synchronous reset implies the reset signal should satisfy setup and hold time requirements to a clock edge and the reset operation should commence from the clock edge.

Memory Core Reset

The memory core contains data output latches for ports A and B as shown in Figure 2-9. These are simple latches that can be reset synchronously or asynchronously.

Figure 2-9. Memory Core Reset



LatticeECP4 sysDSP Slice Architecture Features

The LatticeECP4 family provides an enhanced sysDSP architecture, making it ideally suited for low-cost, advanced high-performance Digital Signal Processing (DSP) applications and allows for improved flexibility, and resource utilization. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders.

The LatticeECP4 sysDSP slice supports many functions that include:

- Multiply (one 18x36, two 18x18 or four 9x9 multiplies per slice)
- Multiply (36x36 by cascading across two sysDSP slices)

- Multiply Accumulate (up to 18x36 multipliers feeding an accumulator that can have up to 54-bit resolution)
- Two multiplies feeding one accumulate per cycle for increased processing with lower latency (two 18x18 multiplies feed into an accumulator that can accumulate up to 52 bits)
- Pre-adder (two 18-bit per slice) supports:
  – 1D symmetry for wireless applications
  – 2D symmetry for video applications
  – Long tap FIR filter support across multiple DSP rows
  – Full 54-bit accumulator support
  – Operating frequency of 500 MHz based on double data rate conversion
- Flexible saturation and rounding options to satisfy a diverse set of application situations
- Flexible cascading across sysDSP slices
  – Minimizes fabric use for common DSP and ALU functions
  – Enables implementation of FIR Filter or similar structures using dedicated sysDSP slice resources only
  – Provides matching pipeline registers
  – Can be configured to continue cascading from one row of sysDSP slices to another for longer cascade chains
- Flexible and powerful Arithmetic Logic Unit (ALU) supports:
  – Dynamically selectable ALU OPCODE
  – Ternary arithmetic (addition/subtraction of three inputs)
  – Bit-wise two-input logic operations (AND, OR, NAND, NOR, XOR and XNOR)
  – Eight flexible and programmable ALU flags that can be used for multiple pattern detection scenarios, such as overflow, underflow and convergent rounding, etc.
  – Flexible cascading across slices to get larger functions
- RTL-synthesis-friendly synchronous reset on all registers, while still supporting asynchronous reset for legacy users
- Dynamic MUX selection to allow Time Division Multiplexing (TDM) of resources for applications that require processor-like flexibility that enables different functions for each clock cycle

sysDSP Slice Approach Compared to General DSP

Conventional general-purpose DSP chips typically contain one to four Multiply and Accumulate (MAC) units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP4, on the other hand, has many sysDSP slices that support different data widths. This allows designers to use highly-parallel implementations of DSP functions. Designers can optimize DSP performance versus area by choosing appropriate levels of parallelism.

The sysDSP unique Double-Data-Rate mode provides twice (2x) the performance improvement by doubling the number of multipliers in the device. The integrated Pre-Adders provide further 2x resource improvement be leveraging the coefficient symmetry for FIR filters. For additional details, refer to TN1237, LatticeECP4 sysDSP Usage Guide.

Figure 2-10. Comparison of the General DSP and LatticeECP4 Approach

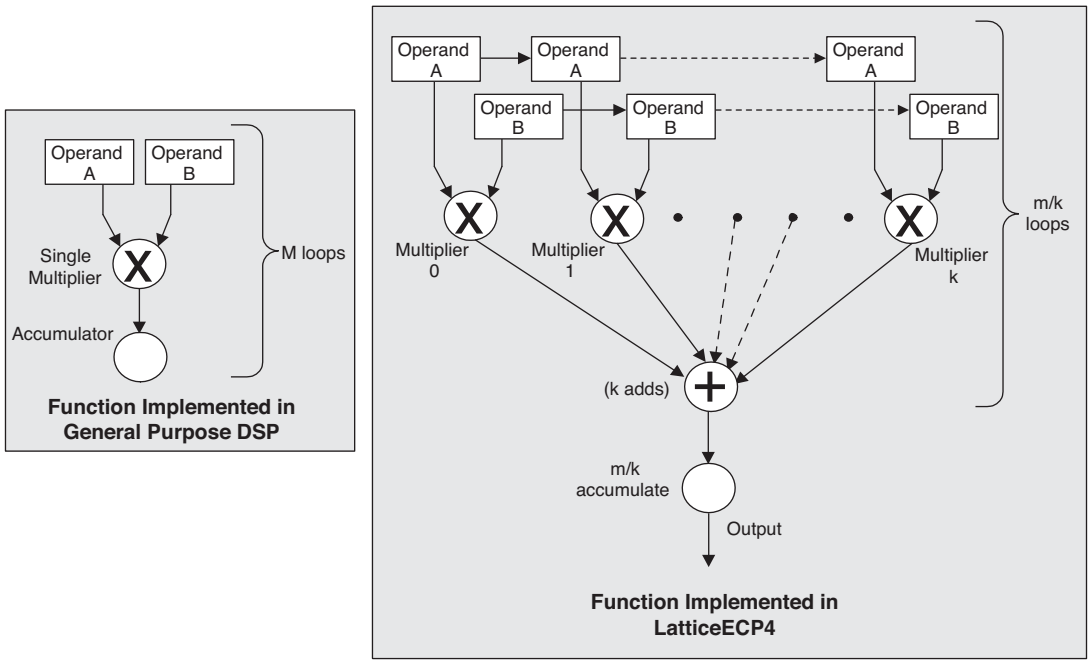
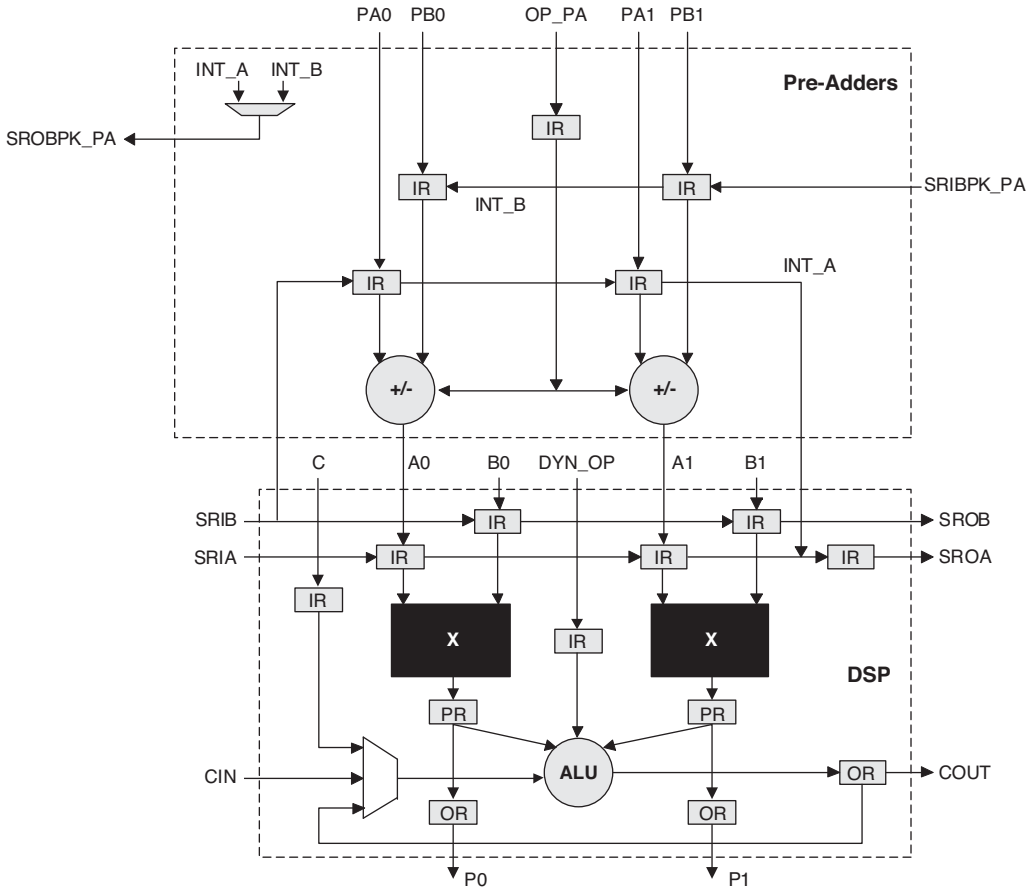


Figure 2-11. Detailed sysDSP Slice Diagram



The LatticeECP4 sysDSP slice port list is shown in Table 2-7.

Table 2-7. LatticeECP4 sysDSP Slice Port List

Port I/O Description	I/O	Description
A0[17:0]	I	Multiplier parallel Input A0
B0[17:0]	I	Multiplier parallel Input B0
A1[17:0]	I	Multiplier parallel Input A1
B1[17:0]	I	Multiplier parallel Input B1
C[53:0]	I	ALU Input C
PA0[17:0]	I	Pre-adder Parallel Input A0
PB0[17:0]	I	Pre-adder Parallel Input B0
PA1[17:0]	I	Pre-adder Parallel Input A1
PB1[17:0]	I	Pre-adder Parallel Input B1
CE[3:0]	I	Clock Enable Inputs
CLK[3:0]	I	Clock Inputs
RST[3:0]	I	Reset Inputs
SRIA[17:0]	I	Multiplier shift Input A
SRIB[17:0]	I	Multiplier shift Input B
SROA[17:0]	O	Shift Output A
SROB[17:0]	O	Shift Output B
SRIBKA_PA	I	Pre-Adder Feedback Input
SROBKA_PA	O	Pre-Adder Feedback Output
OP_PA[1:0]	I	Opcode for Pre-Adder
DYN_OP[11:0]	I	Opcode for ALU
P0[35:0]	O	Product Output P0
P1[35:0]	O	Product Output P1

LatticeECP4 I/O Banking Scheme

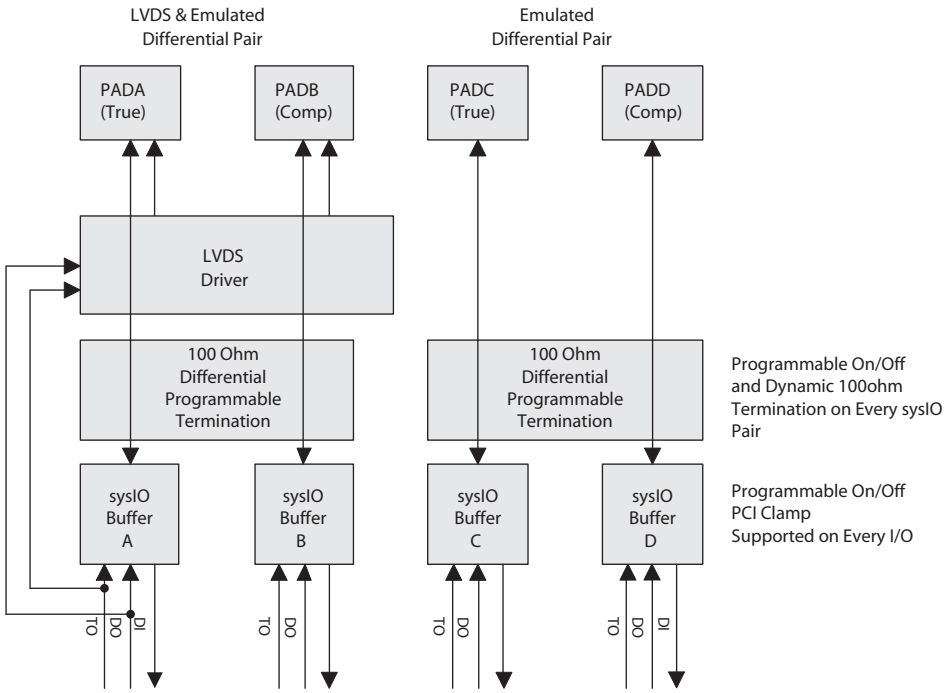
On the LatticeECP4-30, LatticeECP4-50, LatticeECP4-95, and LatticeECP4-130 devices, there are six banks: two banks per left, top, and right sides. On the LatticeECP4-190 and LatticeECP4-250 devices, there are eight banks: four on the top of the device (Banks 0, 1, 2, and 3), two on the left side of the device (Banks 6 and 7), and two on the right side of the device (Banks 4 and 5). Each bank contains a Programmable I/O Cell (PIC). Each PIC contains two General purpose Programmable I/Os (GPIO), PIOA and PIOB. Each bank has a VCCIO power supply. The individual PIOs are connected to their respective sysIO buffers and pads.

Every LatticeECP4 device has a TAP controller interface bank in the lower left corner of the device. This bank has four pins (TCK, TMS, TDI, and TDO) and is powered by VCCJ. Bank 6 is located on the lower left side of the device, next to the TAP bank and contains shared I/O for device configuration. The VCCIO in Bank 6 also powers the dedicated configuration pins (PROGRAMN, INITN, DONE, CCLK, CFG[2:0]).

sysIO Interface

The LatticeECP4 sysIO interface consists of four sysIO blocks. The LatticeECP4 minimum building bock is a quad of four GPIO and is the same on all three sides of the device, left, top, and right edges. Each quad is composed of two pairs of pads. The GPIOs are designed to handle high-speed outputs on every pad with differential LVDS outputs on half of the I/O pad pairs as shown in Figure 2-12. The true LVDS outputs are only available on the A/B pair of pads. Emulated differential outputs are available on every output pair. Half of the I/O pads are true differential outputs. The true differential outputs are always located on the A/B pins. The C/D pins do not support true differential outputs. All A/B and C/D pin pairs support emulated differential outputs.

Figure 2-12. sysIO Interface



The LatticeECP4 sysIO buffer supports both single-ended and differential standards. Table 2-8 lists the supported single-ended standards.Table 2-9 lists the supported true differential I/O standards.

Table 2-8. Single-Ended I/O Standards Supported by LatticeECP4

Standard	Input	Output	Bidi
PCI33	Yes	Yes	Yes
LVTTL/LVCMOS33	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes
SSTL25_I	Yes	Yes	Yes
SSTL25_II	Yes	Yes	Yes
SSTL18_I	Yes	Yes	Yes
SSTL18_II	Yes	Yes	Yes
SSTL15_I	Yes	Yes	Yes
SSTL15_II	Yes	Yes	Yes
HSTL18_I	Yes	Yes	Yes
HSTL18_II	Yes	Yes	Yes
HSTL18_III	Yes	No	No
HSTL18_IV	Yes	No	No
HSTL15_I	Yes	Yes	Yes
HSTL15_II	Yes	Yes	Yes
HSTL15_III	Yes	No	No
HSTL15_IV	Yes	No	No
HSUL12	Yes	Yes	Yes

Table 2-9. Differential I/O Standards Supported by LatticeECP4

Standard	Input	Output	Bi-directional
LVDS	Yes	AB pairs only	No
LVDS25E (emulated)	No	Yes	No
RSDS	Yes	AB pairs only	No
RSDS25E (emulated)	No	Yes	No
TRLVDS	Yes	AB pairs only	No
PPLVDS	Yes	AB pairs only	No
MINILVDS	Yes	AB pairs only	No
MINLVDS25E	No	Yes	Yes
SLVS	Yes	AB pairs only	No
SLVS15E (emulated)	No	Yes	No
SUBLVDS	Yes	AB pairs only	No
MLVDS25E (emulated)	No	Yes	Yes
MLVDS25	Yes	no	No
BLVDS25E (emulated)	No	Yes	Yes
BLVDS25	Yes	No	No
LVPECL33E (emulated)	No	Yes	No
LVPELCL33	Yes	No	No
MIPI	Yes	No	No

For more information on the Programmable I/O and sysIO buffers, see TN1232, LatticeECP4 sysIO Usage Guide.

High-Speed I/O Features

Application	Solutions
DDR2	533 Mbps can be achieved using the 2:1 IDDR/ODDR gearing logic with core speed at 267 MHz. 800 Mbps can be achieved using 4:1 IDDR/ODDR gearing with core speed at 200 MHz.
DDR3	1066 Mbps can be done using 4:1 IDDR/ODDR gearing logic with core speed at 267 MHz. 1066 Mbps can be achieved using 8:1 IDDR/ODDR gearing with core speed at 133 MHz.
QDR-II/II+	500 Mbps can be done using 2:1 IDDR/ODDR gearing logic with core speed at 250 MHz. 900 Mbps can be achieved using 4:1 IDDR/ODDR gearing with core speed at 225MHz.
LPDDR2	300 Mbps can be achieved using 2:1 IDDR/ODDR gearing core speed at 150 MHz.
SPI4.2	1000 Mbps can be achieved using the 4:1 IDDR/ODDR gearing logic with core speed at 250 MHz.
ADC/DAC	1200 Mbps DAC can be implemented using 8:1 gearing logic. 800 Mbps ADC can be implemented using 4:1 gearing logic.
SGMII	Can be implemented using 10:1 IDDR/ODDR gearing and the new CRU block in the I/O logic block to recover the clock.
Video 7:1 LVDS and 10:1	784 Mbps (112 MHz) can be implemented using 7:1 or 10:1 IDDR/ODDR gearing logic.

Hot Socketing

All LatticeECP4 devices have been carefully designed to ensure predictable behavior during power-up and power-down. The GPIOs located on all three sides of the devices (top, left, and right) are fully hot socketable. The LatticeECP4 sysIO buffer is disabled during the initial power-on state when the Hot Socket Not signal (HS_N) is active low. During hot socket, the output driver is disabled and the input receivers are disconnected from the pad. The receiver inputs are held low and not floating. No weak pull-up or weak pull-down or bus input keeper is connected to the pad and the clamp is off. All DC current sources are disabled in differential inputs, outputs, and reference circuits.

On-chip Oscillator

The LatticeECP4 has an on-chip oscillator which is used to generate clocks for users and the configuration block. The oscillator and clocks run continuously and are available to user logic after configuration is complete. Table 2-10 lists the MCLK frequencies during configuration.

Table 2-10. Nominal MCLK Frequencies During Configuration

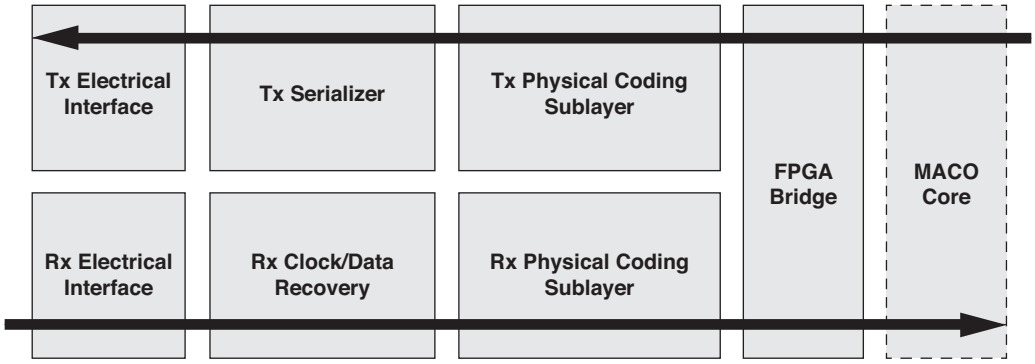
MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.4	15.5	44.3
3.2	16.3	51.7
4.1	19.4	62.0
4.8	20.7	77.5
6.5	25.8	103.3
8.2	31.0	155.0
9.7	34.4	
12.9	38.8	

SERDES and PCS (Physical Coding Sublayer)

LatticeECP4 devices have between four and sixteen SERDES channels at the bottom side of the device. Each quad contains four dedicated SERDES channels, providing up to 16 channels, for high-speed, full-duplex serial data transfer. Each quad can be configured as four single lanes, two pairs of two lanes, one pair of two lanes, and two single lanes, or as a group of four lanes, where protocols and rates are selectable per channel. On the low-speed (parallel interface) side, each SERDES quad interfaces directly to a digital PCS, which in turn interfaces to the general FPGA fabric. Digital functions such as word alignment, encoding/decoding, multi-channel lane alignment and clock tolerance compensation are handled by the PCS logic. Each SERDES channel has a RX and TX block. This is also true for the PCS block. There are two TX PLLs per quad in the LatticeECP4.

Figure 2-13 shows a high-level diagram of the SERDES/PCS block including the optional MACO core.

Figure 2-13. Channel Block Diagram



The LatticeECP4 SERDES/PCS supports a range of popular protocols, as shown in Table 2-11. A list of protocols that are supported but with limitations are show in Table 2-11. For more information, refer to TN1231, LatticeECP4 SERDES/PCS Usage Guide.

Table 2-11. SERDES-Supported Standards and Performance

Standard	Data Rate (Mbps)	Reference Clock (MHz)	SERDES/PCS Interface Clock (MHz)	Channels/Links	Encoding Style
PCI Express (PIPE)	2500 5000	100	250 (8-bit) 500 (61-bit)	x1, x4	8b10b
XAUI HiGig HiGig+ HiGig2	3125 3750 3750 4062.5	156.25 187.50 187.50 203.125	156.25 (16-bit) 187.50 (16-bit) 187.50 (16-bit) 203.125 (16-bit)	x4	8b10b
GMII	1250	125	125	x1	8b10b
SGMII	1250 2500	125	125 250	x1	8b10b
QSGMII	5000	125	125x4	x1	8b10b
Serial RapidIO T1 Serial RapidIO T2 Serial RapidIO T3 Serial RapidIO 2.1	1250 2500 3125 5000 6250	125 — — — —	125.0 (8-bit) 125.0 (16-bit) 156.25 (16-bit) 125.0 (32-bit) 156.25 (32-bit)	x1, x2, x4	8b10b
CPRI-1 CPRI-2 CPRI-3 CPRI-4 CPRI-5 CPRI-6	614.4 1228.8 2457.6 3072.0 4915.2 6144.0	122.88 — — — — —	61.44 (8-bit) 122.88 (8-bit) 122.88 (16-bit) 153.60 (16-bit) 122.88 (32.bit) 153.60 (32.bit)	x1	8b10b
SONET (STS-12) (STS-48) (STS-3)	 622 2488 155.2	 77.76 155.52 77.76	 77.76 (8-bit) 155.52 (16-bit) 19.44 (8-bit)	x1, x4	SONET-scrambled
G8B10B	155 to 6375				8b10b
10BSER	155 to 6375				—
8BSER	155 to 6375				—
SD-SDI (SERDES/PCS bypass)	143 177	14.3 17.7	143 177	x1	SMPTE-scrambled

Table 2-11. SERDES-Supported Standards and Performance (Continued)

Standard	Data Rate (Mbps)	Reference Clock (MHz)	SERDES/PCS Interface Clock (MHz)	Channels/Links	Encoding Style
SD-SDI	270 360 540	54 72	27 36 54		SMPTE-scrambled
HDI-SDI	1483.5 1485	74.175 74.25	148.35 148.5	x1	SMPTE-scrambled
3G-SDI	2967 2970	74.175 74.25	296.7 297.0	x1	SMPTE-scrambled
RXAUI	3125 6250	156.25	312.5 625.0	x2, x3, x4, x6	8b10b

Other SERDES electrical interfaces and protocols such as OIF CEI-6G-LR, OIF CEI-6GSR, Interlaken, OBSAI-1, OBSAI-2, OBSAI-3, SATA Gen1, and SATA Gen2 are supported but with limitations. For more information on using these interfaces and protocols, refer to TN1231 LatticeECP4 SERDES/PCS Usage Guide.

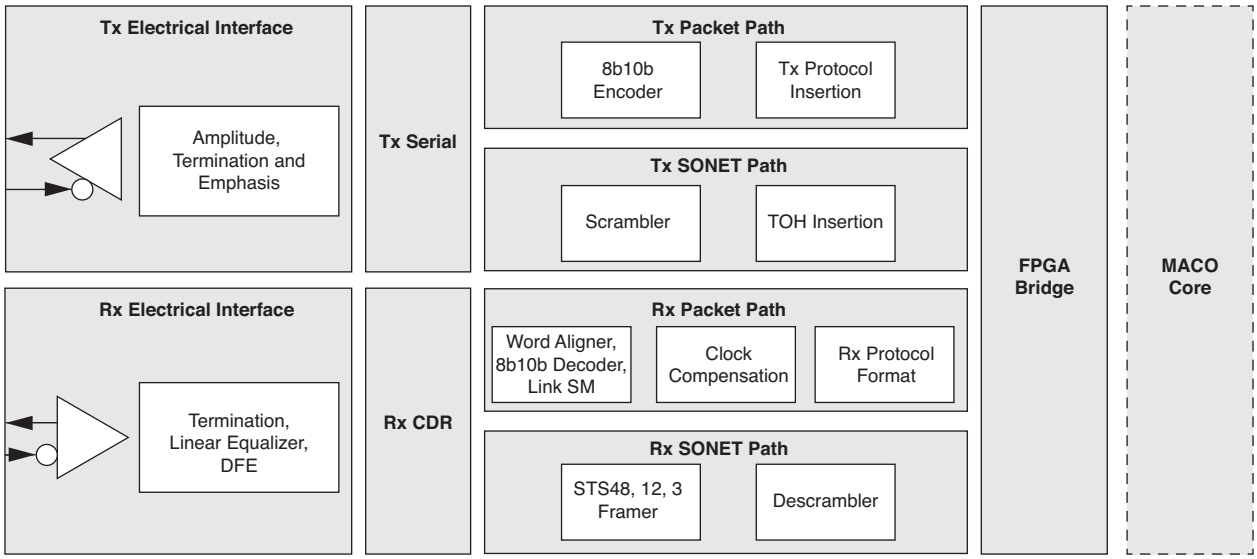
The PCS and SERDES are arranged in four-channel quad units. The PCS connects to the SERDES, the fabric and optional MACO cores, and neighboring PCS quads. The number of quads per LatticeECP4 device are shown in Table 2-12.

Table 2-12. Available SERDES Quads per LatticeECP4 Device

Package	ECP4-30	ECP4-50	ECP4-95	ECP4-130	ECP4-190	ECP4-250
484-ball fpBGA (23x23 mm)	1	1	—	—	—	—
648-ball fpBGA (27x27 mm)	1	1	1	1	—	—
868-ball fpBGA (31x31 mm)	—	—	2	2	—	—
676-ball fcBGA (27x27 mm)	1	1	1	1	1	—
900-ball fcBGA (31x31 mm)	—	—	2	2	2	2
1152-ball fcBGA (35x35 mm)	—	—	—	—	3	4

A functional diagram for the SERDES/PCS is shown in Figure 2-14.

Figure 2-14. PCS Functional Diagram



IEEE 11.49 - Compliant Boundary Scan Testability

All LatticeECP4 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS.

Device Configuration

The LatticeECP4 FPGAs are configured by loading customer-specific design data (a bitstream) into an internal SRAM-type configuration memory. The application-specific data determines the circuit functionality of the device. The FPGAs can load themselves from external, non-volatile memory devices or they can be configured externally from a CPU, microcontroller, or PCB board tester.

All LatticeECP4 devices contain a dedicated JTAG test access port (TAP) that supports bit-wide configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. A sysCONFIG port is shared with dual-purpose GPIO pins that supports serial configuration through I^2C and SPI as well as parallel programming interfaces to CPU type and processor busses.

There are various ways to configure a LatticeECP4 device including:

1. JTAG TAP Interface
2. Standard Serial Peripheral Interface (Master SPI mode) – interface to boot x1, x2, x4, x8, and x16 Flash SPI memory
3. System microprocessor driven serial slave SPI port (S-SPI mode)
4. Standard I^2C Interface of system microprocessor
5. Slave x1, x8, x16-bit Interface to CPU or microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected JTAG or sysCONFIG port. JTAG is always available as a programming port. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Once a sysCONFIG configuration port is selected, it will remain active throughout that configuration cycle. Three pins, CFG[2:0], determine the configuration port for loading configuration for either slave or master modes.

In master mode, the FPGA can drive the configuration clock from its internally generated clock to external devices and read the configuration bitstreams. For faster programming, the FPGA can use an externally driven configuration clock source. Slave modes up to 16 bits wide are directly supported by the FPGA that are especially useful for processor-driven loading of bitstreams.

Configuration or FPGA programming is generally accomplished by one of two general configuration interfaces. Serial data, which minimizes the FPGA device pin requirements or parallel data, such as 8-bit or 16-bit data, that are utilized for higher performance or access to industry-standard interfaces, ideal for external data sources like microprocessors.

The number of configuration bits required by the LatticeECP4 devices ranges between 10.7Mb and 54.5Mb, depending on device size and the user's design implementation. The configuration data includes information for pre-loading embedded memory and internal device blocks. It also stores information required by the device to properly control optional on-die features. The volatile configuration storage must be re-loaded whenever the FPGA is powered up or on-demand by the user or system application using several available methods. Re-loading can be done an unlimited number of times.

Lattice design software uses proprietary compression technology to compress bitstreams for use in the LatticeECP4 devices. Use of this technology allows Lattice to provide a lower cost solution by reducing the amount of off-chip memory required to store the design bitstream. Devices also run CRC checks on the incoming bitstreams to ensure that the device was correctly configured with a valid bitstream.

The SPI interface programming (x1, x2, x4, x8 and x16 modes) interface directly to external SPI Flash devices. The LatticeECP4 supports configuring from a traditional, single bit-wide SPI Flash device or from one, two, and four Quad SPI Flash devices. One Dual/Quad I/O SPI Flash device can be connected to the FPGA, supplying two bits or four bits of data to the FPGA per clock. The FPGA internal configuration logic reads the bitstream out of the Flash and configures itself. The FPGA automatically detects the bus width on-the-fly, eliminating the need for any external controls or switches. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on or any time the device is reloaded.

The LatticeECP4 devices also provide flexible, reliable and secure configuration options, such as dual and multi-boot capability, bitstream security and encryption, daisy-chaining, and TransFR field upgrade features.

Dual-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update, the FPGA can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the device can revert back to the original backup “golden” configuration and try again. This all can be done without power cycling the system.

Multi-boot images provide the capability to have more than one primary bitstream stored in the external boot flash. The primary bitstreams can be loaded into the FPGA configuration memory on-demand. This can be by toggling the PROGRAMN device pin or issuing a REFRESH command from JTAG, I^2C, or SSPI.

The LatticeECP4 can be optionally programmed to prohibit read back of the bitstream as well as bitstream encryption. Encryption provides security which prevents another unauthorized encrypted bitstream from being used. This is because an encrypted bitstream will only work with an FPGA containing the same Encryption Key used to secure the bitstream. A one-time Programmable (OTP) fuse in the device is utilized to enable and store the Key Code that is programmed by the user. The Key code is needed to permit the proper deciphering of the encrypted bitstream allowing the secure design to be programmed correctly.

Encryption cannot be changed or disabled once the encryption key is first programmed. It only allows for the device to be re-programmed without the security provided by encryption. Users can re-program a device with a normal (un-encrypted) bitstream on devices that the encryption key has been programmed. Even if a device encryption key is inadvertently programmed, it does not render the device totally useless. The only means to re-program the device in a secure manner will be to use only the secured encryption key that was previously programmed.

Multiple FPGAs can be configured by a single bitstream, reducing the amount of memory devices needed to hold multiple configuration bitstreams. Both serial and parallel daisy chain capabilities are included in the LatticeECP4 devices. A serial daisy chain is a simple one-wire data connection formed by connecting a device DOUT pin to the next device DIN pin and connecting all CCLK pins in parallel. Parallel daisy chaining capabilities uses a common data bus and clock and utilizes the FPGA controlled chip select to methodically configure each FPGA in the chain.

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation on command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field-updated with a minimum of system disruption and downtime.

LatticeECP4 Family Overview Revision History

February 2012 **Advance Data Sheet DS1037A**

Date	Version	Section	Change Summary
November 2011	01.0	—	Initial release, LatticeECP4 Early Access Program.
February 2012	01.1	All	Updated document with new corporate logo.

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