intoPIX JPEG 2000 Encoder and Decoder IP-Cores respect and protect high value images. Handling simultaneously deep color, low and high data rates and extensive JPEG 2000 encoding know-how, intoPIX IP-Cores enable best-in-class picture quality. Amongst all the existing JPEG 2000 FPGA products, the intoPIX solution is currently the most widely adopted by the industry.

intoPIX IP-Cores achieve low and high frame rate and resolution with unprecedented performances. They are available and optimized for the most recent FPGA platforms.

intoPIX IP-Cores combine more power, more flexibility and more efficiency while ensuring lower consumption, lower temperature dissipation and lower bill of material.

Fully benefiting from a modular architecture and completed with a wide range of companion IP-Cores, the intoPIX solutions provide an easy, timely and cost-effective way to implement JPEG 2000 technology.
The HD Family
JPEG 2000 for Content Production

The JPEG 2000 HD Family allows you to retain image quality throughout your complete production process.

These IP-Cores have a decoded bitrate range from 250 Mbps up to 1 Gbps, and can process up to 120 progressive frames per second in HD resolution (1920 x 1080).

Moreover, the IP-Cores flexibility enables them to address all known broadcast standards in terms of resolution and frame rates.

• Single Chip
• Broadcast profile compliant (JPEG 2000 Part 1 Amd 3)
• Any resolution up to 1080p-120 fps
• Up to 1Gps Compressed Bitrates
• Progressive/interlaced
• 4:2:2/4:4:4
• Easy 3D stereoscopy
• Multi streams support
• CBR/VBR

APPLICATIONS
Camera on-board encoder
Field recorder
Post-production video server

Ultra Low Latency Option
JPEG 2000 for Live streams

The HD family also offers an Ultra Low Latency option that enables you to carry HD streams within the network with a point-to-point latency below 5 milliseconds while guaranteeing high image quality.

• 3/11 of a frame or field period
• Very low bitrate overhead
• Visually lossless quality

APPLICATIONS
Contribution transceiver
Live events transmitter
Wireless Transmission
Remote control & Monitoring

The Lossless Family
JPEG 2000 for pristine content

The intoPIX Lossless encoders and decoders preserve the original image quality and value. They support any image format up to 4K+ (4096x3112) with color depth up to 12 bit per component and JPEG 2000 Lossless compression.

• Single Chip
• Fully flexible image format up to 4K single tile
• Lossless Encoding

APPLICATIONS
Archiving
Store and Forward
Medical
Aerospace
Geospace

The Digital Cinema Family
DCI compliant IP-Cores

The intoPIX Digital Cinema IP-Cores are optimized to meet the highest requirements of Digital Cinema including 2K-120 fps and 4K-3D formats.

The Digital Cinema solution enables the integration within a single chip of a complete image processing chain, i.e. decryption-decoding-watermarking and encryption, together with video I/O interfaces, system control and system interfaces.

• Single Chip
• DCI compliant (JPEG 2000 Part 1 Amd 1)
• 2K resolution at up to 120 fps
• 4K resolution at up to 30 fps
• Bitrates up to 1000 Mbps

APPLICATIONS
Embedded Mediablock
Digital Cinema Exhibition
Digital Cinema Post-Production
Faster than real-time encoder
Theme park advanced display

The Ultra HD
4K/8K Family
JPEG 2000 for extreme resolutions

The intoPIX Ultra HD 4K & 8K IP-Cores go one step further in terms of encoding power and high-end applications. This range of IP-Cores gives you access to the new defined ITU UHDTV standards, 4K and 8K.

• Single Chip
• 4K resolution at up to 60fps
• 8K resolution at up to 60fps
• High bitrate flexibility

APPLICATIONS
UHDTV
Digital signage, Shows & Theme park
Advanced Cinema Mediablock
Geospace/Aerospace

www.intoPIX.com
Various IP-Cores

Companion IP-Cores
intoPIX proposes companion IP-Cores specially designed to ease the integration of JPEG 2000 and minimize your time-to-market.

DRAM Memory controller Cores
The IPX-DDR2 and IPX-DDR3 cores guarantee efficient memory accesses between the intoPIX JPEG 2000 IP-Cores and external DDR2 or DDR3 DRAM memory.

The IPX-DDR2 core runs up to 266 MHz on a 64 bit physical bus reaching peak transfer rates of 34 Gbit/s. Providing a low footprint, high efficiency DDR2 memory controller, it supports various user interfaces of 8, 16, 32 or 64 bit and a wide variety of DDR2 chip vendors and memory chip configurations.

The IPX-DDR3 core adds functionality to FPGA vendor DDR3 controllers in order to provide a flexible and efficient interface towards the intoPIX JPEG 2000 IP-Cores. It runs to up to 800 MHz, allowing you to reach peak transfer rates of 68 Gbit/s on 64 bit wide interface.

Memory arbiter Core
The IPX-MA memory arbiter enables the external memory to be shared between different processes i.e. frame buffers, watermarking etc. It is a 4-port arbiter. Each port presents the same width of 32, 64, 128 or 256 and runs up to 133 MHz.

Stream Serializer-Deserializer Core
The IPX-SERDES Serializer Companion Core transforms several parallel video streams into a single one. This serialized video stream can then be fed into one of the intoPIX Cores for high speed processing. The Deserializer Core processes the output stream into several parallel video streams in order to recreate several independent video channels. These cores are typically used to implement 3D stereoscopic or multi synchronous channel applications.

Security IP-Cores

AES Encryption-Decryption Cores
The IPX-AES Modules are encryptor-decryptor IP-Cores providing an efficient FPGA implementation of the Advanced Encryption Standard (AES).

The IPX-AES modules can be customized for each specific application. They support an extremely wide range of bitrates. Its flexibility allows combining several functions and operating modes on very small footprints.

Hash function Core
The IPX-HMAC-SHA-1 IP-Core is the hashing function required for content integrity check and content identification as specified in DCI documents. It enables computation of the keyed-hash message authentication code (HMAC) for audio and video assets.

RSA Public Key Cryptography Accelerator Core
The modular exponentiation accelerator IPX_RSA is an efficient arithmetic coprocessor for the RSA public-key cryptosystem. It performs the modular exponentiation calculation and therefore offloads the most computer-intensive operation of RSA from the main processor. The RSA cryptosystem can be used for public key encryption, decryption and signature/authentication.

The key advantage of the IPX_RSA IP-Core is its low footprint, thanks to an efficient balance between logic fabric and embedded RAMs and Multipliers.
## JPEG 2000 Encoding/Decoding

### Image features
- Bit depth: 8, 10, 12
- Color Space: RGB, XYZ and YCbCr
- Color Sampling: 4:2:2, 4:4:4
- Interlaced field, progressive frame
- Monochrome and 3 or 4 component color images

### JPEG 2000 (ISO 15444-1)
- Wavelet transforms: 5/3 and 9/7
- Reversible and irreversible color transforms
- Decomposition levels: up to 6 levels
- Quantization steps: programable per level and per component
- Quality layer: 1 layer
- Digital Cinema (DCI) compliant - JPEG 2000 Part 1 Amd 1
- Broadcast profiles compliant - JPEG 2000 Part 1 Amd 3
- Tiling: Single tile
- Progression Order: CRPL
- Code Block Size: 32x32, 64x64, 128x128
- Contrast sensitivity function

### Quality and Bit Rate Control
- Maximum codestream bitrate: 250 Mbps, 500 Mbps, 1 Gbps, 2 Gbps and 8 Gbps for Lossy compression and unlimited for Lossless compression
- Variable bit rate (VBR): The overall bit rate is variable for a selectable constant quality
- Capped VBR: 9/7 wavelet filter - Constant quality but variable bit rate is capped at a given maximum limit

### JPEG 2000 (ISO 15444-1)
- Rate is capped at a given maximum limit
- Capped VBR: 9/7 wavelet filter - Constant quality but variable bit rate is selectable constant quality
- Lossless compression
  - Maximum codestream bitrate: 250 Mbps, 500 Mbps, 1 Gbps, 2 Gbps and 8 Gbps
  - Contrast sensitivity function

### External memory requirements
- DDR2 at 250 MHz
- DDR3 from 400 to 800 MHz
- Physical data bus from 16 to 64 bits for DDR2 or DDR3

### Control
- Encoder:
  - 8 preloaded configurations and frame per frame control
  - Configuration control: through OPB bus or through video interface
  - Real-time access to status registers for monitoring and debug
- Decoder:
  - Up to 16 preloaded channel configurations
  - Configuration control: through OPB bus or through Code Stream control packets
  - Real-time access to status registers for monitoring and debug
  - On the fly code stream integrity check
  - Optional automatic frame repeater

### FPGA IP-Core MATRIX

#### Ip-core reference
- Encoder / Decoder
- Max resolution
- Max Bitrate
- Max Bitrate

#### TARGET ALTERA FPGA
- Speed grade is C4 in the Arria V family

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