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ABSTRACT

This document provides Draft 3 of a new Electrical Characteristic Standard.

ANSI/TIA-PN-3-4963

Draft 3

Electrical Characteristic of Generators and Receivers with Reversed-wire Immunity for Use in Balanced Digital Multipoint Systems

Revision Information

Rev.1: initial draft

Rev.2: Fixed 2.12; 2.13 figures. Added background section

Rev 3: Format and editorial clean-up.

Electrical Characteristic of Generators and Receivers with Reversed-wire Immunity for Use in Balanced Digital Multipoint Systems

(From TIA Standards Proposal ANSI/TIA-PN-3-4963 formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces)

Contents

FOREWORD

(This foreword is not part of this Standard.)

This Standard was formulated under the cognizance of TIA Subcommittee TR-30.2 on Data Transmission Interfaces.

1 SCOPE

This Standard specifies the electrical characteristics of generators and receivers that may be employed when specified for the interchange of binary signals in multipoint interconnection of digital equipment. When implemented within the guidelines of this Standard, multiple generators and receivers may be attached to a common interconnecting cable. The generators and receivers operate with no errors if the balanced interconnecting cables are connected normally or with the differential signal wires reversed.

An interchange system includes one or more generators connected by a balanced interconnecting cable to one or more receivers with or without terminating resistors. The electrical characteristics of the circuit are specified in terms of the required voltage, current, and resistance values obtained by measurements at the equipment interconnect points.

This Standard does not specify other characteristics, such as signal quality, timing, protocol, pin assignments, power supply voltage, operating temperature range, etc., that are essential for proper operation of interconnected equipment. Any devices complying with this Standard shall do so within the ranges of those factors appropriate for the device operation, such as power supply voltages, and ambient temperature. It is intended that this Standard be referenced by other standards and specifications that specify the additional characteristics necessary to assure satisfactory interoperation of equipment.

2 DEFINITIONS, SYMBOLS AND ABBREVIATIONS

For the purposes of this Standard, the following definitions, symbols and abbreviations apply:

2.1 Common-mode voltage (Vcm), one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. The common-mode voltage is the sum of ground potential difference; generator offset voltage and longitudinally coupled noise voltage.

2.2 Data signaling rate, expressed in the units bits (bits per second), is defined as *1/T* where T is the minimum interval between two significant instants.

2.3 Differential, the signal is the voltage difference between the A and B, not *with* respect to common (C).

2.4 Generator (Driver), the component of an interchange circuit that is a source of the transmitted signal.

2.5 Ground potential difference (Vgpd), the difference between the signal ground potential between the active generator and a receiver of an interchange circuit.

2.6 Longitudinally coupled noise voltage, unwanted voltage coupled inductively or capacitively between any two points along the balanced interconnecting cable (see 2.1).

2.7 Multipoint, a bus structure that has two or more generators and one or more receivers.

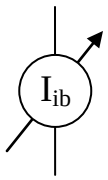
2.8 Passive-state, the output state of the generator presents high impedance. The generator either provides binary 0 outputs or the generator is off.

2.9 Receiver, the component of an interchange circuit that provides for the detection of interchange circuit signals at the receiving equipment.

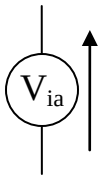
2.10 Star (*) represents the complementary logical state of a binary signal. For example, the symbol Q represents the receiver output state for one input condition, while Q* represents the output state for the opposite input state.

2.11 Transceiver, a component that includes both a receiver and generator.

2.12 Measured parameter:



2.13 Forced voltage:



3 APPLICABILITY

The provisions of this Standard apply only to the electrical characteristics of generators and receivers employed in communications between equipments. The information being conveyed is in the form of binary signals that may have a DC component. This Standard is not, therefore, an interface standard, but shall be referenced by those interface standards or specifications employing generators and receivers having these electrical characteristics.

The circuits whose characteristics are specified herein will be utilized normally in data, timing, or control interconnections where the data signaling rate is up to 5 Mbit/s. Devices meeting the electrical characteristics of this Standard need not operate over the entire data signaling rate range specified nor be limited to 5 Mbps. They may be specified to operate at data rates to satisfy specific applications. The upper bound is application dependent and beyond the scope of this Standard. Maximum data signaling rate is typically limited by the following: ratio of signal transition time to the unit interval, maximum allowable stub length, and the bandwidth of the interconnecting media. The characteristics are defined such that any device in the system can operate with a common-mode voltage as great as ±7V.

Compliant generators may be active simultaneously (contention) without damage. While generator contention may exist, there is no provision within this Standard for the detection of contention.

While the balanced generators and receivers described in this Standard are intended for use at high data signaling rates, they may (in preference to the unbalanced generators and receivers) generally be required where any of the following conditions prevail:

a) A multipoint (multiple generators) system is required.

b) The interconnecting cable is too long for effective unbalanced circuit operation.

c) The interconnecting cable is exposed to extraneous noise sources that may cause an unwanted voltage up to ±7V measured differentially between the signal conductor and circuit common at the load end of the cable with a 50Ω resistor substituted for the generator.

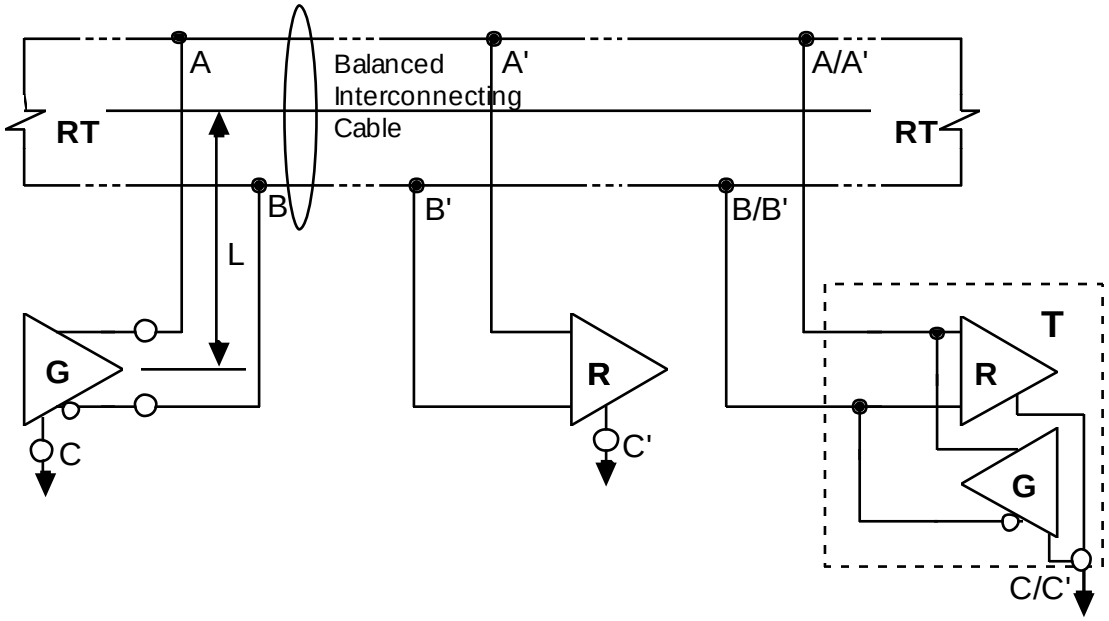
d) Logical inversion of the signals is NOT required.

4 ELECTRICAL CHARACTERISTICS

Figure 1 shows an interconnection application of generators and receivers having the electrical parameters specified in this Standard. The elements in the application are:

- Generators
- Receivers
- Transceivers
- Balanced interconnecting cable
- Termination resistors (RT)

The steady-state load on a single active generator shall be defined in the terms of unit loads (ULs). The load on the system caused by each receiver and passive generator shall be specified by the number or fractions of unit loads each presents. A unit load is defined by the current-voltage characteristics specified in 4.1.1. A load is defined as a passive generator (G), a receiver (R), or both (a Transceiver (T)). The electrical parameters specified in the following sections are selected so that a generator can drive a total load, having the value of 32 unit loads and an effective total termination resistance as low as 60Ω while providing a minimum differential voltage of 1.5 V or alternatively, a total load, having the value of 200 unit loads and no termination resistance while providing the same differential output.



Legend:

G = Generator	R = Receiver	T = Transceiver
L = Stub Length	RT = Termination Resistor	
A = Generator Interface Point	B = Generator Interface Point	C= Generator Common
A' = Receiver Interface Point	B' = Receiver Interface Point	C'= Receiver Common

A /A' = Transceiver Interface Point
B/B' = Transceiver Interface Point
C/C' = Transceiver Common

Figure 1 - Multipoint interconnect application

The electrical characteristics that are specified are those that are measured at the interface points. Tests made at the equipment interconnect points in accordance with referencing standards should recognize that the electrical performance at these points may be different than the interface points due to internal wiring and other receivers and passive generators within the equipment. In figure 1 and subsequent figures, points A, B, and C represent generator interface points, A', B' and C' represent the interface points associated with the receivers, and A/A', B/B' and C/C' represent the interface points associated with transceivers. The terminating resistors are considered part of the balanced interconnecting media.

The signaling sense of the voltages appearing across the interconnecting cable are defined as follows and is shown in Figure 2:

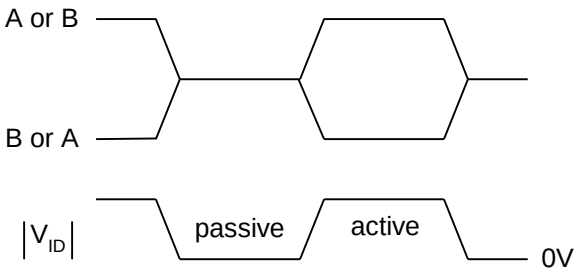


Figure 2 - Signaling Sense

a) The A terminal of the generator shall be different with respect to the B terminal for an active state.

b) The A terminal of the generator shall be the same with respect to the B terminal for a passive state.

The logic function of the generator and the receiver is beyond the scope of this Standard, and therefore is not defined.

4.1 Unit load characteristics

In order that the current required from a generator in the active state be limited to a practical value, the loading effect of any combination of receivers, passive generators or passive networks excluding the across-pair termination resistors is specified in terms of the loading produced by a hypothetical unit load (U.L.). Two areas of concern are: the DC load and the AC load characteristics. The DC load each device places on the system is defined as a number or fractions of unit loads as defined in 4.1.1. The AC loading is not standardized but must be considered in the design of a system using the devices meeting this Standard.

4.1.1 DC Unit load specification (Figures 3 and 4)

With the voltage Via (or Vib) ranging from -7.0 V to +12.0 V, while Vib (or Via) is held at 0.0 V(grounded), the resulting input current lia (or lib) shall be measured and remain within the shaded region shown in figure 3 for one unit load. The actual curve of current versus voltage should always have a positive slope to lower the possibility of oscillations caused by negative input resistance.

To determine the number of fractions of unit loads a passive generator or a receiver exhibits, the slope of the bounds in figure 3 shall be modified to the minimum slope required to fully contain the current-voltage characteristic, while the -3.0 V and +5.0 V intercept points are maintained. The number of unit loads is equal to the larger of the two ratios of the new currents to the original currents at the -7.0 V and +12.0 V intercept points. Example determinations are shown in figure 4. The number of equivalent UL is represented by nUL in subsequent sections.

The above described determinations should be performed in both power-on and power-off conditions. The system designer should consider both of these conditions in determining the total number of loads presented to the active generator. The current-voltage characteristics as a load's power supply is turned on or off is not standardized, but a user should recognize that such a transition may have some effect on system operation

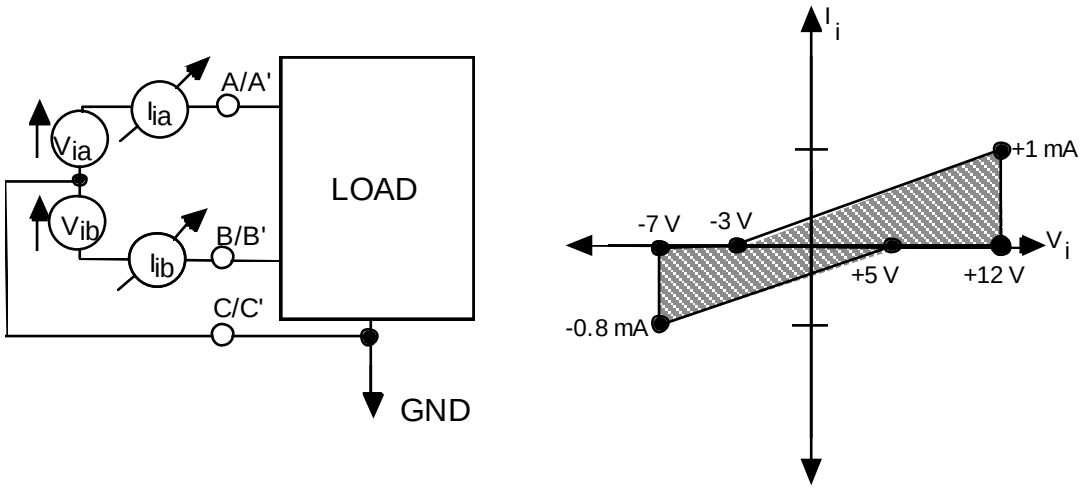


Figure 3. Unit load input current-voltage relationship

NOTE - A load is a passive generator, a receiver, a transceiver, or a passive network.

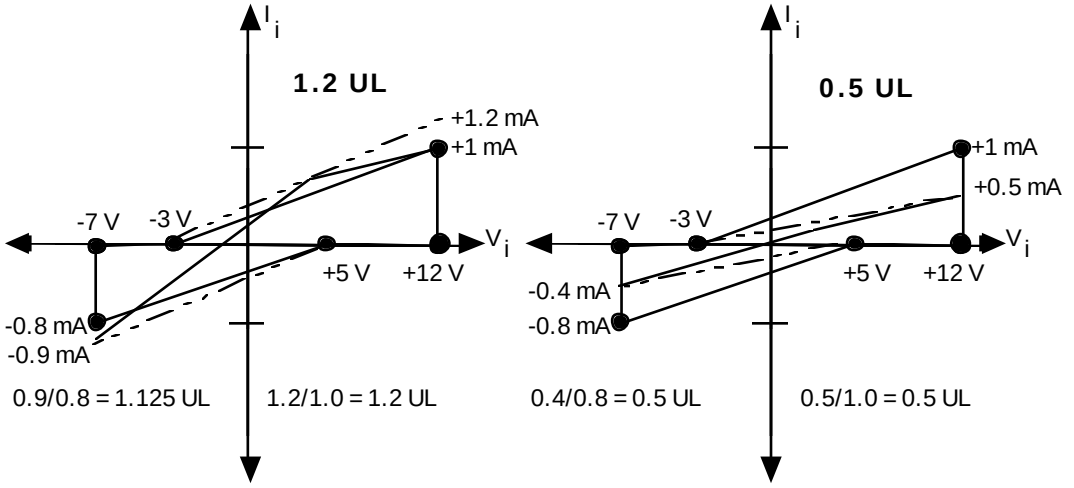


Figure 4. Unit load examples (1.2 UL and 0.5 UL)

4.1.2 AC Load characteristics

Devices connected to the interconnect means also display reactive characteristics which will have effects on the transmission characteristic of the interconnect means. These lumped effects will result in: reflections, unbalance, and or distortion of the signal.

These may cause effects to the differential impedance, the impedance from A' to C', and from B' to C' on a receiver or the impedance from A to C and from B to C on a passive generator. These parameters may be specified by a referencing standard if they are, deemed critical, as they are application dependent and not further specified in this Standard.

4.2 Generator characteristics

A generator is in either the passive or in one of two active states. While in the passive state, the generator output characteristics shall be specified in terms of equivalent ULs as defined in 4.1.1. While in the active state, the generator electrical characteristics are specified in accordance with the measurements described in 4.2.1 through 4.2.7. A generator circuit meeting these requirements results in a balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 1.5 to 5V.

The generator characteristics includes tests (4.2.5 and 4.2.6) which are intended to assure that it will not be damaged due to single fault conditions. While some of the mechanisms of potential circuit failure are tested by these sections, certain other extraneous conditions may over stress the generator. These conditions should be specified in the referencing standard if required.

4.2.1 Open circuit output voltages (Figure 5)

For either active state, the magnitude of the differential voltage (Vo or Vo*) measured between the two generator output terminals shall not be less than 1.5 V and not more than 6 V. The magnitudes of Voa and Vob respectively, measured with respect to generator circuit common, shall not exceed 6 V for either binary state.

For the passive state, the magnitude of the differential voltage measured between the two generator output terminals shall not be more than 50 mV. The magnitudes of Voa and Vob respectively, measured with respect to generator circuit common, shall not exceed 6 V for the passive state.

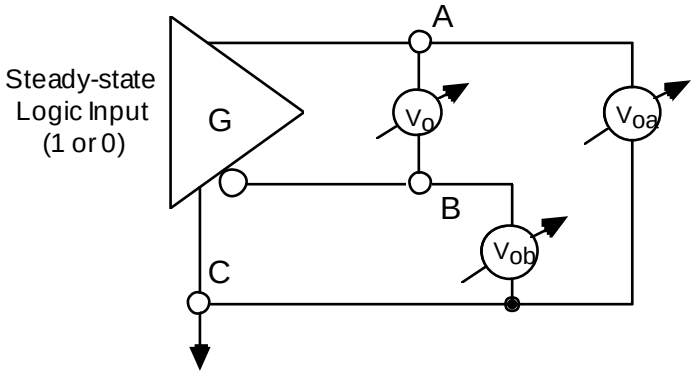


Figure 5 - Open circuit output voltages

Note: Only one of the active states is required for generator.

4.2.2 Differential and offset output voltages (Figure 6)

With a test load of two resistors, 27Ω ±1% each, connected in series between the generator output terminals, the magnitude of the differential output voltage (Vt1) measured between the two output terminals shall not be less than 1.5 V nor greater than 6V for active state.

The passive state is the magnitude of the differential voltage measured between the two generator output terminals shall not be more than 50 mV. The magnitudes of Voa and Vob respectively, measured with respect to generator circuit common, shall not exceed 6 V for the passive state.

The generator offset voltage (Vos), measured between the center point of the resistors and the generator circuit common shall be between -1.0 V and +3.0 V for both active and passive states. While the common mode specifications are designed for deliberate offset voltage, the user is permitted to use zero offset. However, if zero offset is used, the tolerance to common mode is reduced. The magnitude of the difference of Vos for the active state and Vos* for the passive state shall less than 0.2 V.

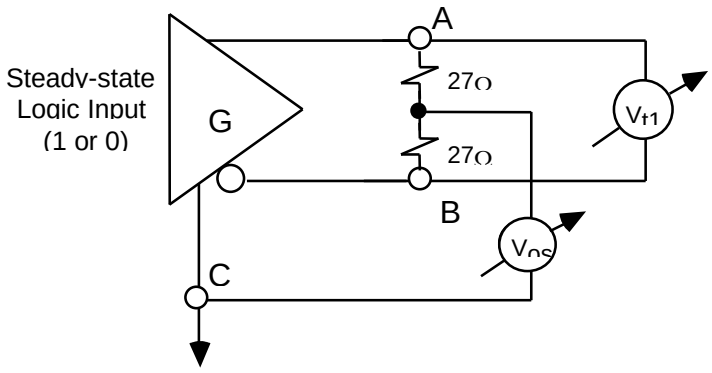


Figure 6 - Differential and offset output voltages

4.2.3 Differential output voltages with common-mode loading *(Figure 7)*

This test is performed with a test load of 60Ω±1%, paralleled with two 375Ω±1% resistors connected in series. The center point of the two 375Ω resistors is connected to a voltage source that is varied between -7.0 V and +12.0 V, to simulate common-mode voltages.

For the active state, the magnitude of the differential output voltage (Vt2) measured between the two output terminals shall not be less than 1.5 V nor greater than 6V over the entire -7.0 V to +12.0 V range.

For the passive state, the magnitude of the differential voltage measured between the two generator output terminals shall not be more than 50 mV. The magnitudes of Voa and Vob respectively, measured with respect to generator circuit common, shall not exceed 6 V for the passive state.

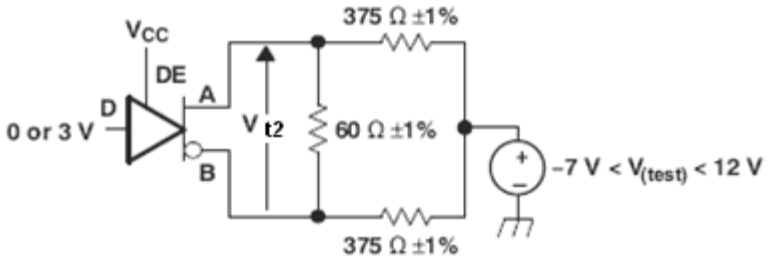


Figure 7 - Differential output voltages with common-mode loading

4.2.4 Off-state output current

Under the power-on off-state (passive state), and power-off conditions, the magnitude of the generator output currents (Ixa and Ixb) with voltages ranging from -7.0 V to +12.0 V applied between each output terminal and generator circuit common, should be small in magnitude and specified in term of U.L.. See 4. 1.1

4.2.5 Short-circuit output characteristics (Figures 8 and 9)

With the generator output terminals short-circuited to each other, the generator shall not be damaged.

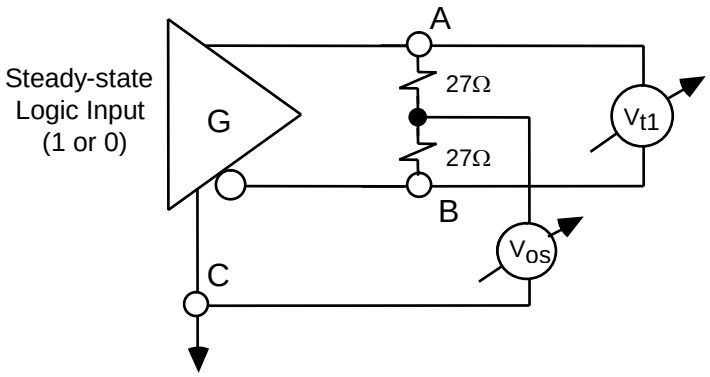


Figure 8. Short-circuit output current (A to B)

A generator shall not sustain any damage as a result of connecting its output terminals to a voltage source, variable from -7.0 V to +12.0 V, under any output condition, binary active or passive.

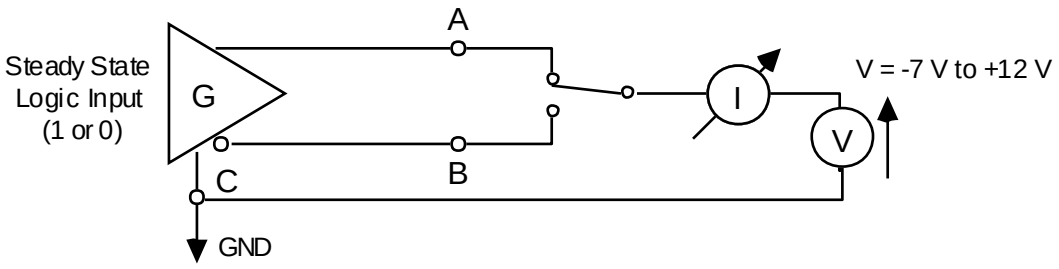


Figure 9 - Short-circuit output current (over common-mode)

Under any condition of the applied voltage test specified above and with a slew rate of the variable voltage source equal to or less than 1.2 V/us, the peak current magnitude shall not exceed 350 mA. This criterion is not to be interpreted as a requirement that a generator be capable of sourcing 350 mA. Rather, the sinking generator shall not permit a composite current in excess of 350 mA, if multiple (sourcing) generators are providing that current.

4.2.6 Transient over voltage tolerance (Figure 10)

This requirement is necessary to provide for protection from transients that may occur on a line when the high current due to single contending pair is interrupted. The test shall be performed in both power-on and power-off conditions.

A passive generator or a receiver must be able to withstand without permanent damage applied pulses of 15 us duration at a 1% duty cycle from a ±25.0 V source having a 100Ω source impedance. Both positive and negative pulses shall be applied at the interface points.

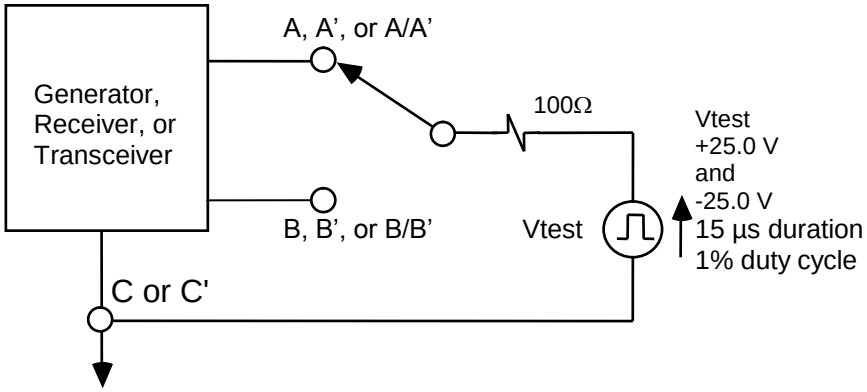


Figure 10 - Transient over voltage tolerance

4.2.7 Output signal waveform (Figure 11)

During transitions (tr and tf) of the generator output voltage between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across a test load composed of a 54Ω±1 % resistance paralleled with 50 pF ±20% capacitance connected between the generator output terminals shall be such that the voltage monotonically

changes between 0.1 and 0.9 of Vss and within 0.3 of the unit interval (tui). Thereafter, the signal voltage shall not vary more than 10% of Vss from the steady state value until the next binary transition occurs. At no time shall the instantaneous magnitude of Vt or Vt * exceed 5.0 V. Vss is defined as the voltage difference between the two steady-state values of the generator output (Vss=IVt-Vt*I) and is also known as peak-to-peak voltage.

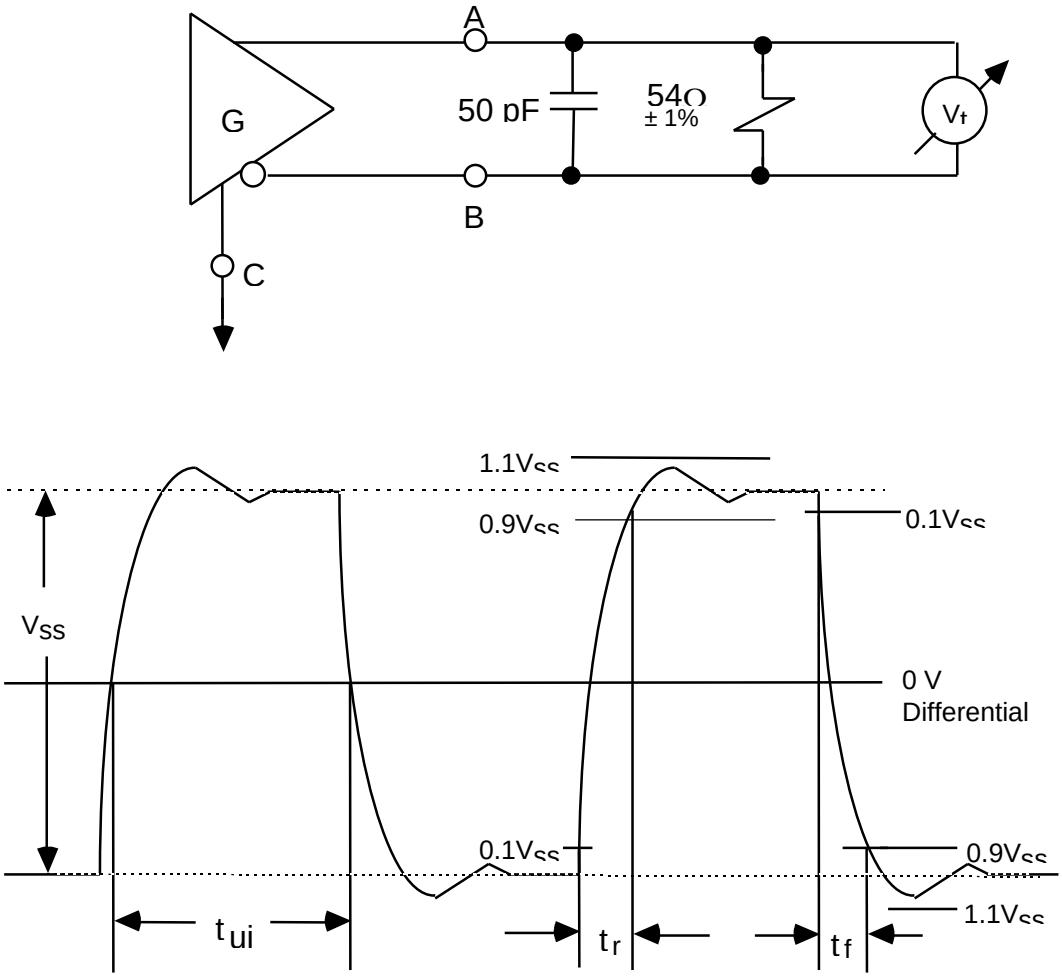


Figure 11 - Output signal waveform (signal transition time)

4.3 Receiver characteristics

The receiver electrical characteristics are specified in accordance with the load specifications in 4.1.1 and with the measurements described in 4.3.1 through 4.3.5 and illustrated in figures: 3, 10, 12 and 13. A circuit meeting these requirements results in a differential receiver with an input voltage threshold between 0.5V and +0.9 V inclusive.

4.3.1 Input voltage ranges (Figure 12)

The minimum allowable range of input voltages ($V_{A'}$ and $V_{B'}$) appearing at the receiver input terminals (A' and B') measured with respect to the receiver common (C') is between -7V

and +12V inclusive while the resulting differential input voltage magnitude is 6V maximum.

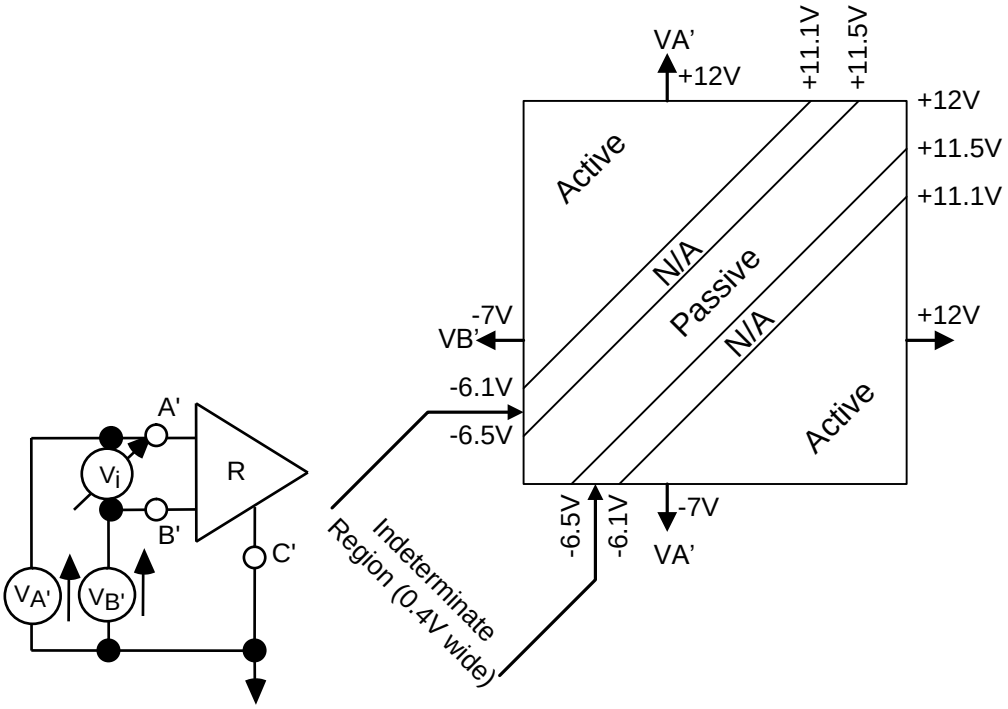


Figure 12 - Input voltage range

4.3.2 Input thresholds

For any combination of receiver input voltages within the allowable ranges, the receiver shall assume the intended binary state with an applied differential input voltage (Vi) of ±0.20V or more. Additionally, the receiver shall not be damaged for any combination and a differential input voltage magnitude of 6V. Table 1 lists the operating voltage extremes of the receiver. Operation outside of this allowable range is not covered by this Standard.

> **NOTE -** Designers of terminating networks should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiver device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, hysteresis may be incorporated into the receiver to help prevent such conditions.

Table 1- Receiver operating voltage extremes

$V_{A'}$(V)	$V_{B'}$(V)	Resulting Vcm(V)	Vi(V)	Output State	Intent
-7.0	-6.5	-6.75	-0.5	Passive	Maximum Vi at extreme negative common mode for passive state
-6.5	-7.0	-6.75	+0.5	Passive	
-7.0	-2.0	-4.5	-5.0	Active	Maximum Vi at extreme negative

$V_{A'}$(V)	$V_{B'}$(V)	Resulting Vcm(V)	Vi(V)	Output State	Intent
-2.0	-7.0	-4.5	+5.0	Active	common mode for active state
+12.0	+11.5	+11.75	+0.5	Passive	Maximum Vi at extreme positive common mode for passive state
+11.5	+12.0	+11.75	-0.5	Passive	
+12.0	+7.0	+9.5	+5.0	Active	Maximum Vi at extreme positive common mode for active state
+7.0	+12.0	+9.5	-5.0	Active	
-7.0	-6.1	-6.55	+0.9	Active	Minimum Vi at extreme negative common mode for active state
-6.1	-7.0	-6.55	-0.9	Active	
+12.0	+11.1	+11.55	+0.9	Active	Minimum Vi at extreme positive common mode for active state
+11.1	+12.0	+11.55	-0.9	Active	

4.3.3 Input balance measurements (Figure 13)

The balance of the receiver input current-voltage characteristics and bias voltage shall be such that the receiver will remain in the intended binary state when a differential voltage (VR3) of ±0.40 V is applied through matched resistors equal to 1500/nUL 1/2 to each input terminal, as shown in figure 13, with the input voltages $V_{R1}$and V_{R2} (and resulting V_{R3}) to achieve any allowed input condition. When the polarity of V_{R3} reverses, the opposite binary state shall be maintained under the same conditions. (The resistor values used will vary depending upon how many unit loads or fractions of a unit load the receiver loading represents.) This test limits the induced differential noise voltage due to imbalance of the inputs (impedance) to 200 mV.

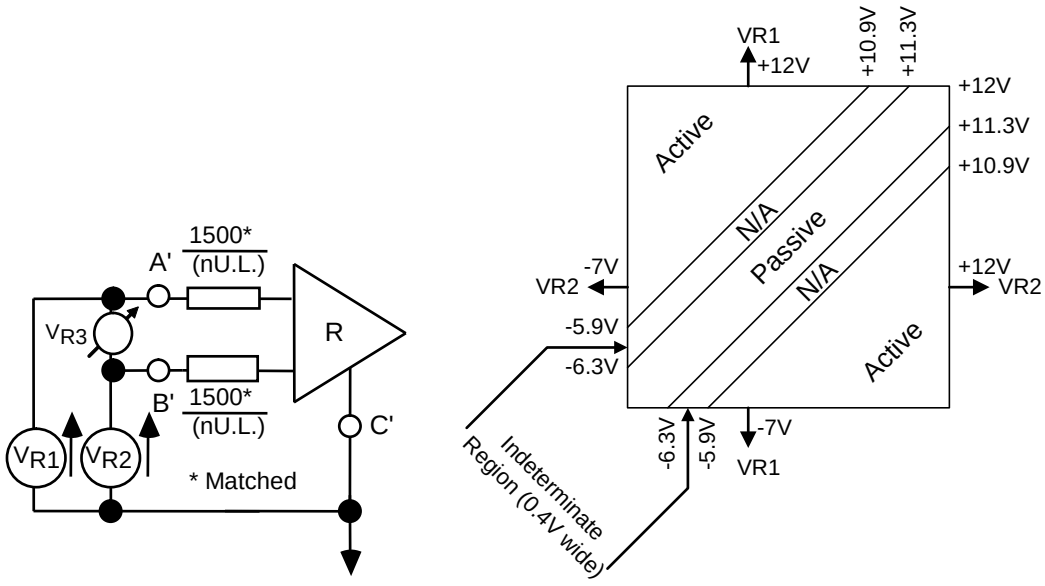


Figure 13 - Input balance measurements

4.3.4 Receiver unit load test (Figure 3)

The receiver unit load (UL) values shall be determined according to the measurements specified in 4.1.1. (The number of equivalent ULs is represented by nUL).

4.3.5 Transient over voltage tolerance (Figure 10)

The requirements of 4.2.6 also apply to receivers, see 4.2.6.

4.4 Transceiver characteristics

A transceiver is defined as the combination of a generator and a receiver. The transceiver electrical characteristics are specified in accordance with the load specifications in 4.1.1, generator characteristics 4.2.1 through 4.2.3 and 4.2.5 though 4.2.7, and receiver characteristics 4.3.1 through 4.3.3.

4.5 System requirements

This Standard allows for numerous applications supporting a wide range of configurations, data signaling rates, and environments. *Application Guidelines* covers the trade off between these application dependent constraints and requirements.

4.5.1 Balanced interconnecting media characteristics

The characteristics of the balanced interconnecting media are not specified. To ensure proper operation, however, paired cable with metallic conductors should be employed. The performance of any interconnecting cable used must be such as to maintain the necessary signal quality required for the specific application. The differential-mode characteristic impedance should nominally be 120Ω to maintain minimum noise margins under worse case conditions. Other differential-mode characteristic impedance (e.g., 100Ω) may be employed, however certain trade off must be made. The user is referenced to Application Guidelines for further guidance.

4.5.2 Cable termination

The use of a cable termination is not strictly required. Its impedance value can be matched to the differential-mode characteristic impedance of the balanced interconnecting cable. Unterminated bus can be used as well.

4.5.3 Total load limit

The total load including all passive generators, receivers, transceivers, optional fail-safe provisions, and cable termination should be no less than 54Ω between the interface points (A and B) as shown in Figure 1.

4.5.4 Fail-safe operation

Other standards and specifications using referring to this Standard may require that specific interchange circuits be made fail safe to certain fault conditions. Such fault conditions may include one or more of the following:

a) generator(s) in power-off condition

b) receiver not connected with the cable

c) open-circuited interconnecting cable

d) short-circuited interconnecting cable

e) input signal to the load remaining within the transition region (500 mV < | VID| < 900 mV) for an abnormal period of time (application dependent)

When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required, and the following items must be determined and specified:

a) which interchange circuits require fault detection

b) what faults must be detected

c) What action must be taken when a fault is detected; the binary state that the receiver assumes.

The method of detection of fault conditions is application-dependent and is therefore not further specified.

Annex A (Informative)

GUIDELINES FOR APPLICATION

When interconnecting equipment which use the electrical characteristics specified in this standard, consideration should be given to some of the problems that may be encountered due to system configuration, data signaling rate vs. cable length, stub length, and grounding arrangements.

A.1 Multipoint system configuration

The multipoint system should be configured in the form of a daisy chain. Star, tree, or branch configurations are generally not recommended.

A.2 Data signaling rate vs. cable length

High data signaling rates and long cable lengths are possible, however, they are mutually exclusive. High data signaling rate applications should be limited to short cable lengths, while low data signaling rate applications may employ long cable lengths. The length of the cable for low speed applications is primarily limited by the dc resistance of the cable. This resistance creates a voltage drop in the cable, thus effects noise margin. For high speed applications, the ac effects of the cable limit the signal quality, and thus primarily limit the cable length to short distances.

A-3 Stub lengths

In order for the stubs (see Figure 1) off the main cable to be seen as a lumped load, their length should be keep as short as possible.

A.4 Optional grounding arrangements

A.4.1 Signal common (Ground)

Proper operation of the interface circuits requires the presence of a signal common path between the circuit commons of the equipment connected along the balanced interconnecting. The signal common interchange lead shall be connected to the circuit common which shall be connected to protective ground by any one of the following methods, shown in figure A.1 or A.2, as required by specific application.

A.4.2 Configuration "A"

The circuit common of the equipment is connected to protective ground, at one point only, by a 100Ω, ±20%, resistor with a power dissipation rating of 1/2 W. An additional provision may be made for the resistor to be bypassed with a strap to connect signal common and protective ground directly together when specific installation conditions necessitate.

A.4.3 Configuration "B"

The circuit common shall be connected directly to protective ground.

The same configuration need not be used at both ends of an interconnection; however, care should be exercised to prevent establishment of ground loops carrying high currents.

NOTE - Under certain ground fault conditions in configuration "A", high ground currents may cause the resistor to fail; therefore, a provision shall be made for inspection and replacement of the resistor.

A.4.4 Shield ground

Some interface applications may require the use of shielded interconnecting cable for RFI/EMI or other purposes. When employed, the shield shall be connected only to frame ground at either or both ends depending on the specific application. The means of connection of the shield and any associated connector are beyond the scope of this annex.

A.5 References

ANSI/TIA/EIA-422-B-1995, *Electrical characteristics of balanced voltage digital interface circuits.*

ANSI/TIA/EIA-485, *Electrical characteristics of balanced voltage digital interface circuits.*

ITU-T V.11-1996, *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications.*

ISO/IEC 8482:1993, *Information technology-telecommunications and information exchange between systems - twisted pair multipoint interconnections*