COMMUNICATIONS ENGINEERING SERIES


# Switchmode RF Power Amplifiers

Andrei Grebennikov
Nathan O. Sokal

Newnes

# *Switchmode RF Power Amplifiers*

This page intentionally left blank

# *Switchmode RF Power Amplifiers*

Andrei Grebennikov

Nathan O. Sokal

ELSEVIER

AMSTERDAM • BOSTON • HEIDELBERG • LONDON
NEW YORK • OXFORD • PARIS • SAN DIEGO
SAN FRANCISCO • SINGAPORE • SYDNEY • TOKYO
Newnes is an imprint of Elsevier

Newnes is an imprint of Elsevier
30 Corporate Drive, Suite 400, Burlington, MA 01803, USA
Linacre House, Jordan Hill, Oxford OX2 8DP, UK



**Library of Congress Cataloging-in-Publication Data**
Grebennikov, Andrei, 1956–
Switchmode rf power amplifiers / By Andrei Grebennikov and Nathan O. Sokal. –1st ed.
p. cm.
Includes bibliographical references and index.
ISBN 978-0-7506-7962-6 (alk. paper)
1. Power amplifiers. 2. Microwave amplifiers. I. Sokal, Nathan O. II. Title.
TK7871.58.P6G75 2007
621.3815′35–dc22 2007017121

**British Library Cataloguing-in-Publication Data**
A catalogue record for this book is available from the British Library.

ISBN: 978-0-7506-7962-6

For information on all Newnes publications
visit our Web site at www.books.elsevier.com

07 08 09 10 10 9 8 7 6 5 4 3 2 1

Printed in the United States of America

# Table of Contents

*About Andrei Grebennikov* ..... *ix*
*About Nathan O. Sokal* ..... *xi*
*Preface* ..... *xiii*
*Acknowledgments* ..... *xvii*

*Chapter 1: Power-Amplifier Design Principles* ..... *1*
1.1 Spectral-Domain Analysis ..... 1
1.2 Basic Classes of Operation: A, AB, B, and C ..... 7
1.3 Active Device Models ..... 15
1.4 High-Frequency Conduction Angle ..... 20
1.5 Nonlinear Effect of Collector Capacitance ..... 27
1.6 Push-Pull Power Amplifiers ..... 30
1.7 Power Gain and Stability ..... 35
1.8 Parametric Oscillations ..... 46
References ..... 50

*Chapter 2: Class-D Power Amplifiers* ..... *55*
2.1 Switched-Mode Power Amplifiers with Resistive Load ..... 55
2.2 Complementary Voltage-Switching Configuration ..... 64
2.3 Transformer-Coupled Voltage-Switching Configuration ..... 69
2.4 Symmetrical Current-Switching Configuration ..... 71
2.5 Transformer-Coupled Current-Switching Configuration ..... 74
2.6 Voltage-Switching Configuration with Reactive Load ..... 78
2.7 Drive and Transition Time ..... 82
2.8 Practical Class-D Power Amplifier Implementation ..... 89
References ..... 92

*Chapter 3: Class-F Power Amplifiers* ..... *95*
3.1 Biharmonic Operation Mode ..... 95

3.2 Idealized Class-F Mode ..... 104
3.3 Class F with Maximally Flat Waveforms ..... 108
3.4 Class F with Quarter-wave Transmission Line ..... 115
3.5 Effect of Saturation Resistance and Shunt Capacitance ..... 119
3.6 Load Networks with Lumped Elements ..... 123
3.7 Load Networks with Transmission Lines ..... 129
3.8 LDMOSFET Power-Amplifier Design Examples ..... 133
3.9 Practical RF and Microwave Class-F Power Amplifiers ..... 138
References ..... 145

***Chapter 4: Inverse Class F ..... 151***
4.1 Biharmonic Operation Mode ..... 151
4.2 Idealized Inverse Class-F Mode ..... 158
4.3 Inverse Class F with Quarter-wave Transmission Line ..... 161
4.4 Load Networks with Lumped Elements ..... 162
4.5 Load Networks with Transmission Lines ..... 164
4.6 LDMOSFET Power-Amplifier Design Examples ..... 167
4.7 Practical Implementation ..... 172
References ..... 176

***Chapter 5: Class E with Shunt Capacitance ..... 179***
5.1 Effect of Detuned Resonant Circuit ..... 179
5.2 Load Network with Shunt Capacitor and Series Filter ..... 183
5.3 Matching with Standard Load ..... 192
5.4 Effect of Saturation Resistance ..... 195
5.5 Driving Signal and Finite Switching Time ..... 198
5.6 Effect of Nonlinear Shunt Capacitance ..... 206
5.7 Push-Pull Operation Mode ..... 208
5.8 Load Network with Transmission Lines ..... 213
5.9 Practical RF and Microwave Class-E Power Amplifiers and Applications ..... 218
References ..... 227

***Chapter 6: Class E with Finite dc-Feed Inductance ..... 233***
6.1 Class E with One Capacitor and One Inductor ..... 233
6.2 Generalized Class-E Load Network with Finite dc-Feed Inductance ..... 241
6.3 Subharmonic Class E ..... 250
6.4 Parallel-Circuit Class E ..... 253
6.5 Even-Harmonic Class E ..... 257
6.6 Effect of Bondwire Inductance ..... 260
6.7 Load Network with Transmission Lines ..... 261
6.8 Broadband Class E ..... 269

6.9 Power Gain ..... 280
6.10 CMOS Class-E Power Amplifiers ..... 283
References ..... 287

***Chapter 7: Class E with Quarter-wave Transmission Line ..... 293***
7.1 Load Network with Parallel Quarter-wave Line ..... 293
7.2 Optimum Load Network Parameters ..... 301
7.3 Load Network with Zero Series Reactance ..... 302
7.4 Matching Circuit with Lumped Elements ..... 307
7.5 Matching Circuit with Transmission Lines ..... 310
7.6 Load Network with Series Quarter-wave Line and Shunt Filter ..... 312
References ..... 314

***Chapter 8: Alternative and Mixed-Mode High-Efficiency Power Amplifiers ..... 315***
8.1 Class-DE Power Amplifier ..... 316
8.2 Class-E/F Power Amplifiers ..... 330
8.3 Biharmonic Class-$E_M$ Power Amplifier ..... 338
8.4 Inverse Class-E Power Amplifiers ..... 344
8.5 Harmonic Tuning Using Load-Pull Techniques ..... 352
References ..... 359

***Chapter 9: Computer-Aided Design of Switched-Mode Power Amplifiers ..... 363***
9.1 HB-PLUS Program for Half-Bridge and Full-Bridge Direct-Coupled Voltage-Switching Class-D and Class-DE Circuits ..... 363
9.2 HEPA-PLUS CAD Program for Class E ..... 368
9.3 Effect of Class-E Load-Network Parameter Variations ..... 371
9.4 HB-PLUS CAD Examples for Class D and Class DE ..... 375
9.5 HEPA-PLUS CAD Example for Class E ..... 381
9.6 Class-E Power-Amplifier Design Using SPICE ..... 392
9.7 ADS Circuit Simulator and Its Applicability to Switched-Mode Class E ..... 398
9.8 ADS CAD Design Example: High-Efficiency Two-Stage *L*-Band HBT Power Amplifier ..... 403
References ..... 418

***Index ..... 421***

This page intentionally left blank

# About Andrei Grebennikov

Dr. Andrei Grebennikov, IEEE Senior Member, has obtained a long-term academic and industrial experience working with Moscow Technical University of Communications and Informatics, Russia; Institute of Microelectronics, Singapore; M/A-COM, Ireland; and Infineon Technologies, Germany, as an engineer, researcher, lecturer, and educator. He lectured as a Guest Professor at the University of Linz, Austria, and presented short courses as an Invited Speaker at the International Microwave Symposium, European Microwave Conference, and Motorola Design Centre, Malaysia. He is an author of more than 60 papers, 3 books, and several European and U.S. patents.

This page intentionally left blank

# About Nathan O. Sokal

In 1989, Mr. Sokal was elected a Fellow of the IEEE for his contributions to the technology of high-efficiency switching-mode power conversion and switching-mode RF power amplification. In 2007, he received the Microwave Pioneer award from the IEEE Microwave Theory and Techniques Society, in recognition of a major, lasting contribution—development of the Class-E RF power amplifier.

In 1965, he founded Design Automation, Inc., a consulting company doing electronics design review, product design, and solving ''unsolvable'' problems for equipment-manufacturing clients. Much of that work has been on high-efficiency switching-mode RF power amplifiers at frequencies up to 2.5 GHz, and switching-mode dc-dc power converters. He holds eight patents in power electronics, and is the author or co-author of two books and approximately 130 technical papers, mostly on high-efficiency generation of RF power and dc power.

During 1950–1965, he held engineering and supervisory positions for design, manufacture, and applications of analog and digital equipment.

He received B.S. and M.S. degrees in Electrical Engineering from the Massachusetts Institute of Technology, Cambridge, Massachusetts, in 1950.

He is a Technical Adviser to the American Radio Relay League, on RF power amplifiers and dc power supplies, and a member of the Electromagnetics Society, Eta Kappa Nu, and Sigma Xi honorary professional societies.

This page intentionally left blank

# Preface

The main objective of this book is to present all relevant information required to design high-efficiency RF and microwave power amplifiers, including well-known and novel theoretical approaches and practical design techniques. Regardless of the different operation classes like Class D, Class E, or Class F and their combination, an efficiency improvement is achieved by providing the nonlinear operation conditions when an active device can subsequently operate in pinch-off, active, and saturation regions resulting in nonsinusoidal collector current and voltage waveforms—for example, symmetrical for Class-F and asymmetrical for Class-E modes. As a result, the power amplifiers operated in Class F can be analyzed explicitly in the frequency domain when the harmonic load impedances are optimized by short-circuit and open-short terminations to control the voltage and current waveforms at the collector to obtain maximum efficiency. However, the power amplifier operated in Class E can be fully analyzed analytically in the time domain when an efficiency improvement is achieved by realizing the ideal on-to-off active device operation in pinch-off and voltage-saturation modes only, so high voltage and high current at the collector do not occur at the same time. Unlike the single-ended power amplifiers operated in Class-F or Class-E modes, a Class-D power amplifier represents a switching-mode power amplifier using two switching-mode active devices driven on and off so that one of the switches is turned on when the other is turned off, and vice versa.

Generally, this book is intended for and can be recommended to practicing RF circuit designers and engineers as an anthology of a wide family of high-efficiency RF and microwave power amplifiers based on both well-known and novel switched-mode operation conditions with detailed description of their operational principles and applications and clear practical demonstration of theoretical results. To bridge the theoretical idealized results with real practical implementation, the theory is supported by design examples, in which the optimum design approaches effectively combine analytical calculations and simulation, resulting in practical schematics of high-efficiency power-amplifier circuits using different types of field effect or bipolar transistors.

The introductory Chapter 1 describes the basic principles of power amplifier design procedures. Based on the spectral-domain analysis, the concept of a conduction angle is

introduced with simple and clear analyses of the basic Class A-, AB-, B-, and C-power amplifiers. Nonlinear models are given for MOSFET, MESFET, HEMT, and bipolar devices (including HBTs), which have very good prospects for power amplifiers using modern microwave monolithic integrated circuits. The effect of the device input parameters on the conduction angle at high frequencies is explained. The concept and design of push-pull amplifiers using balanced transistors are presented. The possibility of the maximum power gain for a stable power amplifier is discussed and analytically derived. Finally, the parasitic parametric effect due to the nonlinear collector capacitance and measures for its cancellation in practical power amplifier are discussed.

In Chapter 2, the voltage-switching and current-switching configurations of Class-D power amplifiers are presented, the increased efficiency of which is a result of operating the active devices as switches. The basic switched-mode power amplifiers with resistive load of different configurations, and the current-switching and voltage-switching configurations based on complementary and transformer-coupled topologies are analyzed. We demonstrate the effects of the transistor saturation resistance, rectangular and sinusoidal driving signals, nonzero switching transition times, and parasitic shunt capacitance and series inductance. We describe practical design examples of voltage-switching and current-switching Class-D power amplifiers that are intended to operate at high frequencies and microwaves.

Highly efficient operation of the power amplifier can be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multi-resonant circuit tuned to the odd harmonics of the fundamental frequency is added to the load network. An infinite number of odd-harmonic resonators results in an idealized Class-F mode with a square voltage waveform and a half-sinusoidal current waveform at the device output terminal providing ideally 100% collector (or drain) efficiency. Chapter 3 describes the different Class-F techniques using lumped and transmission-line elements including a quarter-wave transmission line. The effects of the transistor saturation resistance and parasitic shunt capacitance are demonstrated. Design examples and practical RF and microwave Class-F power amplifiers are given and discussed.

An inverse Class-F mode can be obtained by using a single-resonant or a multi-resonant circuit tuned to the even harmonics of the fundamental frequency added to the load network. An infinite number of even-harmonic resonators results in an idealized inverse Class-F mode with a half-sinusoidal voltage waveform and a square current waveform at the device output terminal. Chapter 4 describes the different inverse Class-F techniques using lumped and transmission-line elements including a quarter-wave transmission line. Design examples and practical RF and microwave inverse Class-F power amplifiers are presented.

The switched-mode Class-E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high-efficiency operation. In the

Class-E power amplifier, the transistor operates as an on/off switch, and the shapes and relative timing of the current and voltage waveforms are such that high current and high voltage do not occur simultaneously. That minimizes the power dissipation and maximizes the power-amplifier efficiency. Chapter 5 presents the historical aspect and modern trends of Class-E power amplifier design. Different circuit configurations and load-network techniques using the push-pull mode, with lumped and transmission-line elements, are analyzed. The effects of the device saturation resistance, finite switching times, and nonlinear shunt capacitance are described. Practical RF and microwave Class-E power amplifiers and their applications are given and discussed.

In Chapter 6, we discuss and analyze the switched-mode second-order Class-E configurations with one capacitor and one inductor and generalized load network including the finite dc-feed inductance, shunt capacitance, and series reactance. We present the results of the Fourier analysis and derivation of the equations for the idealized operation of the circuit. Effects of the device output bondwire inductance on the optimum circuit parameters are demonstrated. The possibilities to realize a Class-E approximation with transmission lines and broadband Class-E load networks are shown and discussed. The operating power gain of a parallel-circuit Class-E power amplifier is evaluated and compared with the operating power gain of a conventional Class-B power amplifier. Circuit design examples and practical implementations of CMOS Class-E power amplifiers are also given.

Chapter 7 presents the results of exact time-domain analysis of the switched-mode tuned Class-E power amplifiers with a quarter-wave transmission line. The load-network parameters are derived analytically. The idealized collector voltage and current waveforms demonstrate the possibility of 100% efficiency. We consider load-network implementation, including output matching circuit at RF and microwave frequencies, using lumped and transmission-line elements. We provide accurate derivation of the matching circuit parameters. Switched-mode Class-E power amplifiers with a quarter-wave transmission line offer a new challenge for RF and microwave power amplification, providing high efficiency and harmonic suppression.

Chapter 8 presents alternative and mixed-mode configurations of high-efficiency power amplifiers. The Class-DE power amplifier is the combination of a voltage-switching Class-D mode and Class-E switching conditions, thus extending the switching Class-D operation to higher frequencies. The switched-mode Class-E/F power amplifier can provide lower peak voltage on the switch, while providing the Class-E zero voltage and zero voltage-derivative switching conditions required to eliminate capacitor-discharge power dissipation. This is achieved by harmonic tuning using resonant circuits tuned to selected harmonic frequencies, realizing Class-F mode. Also described is the biharmonic Class-$E_M$ mode, which can reduce the switching power dissipation of a Class-E circuit operating at higher frequencies, at which the turn-off switching time occupies a larger fraction of the RF period. The requirements of jumpless voltage and current waveforms and sinusoidal load waveform, with nonzero output

power delivered to the load, can be provided by using nonlinear reactive elements in the load network to convert fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source. The inverse Class-E power amplifier is the dual of the classical Class-E power amplifier with a shunt capacitor, in which the load-network inductor and capacitor replace each other. However, this dual circuit is limited to low operating frequencies or low output powers because the transistor must discharge its output capacitance from the peak voltage to zero in every RF cycle. As a result, the transistor must be sufficiently small to reduce the capacitor-discharge power dissipation to an acceptable level. Finally, harmonic-control techniques for designing microwave power amplifiers are given, with a description of a systematic procedure of multiharmonic load-pull simulation using the harmonic balance method and active load-pull measurement system.

Nonlinear circuit simulation in the frequency and time domains is a very important tool for analysis, design, and optimization of high-efficiency switched-mode power amplifiers of Class D, DE, and E. The advantages are the significantly reduced development time and final product cost, better understanding of the circuit behavior, and faster obtaining of the optimum design. It is especially important at very high frequencies, including microwaves, and for MMIC development, where the transistor and circuit parasitics can significantly affect the overall power amplifier performance. Therefore, it is very important to incorporate into the simulator as accurate a transistor model as possible to approximate correctly the device behavior at the fundamental frequency, and at the second and higher harmonics of the operating frequency. Chapter 9 focuses on five CAD programs for analyzing the time-domain and frequency-domain behaviors of the switched-mode high-efficiency power amplifiers in frequency ranges from high frequencies to microwaves: HB-PLUS and SPICE CAD tools for Class-D and Class-DE circuits, and HEPA-PLUS, SPICE, and ADS CAD tools for Class-E circuits.

# Acknowledgments

The authors would like to express their sincere appreciation to:

Dr. Elena Stroganova from Moscow Technical University of Communications and Informatics, Russia, for help in collecting valuable historical information, encouragement, and support.

Dr. Herbert Jaeger from Danube Integrated Circuit Engineering (DICE), Austria, for joint successful work on the theoretical analysis and computer simulation, and design and development of parallel-circuit Class-E GaAs HBT power amplifiers for wireless applications.

Dr. Dmitry Prikhodko from Skyworks Solutions, U.S.A., for helpful discussions and contribution to the generalized Class E with finite dc-feed inductance by demonstrating a variety of solutions for load network parameters using computer-aided analysis.

Richard Frey from Microsemi (formerly Advanced Power Technology), U.S.A., for presenting the material about the design and development of a high-frequency 500-W Class-E power amplifier using a single plastic MOSFET.

Dr. Arturo Mediano from the University of Zaragoza, Spain, for presenting the material about PSPICE model describing the transistor switched-mode operation with the voltage-dependent output capacitance.

Mury Thian from Queen's University of Belfast, U.K., for help in finding typographical errors in mathematical equations.

Dr. Frederick H. Raab from Green Mountain Radio Research, Inc., U.S.A., for support and assistance with his basic papers regarding Class-F and Class-E operation modes.

Prof. Alan D. Sokal of New York University, U.S.A. and University College of London, U.K., for his joint conception of the Class-E power amplifier and his mathematical analysis of the circuit operation, and his reviews and suggestions on many of Nathan Sokal's subsequent published papers.

Finally, author Andrei Grebennikov especially wishes to thank his wife, Galina Grebennikova, for performing important numerical calculation and computer artwork design, and for her constant encouragement, inspiration, support, and assistance.

CHAPTER 1

# Power-Amplifier Design Principles

This introductory chapter presents the basic principles for understanding the power-amplifier's design procedures in principle. Based on the spectral-domain analysis, the concept of a conduction angle is introduced, by which the basic classes A, AB, B, and C of the power-amplifier operation are analyzed and illustrated in a simple and clear form. The frequency-domain analysis is less ambiguous because a relatively complex circuit often can be reduced to one or more sets of immittances at each harmonic component. The different nonlinear models for MOSFET, MESFET, HEMT, and bipolar junction devices including HBTs, which are very prospective for modern microwave monolithic-integrated circuits of power amplifiers, are given. The effects of the input-device parameters on the conduction angle at high frequencies is explained. The design and concept of push-pull amplifiers using balanced transistors are presented. The possibility of the maximum power gain for a stable power amplifier is discussed and analytically derived. Finally, the parasitic-parametric effect due to the nonlinear collector capacitance and measures for its cancellation in practical power amplifier are discussed.

## 1.1 Spectral-Domain Analysis

The best way to understand the electrical behavior of a power amplifier and the fastest way to calculate its basic electrical characteristics like output power, power gain, efficiency, stability, or harmonic suppression is to use a spectral-domain analysis. Generally, such an analysis is based on the determination of the output response of the nonlinear active device when applying the multi-harmonic signal to its input port, which analytically can be written in the form of

$$i(t) = f[v(t)], \tag{1.1}$$

where $i(t)$ is the output current, $v(t)$ is the input voltage, and $f(v)$ is the nonlinear transfer function of the device. Unlike the spectral-domain analysis, time-domain analysis establishes the relationships between voltage and current in each circuit element in the time domain when a system of equations is obtained by applying Kirchhoff's law to the circuit to be analyzed. Generally, such a system will be composed of nonlinear integro-differential equations in a nonlinear circuit. The solution to this system can be found by applying numerical-integration methods.

The voltage $v(t)$ in the frequency domain generally represents the multiple-frequency signal at the device input in the form of

$$v(t) = V_0 + \sum_{k=1}^{N} V_k \cos(\omega_k t + \phi_k), \tag{1.2}$$

where $V_0$ is the constant voltage, $V_k$ is the voltage amplitude, $\phi_k$ is the phase of the $k$-order harmonic component $\omega_k$, $k = 1, 2, \ldots, N$, and $N$ is the number of harmonics.

The spectral-domain analysis, based on substituting Eq. (1.2) into Eq. (1.1) for a particular nonlinear transfer function of the active device, determines the output spectrum as a sum of the fundamental-frequency and higher-order harmonic components, the amplitudes and phases of which will determine the output signal spectrum. Generally, it is a complicated procedure that requires a harmonic-balance technique to numerically calculate an accurate nonlinear circuit response. However, the solution can be found analytically in a simple way when it is necessary to only estimate the basic performance of a power amplifier in the form of the output power and efficiency. In this case, a technique based on a piecewise-linear approximation of the device transfer function can provide a clear insight into the basic behavior of a power amplifier and its operation modes. It can also serve as a good starting point for a final computer-aided design and optimization procedure.

The piecewise-linear approximation of the active device current-voltage transfer characteristic is a result of replacing the actual nonlinear dependence $i = f(v_{in})$, where $v_{in}$ is the voltage applied to the device input, by an approximated one that consists of the straight lines tangent to the actual dependence at the specified points. Such a piecewise-linear approximation for the case of two straight lines is shown in Fig. 1.1($a$).

The output-current waveforms for the actual current-voltage dependence (dashed curve) and its piecewise-linear approximation by two straight lines (solid curve) are plotted in Fig. 1.1($b$). Under large-signal operation mode, the waveforms corresponding to these two dependencies are practically the same for the most part, with negligible deviation for small values of the output current close to the pinch-off region of the device operation and significant deviation close to the saturation region of the device operation. However, the latter case results in a significant nonlinear distortion and is used only for high-efficiency operation modes when the active period of the device operation is minimized. Hence, at least two first output current components, dc and fundamental, can be calculated through a Fourier-series expansion with sufficient accuracy. Therefore, such a piecewise-linear approximation with two straight lines can be effective for a quick estimate of the output power and efficiency of the linear power amplifier.

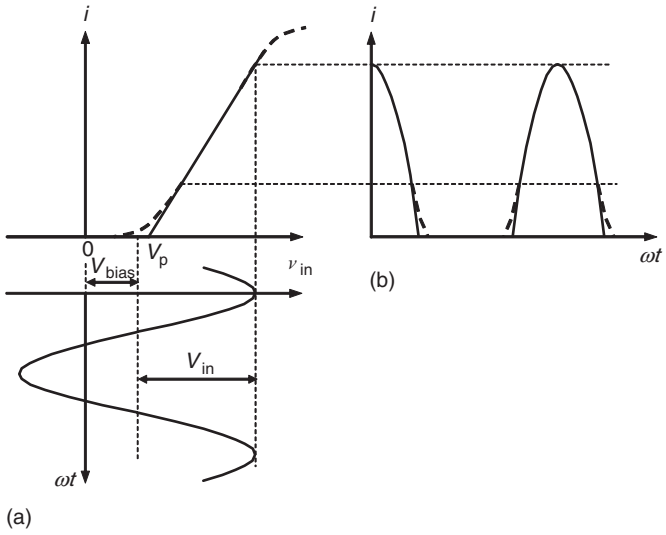



**Figure 1.1: Piecewise-linear approximation technique.**

In this case, the piecewise-linear active device current-voltage characteristic is defined by

$$i = \begin{cases} 0 & v_{in} \le V_p \\ g_m(v_{in} - V_p) & v_{in} \ge V_p, \end{cases} \tag{1.3}$$

where $g_m$ is the device transconductance, and $V_p$ is the pinch-off voltage.

Let us assume the input signal to be in a cosine form of

$$v_{in} = V_{bias} + V_{in} \cos \omega t, \tag{1.4}$$

where $V_{bias}$ is the input dc bias voltage.

At the point on the plot when voltage $v_{in}(\omega t)$ becomes equal to a pinch-off voltage $V_p$ and where $\omega t = \theta$, the output current $i(\theta)$ takes a zero value. At this moment,

$$V_p = V_{bias} + V_{in} \cos \theta \tag{1.5}$$

and $\theta$ can be calculated from

$$\cos \theta = -\frac{V_{bias} - V_p}{V_{in}}. \tag{1.6}$$

As a result, the output current represents a periodic pulsed waveform described by the cosinusoidal pulses with the maximum amplitude $I_{max}$ and width $2\theta$ as

$$i = \begin{cases} I_q + I\cos\omega t & -\theta \le \omega t < \theta \\ 0 & \theta \le \omega t < 2\pi - \theta, \end{cases} \tag{1.7}$$

where the conduction angle $2\theta$ indicates the part of the RF current cycle during which a device conduction occurs, as shown in Fig. 1.2. When the output current $i(\omega t)$ takes a zero value, one can write

$$i = I_q + I\cos\theta = 0. \tag{1.8}$$

Taking into account that, for a piecewise-linear approximation, $I = g_m V_{in}$, Eq. (1.7) can be rewritten for $i > 0$ by

$$i = g_m V_{in}(\cos\omega t - \cos\theta). \tag{1.9}$$

When $\omega t = 0$, then $i = I_{max}$ and

$$I_{max} = I(1 - \cos\theta). \tag{1.10}$$

The Fourier-series expansion of the even function when $i(\omega t) = i(-\omega t)$ contains only even components of this function and can be written as

$$i(\omega t) = I_0 + I_1\cos\omega t + I_2\cos 2\omega t + I_3\cos 3\omega t + \ldots \tag{1.11}$$

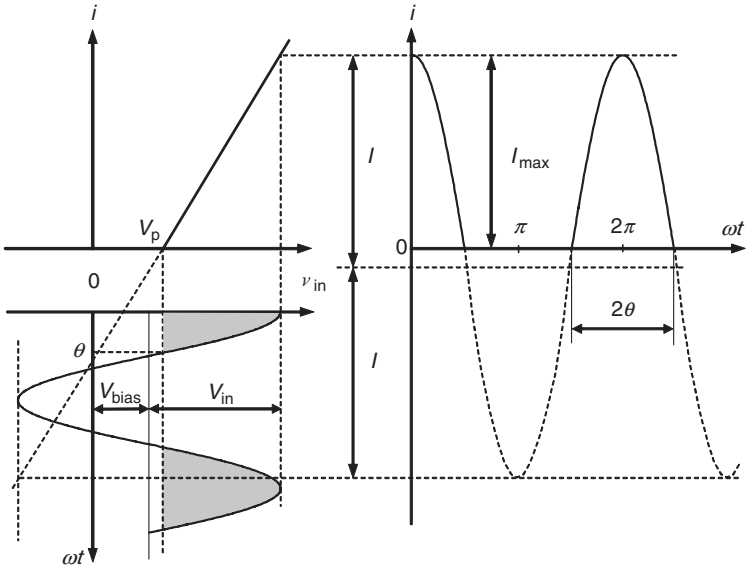



**Figure 1.2: Schematic definition of conduction angle.**

where the dc, fundamental-frequency, and $n$th harmonic components are calculated by

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} g_m V_{in}(\cos\omega t - \cos\theta)d(\omega t) = \gamma_0(\theta)I \tag{1.12}$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V_{in}(\cos\omega t - \cos\theta)\cos\omega t\, d(\omega t) = \gamma_1(\theta)I \tag{1.13}$$

$$I_n = \frac{1}{\pi}\int_{-\theta}^{\theta} g_m V_{in}(\cos\omega t - \cos\theta)\cos(n\omega t)d(\omega t) = \gamma_n(\theta)I, \tag{1.14}$$

where $\gamma_n(\theta)$ are called the coefficients of expansion of the output-current cosine waveform or the current coefficients [1]. They can be analytically defined as

$$\gamma_0(\theta) = \frac{1}{\pi}(\sin\theta - \theta\cos\theta) \tag{1.15}$$

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right) \tag{1.16}$$

$$\gamma_n(\theta) = \frac{1}{\pi}\left[\frac{\sin(n-1)\theta}{n(n-1)} - \frac{\sin(n+1)\theta}{n(n+1)}\right], \tag{1.17}$$

where $n = 2, 3, \ldots$.

The dependencies of $\gamma_n(\theta)$ for the dc, fundamental-frequency, second and higher-order current components are shown in Fig. 1.3. The maximum value of $\gamma_n(\theta)$ is achieved when $\theta = 180°/n$. Special case is $\theta = 90°$, when odd current coefficients are equal to zero, that is $\gamma_3(\theta) = \gamma_5(\theta) = \ldots = 0$. The ratio between the fundamental-frequency and dc components $\gamma_1(\theta)/\gamma_0(\theta)$ varies from 1 to 2 for any values of the conduction angle, with a minimum value of 1 for $\theta = 180°$ and a maximum value of 2 for $\theta = 0°$. It is necessary to pay attention to the fact that, for example, the current coefficient $\gamma_3(\theta)$ becomes negative within the interval of $90° < \theta < 180°$. This implies the proper phase changes of the third current harmonic component when its values are negative. Consequently, if the harmonic components, for which $\gamma_n(\theta) > 0$, achieve positive maximum values at the time moments corresponding to the middle points of the current waveform, the harmonic components, for which $\gamma_n(\theta) < 0$, can achieve negative maximum values at these same time moments. As a result, the combination of different harmonic components with proper loading will result in flattening of the current or voltage waveforms, thus improving efficiency of the power amplifier. The amplitude of corresponding current harmonic component can be obtained by

$$I_{\mathrm{n}} = \gamma_{\mathrm{n}}(\theta) g_{\mathrm{m}} V_{\mathrm{in}} = \gamma_{\mathrm{n}}(\theta) I. \tag{1.18}$$

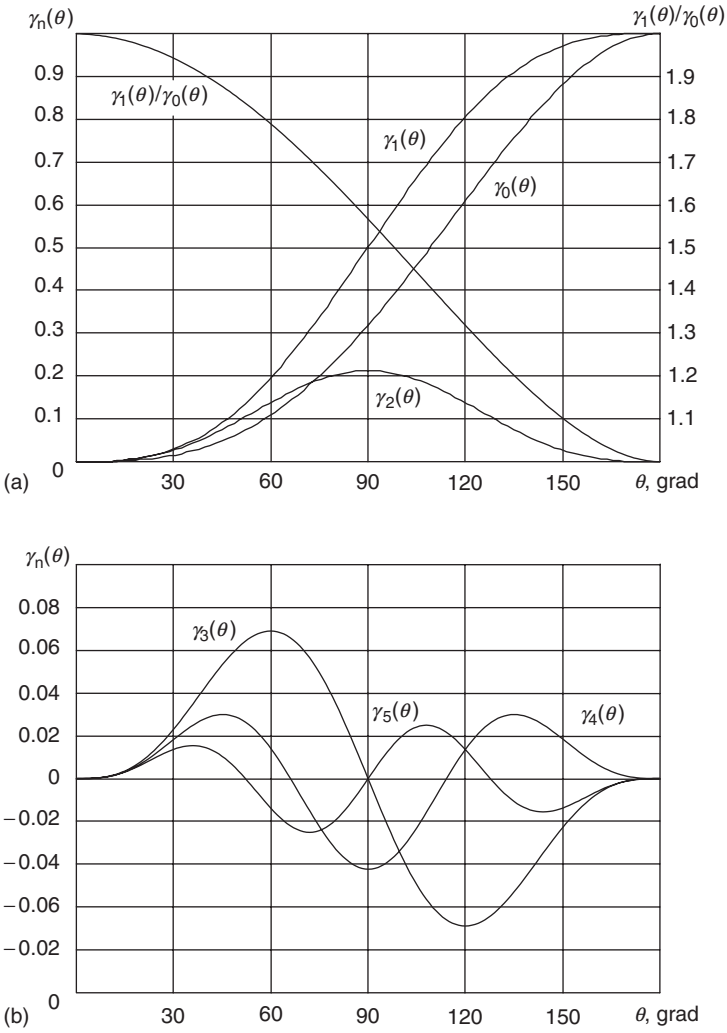



**Figure 1.3: Dependencies of $\gamma_{\mathrm{n}}(\theta)$ for dc, fundamental and higher-order current components.**

Sometimes it is necessary for an active device to provide a constant value of $I_{\max}$ at any values of $\theta$. This requires an appropriate variation of the input voltage amplitude $V_{\mathrm{in}}$. In this case, it is more convenient to use the other coefficients when the $n$th current harmonic amplitude $I_{\mathrm{n}}$ is related to the maximum current waveform amplitude $I_{\max}$, that is

$$\alpha_{\mathrm{n}} = \frac{I_{\mathrm{n}}}{I_{\max}}. \tag{1.19}$$

From Eqs. (1.10), (1.18), and (1.19), it follows that

$$\alpha_n = \frac{\gamma_n(\theta)}{1-\cos\theta}, \tag{1.20}$$

and maximum value of $\alpha_n(\theta)$ is achieved when $\theta = 120^\circ/n$.

## 1.2 Basic Classes of Operation: A, AB, B, and C

To determine the operation classes of the power amplifier, consider a simple resistive stage shown in Fig. 1.4, where $L_{ch}$ is the ideal choke inductor with zero series resistance and infinite reactance at the operating frequency, $C_b$ is the dc-blocking capacitance with infinite value having zero reactance at the operating frequency, and $R$ is the load resistance. The dc supply voltage $V_{cc}$ is applied to both plates of the dc-blocking capacitor, being constant during the entire signal period. The active device behaves as an ideal voltage-controlled current source having zero saturation resistance.

For an input cosine voltage given by Eq. (1.4), the operating point must be fixed at the middle point of the linear part of the device transfer characteristic with $V_{in} \le V_{bias} - V_p$, where $V_p$ is the device pinch-off voltage. Normally, to simplify an analysis of the power-amplifier operation, the device transfer characteristic is represented by a piecewise-linear approximation. As a result, the output current is cosinusoidal,

$$i = I_q + I\cos\omega t \tag{1.21}$$

with the quiescent current $I_q$ greater or equal to the collector current amplitude $I$. In this case, the output collector current contains only two components—dc and cosine—and the averaged current magnitude is equal to a quiescent current $I_q$.

The output voltage $v$ across the device collector represents a sum of the dc supply voltage $V_{cc}$ and cosine voltage $v_R$ across the load resistance $R$. Consequently, the greater output current $i$, the greater voltage $v_R$ across the load resistance $R$ and the smaller output voltage $v$. Thus, for a purely real load impedance when $Z_L = R$, the collector voltage $v$ is shifted by $180^\circ$ relative to the input voltage $v_{in}$ and can be written as

$$v = V_{cc} + V\cos(\omega t + 180^\circ) = V_{cc} - V\cos\omega t, \tag{1.22}$$

where $V$ is the output voltage amplitude.

Substituting Eq. (1.21) into Eq. (1.22) yields

$$v = V_{cc} - \left(i - I_q\right)R. \tag{1.23}$$

Eq. (1.23) can be rewritten in the form of

$$i = \left(I_q + \frac{V_{cc}}{R}\right) - \frac{v}{R}, \tag{1.24}$$

which determines a linear dependence of the collector current versus collector voltage. Such a combination of the cosine collector voltage and current waveforms is known as a Class-A operation mode. In real practice, because of the device nonlinearities, it is necessary to connect a parallel LC circuit with resonant frequency equal to the operating frequency to suppress any possible harmonic components.

Circuit theory prescribes that the collector efficiency $\eta$ can be written as

$$\eta = \frac{P}{P_0} = \frac{1}{2}\frac{I}{I_q}\frac{V}{V_{cc}} = \frac{1}{2}\frac{I}{I_q}\xi, \tag{1.25}$$

where

$$P_0 = I_q V_{cc} \tag{1.26}$$

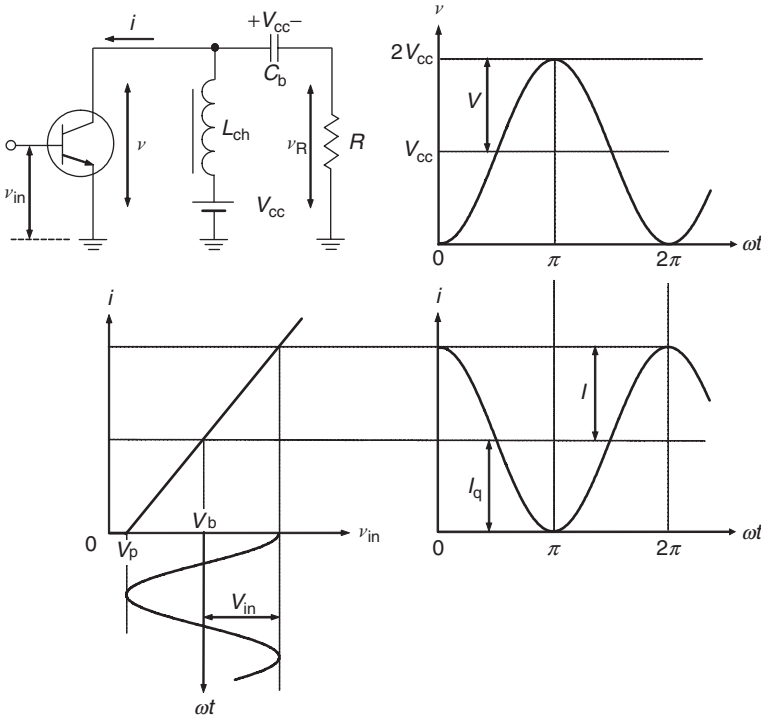



**Figure 1.4: Voltage and current waveforms in Class-A operation.**

is the dc output power,

$$P = \frac{IV}{2} \tag{1.27}$$

is the power delivered to the load resistance $R$ at the fundamental frequency $f_0$, and

$$\xi = \frac{V}{V_{cc}} \tag{1.28}$$

is the collector voltage peak factor.

Then, by assuming the ideal conditions of zero saturation voltage when $\xi = 1$ and maximum output current amplitude when $I/I_q = 1$, from Eq. (1.25) it follows that the maximum collector efficiency in a Class-A operation mode is equal to

$$\eta = 50\%. \tag{1.29}$$

However, as it follows from Eq. (1.25), increasing the value of $I/I_q$ can further increase the collector efficiency. This leads to a step-by-step nonlinear transformation of the current cosine

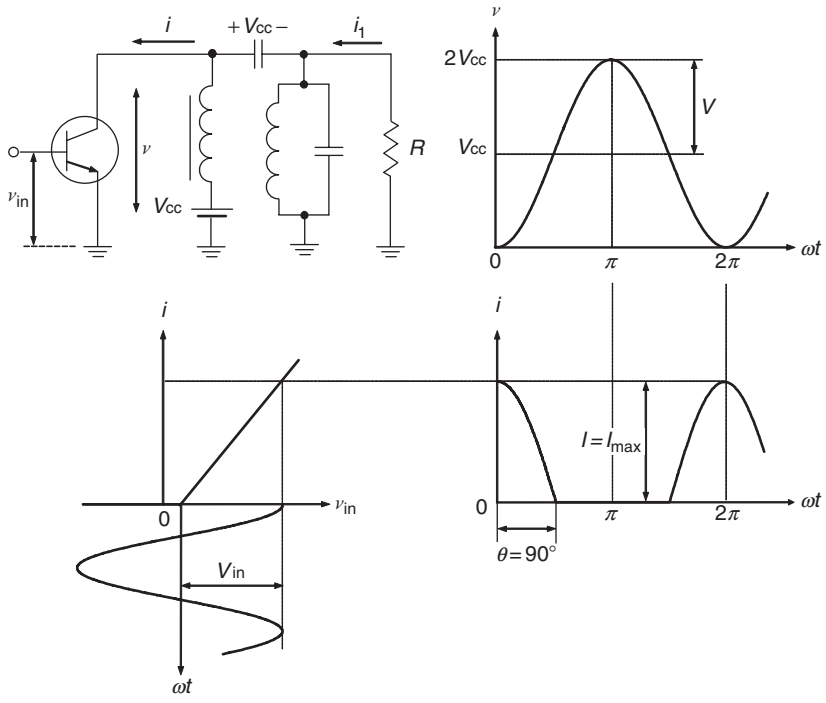



**Figure 1.5: Voltage and current waveforms in Class-B operation.**

waveform to its pulsed waveform when the magnitude of the collector current exceeds zero value during only a part of the entire signal period. In this case, an active device is operated in the active region followed by the operation in the pinch-off region when the collector current is zero, as shown in Fig. 1.5. As a result, the frequency spectrum at the device output will generally contain the second, third, and higher-order harmonics of the fundamental frequency. However, due to high quality factor of the parallel resonant LC circuit, only the fundamental-frequency signal is flowing into the load, while the short-circuit conditions are fulfilled for higher-order harmonic components. Therefore, ideally the collector voltage represents a purely sinusoidal waveform with the voltage amplitude $V \leq V_{cc}$.

Eq. (1.8) for the output current can be rewritten through the ratio between a quiescent current $I_q$ and a current amplitude $I$ as

$$\cos\theta = -\frac{I_q}{I}. \tag{1.30}$$

As a result, the basic definitions for nonlinear operation modes of a power amplifier through half the conduction angle can be introduced as

- When $\theta > 90^\circ$, then $\cos\theta < 0$ and $I_q > 0$ corresponding to Class-AB operation.
- When $\theta = 90^\circ$, then $\cos\theta = 0$ and $I_q = 0$ corresponding to Class-B operation.
- When $\theta < 90^\circ$, then $\cos\theta > 0$ and $I_q < 0$ corresponding to Class-C operation.

The periodic pulsed output current $i(\omega t)$ can be represented as a Fourier-series expansion

$$i(\omega t) = I_0 + I_1\cos\omega t + I_2\cos 2\omega t + I_3\cos 3\omega t + \ldots \tag{1.31}$$

where the dc and fundamental-frequency components can be obtained from

$$I_0 = \frac{1}{2\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)d(\omega t) = I\gamma_0, \tag{1.32}$$

$$I_1 = \frac{1}{\pi}\int_{-\theta}^{\theta} I(\cos\omega t - \cos\theta)\cos\omega t\, d(\omega t) = I\gamma_1, \tag{1.33}$$

respectively, where

$$\gamma_0 = \frac{1}{\pi}(\sin\theta - \theta\cos\theta) \tag{1.34}$$

$$\gamma_1 = \frac{1}{\pi}(\theta - \sin\theta\cos\theta). \tag{1.35}$$

From Eq. (1.32) it follows that the dc current component is a function of $\theta$ in the operation modes with $\theta < 180^\circ$, in contrast to a Class-A operation mode where $\theta = 180^\circ$ and the dc current is equal to the quiescent current during the entire period.

The collector efficiency of a power amplifier with resonant circuit, biased to operate in the nonlinear modes, can be obtained from

$$\eta = \frac{P_1}{P_0} = \frac{1}{2}\frac{I_1}{I_0}\xi = \frac{1}{2}\frac{\gamma_1}{\gamma_0}\xi. \tag{1.36}$$

If $\xi = 1$ and $\theta = 90^\circ$, then from Eqs. (1.34) and (1.35) it follows that the maximum collector efficiency in a Class-B operation mode is equal to

$$\eta = \frac{\pi}{4} \cong 78.5\%. \tag{1.37}$$

The fundamental-frequency power delivered to the load, $P_L = P_1$, is defined by

$$P_1 = \frac{VI_1}{2} = \frac{VI\gamma_1(\theta)}{2}, \tag{1.38}$$

showing its direct dependence on the conduction angle $2\theta$. This means that reduction in $\theta$ results in lower $\gamma_1$, and to increase fundamental-frequency power $P_1$, it is necessary to increase the current amplitude $I$. Since the current amplitude $I$ is determined by the input voltage amplitude $V_{in}$, the input power $P_{in}$ must be increased. The collector efficiency also increases with reduced value of $\theta$ and becomes maximum when $\theta = 0^\circ$ where a ratio of $\gamma_1/\gamma_0$ is maximal, as follows from Fig. 1.3(*a*). For example, the collector efficiency $\eta$ increases from 78.5% to 92% when $\theta$ reduces from 90° to 60°. However, it requires increasing the input voltage amplitude $V_{in}$ by 2.5 times resulting in a lower value of the power-added efficiency (*PAE*), which is defined as

$$PAE = \frac{P_1 - P_{in}}{P_0} = \frac{P_1}{P_0}\left(1 - \frac{1}{G_p}\right), \tag{1.39}$$

where

$$G_p = \frac{P_1}{P_{in}}$$

is the operating power gain.

Consequently, to obtain an acceptable trade-off between a high power gain and a high power-added efficiency in different situations, the conduction angle should be chosen within the range of $120^\circ \leq 2\theta \leq 190^\circ$. If it is necessary to provide high collector efficiency of the active device having a high gain capability, it is necessary to choose a Class-C operation mode with $\theta$ close to $60^\circ$. However, when the input power is limited and power gain is not sufficient, it is recommended to choose a Class-AB operation mode with small quiescent current when $\theta$ is slightly greater than $90^\circ$. In the latter case, the linearity of the power amplifier can be significantly improved.

Since the parallel LC circuit is tuned to the fundamental frequency, the voltage across the load resistor $R$ can be considered cosinusoidal. By using Eqs. (1.7), (1.22), and (1.30), the relationship between the collector current $i$ and voltage $v$ during a time period of $-\theta \leq \omega t < \theta$ can be expressed by

$$i = \left(I_{\mathrm{q}} + \frac{V_{\mathrm{cc}}}{\gamma_1 R}\right) - \frac{v}{\gamma_1 R}, \tag{1.40}$$

where the fundamental current coefficient $\gamma_1$ as a function of $\theta$ is determined by Eq. (1.35), and the load resistance is defined by $R = V/I_1$ where $I_1$ is the fundamental current amplitude. Eq. (1.40) determining the dependence of the collector current on the collector voltage for any values of conduction angle in the form of a straight line function is called the load line of the active device. For a Class-A operation mode with $\theta = 180^\circ$ when $\gamma_1 = 1$, Eq. (1.40) is identical to Eq. (1.24).

Fig. 1.6 shows the idealized active device output *I-V* curves and load lines for different conduction angles according to Eq. (1.40) with the corresponding collector and current waveforms. From Fig. 1.6 it follows that the maximum collector current amplitude $I_{\max}$ corresponds to the minimum collector voltage $V_{\mathrm{sat}}$ when $\omega t = 0$, and is the same for any conduction angle. The slope of the load line defined by its slope angle $\beta$ is different for the different conduction angles and values of the load resistance, and can be obtained by

$$\tan\beta = \frac{I}{V(1-\cos\theta)} = \frac{1}{\gamma_1 R}, \tag{1.41}$$

from which it follows that the greater slope angle $\beta$ of the load line, the smaller value of the load resistance $R$ for the same $\theta$.

In general, the entire load line represents a broken line *PK* including a horizontal part, as shown in Fig. 1.6. Fig. 1.6(*a*) represents a load line *PNK* corresponding to a Class-AB mode with $\theta > 90^\circ$, $I_{\mathrm{q}} > 0$, and $I < I_{\max}$. Such a load line moves from point *K* corresponding to the maximum output-current amplitude $I_{\max}$ at $\omega t = 0$ and determining the device saturation voltage $V_{\mathrm{sat}}$ through the point *N* located at the horizontal axis $v$ where $i = 0$ and $\omega t = \theta$. For a

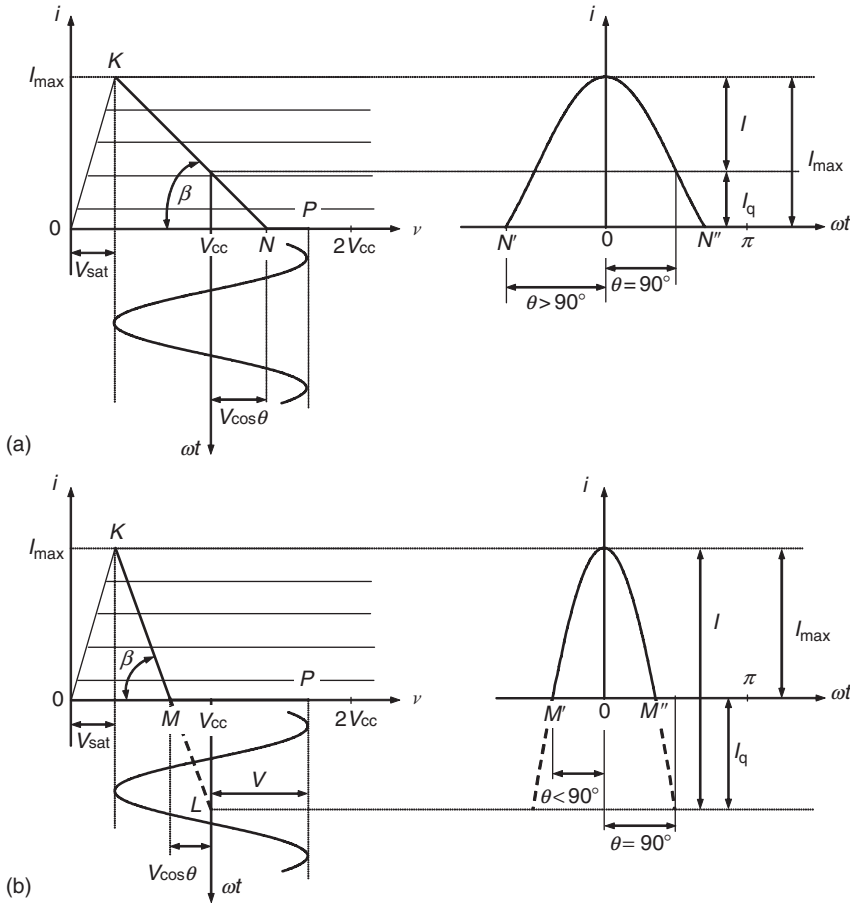



**Figure 1.6: Collector voltage and current waveforms in Class-AB and Class-C operations.**

Class-AB operation, the conduction angle for the output-current pulse between points $N'$ and $N''$ is greater than 180°. Fig. 1.6(*b*) represents a load line *PMK* corresponding to a Class-C mode with $\theta < 90°$, $I_q < 0$, and $I > I_{max}$. For a Class-C operation, the load line intersects a horizontal axis $v$ in a point $M$, and the conduction angle for the output-current pulse between points $M'$ and $M''$ is smaller than 180°. Hence, generally the load line represents a broken line with the first section having a slope angle $\beta$ and another horizontal section with zero current $i$. In a Class-B mode, the collector current represents half-cosine pulses with the conduction angle of $2\theta = 180°$ and $I_q = 0$.

Now let us consider a Class-B operation with increased amplitude of the cosine collector voltage. In this case, as shown in Fig. 1.7, an active device is operated in the saturation, active, and pinch-off regions, and the load line represents a broken line *LKMP* with three linear sections (*LK*, *KM*, and *MP*). The new section *KL* corresponds to the saturation region

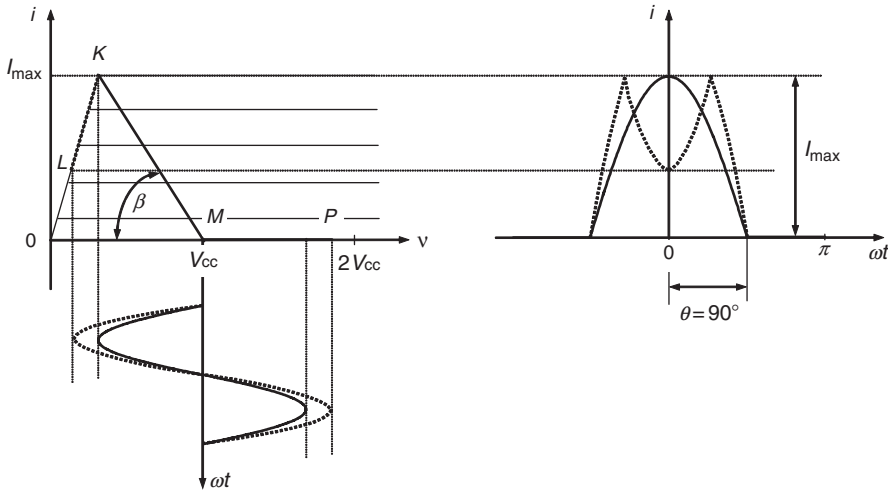



**Figure 1.7: Collector voltage and current waveforms for the device operating in saturation, active, and pinch-off regions.**

resulting in the half-cosine output-current waveform with a depression in the top part. With further increase of the output-voltage amplitude, the output-current pulse can be split into two symmetrical pulses containing a significant level of the higher-order harmonic components. The same result can be achieved by increasing a value of the load resistance $R$ when the load line is characterized by smaller slope angle $\beta$.

The collector current waveform becomes asymmetrical for the complex load, the impedance of which represents the load resistance and capacitive or inductive reactances. In this case, the Fourier expansion of the output current given by Eq. (1.31) includes a particular phase for each harmonic component. Then, the output voltage at the device collector is written by

$$v = V_{cc} - \sum_{n=1}^{\infty} I_n |Z_n| \cos(n\,\omega t + \phi_n), \tag{1.42}$$

where $I_n$ is the amplitude of $n$th output-current harmonic component, $|Z_n|$ is the magnitude of the load network impedance at $n$th output-current harmonic component, and $\phi_n$ is the phase of $n$th output-current harmonic component. Assuming that $Z_n$ is zero for $n = 2, 3, \ldots$, which is possible for a resonant load network having negligible impedance at any harmonic component except the fundamental, Eq. (1.42) can be rewritten as

$$v = V_{cc} - I_1 |Z_1| \cos(\omega t + \phi_1). \tag{1.43}$$

As a result, for the inductive load impedance, the depression in the collector current waveform reduces and moves to the left side of the waveform, whereas the capacitive load impedance

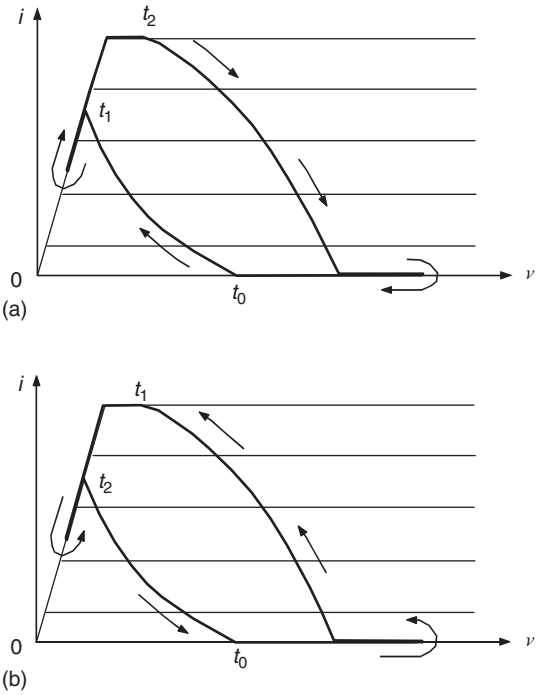



**Figure 1.8: Load lines for (*a*) inductive and (*b*) capacitive load impedances.**

causes the depression to deepen and shift to the right side of the collector current waveform [2]. This effect can simply be explained by the different phase conditions for fundamental and higher-order harmonic components composing the collector current waveform and is illustrated by the different load lines for (*a*) inductive and (*b*) capacitive load impedances shown in Fig. 1.8. Note that now the load line represents a two-dimensional curve with a complicated behavior.

## 1.3 Active Device Models

Normally, for an accurate power-amplifier circuit design and simulation in a frequency bandwidth and over high dynamic range of the output power, it is necessary to represent an active device in the form of a nonlinear equivalent circuit, which can adequately describe the electrical behavior of the power amplifier close to the device transition frequency $f_T$ and maximum frequency $f_{max}$, to take into account the sufficient number of harmonic components. Accurate device modeling is extremely important to develop monolithic integrated circuits. Better approximations of the final design can only be achieved if the nonlinear device behavior is described accurately.

Fig. 1.9(*a*) shows the nonlinear MOSFET equivalent circuit with the extrinsic parasitic elements [3, 4]. The nonlinear current source $i(v_{gs}, v_{ds}, \tau)$ as a function of the input gate-source and output drain-source voltages incorporating self-heating effect can be described sufficiently simple and accurate using hyperbolic functions [4, 5]. Careful analytical description of the transition from quadratic to linear regions of the device transfer characteristic enables the more accurate prediction of the intermodulation distortion [6]. The overall channel carrier transit time $\tau$ also includes an effect of the transcapacitance required for charge conservation. The drain-source capacitance $C_{ds}$ and gate-drain capacitance $C_{gd}$ are considered as the junction capacitances that strongly depend on the drain-source voltage. The gate-source capacitance $C_{gs}$ can be described as a function of the gate-source voltage. It is equal to the oxide capacitance in accumulation region, slightly decreases in the weak-inversion region, significantly reduces in the moderate-inversion region, and then becomes practically constant in the strong-inversion or saturation region. The extrinsic parasitic elements are represented by the gate bondwire and lead inductance $L_g$, the extrinsic contact and ohmic gate resistance $R_g$, the source bulk and ohmic resistance $R_s$, the source lead

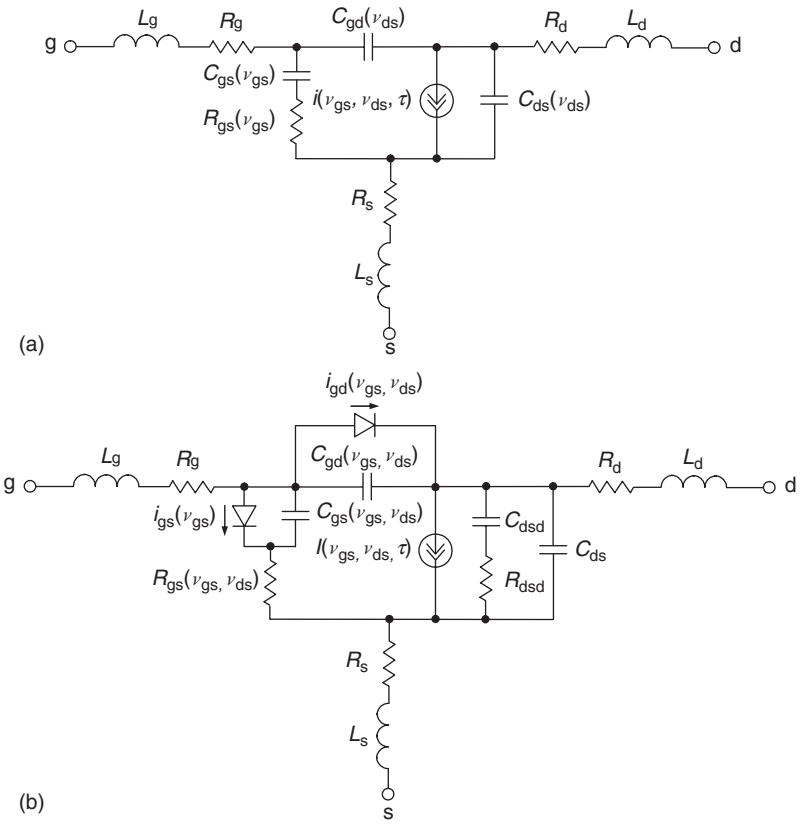



**Figure 1.9: Nonlinear MOSFET and MESFET models with extrinsic linear elements.**

inductance $L_s$, the drain bulk and ohmic resistance $R_d$, and the drain bondwire and lead inductance $L_d$. The effect of the gate-source channel resistance $R_{gs}$ becomes significant at higher frequencies close to $f_T$.

Adequate representation for MESFETs and HEMTs in a frequency range up to at least 25 GHz can be provided using a nonlinear model shown in Fig. 1.9(*b*), which is very similar to a nonlinear MOSFET model [4, 7]. The intrinsic model is described by the channel charging resistance $R_{gs}$, which represents the resistive path for the charging of the gate-source capacitance $C_{gs}$, the feedback gate-drain capacitance $C_{gd}$, the drain-source capacitance $C_{ds}$, the gate-source diode to model the forward conduction current $i_{gs}(v_{gs})$, and the gate-drain diode to account for the gate-drain avalanche current $i_{gd}(v_{gs},v_{ds})$, which can occur for large-signal operation conditions. The gate-source capacitance $C_{gs}$ and gate-drain capacitance $C_{gd}$ represent the charge depletion region and can be treated as the voltage-dependent Schottky-barrier diode capacitances, being the nonlinear functions of the gate-source voltage $v_{gs}$ and drain-source voltage $v_{ds}$. For negative gate-source voltage and small drain-source voltage, these capacitances are practically equal. However, when the drain-source voltage is increased beyond the current saturation point, the gate-drain capacitance $C_{gd}$ is much more heavily back-biased than the gate-source capacitance $C_{gs}$. Therefore, the gate-source capacitance $C_{gs}$ is significantly more important and usually dominates the input impedance of the MESFET device. The influence of the drain-source capacitance $C_{ds}$ on the device behavior is insignificant and its value is bias independent. The capacitance $C_{dsd}$ and resistance $R_{dsd}$ model the dispersion of the MESFET or HEMT current-voltage characteristics due to a trapping effect in the device channel, which leads to discrepancy between dc measurement and *S*-parameter measurements at high frequencies [8, 9]. A large-signal model for monolithic power-amplifier design should be accurate for all operating conditions. In addition, the model parameters should be easily extractable and the model must be as simple as possible. Various nonlinear MESFET and HEMT models with different complexity are available, however each can be considered sufficiently accurate for a particular application. For example, although the Materka model does not fulfill charge conservation, it seems to be an acceptable compromise between accuracy and model simplicity for MESFETs, but not for HEMTs, where it is preferable to use the Angelov model [10, 11].

Fig. 1.10(*a*) shows the modified Gummel-Poon nonlinear model of the bipolar transistor with extrinsic parasitic elements [12, 13]. This hybrid-$\pi$ equivalent circuit can model the nonlinear electrical behavior of bipolar transistors, in particularly HBT devices, with sufficient accuracy up to about 20 GHz. The intrinsic model is described by the dynamic diode resistance $r_\pi$, the total base-emitter junction capacitance and base charging diffusion capacitance $C_\pi$, the base-collector diode required to account for the nonlinear effects at the saturation, the internal collector-base junction capacitance $C_{ci}$, the external distributed collector-base capacitance $C_{co}$, the collector-emitter capacitance $C_{ce}$, and the nonlinear current source $i(v_{be},v_{ce})$.

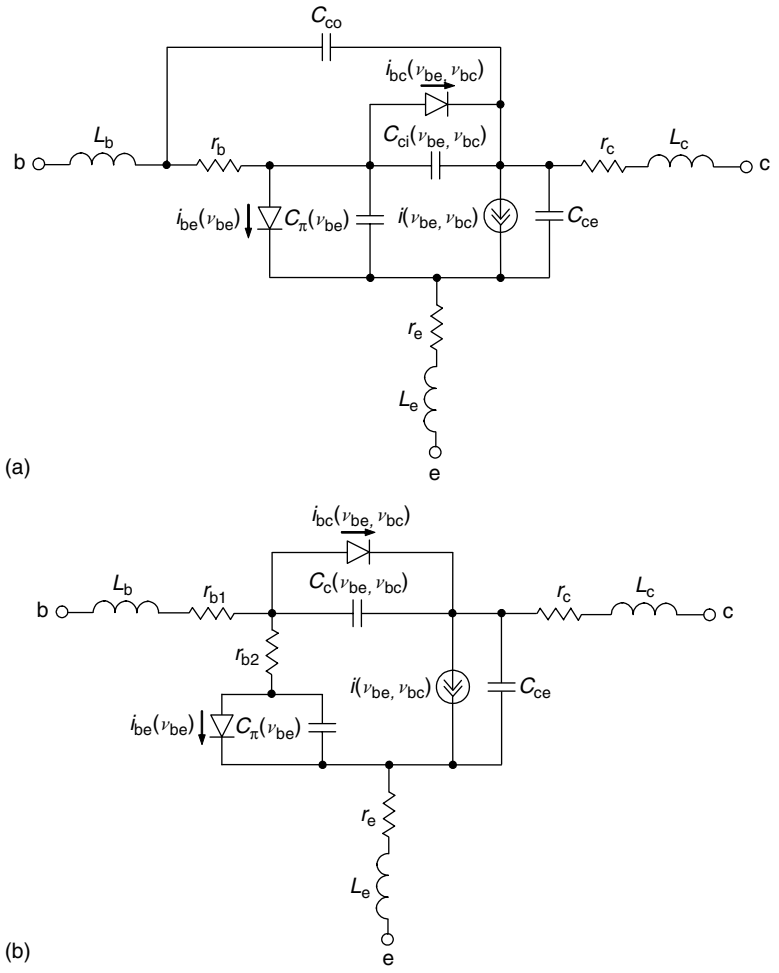



**Figure 1.10: Nonlinear BJT and HBT models with extrinsic linear elements.**

The lateral resistance and the base semiconductor resistance underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance $r_b$. The extrinsic parasitic elements are represented by the base bondwire and lead inductance $L_b$, the emitter ohmic resistance $r_e$, the emitter lead inductance $L_e$, the collector ohmic resistance $r_c$, and the collector bondwire and lead inductance $L_c$. The more complicated models, such as VBIC, HICUM, or MEXTRAM, include the effects of self-heating of a bipolar transistor, take into account the parasitic *p-n-p* transistor formed by the base, collector, and substrate regions, provide an improved description of depletion capacitances at large forward bias, and take into account avalanche and tunneling currents and other nonlinear effects corresponding to distributed high-frequency effects [14].

Fig. 1.10(*b*) shows a modified version of the bipolar transistor equivalent circuit, where $C_c = C_{co} + C_{ci}$, $r_{b1} = r_b C_{ci}/C_c$, $r_{b2} = r_b C_{co}/C_c$ [15]. This equivalent circuit becomes possible due to an equivalent π-to-*T* transformation of the elements $r_b$, $C_{co}$, and $C_{ci}$ and a condition $r_b << (C_{ci} + C_{co})/\omega C_{ci} C_{co}$, which is usually fulfilled over a frequency range close to the device maximum frequency $f_{max}$. Then, from a comparison of the transistor nonlinear models, for a bipolar transistor shown in Fig. 1.10(*b*) and for the MOSFET or MESFET devices shown in Fig. 1.9, it is clear to see the circuit similarity of all these equivalent circuits, which means that the basic circuit design procedure is very similar for any type of bipolar or field-effect transistors. The difference is in the device physics and values of the model parameters. However, techniques for the representation of the input and output impedances, stability analysis based on the feedback effect, derivation of power gain, and efficiency, are very similar.

Fig. 1.11(*a*) shows the equivalent representation of the MOSFET input circuit derived from Fig. 1.9(*a*), where $\tau_g = C_{gs} R_{gs}$, $g_m(\theta)$ is the large-signal transconductance as a function of one-half the conduction angle $\theta$, and $R_L$ is the load resistance connected to the drain-source port. It is assumed that the series source resistance $R_s$, lead inductance $L_s$, and transit time $\tau$ are sufficiently small for high-power MOSFETs in a frequency range up to $f \leq 0.3 f_T$, $R_L >> R_d$, and the device drain-source capacitance $C_{ds}$ is inductively compensated. As a result, the equivalent input circuit shown in Fig. 1.11(*a*) can be significantly simplified to an equivalent

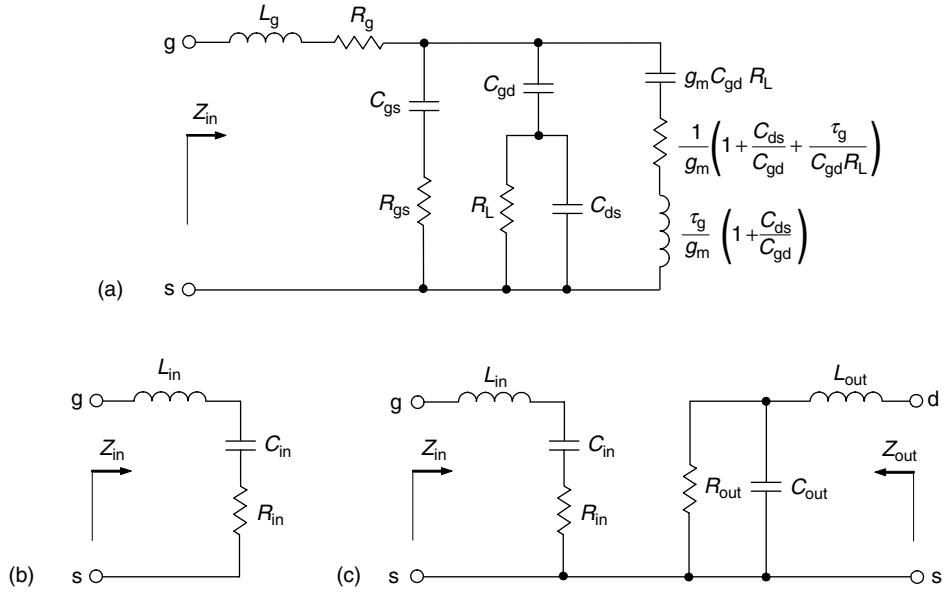



**Figure 1.11: Equivalent circuits characterizing device input and output.**

input circuit shown in Fig. 1.11(*b*) with the input inductance $L_{in} = L_g$, resistance $R_{in}$, and capacitance $C_{in}$ connected in series and defined by

$$R_{in} \cong R_g + R_{gs}, \tag{1.44}$$

$$C_{in} \cong C_{gs} + C_{gd}\,(1 + g_m R_L). \tag{1.45}$$

Taking into account that usually $C_{gd} << C_{gs}$, the device equivalent output circuit can be represented by the series inductance $L_{out} = L_d$ and a parallel connection of the equivalent output resistance $R_{out}$ and output capacitance $C_{out}$, as shown in Fig. 1.11(*c*), which are defined by

$$R_{out} = \frac{V}{I_1}, \tag{1.46}$$

$$C_{out} \cong C_{ds} + C_{gd}, \tag{1.47}$$

where $V$ is the amplitude of the output cosine voltage given by Eq. (1.22), and $I_1$ is the fundamental amplitude of the output current given by Eq. (1.33). The term ''equivalent output resistance'' means that, in order to provide a maximum power delivery to the load for the specified conduction angle and supply voltage, the device nonlinear current source must see the load at the fundamental frequency which value is defined by Eq. (1.46). In this case, the impedance at the harmonic components is negligibly small provided by a parallel resonant circuit. However, due to the effect of the second and higher-order harmonic components, the output current will have zero values when output voltage is positive, thus improving efficiency.

In the case of a bipolar transistor, since $C_{ce}$ is usually much smaller than $C_c$, the equivalent output capacitance can be defined as $C_{out} \cong C_c$. The input equivalent $R_{in}$ can approximately be represented by the base resistance $r_b$, while the input equivalent capacitance can be defined as $C_{in} \cong C_\pi + C_c$. The feedback effect of the collector capacitance $C_c$ through $C_{c0}$ and $C_{ci}$ is sufficiently high when load variations are directly transferred to the device input with a significant extent.

## 1.4 High-Frequency Conduction Angle

An idealized analysis of the physical processes in the nonlinear power amplifier based on the cosinusoidal input signal can be considered sufficiently accurate only at low frequencies when all phase delays due to the effect of the elements of the device equivalent circuit is neglected and it is represented as an ideal voltage- or current-control current source. However, as it is seen in Figs. 1.9 and 1.10, the electrical behavior of the transistor over its entire operating frequency range is described by the sufficiently complicated equivalent circuit, including

linear and nonlinear internal and external parasitic elements. The bipolar transistor linear operation at low and medium frequencies up to approximately $(0.1–0.2)f_T$, where $f_T$ is the transition frequency, can be adequately characterized by a Giacoletto equivalent circuit shown in Fig. 1.12(*a*) [16]. In a linear small-signal mode, all elements of the device equivalent circuit are considered constant, including the base-emitter diffusion capacitance $C_d$ and differential resistance $r_\pi$. To analyze device behavior in a large-signal mode when device is operated in the pinch-off and active regions, it is necessary to compose two equivalent circuits: the first should correspond to a linear-active region shown in Fig. 1.12(*b*), and the other corresponding to a pinch-off region as shown in Fig. 1.12(*c*). It is necessary to take into account that the capacitance $C_d$ and resistance $r_\pi$ depend significantly on the driving signal amplitude by setting their averaged values in an active mode. The external feedback capacitance $C_{co}$ can be included to external circuitry.

By applying a piecewise-linear approximation of the transistor transfer current-voltage characteristic, the current $i$ as a function of the driving junction voltage $v$ can be written as

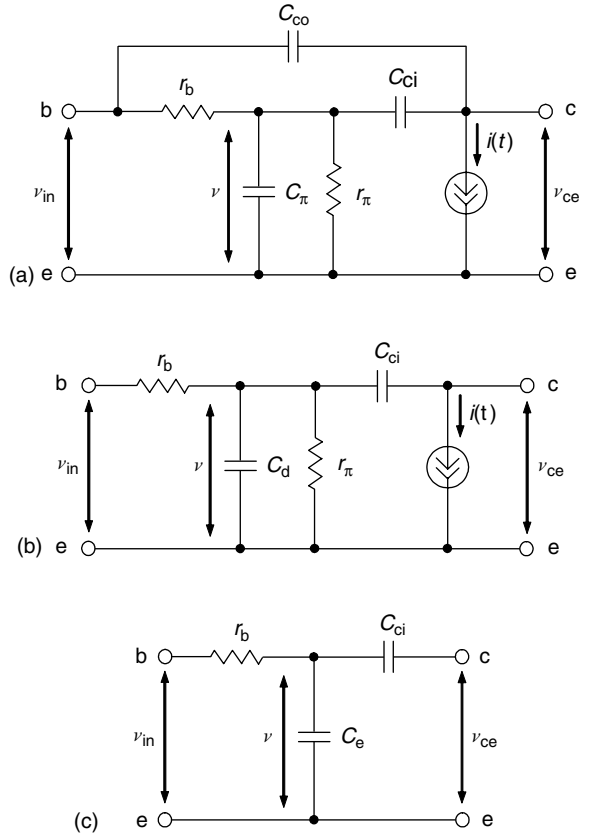



**Figure 1.12: Giacoletto model for bipolar transistor.**

$$i(v) = \begin{cases} g_m(v - V_p) & v \geq V_p \\ 0 & v < V_p, \end{cases} \tag{1.48}$$

while the input driving signal applied to the device input port is defined by

$$v_{in}(\omega t) = V_p + V_{in}(\cos \omega t - \cos \theta). \tag{1.49}$$

Let us assume that the current flowing through the internal feedback capacitance $C_{ci}$ is sufficiently small and its effect can be neglected. Then, to compose the differential equation describing the device behavior in an active mode, we can write

$$\frac{v_{in} - v}{r_b} = \frac{v}{r_d} + \omega C_d \frac{dv}{d\omega t}. \tag{1.50}$$

As a result, for $v \geq V_p$, the transistor behavior can be described by the following first-order linear differential equation:

$$\omega \tau_1 \frac{dv}{d\omega t} + v = kV_p - kV_{in}(\cos \omega t - \cos \theta), \tag{1.51}$$

where $\tau_1 = r_b k C_d$ and $k = r_\pi/(r_b + r_\pi)$.

Similarly, for $v < V_p$,

$$\omega \tau_2 \frac{dv}{d\omega t} + v = V_p - V_{in}(\cos \omega t - \cos \theta), \tag{1.52}$$

where $\tau_2 = r_b c_e$.

Depending on the bipolar transistor type, the ratio between the differential capacitance $C_d$ and junction capacitance $C_e$ can be different. In most cases when $C_d$ is greater than $C_e$ by an order, the effect of the junction capacitance $C_e$ can be neglected for analysis simplicity. Then, assuming that $\tau_2 = 0$, Eq. (1.52) can be rewritten as

$$v = V_p - V_{in}(\cos \omega t - \cos \theta), \tag{1.53}$$

which means that the input driving signal is applied to the device junction without any changes in its voltage shape during a pinch-off mode.

Thus, the solution of Eq. (1.51) in time domain for an initial condition of $v(-\theta) = V_p$ can be obtained in the form of

$$v = V_{\mathrm{p}} + V_{\mathrm{in}} \cos\phi_1 \left\{ \cos(\omega t + \phi_1) - \frac{\cos\theta}{\cos\phi_1} \right.$$

$$\left. - \left[ \cos(\theta - \phi_1) - \frac{\cos\theta}{\cos\phi_1} \right] \exp\left( - \frac{\omega t + \theta}{\omega\tau_1} \right) \right\}, \tag{1.54}$$

where $\cos\phi_1 = 1/\sqrt{1 + (\omega\tau_1)^2}$ and $\phi_1 = -\tan^{-1}\omega\tau_1$ [15].

Fig. 1.13 shows the time domain dependencies of the periodical base input voltage $v_{\mathrm{in}}$, base junction voltage $v$, and collector current $i$ for the base bias voltage $V_{\mathrm{bias}} = 0$. In this case, if the input driving voltage $v_{\mathrm{in}}$ is cosinusoidal, the junction voltage $v$ contains an exponential component demonstrating a transient response that occurs when the transistor is turned on. At the time moment of $\theta_1$ when the voltage $v$ becomes equal to $V_{\mathrm{p}}$, the transistor is turned off and the voltage $v$ provides an instant step change to a certain negative value, since it was assumed that $C_{\mathrm{e}} = 0$ and any transient response during the pinch-off mode is not possible. Due to the effect of the diffusion capacitance $C_{\mathrm{d}}$ during an active device mode, the transistor is turned off when the input driving voltage $v_{\mathrm{in}}$ is negative at that time. In this case, the shape of the junction voltage $v$ is no longer cosinusoidal. Now it is characterized by a much smaller amplitude and is stretched to the right-hand side, thus making the conduction angle longer compared to a low-frequency case. According to Eq. (1.48), the time-domain behavior of the collector current $i$ represents the waveform similar to that of the junction voltage waveform during active mode and equal to zero during a pinch-off mode.

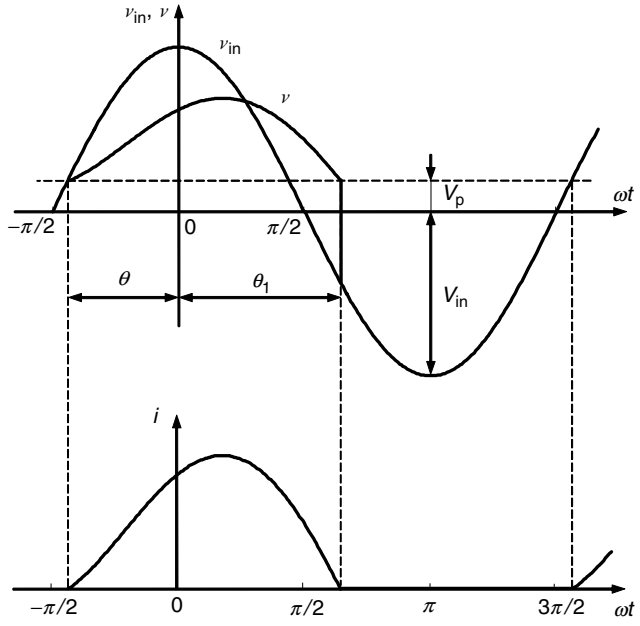



**Figure 1.13: Device voltage and current waveforms for $C_{\mathrm{e}} = 0$.**

The time moment $\theta_1$ can be defined from Eq. (1.54) by setting $\omega t = \theta_1$ and $v = V_p$ that results in a transcendental equation of

$$\cos(\theta_1 + \phi_1) - \frac{\cos\theta}{\cos\phi_1} - \tan\phi_1 \sin(\theta - \phi_1) \exp\left(\frac{\theta_1 + \theta}{\tan\phi_1}\right) = 0, \tag{1.55}$$

from which the dependencies $\theta_1(\theta)$ for different values of the input time constant $\omega\tau_1$ can be numerically calculated [15, 17]. As it is seen from Fig. 1.14, $\theta_1 = \theta$ when $\omega\tau_1 = 0$ corresponding to a low-frequency case. However, at higher-operating frequencies, the collector current pulses corresponding to the conduction state become longer with increased values of $\theta_1 > \theta$. Beginning from a boundary value of $\theta = 180^\circ + \phi_1$, the transistor is operated in an active region only because the pinch-off operation region doesn't occur anymore. As a result, the sum $(\theta_1 + \theta)$, which is called the *high-frequency conduction angle*, is always greater than the low-frequency conduction angle $2\theta$ for any certain value of $\omega\tau_1$.

In a common case when it is impossible to neglect the effect of the junction capacitance $C_e$, Eq. (1.53) is rewritten by using Eq. (1.52) as

$$v = V_p + V_{in}\cos\phi_2 \left\{\cos(\omega t + \phi_2) - \frac{\cos\theta}{\cos\phi_2} - \left[\cos(\theta_1 + \phi_2) - \frac{\cos\theta}{\cos\phi_2}\right] \exp\left(-\frac{\omega t - \theta_1}{\omega\tau_2}\right)\right\}, \tag{1.56}$$

where $\cos\phi_2 = 1/\sqrt{1 + (\omega\tau_2)^2}$ and $\phi_2 = -\tan^{-1}\omega\tau_2$.

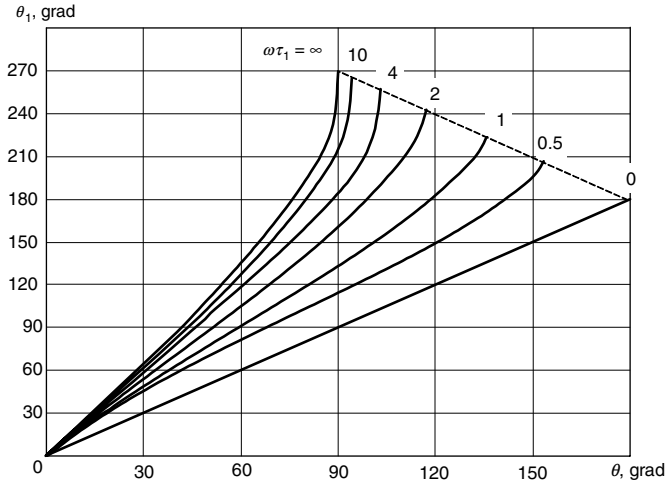



**Figure 1.14: High-frequency conduction angle as a function of $\omega\tau_1$.**

Eq. (1.56) describes the transient response when $v < V_p (V_p > V_{bias} = 0)$, which occurs when the transistor is turned off. This transient response arises when the transistor turns off for the first time, as shown in Fig. 1.15. Then, when the junction voltage $v$ becomes equal to a pinch-off voltage $V_p$ again, the transistor turns on. The more the active mode time constant $\tau_1$ exceeds the pinch-off mode time constant $\tau_2$, the shorter the transient response, resulting in a steady-state periodical pulsed current $i$ with fixed amplitude and conduction angle. The time constant $\tau_2$ directly affects the duration of the transient response. When $\tau_2 = 0$, the instant damping of the transient response will occur and voltage $v$ steps down to the value of the input voltage $v_{in}$. However, when $\tau_2 \neq 0$, the voltage dependence becomes smooth and more symmetrical.

For a boundary case of equal capacitances in active and pinch-off modes when $\tau_1 = \tau_2$, both the junction voltage and collector current pulses become fully symmetrical representing the truncated cosine waveform with a high-frequency conduction angle $\theta_1 + \theta$ different from a low-frequency conduction angle $2\theta$. The high-frequency conduction angle can be greater, equal, or smaller than its low-frequency counterpart depending on the device base bias conditions. For a Class-C mode with $V_{bias} < V_p$, the junction voltage pulse when $v > V_p$ is shorter since $\theta_1 + \theta < 2\theta$, as shown in Fig. 1.16($a$) for $V_p = 0$. For a Class-B mode when $V_{bias} = V_p$, both high-frequency and low-frequency conduction angles are equal and $\theta_1 = \theta$, as shown in Fig. 1.16($b$) for $V_p = 0$. Finally, in a Class-AB mode when $V_{bias} > V_p$, the

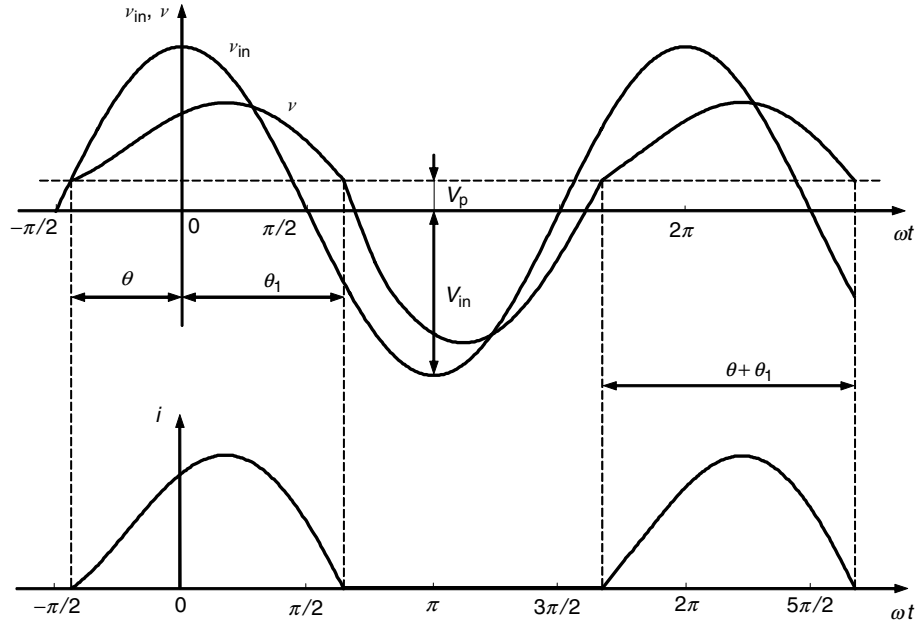



**Figure 1.15: Device voltage and current waveforms for $C_e \neq 0$.**

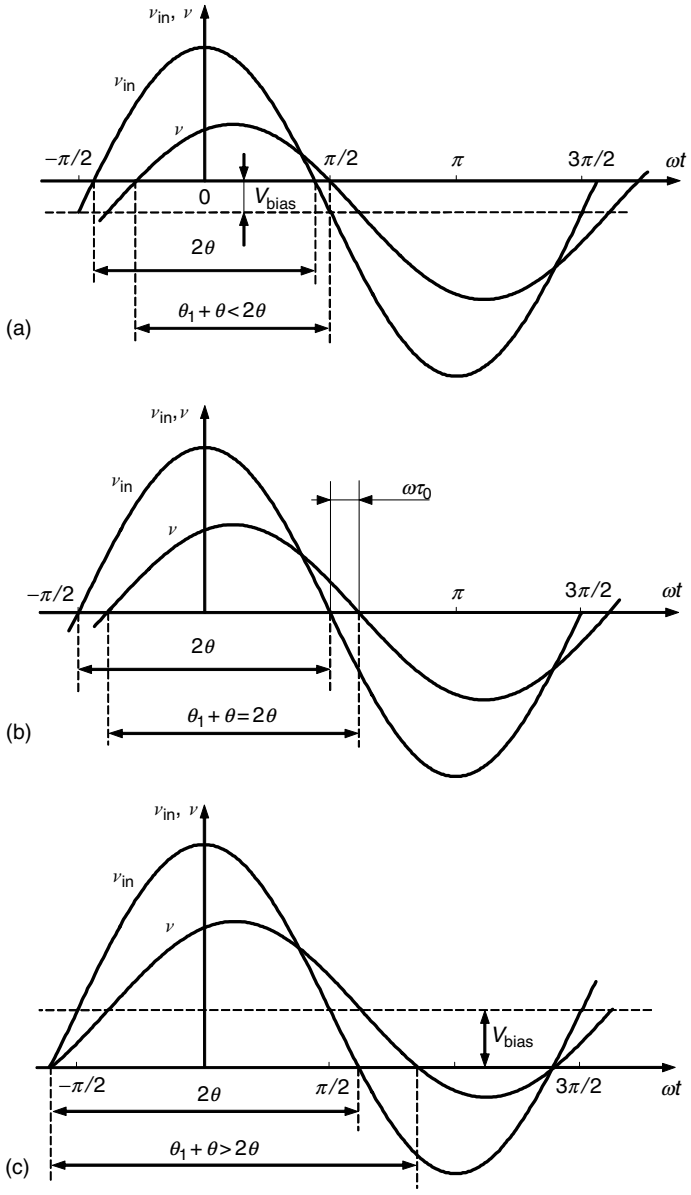



**Figure 1.16: Device voltage and current waveforms for $C_d = C_e$.**

junction voltage pulse becomes longer when $v > V_p$ since $\theta_1 + \theta > 2\theta$, as shown in Fig. 1.16($c$) for $V_p = 0$.

Analytically, the high-frequency angle can be easily calculated when $C_\pi = C_d = C_e$ and $\phi = \phi_1 = \phi_2$ from

$$\cos\theta_1 = -\frac{V_{\text{bias}} - V_{\text{p}}}{V_{\text{in}}}\frac{1}{\cos\phi}, \tag{1.57}$$

where $\cos\phi = 1/\sqrt{1+(\omega\tau_0)^2}$ and $\tau_0 = r_{\text{b}}C_{\pi}$.

To take into account an effect of the feedback collector capacitance $C_{\text{ci}}$, the equivalent input driving voltage $v'_{\text{in}}(\omega t)$ can be represented through the input base-emitter voltage $v_{\text{in}}$ and collector-emitter voltage $v_{\text{ce}}$ as

$$v'_{\text{in}}(\omega t) = v_{\text{in}}(\omega t) + j\omega\tau_{\text{c}}v_{\text{ce}}(\omega t), \tag{1.58}$$

where $\tau_{\text{c}} = r_{\text{b}}C_{\text{ci}}$.

## 1.5 Nonlinear Effect of Collector Capacitance

Generally, the dependence of the collector capacitance on the output voltage represents a nonlinear function. To evaluate the influence of the nonlinear collector capacitance on electrical behavior of the power amplifier, let us consider the load network including a series resonant $L_0C_0$ circuit tuned to the fundamental frequency that provides open-circuit conditions for second and higher-order harmonic components of the output current and an L-type matching circuit with the series inductor $L$ and shunt capacitor $C$, as shown in Fig. 1.17(*a*). The matching circuit is needed to match the equivalent output resistance $R$, corresponding to the required output power at the fundamental frequency, with the standard load resistance $R_{\text{L}}$. Fig. 1.17(*b*) shows the simplified output equivalent circuit of the bipolar power amplifier.

The total output current flowing through the device collector can be written as

$$i = I_0 + \sum_{\text{n}=1}^{\infty} I_{\text{n}}\cos(n\omega t + \phi_{\text{n}}), \tag{1.59}$$

where $I_{\text{n}}$ and $\phi_{\text{n}}$ are the amplitude and phase of the $n$th harmonic component, respectively.

An assumption of a high-quality factor of the series resonant circuit allows the only fundamental-frequency current component to flow into the load. The current flowing through the nonlinear collector capacitance consists of the fundamental-frequency and higher-harmonic components:

$$i_{\text{C}} = I_{\text{C}}\cos(\omega t + \phi_1) + \sum_{\text{n}=2}^{\infty} I_{\text{n}}\cos(n\omega t + \phi_{\text{n}}), \tag{1.60}$$

where $I_{\text{C}}$ is the fundamental-frequency capacitor current amplitude.

The nonlinear behavior of the collector junction capacitance is described by

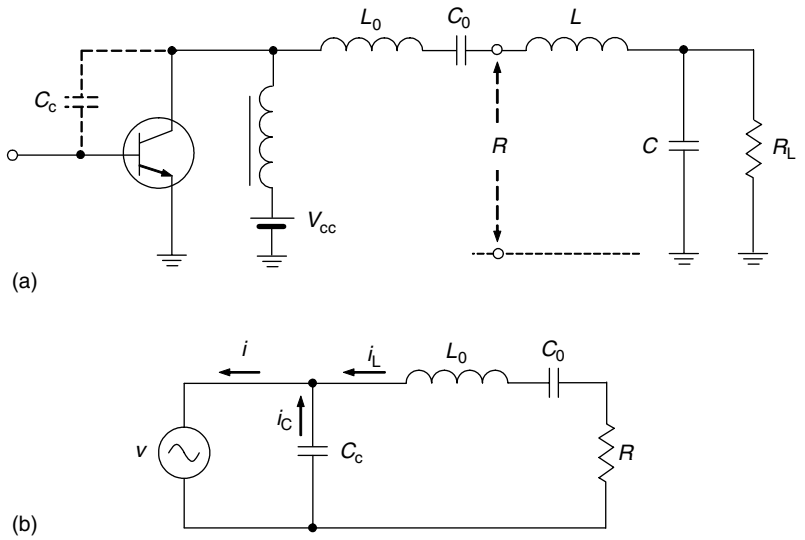



**Figure 1.17: Resonant power-amplifier circuit schematics.**

$$C_c = C_0\left(\frac{\varphi + V_{cc}}{\varphi + v}\right)^{\gamma}, \tag{1.61}$$

where $C_0$ is the collector capacitance at $v = V_{cc}$, $V_{cc}$ is the supply voltage, $\varphi$ is the contact potential, and $\gamma$ is the junction sensitivity equal to 0.5 for abrupt junction.

As a result, the expression for charge flowing through collector capacitance can be obtained by

$$q = \int_0^v C(v)dv = \int_0^v \frac{C_0(\varphi + V_{cc})^{\gamma}}{(\varphi + v)^{\gamma}}dv. \tag{1.62}$$

When $v = V_{cc}$, then

$$q_0 = \frac{C_0(\varphi + V_{cc})}{1 - \gamma}\left[1 - \left(\frac{\varphi}{\varphi + V_{cc}}\right)^{1-\gamma}\right]. \tag{1.63}$$

Although the dc charge component $q_0$ is a function of the voltage amplitude, its variations at maximum voltage amplitude normally do not exceed 20% for $\gamma = 0.5$. Then, assuming $q_0$ is determined by Eq. (1.63) as a constant component, the total charge $q$ of the nonlinear capacitance can be represented by the dc component $q_0$ and ac component $\Delta q$ written by

$$q = q_0 + \Delta q = q_0\left(1 + \frac{\Delta q}{q_0}\right) = q_0 \frac{(\varphi + v)^{1-\gamma} - \varphi^{1-\gamma}}{(\varphi + V_{cc})^{1-\gamma} - \varphi^{1-\gamma}}. \tag{1.64}$$

Since in the normal case of $V_{cc} >> \varphi$, from Eq. (1.64) it follows that

$$\frac{v}{V_{cc}} = \left(1 + \frac{\Delta q}{q_0}\right)^{\frac{1}{1-\gamma}}, \tag{1.65}$$

where $q_0 \cong C_0 V_{cc}/(1-\gamma)$.

On the other hand, the charge component $\Delta q$ can be written using Eq. (1.60) as

$$\Delta q = \int i_C(t)dt = \frac{I_C}{\omega}\sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} \frac{I_n}{n\omega}\sin(n\omega t + \phi_n). \tag{1.66}$$

As a result, substituting Eq. (1.66) into Eq. (1.65) yields

$$\frac{v}{V_{cc}} = \left[1 + \frac{I_C(1-\gamma)}{\omega C_0 V_{cc}}\sin(\omega t + \phi_1) + \sum_{n=2}^{\infty} \frac{I_n(1-\gamma)}{n\omega C_0 V_{cc}}\sin(n\omega t + \phi_n)\right]^{\frac{1}{1-\gamma}}. \tag{1.67}$$

After applying a Taylor series expansion to Eq. (1.67), it is sufficient to be limited to its first three terms to reveal the parametric effect. Then, equating the fundamental-frequency collector voltage components gives

$$\begin{aligned}\frac{v_1}{V_{cc}} = {} & \frac{I_C}{\omega C_0 V_{cc}}\sin(\omega t + \phi_1) + \frac{I_C I_2 \gamma}{(2\omega C_0 V_{cc})^2}\cos(\omega t + \phi_2 - \phi_1) \\ & + \frac{I_2 I_3 \gamma}{12(\omega C_0 V_{cc})^2}\cos(\omega t + \phi_3 - \phi_2).\end{aligned} \tag{1.68}$$

Consequently, by taking into account that $v_1 = V_1 \sin(\omega t + \phi_1)$, the fundamental voltage amplitude $V_1$ can be obtained from Eq. (1.68) by

$$\begin{aligned}\frac{V_1}{V_{cc}} = \frac{I_C}{\omega C_0 V_{cc}}\Bigg[ & 1 + \frac{I_2 \gamma}{4\omega C_0 V_{cc}}\cos(90^\circ + \phi_2 - 2\phi_1) \\ & + \frac{I_2 I_3 \gamma}{12\omega C_0 V_{cc} I_C}\cos(90^\circ + \phi_3 - \phi_2 - \phi_1)\Bigg].\end{aligned} \tag{1.69}$$

Since a large-signal value of the abrupt junction collector capacitance usually doesn't exceed 20%, the fundamental-frequency capacitor current amplitude $I_C$ as a first-order approximation can be written as

$$I_C \cong \omega C_0 V_1. \tag{1.70}$$

As a result, from Eq. (1.69) it follows that, because of the parametric transformation due to the collector capacitance nonlinearity, the fundamental-frequency collector voltage amplitude increases by $\sigma_p$ times according to

$$\sigma_p = 1 + \frac{I_2\gamma}{4\omega C_0 V_{cc}}\cos(90^\circ + \phi_2 - 2\phi_1) + \frac{I_2 I_3 \gamma}{12(\omega C_0)^2 V_1 V_{cc}}\cos(90^\circ + \phi_3 - \phi_2 - \phi_1), \tag{1.71}$$

where $\sigma_p = \xi_p/\xi$, $\xi_p$ is the collector voltage peak factor with parametric effect [2].

From Eq. (1.71) it follows that to maximize the collector voltage peak factor and, consequently, the collector efficiency for a given value of the supply voltage $V_{cc}$, it is necessary to provide the following phase conditions:

$$\phi_2 = 2\phi_1 - 90^\circ, \tag{1.72}$$

$$\phi_3 = 3\phi_1 - 180^\circ. \tag{1.73}$$

Then, for $\gamma = 0.5$,

$$\sigma_p = 1 + \frac{I_2}{8\omega C_0 V_{cc}} + \frac{I_2 I_3}{24(\omega C_0)^2 V_1 V_{cc}}. \tag{1.74}$$

Eq. (1.74) shows the theoretical possibility to increase the collector voltage peak factor by 1.1 to 1.2 times, thus achieving collector efficiency of 85 to 90%. Physically, the improved efficiency can be explained by the transformation of powers corresponding to the second and higher-order harmonic components into the fundamental-frequency output power because of the nonlinearity of the collector capacitance. However, this becomes effective only in the case of the load network with a series resonant circuit, since it ideally provides infinite impedance at the second and higher-order harmonic components unlike the load network with a parallel resonant circuit having ideally zero impedance at these harmonics.

## 1.6 Push-Pull Power Amplifiers

Generally, if it is necessary to increase the overall output power of the power amplifier, several active devices can be used in parallel or push—pull configurations. In a parallel configuration, the active devices are not isolated from each other—that requires a very good circuit symmetry—and output impedance becomes too small in the case of high output power. The latter drawback can be eliminated in a push-pull configuration, which provides increased values of the input and output impedances. For the same output power level, the input

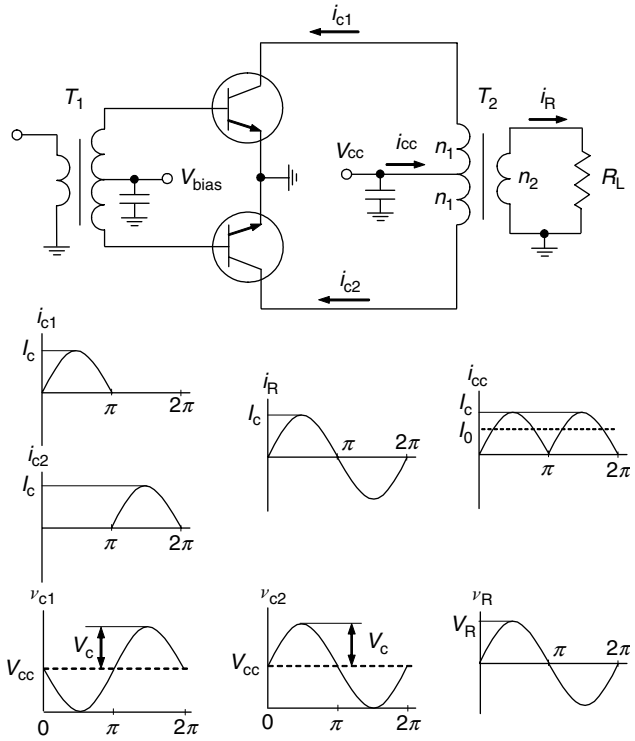



**Figure 1.18: Basic concept of push-pull operation.**

impedance $Z_{in}$ and output impedance $Z_{out}$ under a push-pull operation mode are approximately four times as high as a parallel connection of the active devices. At the same time, the loaded quality factors of the input and output matching circuits remain unchanged because both the real and reactive parts of these impedances are increased by the factor of four. Very good circuit symmetry can be provided using the balanced active devices with common emitters in a single package. The basic concept of a push-pull operation can be analyzed by using the equivalent circuit shown in Fig. 1.18 [18].

It is most convenient to consider an ideal Class-B operation, which means that each transistor conducts exactly half a 180° cycle with zero quiescent current. Let us also assume that the number of turns of both primary and secondary windings of the output transformer $T_2$ is equal—that is, $n_1 = n_2$—and the collector current of each transistor can be presented in the following half-sinusoidal form:

for the first transistor:

$$i_{c1} = \begin{cases} +I_c \sin \omega t & 0 \leq \omega t < \pi \\ 0 & \pi \leq \omega t < 2\pi, \end{cases} \tag{1.75}$$

for the second transistor:

$$i_{c2} = \begin{cases} 0 & 0 \le \omega t < \pi \\ -I_c \sin \omega t & \pi \le \omega t < 2\pi, \end{cases} \tag{1.76}$$

where $I_c$ is the output current amplitude.

Being transformed through the output transformer $T_2$ with the appropriate phase conditions, the total current flowing across the load $R_L$ is obtained by

$$i_R(\omega t) = i_{c1}(\omega t) - i_{c2}(\omega t) = I_c \sin \omega t. \tag{1.77}$$

The current flowing into the center tap of the primary windings of the output transformer $T_2$ is the sum of the collector currents resulting in

$$i_{cc}(\omega t) = i_{c1}(\omega t) + i_{c2}(\omega t) = I_c |\sin \omega t|. \tag{1.78}$$

Ideally, even-order harmonics being in phase are canceled out and should not appear at the load. In practice, a level of the second harmonic component of 30 to 40 dB below the fundamental is allowable. However, it is necessary to connect a bypass capacitor to the center tap of the primary winding to exclude power losses due to even-order harmonics. The current $i_R(\omega t)$ produces the load voltage $v_R(\omega t)$ onto the load $R_L$ as

$$v_R(\omega t) = I_c R_L \sin(\omega t) = V_R \sin(\omega t), \tag{1.79}$$

where $V_R$ is the load voltage amplitude.

The total dc collector current is defined as the average value of $i_{cc}(\omega t)$, which yields

$$I_0 = \frac{1}{2\pi} \int_0^{2\pi} i_{cc}(\omega t) d(\omega t) = \frac{2}{\pi} I_c. \tag{1.80}$$

The total dc power $P_0$ and fundamental-frequency output power $P_{out}$, for the ideal case of zero saturation voltage of both transistors when $V_c = V_{cc}$ and taking into account that $V_R = V_c$ for equal turns of windings when $n_1 = n_2$, are calculated from

$$P_0 = \frac{2}{\pi} I_c V_{cc}, \tag{1.81}$$

$$P_{out} = \frac{I_c V_{cc}}{2}. \tag{1.82}$$

Consequently, the maximum theoretical collector efficiency that can be achieved in a push-pull Class-B operation is equal to

$$\eta = \frac{P_{\text{out}}}{P_0} = \frac{\pi}{4} \cong 78.5\%. \tag{1.83}$$

In a balanced circuit, identical sides carry 180° out-of-phase signals of equal magnitude. If perfect balance is maintained on both sides of the circuit, the difference between signal magnitudes becomes equal to zero in each midpoint of the circuit, as shown in Fig. 1.19. This effect is called the *virtual grounding*, and this midpoint line is referred to as the *virtual ground*. The virtual ground, being actually inside the device package, reduces a common mode inductance and results in better stability and usually higher-power gain.

When using a balanced transistor, new possibilities for both internal and external impedance matching procedure emerge. For instance, for a push-pull operation mode of two single-ended transistors, it is necessary to provide reliable grounding for input- and output-matching circuits for each device, as shown in Fig. 1.20(*a*). Using the balanced transistors simplifies significantly the matching circuit topologies with the series inductors and parallel capacitors connected between amplifying paths, as shown in Fig. 1.20(*b*), and dc-blocking capacitors are not needed.

For a push-pull operation of the power amplifier with a balanced transistor, it is also necessary to provide the unbalanced-to-balanced transformation referenced to the ground both at the input and at the output of the power amplifier. The most suitable approach to solve this problem in the best possible manner at high frequencies and microwaves is to use the transmission-line transformers, as shown in Fig. 1.21. If the characteristic impedance $Z_0$ of the coaxial transmission line is equal to the input impedance at the unbalanced end of the

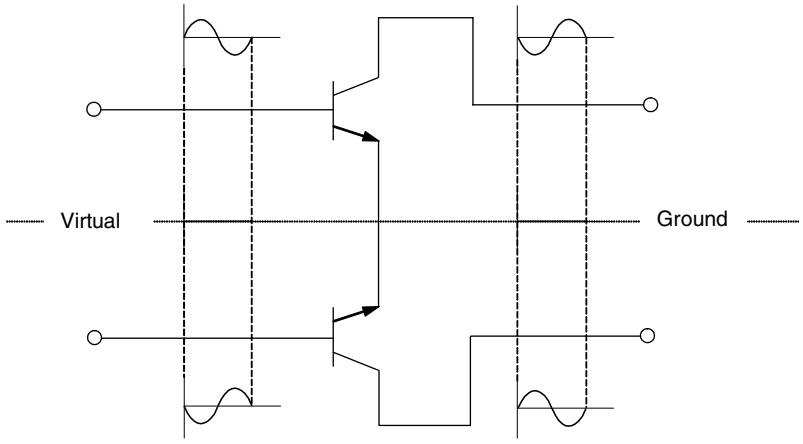



**Figure 1.19: Basic concept of balanced transistor.**

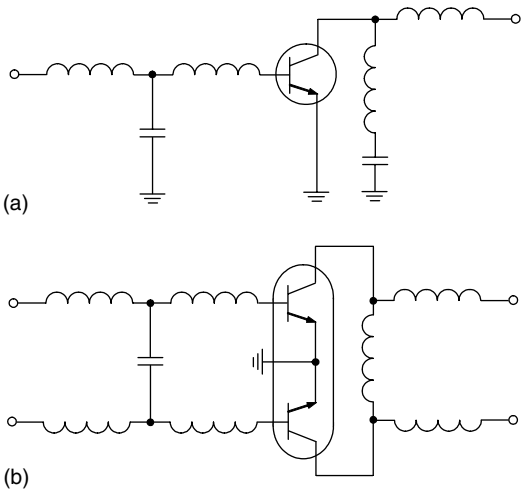



**Figure 1.20: Matching technique for (*a*) single-ended and (*b*) balanced transistors.**

transformer, the total impedance from both devices seen at the balanced end of the transformer will be equal to the input impedance. Hence, such a transmission-line transformer can be used as a 1:1 unbalanced-to-balanced transformer. If $Z_0 = 50\ \Omega$, for the standard input impedance of 50 Ω, the impedance seen at each balanced part is equal to 25 Ω, which then is necessary to match with the appropriate input impedance of each part of a balanced transistor. The input-and output-matching circuits can easily be realized by using the series microstrip lines with parallel capacitors.

The miniaturized compact input unbalanced-to-balanced transformer shown in Fig. 1.22 covers the frequency bandwidth up to an octave with well-defined rejection-mode impedances [19]. To avoid the parasitic capacitance between the outer conductor and the ground, the coaxial semirigid transformer $T_1$ is mounted atop microstrip shorted stub $l_1$ and soldered continuously along its length. The electrical length of this stub is usually chosen from the condition of $\theta \leq \pi/2$ on the high bandwidth frequency depending on the matching requirements. To maintain circuit symmetry on the balanced side of the transformer network,

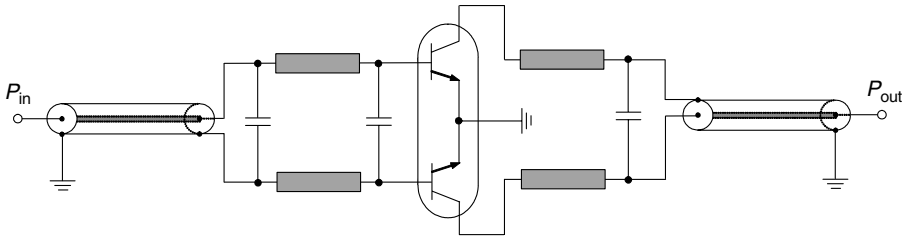



**Figure 1.21: Push-pull power amplifier with balanced-to-unbalanced transformers.**

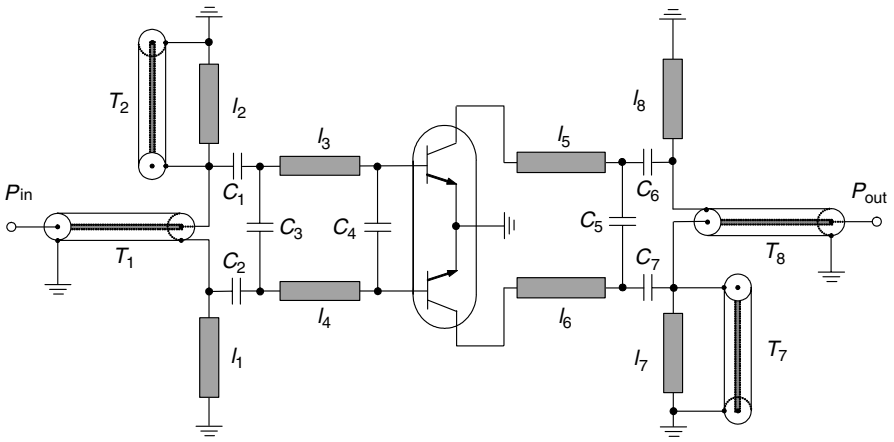



**Figure 1.22: Push-pull power amplifier with compact balanced-to-unbalanced transformers.**

another semi-rigid coaxial section $T_2$ with unconnected center conductor is soldered continuously along microstrip shorted stub $l_2$. The lengths of $T_2$ and $l_2$ are equal to the lengths of $T_1$ and $l_1$, respectively. Because the input short-circuited microstrip stubs provide inductive impedances, the two series capacitors $C_1$ and $C_2$ of the same value are used for matching purposes, thereby forming the first high-pass matching section and providing dc blocking at the same time. The practical circuit realization of the output-matching circuit and balanced-to-unbalanced transformer can be the same as for the input-matching circuit.

## 1.7 Power Gain and Stability

Power-amplifier design aims for maximum power gain and efficiency for a given value of output power with a predictable degree of stability. Instability of the power amplifier will lead to undesired parasitic oscillations and, as a result, to the distortion of the output signal. One of the main reasons for amplifier instability is a positive feedback from the device output to its input through the internal feedback capacitance, inductance of a common grounded device electrode and external circuit elements. Consequently, a stability analysis is crucial to any power-amplifier design, especially at high frequencies.

Fig. 1.23 shows the basic block schematic of the single-stage power-amplifier circuit, which includes an active device, an input-matching circuit to match with the source impedance, and an output-matching circuit to match with the load impedance. Generally, the two-port active device is characterized by a system of immittance $W$-parameters; i.e., any system of impedance $Z$-parameters or admittance $Y$-parameters [4, 15]. The input- and output-matching circuits transform the source and load immittances, $W_S$ and $W_L$, into specified values between points *1–2* and *3–4*, respectively, by means of which the optimal design operation mode of the power amplifier is realized.

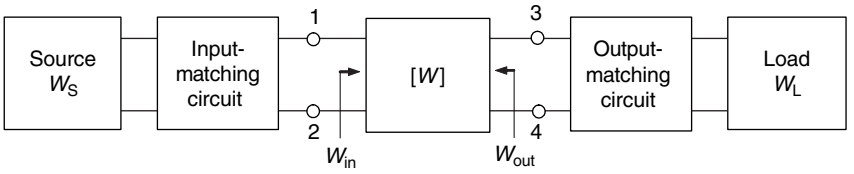



**Figure 1.23: Generalized single-stage power-amplifier circuit.**

The operating power gain $G_P$, which represents the ratio of power dissipated in the active load $\mathrm{Re}W_L$ to the power delivered to the input port of the active device, can be expressed in terms of the immittance $W$-parameters as

$$G_P = \frac{|W_{21}|^2 \mathrm{Re}W_L}{|W_{22} + W_L|^2 \mathrm{Re}W_{in}}, \tag{1.84}$$

where

$$W_{in} = W_{11} - \frac{W_{12}W_{21}}{W_{22} + W_L} \tag{1.85}$$

is the input immittance and $W_{ij}$ $(i, j = 1, 2)$ is the immittance two-port parameters of the active device equivalent circuit.

The transducer power gain $G_T$, which represents the ratio of power dissipated in the active load $\mathrm{Re}W_L$ to the power available from the source, can be expressed in terms of the immittance $W$-parameters as

$$G_T = 4\frac{|W_{21}|^2 \mathrm{Re}W_S \mathrm{Re}W_L}{|(W_{11} + W_S)(W_{22} + W_L) - W_{12}W_{21}|^2}. \tag{1.86}$$

The operating power gain $G_P$ does not depend on the source parameters and characterizes only the effectiveness of the power delivery from the input port of the active device to the load. This power gain helps to evaluate the gain property of a multistage amplifier when the overall

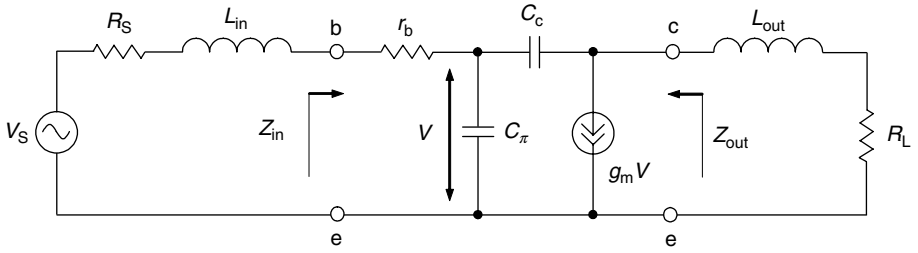



**Figure 1.24: Simplified equivalent circuit of matched bipolar power amplifier.**

operating power gain $G_{P(total)}$ is equal to the product of each stage $G_P$. The transducer power gain $G_T$ includes an assumption of conjugate matching of the load and the source.

The bipolar transistor simplified small-signal $\pi$-hybrid equivalent circuit shown in Fig. 1.24 provides an example for a conjugate-matched bipolar power amplifier. The impedance $Z$-parameters of the equivalent circuit of the bipolar transistor in a common emitter configuration can be obtained as

$$\begin{aligned} Z_{11} &= r_b + \frac{1}{g_m + j\omega C_\pi} & Z_{12} &= \frac{1}{g_m + j\omega C_\pi} \\ Z_{21} &= -\frac{1}{j\omega C_c}\,\frac{g_m - j\omega C_c}{g_m + j\omega C_\pi} & Z_{22} &= \left(1 + \frac{C_\pi}{C_c}\right)\frac{1}{g_m + j\omega C_\pi}, \end{aligned} \tag{1.87}$$

where $g_m$ is the transconductance, $r_b$ is the series base resistance, $C_\pi$ is the base-emitter capacitance including both diffusion and junction components, and $C_c$ is the feedback collector capacitance.

By setting the device feedback impedance $Z_{12}$ to zero and complex conjugate-matching conditions at the input of $R_S = \mathrm{Re}\, Z_{in}$ and $L_{in} = -\mathrm{Im}\, Z_{in}/\omega$ and at the output of $R_L = \mathrm{Re}\, Z_{out}$ and $L_{out} = -\mathrm{Im}\, Z_{out}/\omega$, the small-signal transducer power gain $G_T$ can be calculated from

$$G_T = \left(\frac{f_T}{f}\right)^2 \frac{1}{8\pi f_T r_b C_c}, \tag{1.88}$$

where $f_T = g_m/2\pi C_\pi$ is the device transition frequency.

Fig. 1.25 shows an example for a conjugate-matched FET (field-effect transistor) power amplifier. The admittance $Y$-parameters of the small-signal equivalent circuit of any FET device in a common source configuration can be obtained by

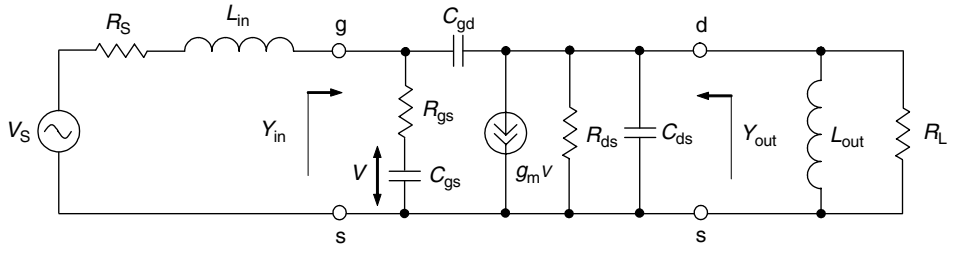



**Figure 1.25: Simplified equivalent circuit of matched FET power amplifier.**

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{gs}} + j\omega C_{gd} \quad Y_{12} = -j\omega C_{gd}$$
$$Y_{21} = \frac{g_m}{1 + j\omega C_{gs} R_{gs}} - j\omega C_{gd} \quad Y_{22} = \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{gd}\right), \tag{1.89}$$

where $g_m$ is the transconductance, $R_{gs}$ is the gate-source resistance, $C_{gs}$ is the gate-source capacitance, $C_{gd}$ is the feedback gate-drain capacitance, $C_{ds}$ is the drain-source capacitance, and $R_{ds}$ is the differential drain-source resistance.

Since the value of the gate-drain capacitance $C_{gd}$ is normally relatively small, the effect of the feedback admittance $Y_{12}$ can be neglected in a simplified case. Then, it is necessary to set $R_S = R_{gs}$ and $L_{in} = 1/\omega^2 C_{gs}$ for input matching while $R_L = R_{ds}$ and $L_{out} = 1/\omega^2 C_{ds}$ for output matching. Hence, the transducer power gain $G_T$ can approximately be calculated from

$$G_T\left(C_{gd} = 0\right) = MAG = \left(\frac{f_T}{f}\right)^2 \frac{R_{ds}}{4R_{gs}}, \tag{1.90}$$

where $f_T = g_m/2\pi C_{gs}$ is the device transition frequency and *MAG* is the maximum available gain representing a theoretical limit on the power gain that can be achieved under complex conjugate-matching conditions.

From Eqs. (1.88) and (1.90) it follows that the small-signal power gain of a conjugate-matched power amplifier for any type of the active device drops off as $1/f^2$ or 6 dB per octave. Therefore, $G_T(f)$ can readily be predicted at a certain frequency $f$, if it is known a power gain at the transition frequency $f_T$, by

$$G_T(f) = G_T(f_T)\left(\frac{f_T}{f}\right)^2. \tag{1.91}$$

It should be noted that previous analysis is based on the linear small-signal consideration when generally nonlinear device current source as a function of the both input and output voltages can be characterized by the linear transconductance $g_m$ as a function of the input voltage and the output differential resistance $R_{ds}$ as a function of the output voltage. This is a result of a Taylor series expansion of the output current as a function of the input and output voltages with maintaining only the dc and linear components. Such an approach helps to understand and derive the maximum achievable power-amplifier parameters in a linear approximation. In this case, an active device is operated in a Class-A mode when one-half dc power is dissipated in the device, while the other half is transformed to the fundamental-frequency output power flowing into the load, resulting in a maximum ideal collector efficiency of 50%. The device output resistance $R_{out}$ remains constant and can be calculated as a ratio of the dc supply voltage to the dc current flowing through the active device. In a common case, for

a complex conjugate-matching procedure, the device output immittance under large-signal consideration should be calculated using Fourier analysis of the output current and voltage fundamental components. This means that, unlike a linear Class-A mode, an active device is operated in a device linear region only part of the entire period, and its output resistance is defined as a ratio of the fundamental-frequency output voltage to the fundamental-frequency output current. This is not a physical resistance resulting in a power loss inside the device, but an equivalent resistance required to use for a conjugate matching procedure. In this case, the complex conjugate matching is valid and necessary, firstly, to compensate for the reactive part of the device output impedance and, secondly, to provide a proper load resistance resulting in a maximum power gain for a given supply voltage and required output power delivered to the load. Note that this is not a maximum available small-signal power gain that can be achieved in a linear operation mode, but a maximum achievable large-signal power gain that can be achieved for a particular operation mode with a certain conduction angle. Of course, the maximum large-signal power gain is smaller than the small-signal power gain for the same input power, since the output power in a nonlinear operation mode also includes the powers at the harmonic components of the fundamental frequency.

According to the immittance approach to the stability analysis of the active two-port network, it is necessary and sufficient for its unconditional stability if the following system of equations can be satisfied for the given active device with both open-circuit input and output ports:

$$\begin{cases} \mathrm{Re}[W_{\mathrm{S}}(\omega) + W_{\mathrm{in}}(\omega)] > 0 \\ \mathrm{Im}[W_{\mathrm{S}}(\omega) + W_{\mathrm{in}}(\omega)] = 0. \end{cases} \tag{1.92}$$

or

$$\begin{cases} \mathrm{Re}[W_{\mathrm{L}}(\omega) + W_{\mathrm{out}}(\omega)] > 0 \\ \mathrm{Im}[W_{\mathrm{L}}(\omega) + W_{\mathrm{out}}(\omega)] = 0. \end{cases} \tag{1.93}$$

In the case of the opposite signs in Eqs. (1.92) and (1.93), the active two-port network can be treated as unstable or potentially unstable.

Analysis of Eq. (1.92) or (1.93) on extremum results in a special relationship between the device immittance parameters called the device stability factor

$$K = \frac{2\mathrm{Re}W_{11}\mathrm{Re}W_{22} - \mathrm{Re}(W_{12}W_{21})}{|W_{12}W_{21}|}, \tag{1.94}$$

which shows a stability margin indicating how far from zero value are the real parts in Eqs. (1.92) and (1.93) being positive [20]. An active device is unconditionally stable if $K \geq 1$ and potentially unstable if $K < 1$.

When the active device is potentially unstable, an improvement of the power-amplifier stability can be provided with the appropriate choice of the source and load immittances, $W_S$ and $W_L$. The circuit stability factor $K_T$ in this case is defined in the same way as the device stability factor $K$, with taking into account of $\mathrm{Re}W_S$ and $\mathrm{Re}W_L$ along with the device $W$-parameters. The circuit stability factor is given by

$$K_T = \frac{2\mathrm{Re}(W_{11} + W_S)\mathrm{Re}(W_{22} + W_L) - \mathrm{Re}(W_{12}W_{21})}{|W_{12}W_{21}|}. \tag{1.95}$$

If the circuit stability factor $K_T \geq 1$, the power amplifier is unconditionally stable. However, the power amplifier becomes potentially unstable if $K_T < 1$. The value of $K_T = 1$ corresponds to the border of the circuit unconditional stability. The values of the circuit stability factor $K_T$ and device stability factor $K$ become equal, if $\mathrm{Re}W_S = \mathrm{Re}W_L = 0$.

When the active device stability factor $K > 1$, the operating power gain $G_P$ has to be maximized. By analyzing Eq. (1.84) on extremum, it is possible to find optimum values $\mathrm{Re}W_L^o$ and $\mathrm{Im}W_L^o$ when the operating power gain $G_P$ is maximal [20, 21]. As a result,

$$G_{P\max} = \left|\frac{W_{21}}{W_{12}}\right| \Big/ \left(K + \sqrt{K^2 - 1}\right). \tag{1.96}$$

The power amplifier with an unconditionally stable active device provides a maximum power gain operation only if the input and output of the active device are conjugate-matched with the source and load impedances, respectively. For the lossless input-matching circuit when the power available at the source is equal to the power delivered to the input port of the active device, that is $P_S = P_{in}$, the maximum operating power gain is equal to the maximum transducer power gain, that is $G_{P\max} = G_{T\max}$.

Domains of the device potential instability include the operating frequency ranges where the active device stability factor is equal to $K < 1$. Within the bandwidth of such a frequency domain, parasitic oscillations can occur, defined by internal positive feedback and operating conditions of the active device. The instabilities may not be self-sustaining induced by the RF drive power but remaining on its removal. One of the most serious cases of the power-amplifier instability can occur when there is a variation of the load impedance. Under these conditions, the transistor may be destroyed almost instantaneously. However, even if it is not destroyed, the instability can result in an increased level of the spurious emissions in the output spectrum of the power amplifier tremendously. Generally, the following classification for linear instabilities can be made [22]:

- Low-frequency oscillations produced by thermal feedback effects
- Oscillations due to internal feedback

- Negative resistance or conductance-induced instabilities due to transit-time effects, avalanche multiplication, etc.
- Oscillations due to external feedback as a result of insufficient decoupling of the dc supply, etc.

Therefore, it is very important to determine the effect of the device feedback parameters on the origin of the parasitic self-oscillations and to establish possible circuit configurations of the parasitic oscillators. Based on the simplified bipolar equivalent circuit shown in Fig. 1.24, the device stability factor can be expressed through the parameters of the transistor equivalent circuit as

$$K = 2r_{\mathrm{b}}g_{\mathrm{m}}\frac{1+\frac{g_{\mathrm{m}}}{\omega_{\mathrm{T}}C_{\mathrm{c}}}}{\sqrt{1+\left(\frac{g_{\mathrm{m}}}{\omega C_{\mathrm{c}}}\right)^2}}, \tag{1.97}$$

where $\omega_{\mathrm{T}} = 2\pi f_{\mathrm{T}}$ [4, 15].

At very low frequencies, the bipolar transistors are potentially stable and the fact that $K \to 0$ when $f \to 0$ can be explained by simplifying the bipolar equivalent circuit. In practice, at low frequencies, it is necessary to take into account the dynamic base-emitter resistance $r_{\pi}$ and early collector-emitter resistance $r_{\mathrm{ce}}$, the presence of which substantially increases the value of the device stability factor. This gives only one unstable frequency domain with $K < 1$ and low boundary frequency $f_{\mathrm{p1}}$. However, an additional region of possible low-frequency oscillations can occur due to thermal feedback where the collector junction temperature becomes frequently dependent, and the common base configuration is especially affected [23].

Equating the device stability factor $K$ with unity allows us to determine the high-boundary frequency of a frequency domain of the bipolar transistor potential instability as

$$f_{\mathrm{p2}} = \frac{g_{\mathrm{m}}}{2\pi C_{\mathrm{c}}} \Bigg/ \sqrt{(2r_{\mathrm{b}}g_{\mathrm{m}})^2\left(1+\frac{g_{\mathrm{m}}}{\omega_{\mathrm{T}}C_{\mathrm{c}}}\right)^2 - 1}. \tag{1.98}$$

When $r_{\mathrm{b}}\, g_{\mathrm{m}} > 1$ and $g_{\mathrm{m}} >> \omega_{\mathrm{T}}\, C_{\mathrm{c}}$, Eq. (1.98) is simplified to

$$f_{\mathrm{p2}} \approx \frac{1}{4\pi r_{\mathrm{b}}C_{\pi}}. \tag{1.99}$$

At higher frequencies, a presence of the parasitic-reactive intrinsic-transistor parameters and package parasitics can be of great importance in view of power-amplifier stability. The parasitic series-emitter lead inductance $L_{\mathrm{e}}$ shown in Fig. 1.26 has a major effect on the device

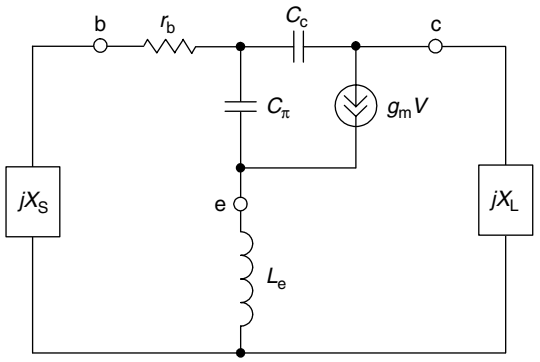



**Figure 1.26: Simplified bipolar π-hybrid equivalent circuit with emitter lead inductance.**

stability factor. The presence of $L_e$ leads to the appearance of the second frequency domain of potential instability at higher frequencies. The circuit analysis shows that the second frequency domain of potential instability can be realized only under the particular ratios between the normalized parameters $\omega_T L_e/r_b$ and $\omega_T r_b C_c$ [4, 15]. For example, the second domain does not occur for any values of $L_e$ when $\omega_T r_b C_c \geq 0.25$.

An appearance of the second frequency domain of the device potential instability is the result of the corresponding changes in the device feedback phase conditions and takes place only under a simultaneous effect of the collector capacitance $C_c$ and emitter lead inductance $L_e$. If the effect of one of these factors is lacking, the active device is characterized by only the first domain of its potential instability.

Fig. 1.27 shows the potentially realizable equivalent circuits of the parasitic oscillators. If the value of a series-emitter inductance $L_e$ is negligible, the parasitic oscillations can occur only when the values of the source and load reactances are positive, that is $X_S > 0$ and $X_L > 0$. In this case, the parasitic oscillator shown in Fig. 1.27(*a*) represents the inductive three-point circuit, where inductive elements $L_S$ and $L_L$ in combination with the collector capacitance $C_c$ form a Hartley oscillator. From a practical point of view, the more a value of the collector dc-feed inductance exceeds a value of the base bias inductance, the more likely are low-frequency parasitic oscillators. It was observed that a very low inductance, even a short between emitter and base, can produce very strong and dangerous oscillations that may easily destroy a transistor [22]. Therefore, it is recommended to increase a value of the base choke inductance and to decrease a value of collector one.

The presence of $L_e$ leads to narrowing of the first frequency domain of the potential instability, which is limited to the high-boundary frequency $f_{p2}$, and can contribute to appearance of the second frequency domain of the potential instability at higher frequencies. The parasitic oscillator that corresponds to the first frequency domain of the device potential instability can

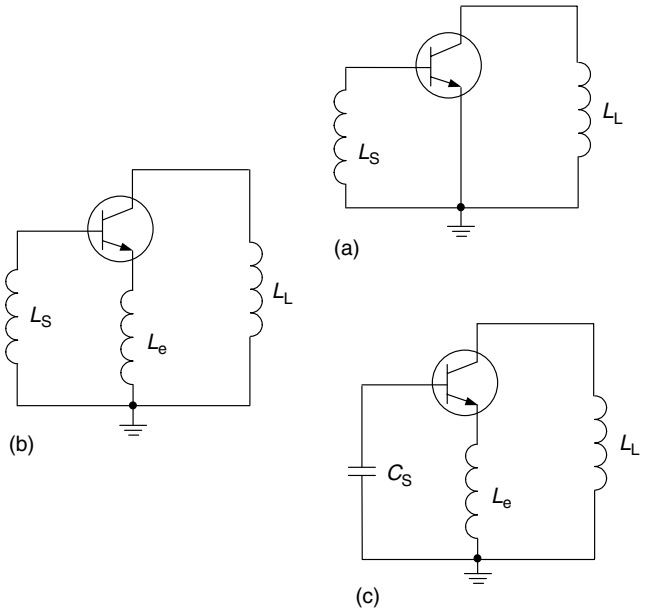



**Figure 1.27: Equivalent circuits of parasitic oscillators.**

be realized only if the source and load reactances are inductive, that is $X_S > 0$ and $X_L > 0$, with the equivalent circuit of such a parasitic oscillator shown in Fig. 1.27(*b*). The parasitic oscillator corresponding to the second frequency domain of the device potential instability can be realized only if the source reactance is capacitive and load reactance is inductive, that is $X_S < 0$ and $X_L > 0$, with the equivalent circuit shown in Fig. 1.27(*c*). The series emitter inductance $L_e$ is an element of fundamental importance for the parasitic oscillator that corresponds to the second frequency domain of the device potential instability. It changes the circuit phase conditions so it becomes possible to establish the oscillation phase-balance condition at high frequencies. However, if it is possible to eliminate the parasitic oscillations at high frequencies by other means, increasing $L_e$ will result in narrowing of a low-frequency domain of potential instability, thus making the power amplifier potentially more stable, although at the expense of reduced power gain.

Similar analysis of the MOSFET power amplifier shows the two frequency domains of MOSFET potential instability due to internal feedback gate-drain capacitance $C_{gd}$ and series source inductance $L_s$ [4]. Because of the very high gate-leakage resistance, the value of the low boundary frequency $f_{p1}$ is sufficiently small. For usually available conditions for power MOSFET devices when $g_m R_{ds} = 10 \div 30$ and $C_{gd}/C_{gs} = 0.1 \div 0.2$, the high boundary frequency $f_{p2}$ can approximately be calculated from

$$f_{p2} \approx \frac{1}{4\pi R_{gs} C_{gs}}. \tag{1.100}$$

It should be noted that power MOSFET devices have a substantially higher value of $g_m R_{ds}$ at small values of the drain current than at its high values. Consequently, for small drain current, the MOSFET device is characterized by a wider domain of potential instability. This domain is significantly wider than the same first domain of the potential instability of the bipolar transistor. The series source inductance $L_s$ contributes to the appearance of the second frequency domain of the device potential instability. The potentially realizable equivalent circuits of the MOSFET parasitic oscillators are the same as for the bipolar device shown in Fig. 1.27 [4].

Thus, to prevent parasitic oscillations and to provide a stable operation mode of any power amplifier, it is necessary to take into consideration the following common requirements:

- Use an active device with stability factor $K > 1$.
- If it is impossible to choose an active device with $K > 1$, it is necessary to provide the circuit stability factor $K_T > 1$ by the appropriate choice of the real parts of the source and load immittances.
- Disrupt the equivalent circuits of the possible parasitic oscillators.
- Choose proper reactive parameters of the matching circuit elements adjacent to the input and output ports of the active device, which are necessary to avoid the self-oscillation conditions.

Generally, the parasitic oscillations can arise on any frequency within the potential instability domains for particular values of the source and load immittances, $W_S$ and $W_L$. The frequency dependencies of $W_S$ and $W_L$ are very complicated and very often cannot be predicted exactly, especially in multistage power amplifiers. Therefore, it is very difficult to propose a unified approach to provide a stable operation mode of the power amplifiers with different circuit configuration and operation frequencies. In practice, the parasitic oscillations can arise close to the operating frequencies due to the internal positive feedback inside the transistor and at the frequencies sufficiently far from the operating frequencies due to the external positive feedback created by the surface mounted elements. As a result, the stability analysis of the power amplifier must include the methods to prevent the parasitic oscillations in different frequency ranges.

Fig. 1.28 shows an example of a stabilized bipolar VHF power amplifier configured to operate in a zero-bias Class-C mode. Conductive input and output loading due to resistances $R_1$ and $R_2$ eliminate a low-frequency instability domain. The series inductors $L_3$ and $L_4$ contribute to

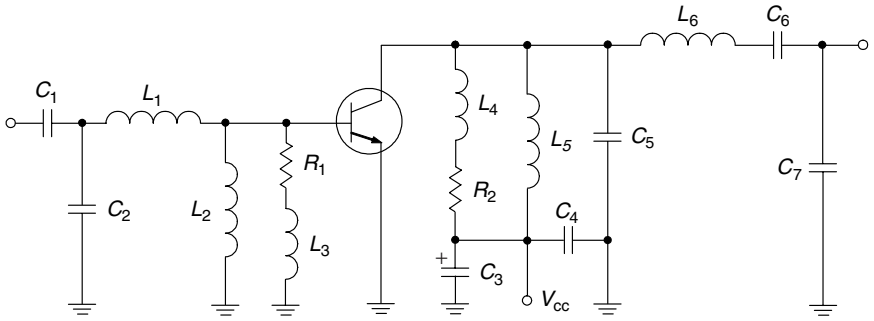



**Figure 1.28: Stabilized bipolar Class-C VHF power amplifier.**

higher-power gain if the resistance values are too small, and can compensate for the capacitive input and output device impedances. To provide a negative-bias Class-C mode, the shunt inductor $L_2$ can be removed. The equivalent circuit of the potential parasitic oscillator at higher frequencies is realized by means of the parasitic-reactive parameters of the transistor and external circuitry. The only possible equivalent circuit of such a parasitic oscillator at these frequencies is shown in Fig. 1.27(*c*). It can only be realized if the series-emitter lead inductance is present. Consequently, the electrical length of the emitter lead should be reduced as much as possible, or, alternatively, the appropriate reactive immittances at the input and output transistor ports are provided. For example, it is possible to avoid the parasitic oscillations at these frequencies if the inductive immittance is provided at the input of the transistor and capacitive reactance is provided at the output of the transistor. This is realized by an input series inductance $L_1$ and an output shunt capacitance $C_5$.

The collector efficiency of the power amplifier can be increased by removing the shunt capacitance and series *RL* circuit in the load network. The remaining series LC circuit provides high impedances at the second and higher-order harmonic components of the output current, which are flowing now through the device collector capacitance unlike being grounded by the shunt capacitance. As a result, the bipolar Class-C power amplifier, the circuit schematic of which is shown in Fig. 1.29, achieved a collector efficiency of 73% and a power gain of 9 dB with an output power of 13.8 W at an operating frequency of 160 MHz [24]. However, special care must be taken to eliminate parasitic spurious oscillations. In this case, the most important element in preventing the potential instability is the base bias resistor $R_b$. For example, for a relatively large base choke inductor $L_b$ and $R_b = 1\,k\Omega$, spurious oscillations exist at any tuning. Tuning becomes possible with no parasitic oscillations for output-voltage standing wave ratio (*VSWR*) less than 1.3 or supply voltage more than 22 V when $R_b$ is reduced to 470 Ω. However, a very small reduction in input drive power causes spurious oscillations. Further reduction of $R_b$ to 47 Ω provides a stable operation for output $VSWR \leq 7$ and supply voltages down to 7 V. Finally, no spurious oscillations occur at any load, supply voltage, and drive power level for $R_b = 26\ \Omega$.

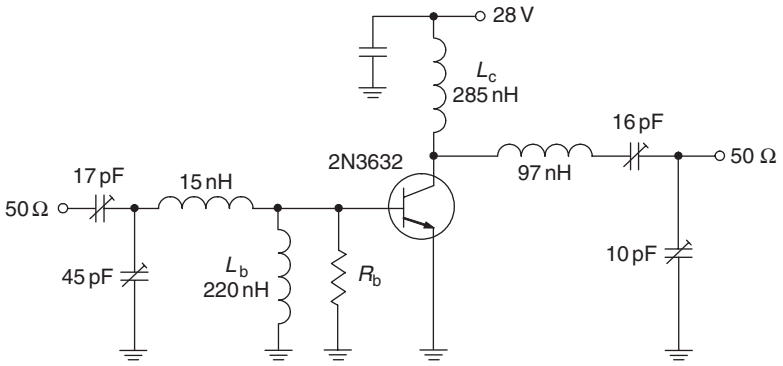



**Figure 1.29: High efficiency bipolar Class-C VHF power amplifier.**

## 1.8 Parametric Oscillations

Since the transistor used as an active device in power amplifiers is characterized by a substantially nonlinear behavior, this can result in nonlinear instabilities, which provide generally the parametric generation of both harmonic and subharmonic components. The subharmonics can be explained by parametric varactor-junction action of the collector-to-base voltage-dependent capacitance when the large-signal driving acts like pumping a varactor diode, as in a parametric amplifier [25, 26]. Such an amplifier exhibits negative resistance under certain conditions when a circuit starts oscillating at subharmonics or rational fractions of the operating frequency [27]. Generally, the parametric oscillations are the result of the external force impact on the element of the oscillation system by varying its parameter. Understanding of the physical origin of this parametric effect is very important in order to disrupt any potentially realizable parametric oscillator circuits. Especially, it is a serious concern for high-efficiency power amplifiers in general and Class-E power amplifiers in particular with very high-voltage peak factor and voltage swing across the device nonlinear output capacitance, since the transistor is operated in pinch-off, active, and saturation regions.

Fig. 1.30 shows the simplified large-signal equivalent circuit of the (*a*) MOSFET or (*b*) bipolar device with a nonlinear current source $i(t)$, respectively. The most nonlinear capacitances are the bipolar collector capacitance $C_c$ and the MOSFET gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$, which can be modeled as junction capacitances with different sensitivities $\gamma$. However, since the drain-source capacitance $C_{ds}$ is normally greater by 8 to 10 times than the gate-drain capacitance $C_{gd}$, the parametric effect due to $C_{ds}$ causes a major effect on potential parametric oscillations in a MOSFET power amplifier. The value of the collector capacitance $C_c$ is by the order smaller than the value of the base-emitter capacitance $C_\pi$ in active mode. In this case, the circuit of a potential parametric oscillator represents a system with one degree of freedom, as shown in Fig. 1.30(*c*), where $V_{cc}$ is the supply voltage applied to the varying output capacitance $C_{out}$ ($C_{out} \approx C_c$ for a bipolar device

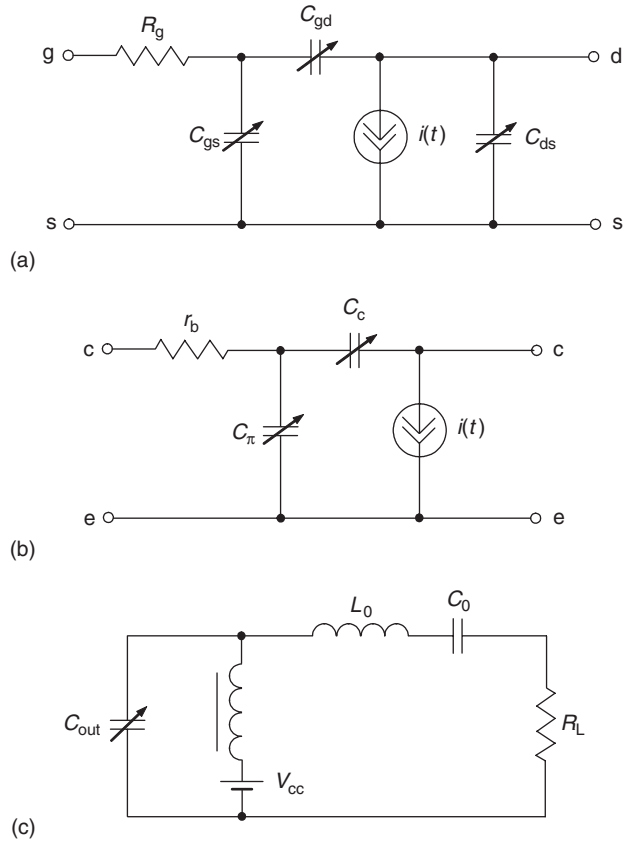



**Figure 1.30: Simplified nonlinear transistor models and output amplifier circuit.**

and $C_{out} \approx C_{ds}$ for a MOSFET device), while the capacitor $C_0$ and inductor $L_0$ represent the series high-$Q$ resonant circuit tuned to the fundamental frequency and having high impedances at the second and higher-order harmonics.

The theoretical analysis can be simplified by representing the output power-amplifier circuit in the form of a basic series *RLC* circuit shown in Fig. 1.31($a$) [28]. Let us assume that the nonlinear capacitance $C$ varies in time relative to its average value $C_0$ due to external large-signal voltage drive representing a pulsed function shown in Fig. 1.31($b$), while the charge $q(t)$ generally represents a sinusoidal function of time shown in Fig. 1.31($c$). When the capacitance $C$ decreases by $2\Delta C$, the voltage amplitude $V_0 = q_0 C_0$ across the capacitor and the energy $W_0 = q_0^2/2C_0$ stored by the capacitor just prior to its stepped change increase. The charge $q(t)$ during these rapid capacitance variations in time does not change its behavior being a slowly time-varying parameter. In this case, if $\Delta C << C_0$, the increment of the energy obtained by the capacitor at the single step moment is defined as $\Delta W = W_0\, 2\,\Delta C/C_0$.

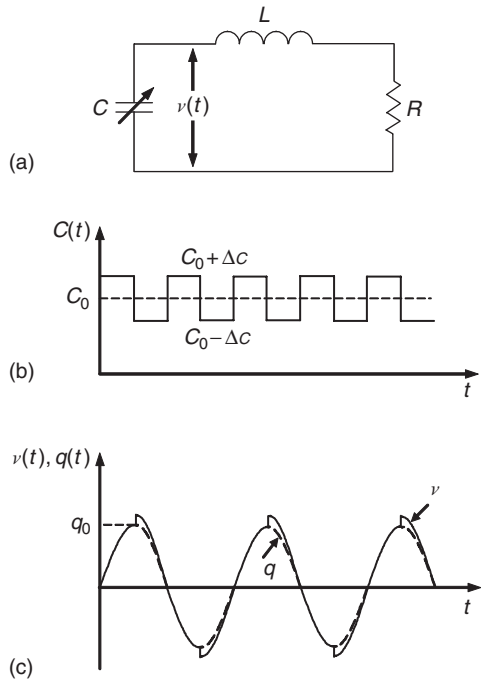



**Figure 1.31: Nonlinear resonant circuit with parametric pumping.**

The maximum energy contribution into the oscillation system will be at the times of maximum charge amplitude $q_0$ and no energy contribution will be at zero crossing. This means that the capacitance as a parameter changes two times faster than the oscillation frequency. The entire energy increment into the system for a period will be $2\Delta W$. At the same time, the energy lost for a period $T$ is defined as $0.5R(dq/dt)^2T = \pi\,\omega q_0^2 R$, where $q = q_0 \sin \omega t$. If the losses in the oscillation system are smaller than the energy input into the system for $m > 0.5\,\pi\omega RC_0$, where $m = \Delta C/C_0$ is the parameter modulation factor, the build-up of the self-oscillations can occur. Such a process of the excitation of self-oscillations due to periodic changes of the energy-storing parameter of an oscillation system is called the *parametric excitation of self-oscillations* or *parametric resonance*. If the capacitance $C$ varies with the same periodicity but having a different behavior, quantitatively the result will be the same.

Now assume that the nonlinear capacitance $C$ in the oscillation system is time-varying according to

$$C(t) = \frac{C_0}{1 + m\cos pt}, \tag{1.101}$$

where $p = 2\omega/n$ is the frequency of the parameter variation, $\omega$ is the frequency of the self-oscillations, and $n = 1, 2, 3, \ldots$.

The voltage across the nonlinear capacitance $C$ with abrupt junction sensitivity $\gamma = 0.5$ can be written as

$$v(t) = \frac{1}{C_0}\left(q - \beta q^2\right), \tag{1.102}$$

where $C_0$ is the small-signal capacitance value corresponding to the dc bias condition and $\beta$ is the coefficient responsible for the capacitance nonlinear behavior. The mathematical description of parametric oscillations in a single-resonant oscillation system with a time-varying junction capacitance $C(t)$ can be done based on the second-order differential equation characterizing this circuit, which can generally be written in the form of

$$\frac{d^2q}{dt^2} + 2\delta\frac{dq}{dt} + \omega_0^2(1 + m\cos pt)\left(q - \beta q^2\right) = 0, \tag{1.103}$$

where $\omega_0 = 1/\sqrt{LC_0}$ is the small-signal resonant frequency, $2\delta = \omega_0/Q$ is the dissipation factor, and $Q = \omega_0 L/R$ is the quality factor of the resonant circuit [28]. In a linear case when $\beta = 0$, Eq. (1.103) simplifies to a well-known Mathieu equation, the stable and unstable solutions and important properties of which are thoroughly developed and analyzed.

The basic results in a graphical form presenting the domains of the potential parametric instability as a function of the parameter $n = 2\omega_0/p$ are plotted in Fig. 1.32. The shaded areas corresponding to a growing self-oscillating process with a frequency $\omega = np/2 \approx \omega_0$ rise, and their ends are located on the line having an angle $\varphi$ with horizontal axis. This means that the greater the dissipation factor $2\delta$ of the oscillation system, the greater modulation factor $m$ is

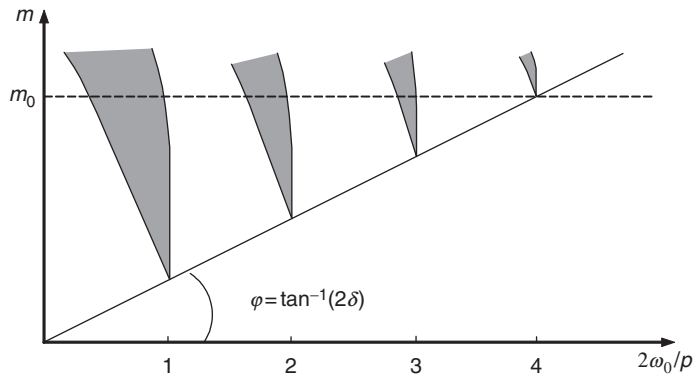



**Figure 1.32: Domains of parametric instability for damping systems.**

necessary to realize the parametric oscillations. For a fixed modulation factor $m_0$, the width of the instability domain for different $n$ is different, being smaller for higher $n$. As this number grows due to more seldom energy input into the system ($p = 2\omega/n$), it is necessary to increase the modulation factor. The effect of nonzero $\beta$ in the nonlinear voltage-charge dependence given in Eq. (1.102) leads to a deviation of the oscillation frequency in a steady-state mode from its start-up value since the averaged junction capacitance value differs from its small-signal value for a large-signal mode. The difference becomes greater with a growth of the oscillation amplitude reaching the border of the instability domain. This decreases energy input into the oscillation, thus limiting the increase in the amplitude.

Consequently, the most probable parametric oscillations in the nonlinear power amplifier can occur at a subharmonic frequency $\omega_{1/2} = \omega_p/2$, where $\omega_p$ is the operating frequency varying the device capacitance. In this case, the subharmonic frequency $\omega_{1/2}$ corresponds to the resonant frequency $\omega_0$ of the circuit shown in Fig. 1.31($a$) being equal to half the operating frequency $\omega_p$, that is $n = 1$ and $p = \omega_p = 2\omega_0$. Hence, to eliminate such a parasitic subharmonic parametric oscillation, it is necessary to provide the circuit design solution when the device output can see very high impedance at a subharmonic frequency $\omega_{1/2}$. Alternatively, an additional lossy element in the subharmonic circuit with its proper isolation from the fundamental circuit can be incorporated. In other words, it is necessary to break out any possible resonant conditions at the subharmonic frequency component, which can cause the parametric oscillations.

## References

[1] A. I. Berg, *Theory and Design of Vacuum-Tube Generators* (in Russian), Moskva: GEI, 1932.

[2] V. I. Kaganov, *Transistor Radio Transmitters* (in Russian), Moskva: Energiya, 1976.

[3] G. A. Holle and H. C. Reader, ''Nonlinear MOSFET Model for the Design of RF Power Amplifiers,'' *IEE Proc. Circuits Devices Syst.,* vol. 139, pp. 574–580, October 1992.

[4] A. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[5] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, ''A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF LDMOS FETs,'' *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 419–422.

[6] C. Fager, J. C. Pedro, N. B. Carvalho, and H. Zirath, ''Prediction of IMD in LDMOS Transistor Amplifiers Using a New Large-Signal Model,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-50, pp. 2834–2842, December 2002.

[7] J.-M. Dortu, J.-E. Muller, M. Pirola, and G. Ghione, ''Accurate Large-Signal GaAs MESFET and HEMT Modeling for Power MMIC Amplifier Design,'' *Int. J. Microwave and Millimeter-Wave Computer-Aided Eng.*, vol. 5, pp. 195–208, September 1995.

[8] A. J. McCamant, G. D. McCormack, and D. H. Smith, ''An Improved GaAs MESFET Model for SPICE,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-38, pp. 822–824, June 1990.

[9] C-J. Wei, Y. Tkachenko, and D. Bartle, ''An Accurate Large-Signal Model of GaAs MESFET Which Accounts for Charge Conservation, Dispersion, and Self-Heating,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 1638–1644, November 1998.

[10] T. Kacprzak and A. Materka, ''Compact DC Model of GaAs FET's for Large-Signal Computer Calculation,'' *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 211–213, April 1983.

[11] I. Angelov, H. Zirath, and N. Rorsman, ''A New Empirical Nonlinear Model for HEMT and MESFET Devices,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-40, pp. 2258–2266, December 1992.

[12] N. M. Rohringer and P. Kreuzgruber, ''Parameter Extraction for Large-Signal Modeling of Bipolar Junction Transistors,'' *Int. J. Microwave and Millimeter-Wave Computer-Aided Eng.*, vol. 5, pp. 161–272, September 1995.

[13] J. P. Fraysee, D. Floriot, P. Auxemery, M. Campovecchio, R. Quere, and J. Obregon, ''A Non-Quasi-Static Model of GaInP/AlGaAs HBT for Power Applications,'' *1997 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 377–382, June 1997.

[14] M. Reisch, *High-Frequency Bipolar Transistors*, Berlin: Springer, 2003.

[15] V. M. Bogachev and V. V. Nikiforov, *Transistor Power Amplifiers* (in Russian), Moskva: Energiya, 1978.

[16] L. J. Giacoletto, ''Study of n-p-n Alloy Junction Transistors from DC through Medium Frequencies,'' *RCA Rev*., vol. 15, pp. 506–562, December 1954.

[17] A. N. Rudiakova, ''BJT Class-F Power Amplifier Near Transition Frequency,'' *IEEE Trans. Microwave Theory Tech*., vol. MTT-53, pp. 3045–3050, September 2005.

[18] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons, 1980.

[19] B. M. Lee, ''Apply Wideband Techniques to Balanced Amplifiers,'' *Microwaves*, vol. 19, pp. 83–88, April 1980.

[20] J. M. Rollett, ''Stability and Power Gain Invariants of Linear Two-Ports,'' *IRE Trans. Circuit Theory Appl*., vol. CT-9, pp. 29–32, January 1962.

[21] J. G. Linvill and L. G. Schimpf, ''The Design of Tetrode Transistor Amplifiers,'' *Bell Syst. Tech. J*., vol. 35, pp. 813–840, April 1956.

[22] O. Muller and W. G. Figel, ''Stability Problems in Transistor Power Amplifiers,'' *Proc. IEEE*, vol. 55, pp. 1458–1466, August 1967.

[23] O. Muller, ''Internal Thermal Feedback in Fourpoles, Especially in Transistors,'' *Proc. IEEE*, vol. 52, pp. 924–930, August 1964.

[24] J. Vidkjaer, ''Instabilities in RF-Power Amplifiers Caused by a Self-Oscillation in the Transistor Bias Network,'' *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 703–712, October 1976.

[25] D. R. Lohrmann, ''Parametric Oscillations in VHF Transistor Power Amplifiers,'' *Proc. IEEE*, vol. 54, pp. 409–410, March 1966.

[26] D. R. Lohrmann, ''Amplifiers Has 85% Efficiency While Providing up to 10 Watts Power Over a Wide Frequency Band,'' *Electronic Design*, vol. 14, pp. 38–43, March 1966.

[27] P. Penfield and R. P. Rafuse, *Varactor Applications*, Cambridge: The M.I.T. Press, 1962.

[28] V. V. Migulin, V. I. Medvedev, E. R. Mustel, and V. N. Parygin, *Basic Theory of Oscillations*, Moscow: Mir Publishers, 1983.

This page intentionally left blank

CHAPTER 2

# Class-D Power Amplifiers

In this chapter, the different configurations of Class-D power amplifiers are presented—the increased efficiency of which is a result of employing the active device as switches. First, the switched-mode power amplifiers with resistive load of different configurations, which can be considered driver power amplifiers, are discussed. Then, the current-switching and voltage-switching configurations based on complementary and transformer-coupled topologies are analyzed. The effect of the saturation resistance, rectangular and sinusoidal driving signals, finite transition time, and parasitic shunt capacitance and series inductance is demonstrated. The practical design examples of voltage-switching and current-switching Class-D power amplifiers intended to operate at high frequencies and microwaves are described.

## 2.1 Switched-Mode Power Amplifiers with Resistive Load

The efficiency of a power amplifier can be maximized if the active device is operated as a switch. When the transistor is turned on, the voltage is nearly zero and high current is flowing through the device; that is, the transistor acts as a low resistance (closed switch) during this part of a period. When the transistor is turned off, the current is zero and there is high voltage across the device; that is, the transistor acts as an open switch during the other part of a period.

Let us consider the three types of a switched-mode power amplifier with resistive load: a single-ended amplifier, a complementary voltage-switching push-pull amplifier, and a transformer-coupled current-switching push-pull amplifier [1]. Fig. 2.1(*a*) shows the simplified circuit schematic of a switched-mode single-ended bipolar power amplifier, where $L_{ch}$ is the RF choke required to isolate a dc power supply from RF circuit, $C_b$ is the bypass capacitor, and $C_0$ is the blocking capacitor with the supply voltage $V_{cc}$ applied to its plates.

The theoretical analysis of the operation conditions of a single-ended switching mode power amplifier can be carried out based on an equivalent circuit shown in Fig. 2.1(*b*), where the active device is considered a switch with a saturation resistance $r_{sat}$ that is driven in such a way to provide the device switching between its on-state and off-state operation conditions under an assumption of a 50% duty cycle.

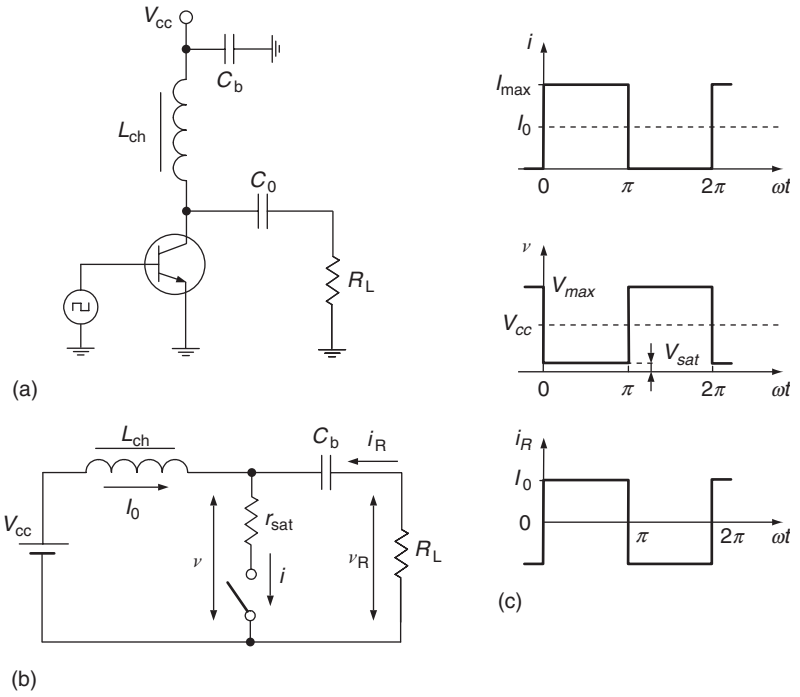



**Figure 2.1: Switched-mode single-ended power amplifier.**

When switch is on for $0 \leq \omega t \leq \pi$,

$$i(\omega t) = I_{\max} = \frac{V_{cc} + R_L I_0}{R_L + r_{sat}} \tag{2.1}$$

$$v(\omega t) = V_{sat} = r_{sat} I_{\max} \tag{2.2}$$

$$i_R(\omega t) = I_0 \tag{2.3}$$

$$v_R(\omega t) = R_L I_0, \tag{2.4}$$

where $I_0$ is the dc current, $I_{\max}$ is a peak collector current, $V_{sat}$ is the saturation voltage, and $R_L$ is the load resistance.

When switch is off for $\pi \leq \omega t \leq 2\pi$,

$$i(\omega t) = 0 \tag{2.5}$$

$$v(\omega t) = V_{\max} = V_{cc} + R_L I_0 \tag{2.6}$$

$$i_R(\omega t) = -I_0 \tag{2.7}$$

$$v_R(\omega t) = -R_L I_0, \tag{2.8}$$

where $V_{max}$ is a peak collector voltage.

The rectangular collector voltage, collector current, and load current waveforms are shown in Fig. 2.1($c$) demonstrating that zero collector current corresponds to maximum collector voltage, and minimum collector voltage corresponds to maximum collector current. However, since the current flowing to the load is not sinusoidal, its harmonic components are also presented in the output spectrum.

The dc current $I_0$ can be calculated by applying a Fourier transform to Eq. (2.1) from

$$I_0 = \frac{1}{2\pi}\int_0^{\pi} i(\omega t)\, d(\omega t) = \frac{V_{cc}}{R_L + r_{sat}}\left(1 + \frac{r_{sat}}{R_L + r_{sat}}\right)^{-1}. \tag{2.9}$$

Similarly, the fundamental-frequency current amplitude $I$ can be calculated from

$$I = \frac{1}{\pi}\int_0^{\pi} i(\omega t)\sin(\omega t)\, d(\omega t) = \frac{4}{\pi} I_0. \tag{2.10}$$

Taking into account that $I_{max} = 2I_0$ for a duty cycle of 50% or a conduction angle of 180°, the fundamental-frequency output power $P$ can be obtained by

$$P = \frac{1}{2} I^2 R_L = \frac{8}{\pi^2}\frac{R_L}{(R_L + r_{sat})^2}\frac{V_{cc}^2}{\left(1 + \frac{r_{sat}}{R_L + r_{sat}}\right)^2}. \tag{2.11}$$

Fig. 2.2($a$) shows the simplified circuit schematic of a quasi-complementary voltage-switching push-pull bipolar power amplifier, where $C_b$ is the bypass capacitor, $C_0$ is the blocking capacitor, and $R_L$ is the load resistance. The input transformer causes both active devices to be driven with currents that are 180° out-of-phase by reversing one secondary winding on the transformer. However, there is no need in phase reversing if the transistors are true-complementary with different base or channel majority-carrier type that simplifies the circuit schematic. Note than any type of the vacuum tubes, bipolar and MOSFET transistors can be used in this circuit if suitable drive is applied. Due to the grounding effect of a bypass capacitor $C_b$, the RF connection of the transistor outputs is parallel, thus resulting in an equivalent load resistance equal to $2R_L$ for each device.

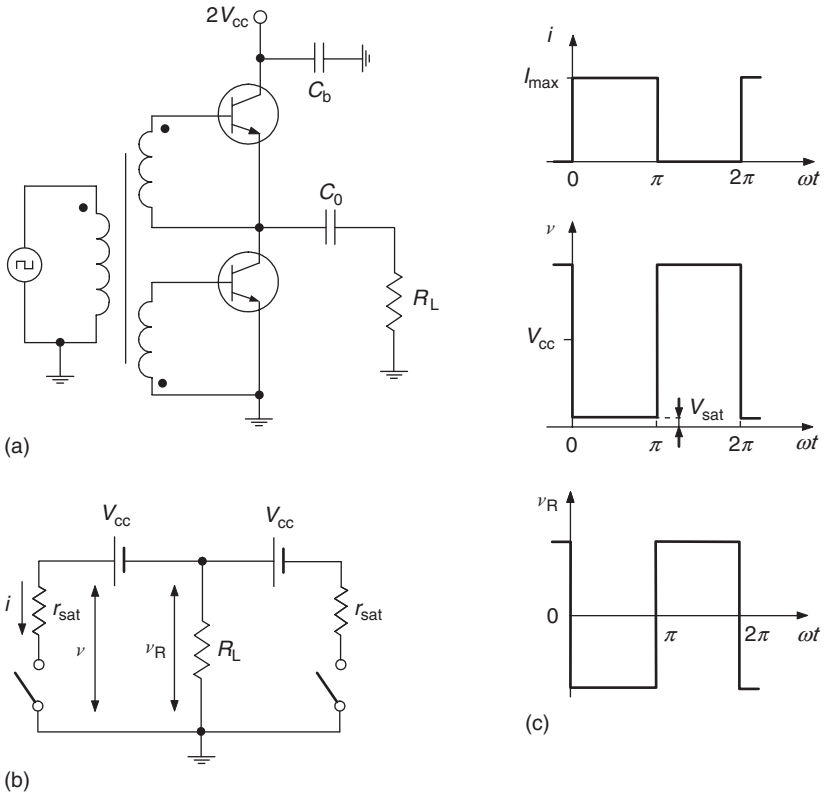



**Figure 2.2: Voltage-switching push-pull power amplifier.**

The theoretical analysis of the operation conditions of a quasi-complementary voltage-switching push-pull power amplifier is based on its equivalent circuit shown in Fig. 2.2(*b*), where each active device is considered a switch with a saturation resistance $r_{sat}$ that is driven in such a way to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty cycle. It should be noted that, for a voltage-switching push-pull power amplifier, the operation conditions with duty cycles equal or less than 50% are acceptable only, since, when both devices are turned on for duty cycles greater than 50%, both dc power supplies are connected to each other through the small saturation resistances of the identical transistors equal to $2r_{sat}$, thus resulting in the significant efficiency reduction due to an increased total current flowing through both transistors.

When the left-hand switch is on for $0 \leq \omega t \leq \pi$,

$$i(\omega t) = I_{max} = \frac{V_{cc}}{R_L + r_{sat}} \tag{2.12}$$

$$v(\omega t) = V_{\text{sat}} = r_{\text{sat}} I_{\max} \tag{2.13}$$

$$v_{\text{R}}(\omega t) = -R_{\text{L}} I_{\max}. \tag{2.14}$$

When the left-hand switch is off for $\pi \leq \omega t \leq 2\pi$,

$$i\,(\omega t) = 0 \tag{2.15}$$

$$v\,(\omega t) = V_{\max} = V_{\text{cc}} \left(2 - \frac{r_{\text{sat}}}{R_{\text{L}} + r_{\text{sat}}}\right) \tag{2.16}$$

$$v_{\text{R}}\,(\omega t) = V_{\text{R}} = R_{\text{L}} I_{\max}. \tag{2.17}$$

The dc current $I_0$ can be calculated by applying a Fourier transform to Eq. (2.12) from

$$I_0 = \frac{1}{2} \frac{V_{\text{cc}}}{R_{\text{L}} + r_{\text{sat}}}. \tag{2.18}$$

The fundamental-frequency output power $P$ can be obtained using Eqs. (2.12) and (2.17) by

$$P = \frac{8}{\pi^2} \frac{V_{\text{R}}^2}{R_{\text{L}}} = \frac{8}{\pi^2} \frac{R_{\text{L}}}{(R_{\text{L}} + r_{\text{sat}})^2} V_{\text{cc}}^2. \tag{2.19}$$

The rectangular collector current, collector voltage, and load voltage waveforms are shown in Fig. 2.2($c$) demonstrating that zero collector current corresponds to maximum collector voltage, and minimum collector voltage corresponds to maximum collector current. However, since the voltage on the load is not sinusoidal, its harmonic components are also presented in the output spectrum. The maximum collector voltage peak factor for an idealized case of zero saturation resistance is equal to $v/V_{\text{cc}} = 2$.

Fig. 2.3($a$) shows the simplified circuit schematic of a transformer-coupled current-switching push-pull bipolar power amplifier, where $C_{\text{b}}$ is the bypass capacitor, $C_0$ is the blocking capacitor, $L_{\text{ch}}$ is the RF choke, and $R_{\text{L}}$ is the load resistance. As before, the input transformer causes both active devices to be driven with currents that are 180° out-of-phase. However, the transistors of the same type have the series output RF connection with an equivalent load resistance equal to $R_{\text{L}}/2$ for each device. The RF chokes provide bipolar $\pm I_0$ pulses of the current flowing to the load through the output balanced-to-unbalanced transformer.

The theoretical analysis of the operation conditions of a transformer-coupled current-switching push-pull power amplifier is based on its equivalent circuit shown in Fig. 2.3($b$), where each active device is considered a switch with a saturation resistance $r_{\text{sat}}$ that is driven in such a way to provide an alternating switching between the on-state and off-state operation

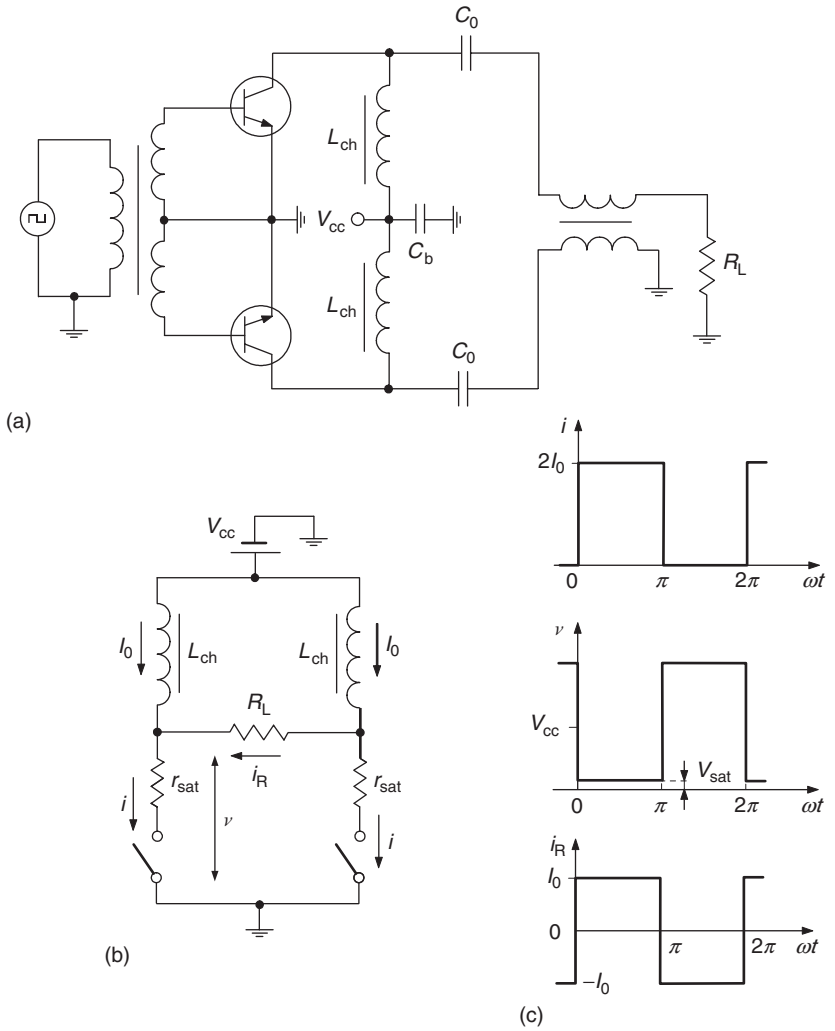



**Figure 2.3: Current-switching push-pull power amplifier.**

conditions of the transistor under an assumption of a 50% duty cycle. It should be noted that, for a current-switching push-pull power amplifier, the operation conditions with duty cycles equal or greater than 50% are acceptable only, since, when both devices are turned off for duty cycles less than 50%, the choke currents will result in significant voltage increase at the device collectors that may cause their breakdown.

When the left-hand switch is on for $0 \leq \omega t \leq \pi$,

$$i(\omega t) = I_{\max} = 2I_0 \tag{2.20}$$

$$v(\omega t) = V_{\text{sat}} = r_{\text{sat}} I_{\max} \tag{2.21}$$

$$i_R(\omega t) = I_R = I_0. \tag{2.22}$$

When the left-hand switch is off for $\pi \leq \omega t \leq 2\pi$,

$$i(\omega t) = 0 \tag{2.23}$$

$$v(\omega t) = V_{max} = (R_L + 2r_{sat})I_0 \tag{2.24}$$

$$i_R(\omega t) = -I_0. \tag{2.25}$$

The dc supply voltage $V_{cc}$ can be calculated by applying a Fourier transform to Eqs. (2.21) and (2.24) from

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)\, d(\omega t) = \frac{V_{max} + V_{sat}}{2}. \tag{2.26}$$

The dc current $I_0$ can then be obtained by

$$I_0 = \left(\frac{1}{2} + 2\frac{r_{sat}}{R_L}\right)^{-1} \frac{V_{cc}}{R_L}. \tag{2.27}$$

Finally, the fundamental-frequency output power $P$ can be written using Eqs. (2.22) and (2.27) as

$$P = \frac{8}{\pi^2} I_R^2 R_L = \frac{8}{\pi^2}\left(\frac{1}{2} + 2\frac{r_{sat}}{R_L}\right)^{-2} \frac{V_{cc}^2}{R_L}. \tag{2.28}$$

To provide sufficient isolation between the two transistors, it is advisable to use the balanced circuit schematic of a switched-mode push-pull power amplifier with an additional broadband transformer Tr1 and a ballast resistor $R_{bal}$ connected to its midpoint through the blocking capacitor $C_0$, as shown in Fig. 2.4. In this case, when $R_{bal} \to 0$, the balanced push-pull schematic transforms to a transformer-coupled voltage-switching push-pull circuit, while when $R_{bal} \to \infty$, this schematic represents a transformer-coupled current-switching push-pull power amplifier. If both transistors are identical, they operate independently from each other being fully isolated, and such a switched-mode balanced power amplifier can be considered as the two switched-mode single-ended power amplifiers operating independently with opposite phases on the same load through the balanced power combiner including a balanced-to-unbalanced transformer Tr2. Since the output currents from both transistors are combined at the load resistor $R_L$ and subtracted at the ballast resistor $R_{bal}$, the load output power spectrum contains the powers corresponding to the fundamental-frequency and odd harmonic components, while the even harmonic components are combined at the ballast resistor.

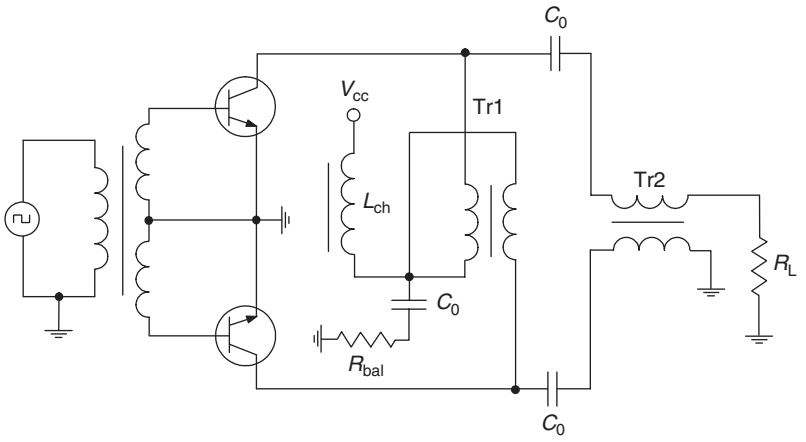



**Figure 2.4: Transformer-coupled switching push-pull power amplifier.**

Generally, the choice of a conduction angle of 180° is optimal since, in this case, it provides the collector efficiency close to maximum, the maximum voltage peak factor of less than 2, the maximum fundamental-frequency power delivered to the load, and zero power at even harmonics for all types of the switched-mode power amplifiers with resistive load. The maximum collector efficiency when the saturation $r_{sat}$ is equal to zero can be obtained using Eqs. (2.9), (2.11), (2.18), (2.19), (2.27), and (2.28) by

$$\eta = \frac{P}{P_0} = \frac{8}{\pi^2} \cong 81\%. \tag{2.29}$$

Consequently, with a rectangular voltage waveform on the load, the relative harmonic power is about 19% of the total output power. As a result, this switched-mode single-ended and push-pull power amplifier can be directly used as the driver power amplifiers when the harmonic level and power loss at the harmonics are not so significant. If it is intended to be used as a final power-amplifier stage, the special filter sections must be included between the device output and the load to suppress the harmonic components down to the required level. For example, a filter-diplexer can be used to separate the signals with fundamental frequency and its harmonic components, as shown in Fig. 2.5(*a*). The simplest representation of a filter-diplexer is a parallel connection of a single low-pass filter section and a single high-pass filter section shown in Fig. 2.5(*b*). To further improve isolation between these two branches, the number of the low-pass and high-pass filter sections can be increased. The better passband and stopband performance with higher cutoff rate can be obtained by using of the elliptic function or Chebyshev polynomial filters. Fig. 2.5(*c*) shows an example of a filter-diplexer using a single passband filter section for a fundamental-frequency signal having very high impedance at the second and higher-order harmonic components, and a single stopband filter section for a fundamental-frequency signal with minimum attenuation at the second and higher-order

harmonic components. In addition, there is a possibility to improve efficiency of the power amplifier by using a power-recycling technique when the harmonic power can be transformed to the dc power by means of the diode RF-to-dc converter and returned back to the dc power supply.

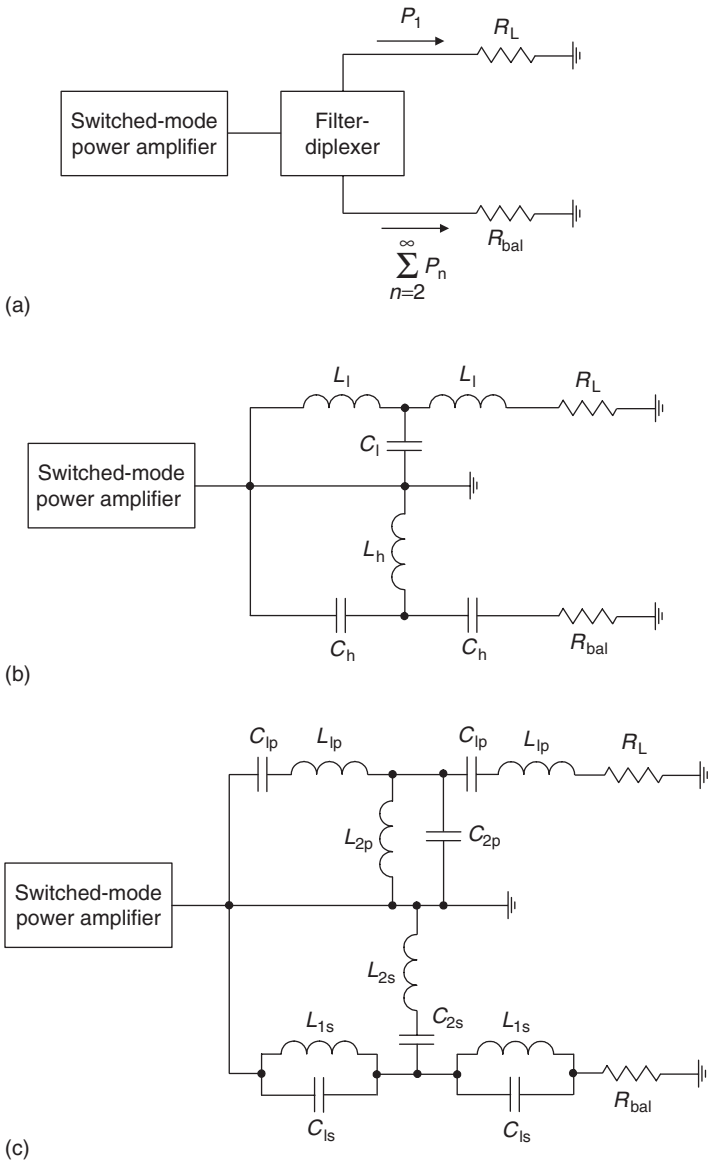



**Figure 2.5: Switched-mode power amplifiers with filter-diplexer.**

## 2.2 Complementary Voltage-Switching Configuration

The switched-mode power amplifiers with output filter tuned to the fundamental frequency, which were called Class-D power amplifiers, transform ideally the total dc power into a fundamental-frequency power delivered to the load without power losses at the harmonics, unlike the switched-mode power amplifiers with resistive load [4, 5]. Conceptually, a Class-D power amplifier employs a pair of active devices operating in a push-pull mode and a tuned output circuit. The active devices are driven to act as a two-pole switch that defines either a rectangular voltage or rectangular current collector (or drain) waveforms. The output circuit is tuned to the switching frequency and removes ideally its all-harmonic components resulting in a purely sinusoidal signal delivered to the load. Consequently, the theoretical efficiency of an idealized Class-D power amplifier achieves 100%. Let us consider the basic principles, circuit schematics, and voltage-current waveforms corresponding to the different types of a Class-D power amplifier with output filter [1, 2, 3].

Fig. 2.6(*a*) shows the simplified circuit schematic of a quasi-complementary voltage-switching Class-D bipolar power amplifier consisting of the same type of the active devices, fundamentally tuned series $L_0C_0$ filter, and load resistance $R_L$. The large-value bypass capacitor $C_b$ is necessary to isolate the dc power supply by bypassing the RF current to ground. The input transformer causes both active devices to be driven with currents that are $180^\circ$ out-of-phase by reversing one secondary winding on the transformer. However, there is no need in phase reversing if the transistors are true-complementary with different base or channel majority-carrier type that simplifies the circuit schematic. Note than any type of the vacuum tubes, bipolar and MOSFET transistors, can be used in this circuit if suitable drive is applied. Due to the grounding effect of a bypass capacitor $C_b$, the RF connection of the transistor outputs is parallel, thus resulting in an equivalent load resistance equal to $2R_L$ for each device.

To determine the collector voltage and current waveform and to calculate the output power and collector efficiency, the following assumptions are taken into account:

- Power loss due to flow of leakage current during transistor pinch-off is negligible.
- Power loss due to non-ideal tuning is negligible.
- Power loss during switching transitions is negligible.

In this case, each active device is considered a switch with the saturation resistance $r_{sat}$ shown in Fig. 2.6(*b*) that is driven in such a way as to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty cycle. The alternating half-period switching of the two transistors between their pinch-off mode and voltage-saturation mode results in rectangular collector-voltage pulses with a maximum amplitude of $2V_{cc}$, as shown in Fig. 2.6(*c*). The collector-voltage pulses, which contain only the odd-harmonic

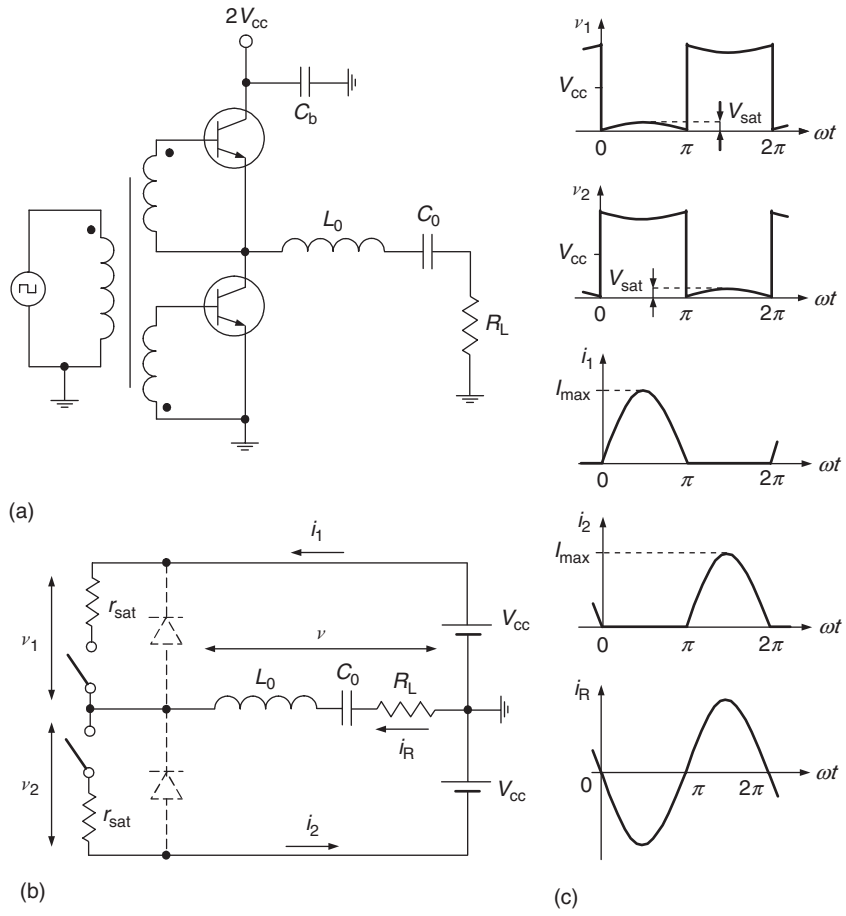



**Figure 2.6: Complementary voltage-switching configuration with series filter.**

components, are applied to the series $L_0C_0$ filter with high-loaded quality factor $Q_L = \omega L_0/R_L >> 1$ tuned to the fundamental frequency $\omega_0 = 1/\sqrt{L_0C_0}$ resulting in the fundamental-frequency sinusoidal current $i_R = -I_R \sin \omega t$ flowing to the load $R_L$. The half waves of this current flow in turn through the transistors representing the half-sinusoidal collector current pulses that contain the fundamental-frequency, second and higher-order even harmonic components only. The shape of the saturation voltage with maximum amplitude $V_{sat}$ is fully determined by the collector current waveform when $i(\omega t) > 0$ according to $v_{sat}(\omega t) = r_{sat} i(\omega t)$, where $i(\omega t) = i_1(\omega t) = i_2(\omega t)$ for a symmetrical circuit with identical transistors. The collector voltage peak factor is equal to $v/V_{cc} = 2$.

It should be noted that, for an operation with conduction angles less than 180° when both active devices are turned on for duty cycles less than 50%, there is a time period when both active devices are turned off simultaneously. Therefore, in order that the load current $i_R(\omega t)$

could flow continuously, it is necessary to include a diode in parallel to each device, as shown in Fig. 2.6(*b*). The operation conditions with conduction angles greater than 180° are unacceptable, since both dc power supplies are connected to each other through the small saturation resistances of the identical transistors equal to $2r_{sat}$, thus resulting in the significant efficiency reduction due to an increased total current flowing through both transistors.

Now let us determine the voltage $v(\omega t) = v_1(\omega t) - V_{cc}$ at the input of a series $L_0C_0$ circuit and collector current $i_1(\omega t)$ for the first transistor working as a switch with a saturation resistance $r_{sat}$. When switch is on for $0 \leq \omega t \leq \pi$,

$$v(\omega t) = -V_{cc} + r_{sat} I_R \sin \omega t \tag{2.30}$$

$$i_1(\omega t) = I_R \sin \omega t, \tag{2.31}$$

where $I_R$ is the load current amplitude.

When switch is off for $\pi \leq \omega t \leq 2\pi$,

$$v(\omega t) = V_{cc} + r_{sat} I_R \sin \omega t \tag{2.32}$$

$$i_1(\omega t) = 0. \tag{2.33}$$

The fundamental-frequency voltage amplitude $V$ of the voltage $v(\omega t)$ can be calculated by applying a Fourier transform to Eqs. (2.30) and (2.32) from

$$V = -\frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin(\omega t)\, d(\omega t) = \frac{4}{\pi} V_{cc} - r_{sat} I_R. \tag{2.34}$$

Similarly, the dc current $I_0$ can be obtained from Eq. (2.31) by

$$I_0 = \frac{1}{2\pi} \int_0^{\pi} i_1(\omega t)\, d(\omega t) = \frac{I_R}{\pi}. \tag{2.35}$$

Taking into account that $I_R = V/R_L$ and the fact that the sinusoidal output current flows through either one or another transistor depending on which device is turned on and having a half-sinusoidal waveform, using Eq. (2.34) will result in

$$I_R = I_{max} = \frac{4}{\pi} \frac{V_{cc}}{R_L} \frac{1}{1 + \frac{r_{sat}}{R_L}}. \tag{2.36}$$

The dc power $P_0$ and fundamental-frequency output power $P$ can be obtained using Eqs. (2.35) and (2.36) by

$$P_0 = 2V_{cc}I_0 = \frac{8}{\pi^2}\frac{V_{cc}^2}{R_L}\frac{1}{1+\frac{r_{sat}}{R_L}} \tag{2.37}$$

$$P = \frac{1}{2}I_R^2 R_L = \frac{8}{\pi^2}\frac{V_{cc}^2}{R_L}\frac{1}{\left(1+\frac{r_{sat}}{R_L}\right)^2}. \tag{2.38}$$

As a result, the collector efficiency $\eta$ of a quasi-complementary voltage-switching push-pull power amplifier with series filter can be written as

$$\eta = \frac{P}{P_0} = \frac{1}{1+\frac{r_{sat}}{R_L}}. \tag{2.39}$$

From Eq. (2.39), it follows that the collector efficiency is equal to 100% for an idealized case of the lossless active devices with zero saturation resistance. It should be mentioned that the dc current drawn from the power supply represents the form of a half-sinusoidal pulse train. Therefore, it is very important to provide the proper RF bypassing circuit representing either a single large-value capacitor or an additional filter with a low cutoff frequency in the power supply line including the series RF choke and shunt capacitors. In addition, the loaded quality factor for a simple series-tuned $L_0C_0$ circuit must be chosen greater than 5 to provide a good compromise between the prevention of harmonic current and coil losses. Additional harmonic suppression can be obtained by inserting standard filters between the series-tuned circuit and the load. Note that the collector efficiency degrades with increasing operating frequency where the switching transitions become an appreciable fraction of the signal period. In practice, it was found that high efficiency of a Class-D power amplifier can be maintained to frequencies of the order of $0.1f_T$ for low-power transistors and to $0.01f_T$ for high-power transistors rated at greater than 10 W, where $f_T$ is the device transition frequency [6].

The circuit schematic of the voltage-switching Class-D power amplifier shown in Fig. 2.6(*a*) is called a quasi-complementary circuit because it is based on the same type of the two identical transistors, *n-p-n* bipolar or *n*-channel MOSFET devices, each in a common emitter or a common source configuration [7]. A true-complementary power-amplifier circuit configuration requires two transistors of different types, *n-p-n* and *p-n-p* bipolar or *n*- and *p*-channel MOSFET devices. Fig. 2.7 shows the two examples of such a true-complementary voltage-switching Class-D push-pull power amplifier, a configuration with input transformer shown in Fig. 2.7(*a*), and transformerless configuration shown in Fig. 2.7(*b*). In the latter case, there is no need for a driving transformer because both transistors can be mounted on a single heat sink without electrical insulation [8]. The coupling capacitor $C_1$ must have a very low

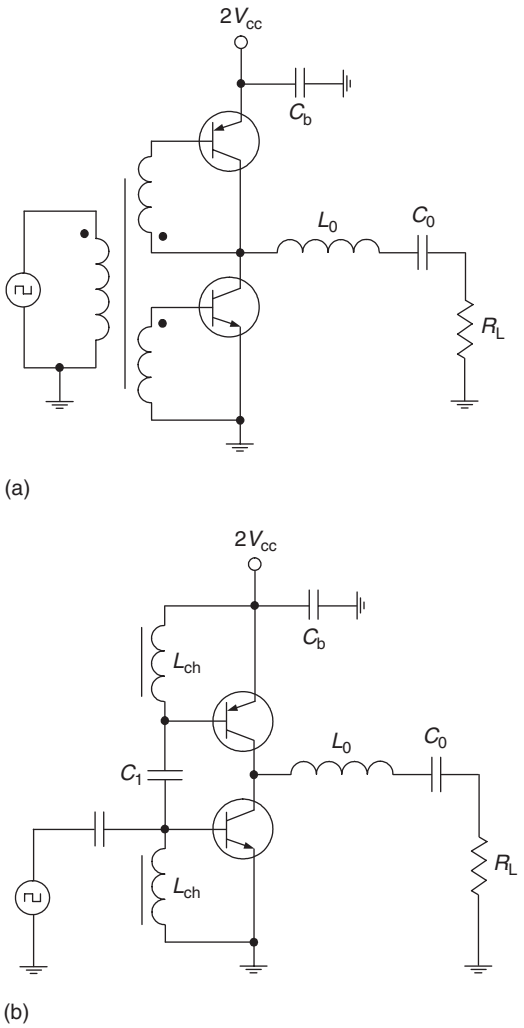



**Figure 2.7: True-complementary voltage-switching Class-D power-amplifier circuits.**

reactance to make a voltage drop at carrier frequency across it negligible compared with the input signal. Its value can be chosen as

$$C_1 >> \frac{1}{2\pi f_0 r_b}, \tag{2.40}$$

where $f_0$ is the fundamental frequency of the input voltage and $r_b$ is the series base resistance of the bipolar transistor.

However, in practice such circuits can be used at sufficiently low frequencies because of the much higher transition losses resulting from performance mismatch between the

complementary transistors. Consequently, further development in technology to provide similar electrical characteristics of truly complementary transistors would offer a new possibility for these Class-D power amplifiers, especially for transformerless configuration, which can easily be integrated in a monolithic structure.

## 2.3 Transformer-Coupled Voltage-Switching Configuration

The broadband center-tapped and balanced-to-unbalanced transformers can also be used in voltage-switching Class-D power amplifiers in much the same manner as they are used in the switched-mode power amplifiers with resistive load or conventional Class-B push-pull power amplifiers. In this case, such a configuration is called the transformer-coupled voltage-switching Class-D power amplifier. Fig. 2.8($a$) shows the simplified circuit schematic of a transformer-coupled voltage-switching Class-D bipolar power amplifier including an output series-tuned $L_0C_0$ circuit and a load resistance $R_L$. The output transformer Tr2 is considered ideal, having $m$ turns in each half of the primary winding and $n$ turns in the secondary winding. As in the complementary voltage-switching configuration, the input transformer Tr1 causes both active devices, $Q_1$ and $Q_2$, to be driven with currents that are 180° out of phase to switch on and off alternately. During the first half-cycle when transistor $Q_1$ is turned on, its collector voltage $v_1(\omega t)$ is equal to zero, assuming zero saturation resistance. As a result, dc supply voltage $V_{cc}$ is placed across one-half of the primary winding of the transformer Tr2, being then transformed to the voltage $(-n/m)V_{cc}$ on its secondary winding. When transistor $Q_2$ is turned on, dc supply voltage $V_{cc}$ is applied to the other half of the primary winding causing voltage $(n/m)V_{cc}$ to appear on the secondary winding [see Fig. 2.8(b)].

Consequently, when switch $Q_1$ is on for $0 \leq \omega t \leq \pi$,

$$v_1(\omega t) = 0 \tag{2.41}$$

$$v_2(\omega t) = 2V_{cc} \tag{2.42}$$

$$v(\omega t) = -\frac{n}{m}V_{cc}. \tag{2.43}$$

When switch $Q_1$ is off for $\pi \leq \omega t \leq 2\pi$,

$$v_1(\omega t) = 2V_{cc} \tag{2.44}$$

$$v_2(\omega t) = 0 \tag{2.45}$$

$$v(\omega t) = \frac{n}{m}V_{cc}. \tag{2.46}$$

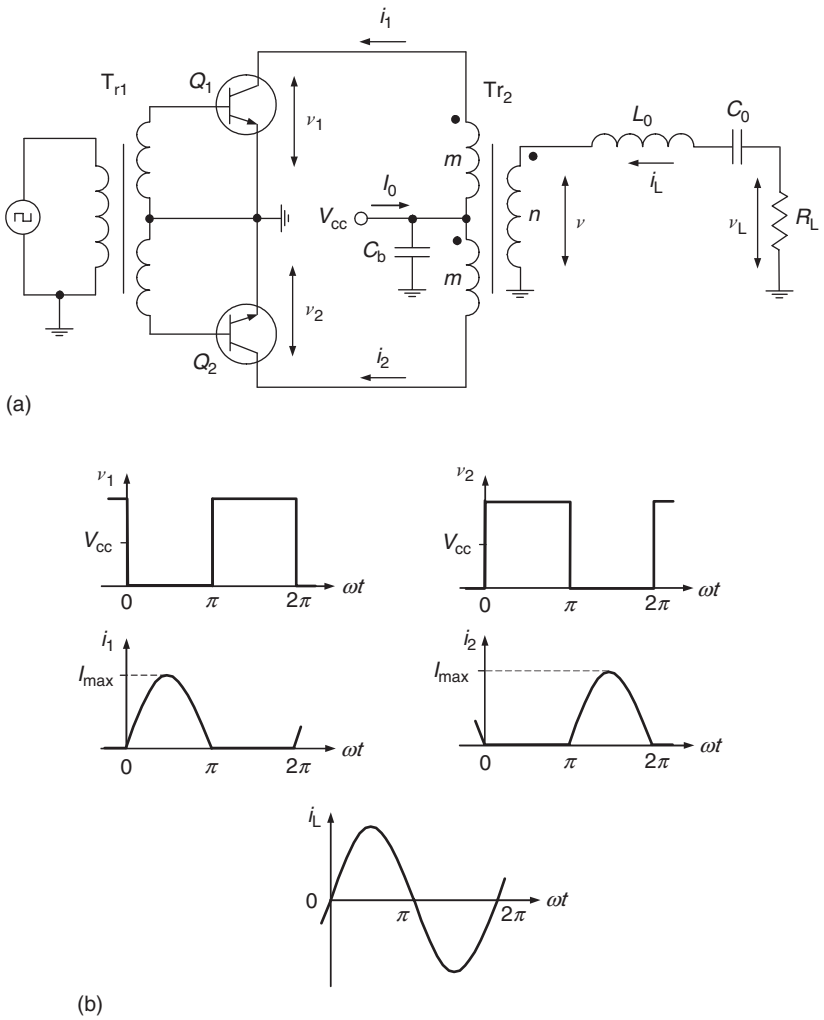



**Figure 2.8: Transformer-coupled voltage-switching push-pull configuration with series filter.**

Thus, the resulting secondary voltage $v(\omega t)$ represents a square wave with levels of $\pm(n/m)V_{cc}$, while the collector voltages are square waves with levels of 0 and $+2V_{cc}$. The fundamental-frequency voltage amplitude $V$ of the voltage $v(\omega t)$ can be calculated from

$$V_L = V = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t)\,d(\omega t) = \frac{4}{\pi}\frac{n}{m}V_{cc}, \tag{2.47}$$

where $V_L$ is the fundamental-frequency voltage amplitude on the load $R_L$.

Then, the fundamental-frequency output power $P$ can be obtained by

$$P = \frac{1}{2}\frac{V_L^2}{R_L} = \frac{8}{\pi^2}\left(\frac{n}{m}\right)^2 \frac{V_{cc}^2}{R_L} = \frac{8}{\pi^2}\frac{V_{cc}^2}{R}, \tag{2.48}$$

where

$$R = \left(\frac{m}{n}\right)^2 R_L \tag{2.49}$$

is the equivalent fundamental-frequency resistance across one-half of the primary winding of the output transformer Tr2 seen by each device output, with the other one-half of the primary winding open.

The amplitude $I_L$ of a sinusoidal current $i_L(\omega t)$ flowing to the load is given by

$$I_L = \frac{V_L}{R_L} = \frac{4}{\pi}\frac{V_{cc}}{R}. \tag{2.50}$$

Consequently, the collector currents of each transistor are half-sinusoidal waveforms with opposite phase of 180° between each other whose peak amplitudes are $(4/\pi)(V_{cc}/R)$. The dc supply current $I_0$ represents a sum of two collector currents drawn into the center tap, hence

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} [i_1(\omega t) + i_2(\omega t)]d(\omega t) = \frac{8}{\pi^2}\left(\frac{n}{m}\right)^2 \frac{V_{cc}}{R_L}, \tag{2.51}$$

resulting in the collector efficiency of 100% because the fundamental-frequency power and dc power are equal.

## 2.4 Symmetrical Current-Switching Configuration

Fig. 2.9(*a*) shows the simplified circuit schematic of a symmetrical current-switching Class-D bipolar power amplifier consisting of the same type of the active devices, fundamentally tuned parallel $L_0C_0$ filter, and load resistance $R_L$. The RF choke $L_{ch}$ connected to the center point of the inductor $L_0$ is necessary to isolate the dc power supply and make the circuit symmetrical. Each active device is considered a switch with the saturation resistance $r_{sat}$ shown in Fig. 2.9(*b*) that is driven in such a way to provide an alternating switching between the on-state and off-state operation conditions of the transistor under an assumption of a 50% duty cycle. Since the only dc current $I_0$ is flowing through the RF choke $L_{ch}$, the alternating half-period device switching between their pinch-off mode and saturation mode results in rectangular collector current pulses with a maximum amplitude of $2I_0$, as shown in Fig. 2.9(*c*).

The collector current pulses, which contain the odd harmonic components only, are applied to the parallel $L_0C_0$ filter with high-loaded quality factor $Q_L = \omega L_0/R_L >> 1$ tuned to the

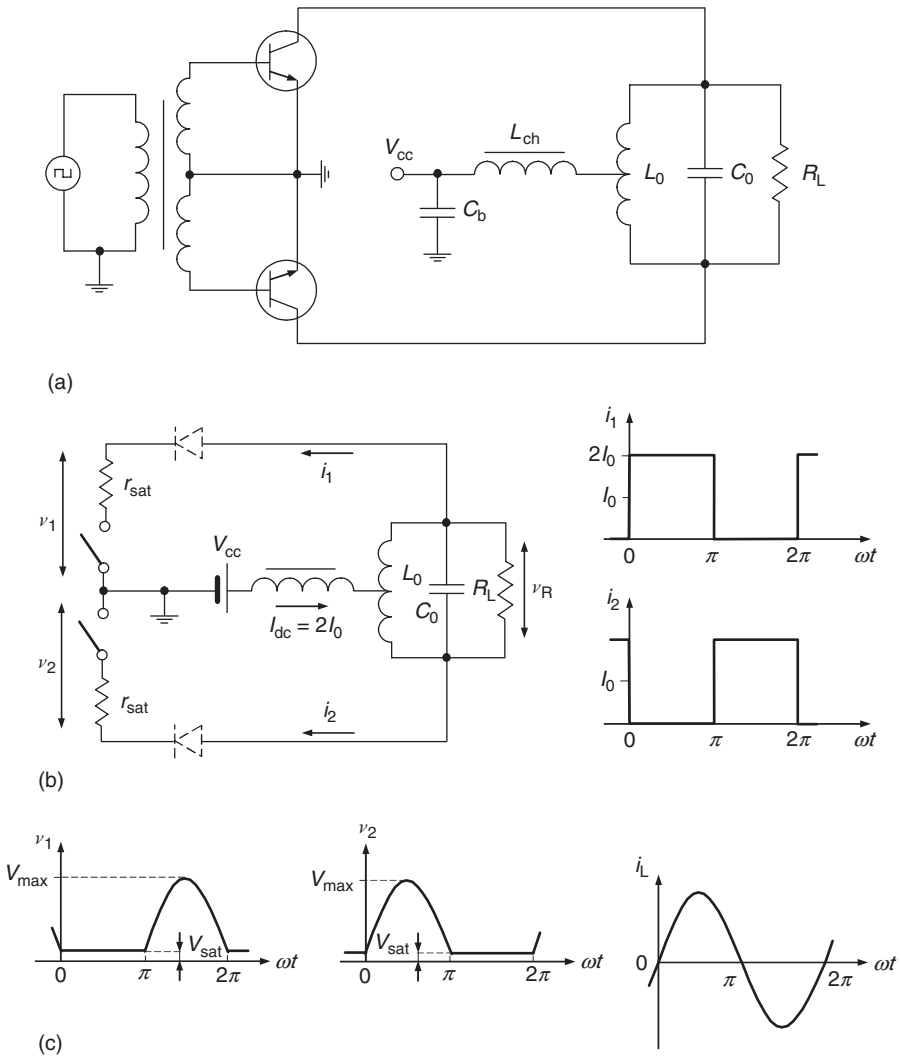



**Figure 2.9: Symmetrical current-switching configuration with parallel filter.**

fundamental frequency $\omega_0 = 1/\sqrt{L_0 C_0}$ resulting in the fundamental-frequency sinusoidal voltage $v_R = V_R \sin \omega t$ across the load $R_L$. During half a period when one transistor is turned on, the half wave of this voltage is applied to the other transistor representing the half-sinusoidal collector voltage pulses, which contain the fundamental-frequency, second and higher-order even harmonic components only. The flat shape of the saturation voltage with maximum amplitude $V_{max}$ is fully determined by the collector current waveform when $i(\omega t) > 0$ according to $v_{sat}(\omega t) = r_{sat}\, i_1(\omega t) = r_{sat}\, i_2(\omega t)$ for a symmetrical circuit with identical transistors. Unlike a complementary voltage-switching configuration, the RF

connection of the transistor outputs its series, thus resulting in an equivalent load resistance equal to $R_L/2$ for each device.

It should be noted that the symmetrical current-switching Class-D power amplifier, the collector voltage and current waveforms of which are shown in Fig. 2.9($c$), is the dual of the complementary voltage-switching Class-D power amplifier, the collector voltage and current waveforms of which are shown in Fig. 2.6($c$), because the voltage and current waveforms are interchanged. However, if, in the case of a voltage-switching configuration, the collector peak voltage is defined by the dc supply voltage $V_{cc}$ only, then, in the latter case of a current-switching configuration, the transistors represent current switches with the current amplitude defined by the dc voltage supply $V_{cc}$, saturation resistance $r_{sat}$, and load resistance $R_L$. For an operation mode with conduction angles greater than 180°, there is a time period when both active devices are turned on simultaneously, and parallel-tuned circuit is shunted by a small resistance $2r_{sat}$. Therefore, to eliminate this shunting effect accompanied by power losses in both transistors, it is necessary to include a diode in series to each device collector, as shown in Fig. 2.9($b$). However, the operation conditions with conduction angles less than 180° are unacceptable, since there are time intervals when both transistors are turned off simultaneously causing the significant increase in the collector voltage amplitude due to the growth of the current flowing through RF choke.

Now let us determine the current $i(\omega t) = i_1(\omega t) - I_0$ in a series $L_0C_0$ circuit and collector voltage $v_1(\omega t)$ for the first transistor working as a current switch with a saturation resistance $r_{sat}$. When the first switch is on for $0 \le \omega t \le \pi$, $i_1(\omega t) = 2I_0$ resulting in

$$i(\omega t) = I_0 \tag{2.52}$$

$$v_1(\omega t) = V_{sat} = 2r_{sat}I_0, \tag{2.53}$$

where $I_0$ is the dc supply current of each device.

When the first switch is off for $\pi \le \omega t \le 2\pi$, $i_1(\omega t) = 0$ resulting in

$$i\,(\omega t) = -I_0 \tag{2.54}$$

$$v_1(\omega t) = -\,(V_{max} - 2r_{sat}I_0)\sin\omega t + 2r_{sat}I_0, \tag{2.55}$$

where $V_{max}$ is the collector peak voltage.

The fundamental-frequency current amplitude $I$ of the current $i(\omega t)$ can be calculated by applying a Fourier transform to Eqs. (2.52) and (2.54) from

$$I = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin(\omega t)\,d(\omega t) = \frac{4}{\pi}I_0. \tag{2.56}$$

Similarly, the dc supply voltage $V_{cc}$ can be written from Eqs. (2.53) and (2.55) by

$$V_{cc} = \frac{1}{2\pi}\int_0^{\pi} v_1(\omega t)\,d(\omega t) = \frac{1}{\pi}\,(V_{max} - 2r_{sat}I_0). \tag{2.57}$$

Taking into account that $V_1 = V_{max} - 2r_{sat}\,I_0 = IR_L$, the dc current $I_0$ and fundamental-frequency collector voltage $V_1$ can be obtained by

$$I_0 = \left(\frac{\pi}{2}\right)^2\left(1 + \frac{\pi^2}{2}\frac{r_{sat}}{R_L}\right)^{-1}\frac{V_{cc}}{R_L} \tag{2.58}$$

$$V_1 = \pi\left(1 + \frac{\pi^2}{2}\frac{r_{sat}}{R_L}\right)^{-1}V_{cc}. \tag{2.59}$$

The dc power $P_0$ and fundamental-frequency output power $P$ can be obtained using Eqs. (2.58) and (2.59) and taking into account that $V_1 = V_R$ by

$$P_0 = 2V_{cc}I_0 = \frac{\pi^2}{2}\frac{V_{cc}^2}{R_L}\frac{1}{1 + \frac{\pi^2}{2}\frac{r_{sat}}{R_L}} \tag{2.60}$$

$$P = \frac{1}{2}\frac{V_R^2}{R_L} = \frac{\pi^2}{2}\frac{V_{cc}^2}{R_L}\frac{1}{\left(1 + \frac{\pi^2}{2}\frac{r_{sat}}{R_L}\right)^2}. \tag{2.61}$$

As a result, the collector efficiency $\eta$ of a symmetrical current-switching push-pull power amplifier with parallel filter can be written as

$$\eta = \frac{P}{P_0} = \frac{1}{1 + \frac{\pi^2}{2}\frac{r_{sat}}{R_L}}. \tag{2.62}$$

## 2.5 Transformer-Coupled Current-Switching Configuration

Fig. 2.10(*a*) shows the circuit schematic of a current-switching Class-D power amplifier where the output balanced-to-unbalanced transformer is used to connect to a standard load. In this case, such a configuration is called the transformer-coupled current-switching Class-D power amplifier, which is the dual of the transformer-coupled voltage-switching Class-D power amplifier because the collector voltage and current waveforms are interchanged. As in the transformer-coupled voltage-switching configuration, the input transformer Tr1 is

necessary to drive both active devices with currents having opposite phases for the on-to-off alternate device switching. The output transformer Tr2 is considered ideal, having $m$ turns in each half of the primary winding and $n$ turns in the secondary winding. However, the dc current supply is connected to the center tap of the transformer primary winding through the RF choke.

The load network of the transformer-coupled current-switching configuration requires a parallel fundamentally tuned resonant $L_0C_0$ circuit connected in parallel to the load $R_L$, instead of a series fundamentally tuned resonant $L_0C_0$ circuit required for the transformer-coupled voltage-switching configuration. Whichever device is turned on during the first half-cycle, it takes the entire dc current $I_0$ resulting in a rectangular collector current waveform with levels of 0 and $I_0$, as shown in Fig. 2.10($b$). Its collector voltage is equal to zero when it is turned on, assuming zero saturation resistance. Transformation of the rectangular collector currents from half of the primary winding to the secondary winding produces a rectangular current $i(\omega t)$ with levels of $\pm(m/n)I_0$.

Consequently, when switch $Q_1$ is on for $0 \leq \omega t \leq \pi$,

$$i_1(\omega t) = I_0 \tag{2.63}$$

$$i_2(\omega t) = 0 \tag{2.64}$$

$$i(\omega t) = \frac{m}{n} I_0. \tag{2.65}$$

When switch $Q_1$ is off for $\pi \leq \omega t \leq 2\pi$,

$$i_1(\omega t) = 0 \tag{2.66}$$

$$i_2(\omega t) = I_0 \tag{2.67}$$

$$i(\omega t) = -\frac{m}{n} I_0. \tag{2.68}$$

Since the output parallel-tuned resonant circuit suppresses the harmonic components of the secondary current $i(\omega t)$ allowing only the fundamental-frequency component $i_L(\omega t)$ to flow to the load $R_L$, its amplitude $I_L$ can be calculated from

$$I_L = \frac{1}{\pi} \int_0^{2\pi} i(\omega t) \sin(\omega t)\, d(\omega t) = \frac{4}{\pi} \frac{m}{n} I_0. \tag{2.69}$$

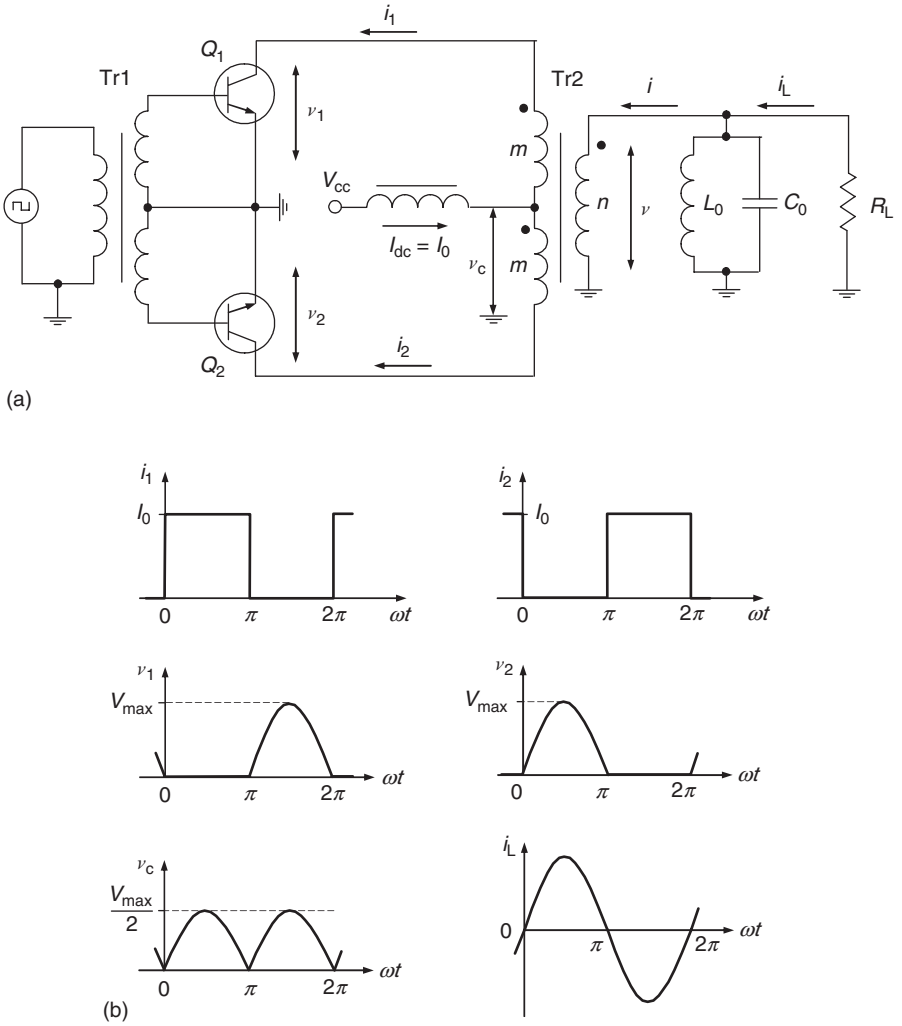



**Figure 2.10: Transformer-coupled current-switching configuration with parallel filter.**

The fundamental-frequency sinusoidal current $i_L(\omega t)$ produces the sinusoidal voltage $v(\omega t) = v_L(\omega t) = i_L(\omega t)R_L$ on the load resistance $R_L$ with amplitude

$$V_L = V = \frac{4}{\pi}\frac{m}{n}I_0 R_L, \tag{2.70}$$

where $V$ is the sinusoidal secondary voltage amplitude.

The sinusoidal voltage $v(\omega t)$ across the secondary winding is transformed to the primary winding, where it produces the sinusoidal voltage across each half of the primary winding

with amplitude of $(m/n)\,V$. Since during half a period one of the two transistors is turned on and the corresponding end of the primary winding is grounded, the peak amplitude of the voltage of the other transistor collector can be obtained by

$$V_{\max} = 2\left(\frac{m}{n}\right)V_{\mathrm{L}} = \frac{8}{\pi} I_0 R, \tag{2.71}$$

where

$$R = \left(\frac{m}{n}\right)^2 R_{\mathrm{L}} \tag{2.72}$$

is the equivalent fundamental-frequency resistance across one-half of the primary winding of the output transformer Tr2 seen by each device output, with the other one-half of the primary winding open. Thus, the sinusoidal voltage $v(\omega t)$ being transformed to the primary winding produces two half-sinusoidal collector voltages with opposite phases.

Since the center-tap voltage $v_{\mathrm{c}}(\omega t)$ represents half of the sum of the two collector voltages, its average value can be calculated using Eq. (2.71) from

$$V_{\mathrm{cc}} = \frac{1}{2\pi}\int_0^{2\pi}\left[\frac{v_1(\omega t)}{2} + \frac{v_2(\omega t)}{2}\right] d(\omega t) = \frac{8}{\pi^2}\left(\frac{m}{n}\right)^2 I_0 R_{\mathrm{L}}, \tag{2.73}$$

where $v_1(\omega t) = -V_{\max}\,\sin(\omega t)$ for $\pi \le \omega t \le 2\pi$ and $v_2(\omega t) = V_{\max}\,\sin(\omega t)$ for $0 \le \omega \le \pi$.

As a result,

$$I_0 = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_{\mathrm{cc}}}{R_{\mathrm{L}}} = \frac{\pi^2}{8}\,\frac{V_{\mathrm{cc}}}{R}. \tag{2.74}$$

Then, the peak collector voltage $V_{\max}$ given by Eq. (2.71) can be rewritten as a function of the dc supply voltage $V_{\mathrm{cc}}$ only as

$$V_{\max} = \pi V_{\mathrm{cc}}. \tag{2.75}$$

Since there is no voltage drop across RF choke, the peak value of the voltage $v_{\mathrm{c}}(\omega t)$ having a full-wave rectified shape is equal to $(\pi/2)V_{\mathrm{cc}}$. By using Eqs. (2.70) and (2.74), the fundamental-frequency output power $P$ and dc supply power $P_0$ can be obtained by

$$P = \frac{1}{2}\,\frac{V_{\mathrm{L}}^2}{R_{\mathrm{L}}} = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_{\mathrm{cc}}^2}{R_{\mathrm{L}}} \tag{2.76}$$

$$P_0 = V_{cc}I_0 = \frac{\pi^2}{8}\left(\frac{n}{m}\right)^2 \frac{V_{cc}^2}{R_L}, \tag{2.77}$$

resulting in the collector efficiency of 100% because the fundamental-frequency power and dc power are equal.

## 2.6 Voltage-Switching Configuration with Reactive Load

In practice, the load network of a switched-mode Class-D power amplifier can have a nonzero reactance at the operating frequency caused by its mistuning or influence of the parasitic-reactive device elements. Fig. 2.11(*a*) shows the circuit schematic of a quasi-complementary voltage-switching configuration with reactive load, where $C_{c1}$ and $C_{c2}$ are the equivalent collector capacitances of each transistor and $X$ is the series load network reactance. The series fundamentally tuned $L_0C_0$ circuit reduces output currents at the harmonic frequencies flowing the load to negligible level. The collector voltage waveforms of each transistor are unchanged by the load reactance. However, due to the effect of the series reactance $X$, the output current $i_R(\omega t)$ is shifted in phase relative to the collector voltage waveform, as shown in Fig. 2.11(*b*). Because of this phase shift, both collector currents $i_1(\omega t)$ and $i_2(\omega t)$ tend to be negative during a portion of each period. In this case, the series resonant circuit represents an inductive load. If both transistors $Q_1$ and $Q_2$ are MOSFET devices, the negative currents can be passed without any potential of their damage, since the MOSFET intrinsic body-drain *p-n* junction diode may be used as an antiparallel diode. However, bipolar devices in general do not conduct in reverse direction. As a result, the negative currents will charge their equivalent collector capacitances $C_c$ and $C_c$, producing large voltage spikes that can damage the transistors.

The series reactance reduces the amplitude of the output current and output power. If $Z_L = R_L + jX_L$, the load current $i_R(\omega t)$ of a complementary voltage-switching configuration with zero saturation resistance can be written using Eq. (2.36) as

$$i_R(\omega t) = \frac{4}{\pi}\frac{V_{cc}}{|Z_L|}\sin(\omega t + \varphi), \tag{2.78}$$

where the phase shift $\varphi$ is defined by

$$\varphi = \tan^{-1}\left(\frac{X_L}{R_L}\right). \tag{2.79}$$

Consequently, the fundamental-frequency power $P$ delivered to the load $R_L$ will be reduced to

$$P = \frac{8}{\pi^2}\frac{V_{cc}^2}{R_L}\rho^2, \tag{2.80}$$

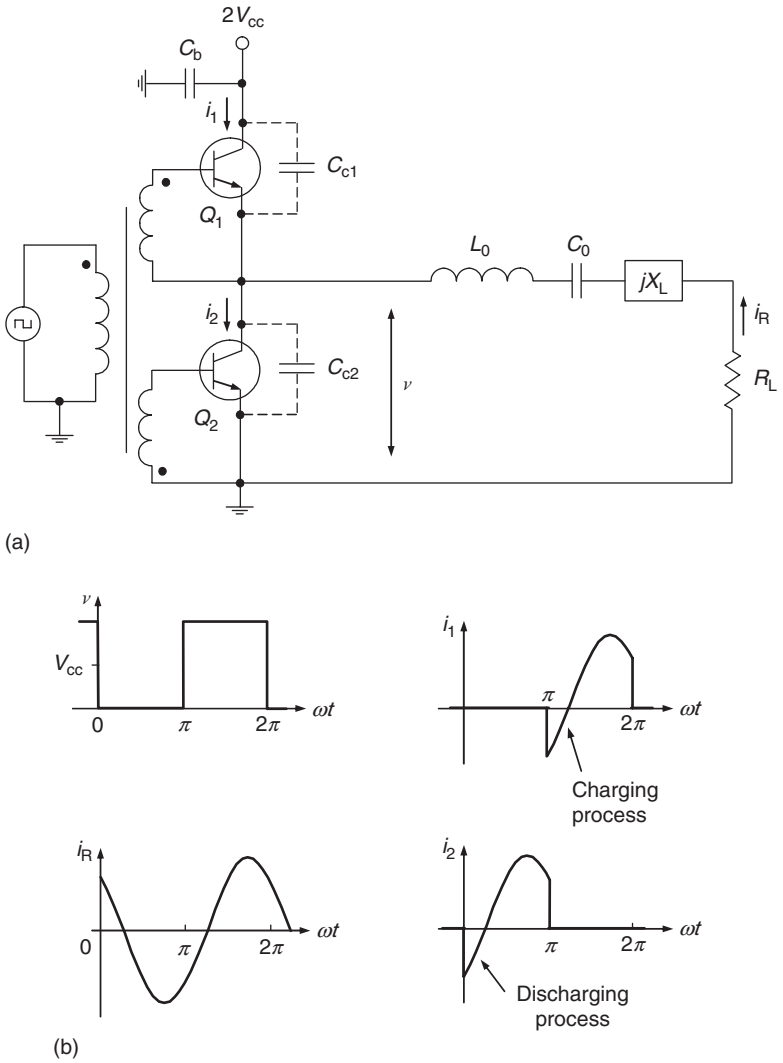



**Figure 2.11: Voltage-switching Class-D power amplifier with reactive load.**

where

$$\rho = \frac{R_{\mathrm{L}}}{|Z_{\mathrm{L}}|} < 1. \tag{2.81}$$

A suitable reverse-direction current path is provided by diodes $D_1$ and $D_2$, as shown in Fig. 2.12(*a*). In this case, the sinusoidal phase-shifted load current always passes through one of the four devices ($Q_1$, $Q_2$, $D_1$, or $D_2$), preventing the collector voltage spikes, as shown in Fig. 2.12(*b*). Here, the shunt capacitance $C_{\mathrm{c}}$ represents a sum of both collector capacitances $C_{\mathrm{c1}}$ and $C_{\mathrm{c2}}$, and may include any parasitic stray circuit capacitance associated with the

method of practical implementation. The same protection approach can be used in a transformer-coupled voltage-switching configuration. Active devices used in the symmetrical and transformer-coupled current-switching Class-D power amplifiers may be protected from the negative collector voltages by placing diodes in series with the collectors. Note that the collector efficiency of a Class-D power amplifier is essentially unchanged by the load network reactance.

The operation with a capacitive load is not recommended because the antiparallel diodes generate high reverse-recovery current spikes [9]. These spikes occur in the switch current waveforms at both the switch turn-on and switch turn-off and may destroy the transistors. The transistors are turned on at high voltage equal to $2V_{cc}$, and the transistor output capacitance is short-circuited by a low transistor saturation resistance, dissipating the energy stored in that capacitance. Therefore, the turn-on switching loss is high, the effect of a feedback capacitance is significant increasing the transistor input capacitance and the gate-drive requirements, and the turn-on transition speed is reduced. Generally, the power amplifier can operate safely with an open circuit at the output. However, it is prone to catastrophic failure if the output is short-circuited at the operating frequency close to the resonant frequency of the output series resonant $L_0C_0$ circuit.

The presence of the parasitic collector capacitances $C_{c1}$ and $C_{c2}$ causes the power losses due to finite charge storage process. When the transistor $Q_1$ is turned on and the transistor $Q_2$ is turned off, the capacitor $C_{c1}$ is discharged through the $Q_1$ and the capacitor $C_{c2}$ is charged instantaneously to $2V_{cc}$. However, when the transistor $Q_2$ is turned on and the transistor $Q_1$ is turned off, the capacitor $C_{c2}$ is discharged instantaneously through $Q_2$ and the capacitor $C_{c1}$ is charged instantaneously to $2V_{cc}$. Since this occurs twice during each period and the power losses due to energy dissipated in the both transistors with charging and discharging processes are equal, the total power losses due to finite switching time for a complementary voltage-switching Class-D power amplifier with supply voltage of $2V_{cc}$ and zero saturation resistance can be written as

$$P_s = (C_{c1} + C_{c2})(2V_{cc})^2 f_0 = 4C_c V_{cc}^2 f_0, \tag{2.82}$$

where $C_c = C_{c1} + C_{c2}$ and $f_0$ is the operating frequency. The total switching power losses described by Eq. (2.82) also can characterize the transformer-coupled voltage-switching Class-D power amplifier with a supply voltage of $V_{cc}$, in which the parasitic collector capacitances $C_{c1}$ and $C_{c2}$ are charged and discharged between 0 and $2V_{cc}$.

In the current-switching Class-D power amplifier, the parasitic capacitances do not provide charging and discharging losses since the collector currents flowing through the transistor have fixed constant values (either zero or maximum $I_{dc}$). However, there is another mechanism of power losses associated with parasitic inductances $L_{c1}$ and $L_{c2}$ (due to finite

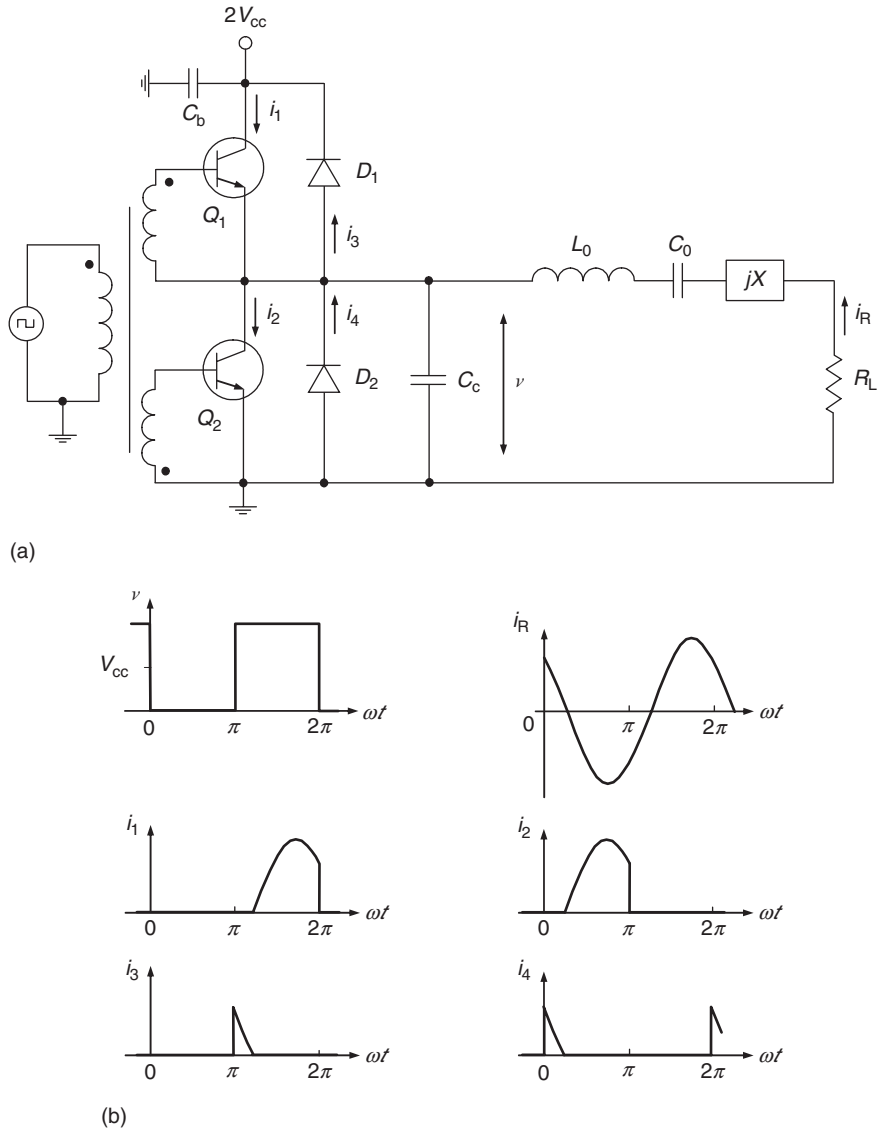



**Figure 2.12: Voltage-switching Class-D power amplifier with reactive load and protection diodes.**

lead length and leakage inductance in transformer) in series with transistor collectors. In this case, the currents flowing through the active devices jump when switching occurs, since they must be changed from zero to $I_{dc}$ instantaneously, twice during each period. Therefore, the total power losses due to finite switching time for a current-switching Class-D power amplifier with zero saturation resistance can be written as

$$P_s = L_c I_{dc}^2 f_0, \tag{2.83}$$

where $L_c = L_{c1} + L_{c2}$.

## 2.7 Drive and Transition Time

The driving circuitry of a Class-D power amplifier must provide the driving signal sufficient to ensure that the active devices are alternately saturated or pinched off during the proper time period. Generally, if a current-switching Class-D power amplifier requires a rectangular current or voltage driving waveform, a voltage-switching Class-D power amplifier can be driven by either a rectangular or sinusoidal driven signal. Fig. 2.13 shows the input part of the voltage-switching Class-D bipolar power amplifier and the waveforms associated with rectangular voltage and sinusoidal current-driving waveforms.

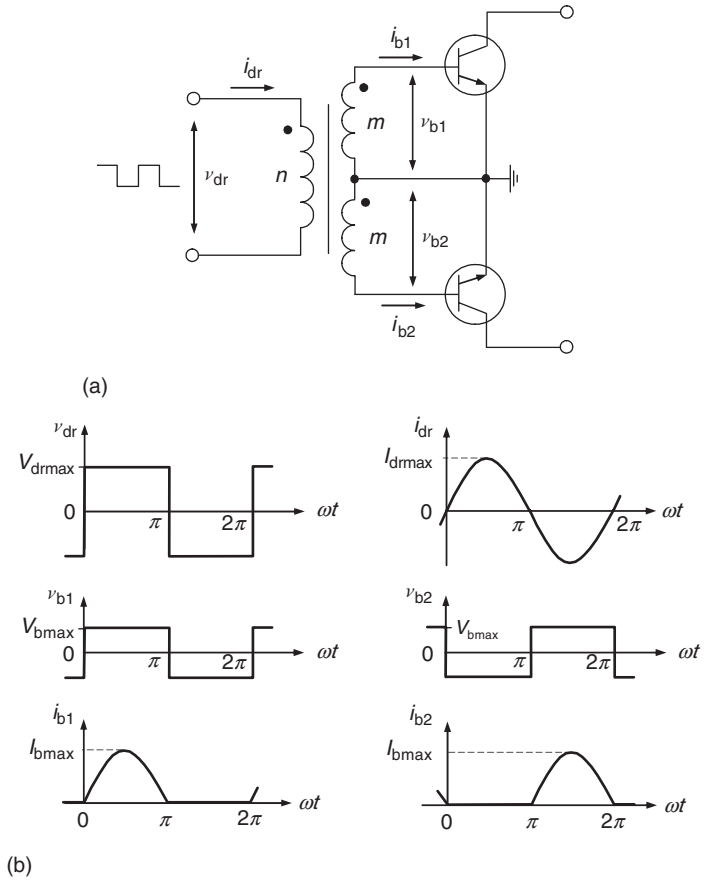



**Figure 2.13: Driving voltage and current waveforms.**

The sinusoidal current driven through the primary winding of the input transformer causes the half-sinusoidal currents to be driven into each base from the transformer secondary winding. The current flowing into the corresponding base results in a rise of the base-to-emitter voltage to $V_{\text{bmax}}$, which is approximately equal to its threshold voltage of 0.7 V for a bipolar device and corresponds to the maximum value required to saturate the MOSFET device. At the same time, the current flowing into the base of the other transistor is shifted by 180°, causing the fall of its base-to-emitter voltage to $-V_{\text{bmax}}$, ensuring that the transistor is pinched off.

Hence, the rectangular voltage with levels $\pm(m/n)V_{\text{bmax}}$ appears across the primary winding. The impedance seen by the driver at the switching frequency represents a ratio of the fundamental-frequency voltage driving amplitude to the current amplitude written as

$$R_{\text{dr}} = \frac{4}{\pi}\left(\frac{n}{m}\right)^2 \frac{V_{\text{bmax}}}{I_{\text{bmax}}}, \tag{2.84}$$

where $I_{\text{bmax}}$ is the peak base current amplitude, which must be large enough to sustain the collector current.

Then, the required driving power is given by

$$P_{\text{dr}} = \frac{2}{\pi} V_{\text{bmax}} I_{\text{bmax}}. \tag{2.85}$$

From Eq. (2.84), it follows that the driving resistance $R_{\text{dr}}$ is a function of the driving current amplitude and is not related to transistor parameters other than the voltage corresponding to a forward-biased base-emitter junction. For this reason, the driver output current must be limited to prevent transistor failure [2].

In a current-switching Class-D power amplifier, the rectangular collector or drain current requires the rectangular voltage and current-driving waveforms. In this case, Eqs. (2.84) and (2.85) can be rewritten as

$$R_{\text{dr}} = \left(\frac{n}{m}\right)^2 \frac{V_{\text{bmax}}}{I_{\text{bmax}}} \tag{2.86}$$

$$P_{\text{dr}} = V_{\text{bmax}} I_{\text{bmax}}, \tag{2.87}$$

where the driver output current also must be limited.

Fig. 2.14 shows four different configurations of the input driving circuits for a current-switching Class-D bipolar power amplifier. In the case of the driver with a rectangular current waveform, the active devices can be connected either in parallel, as shown in Fig. 2.14(*a*), or in series, as shown in Fig. 2.14(*b*), where $L_{\text{ch}}$ is the choke inductor. For a parallel connection,

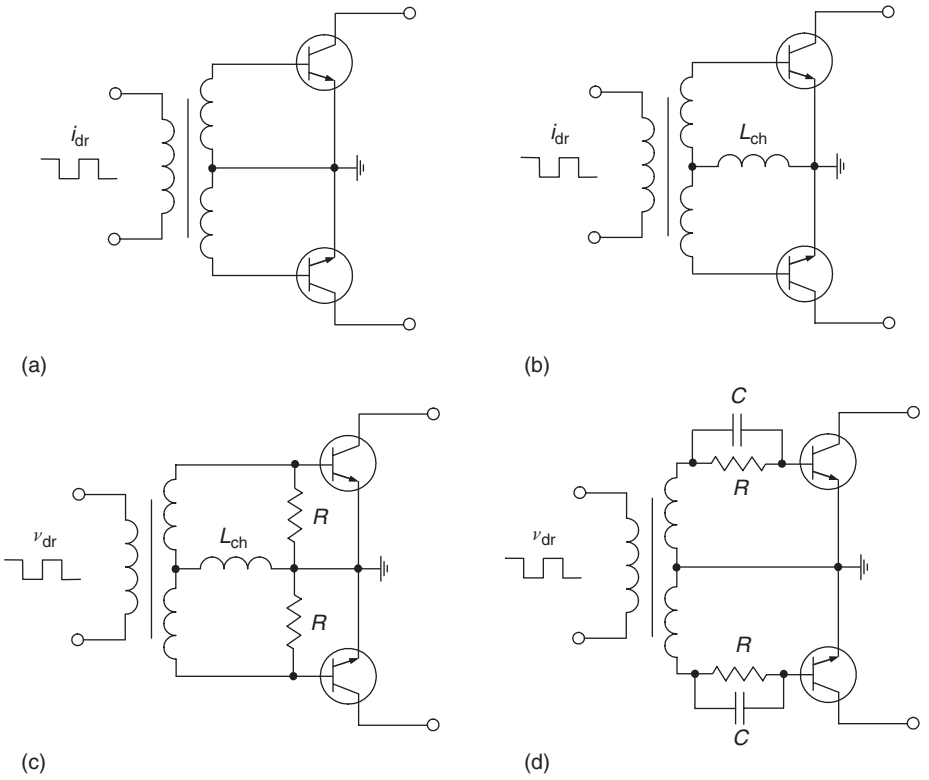



**Figure 2.14: Input-driving circuits.**

the driving current is distributed between bipolar transistors being inversely proportional to their input impedances. The input impedance of the transistor at saturation is significantly less than that in the active and pinch-off regions. Since the transistor cannot change instantly its saturation mode to pinch-off conditions under a negative driving signal, it absorbs most of the driving current, thus preventing the other transistor to go into saturation under a positive driving signal. Therefore, the series connection of the bipolar transistors is more effective because the driving current flows through both devices. However, the voltage across the reverse-biased base-emitter junction will be increased, therefore, value must be controlled to prevent the device failure.

When the driver with a rectangular voltage waveform is used, the driving current flows through the forward-biased base-emitter junction of one transistor and the reverse-biased base-emitter junction of the other transistor when they are connected in a series, as shown in Fig. 2.14(*c*). If a shunt resistor *R* is connected in parallel to the transistor input, the effect of switching losses can be reduced because the device input capacitance is discharged faster through this resistor. A similar correction effects can be achieved by using a parallel *RC* circuit

connected in a series to each transistor when both transistors are connected in parallel, as shown in Fig. 2.14(*d*). However, an increased current is required from the driver to saturate the transistor.

Generally, the input circuit of the transistor, either bipolar or MOSFET, can be represented as purely capacitive and only at low frequencies. In switching applications, however, the finite rise and fall times are the result of the effect of the much higher-frequency components rather than the fundamental. For example, if, at 30 MHz carrier, the switching time of 4 nanoseconds can be tolerated at an amplitude of 80%, it represents roughly a 100 MHz sine wave [10]. Besides, the input capacitance is usually nonlinear and varies over bias conditions. For example, the MOSFET gate-source capacitance varies with gate and drain voltages. At increased gate voltage, it goes down to its lowest value, just before reaching the threshold voltage, and then goes up to be constant at saturation. At the same time, when the MOSFET device begins to draw drain current, the drain voltage is lowered, resulting in reduction of the depletion area and causing an overlap between the gate and bulk material. This in turn increases the value of the gate-drain capacitance, which takes maximum value at zero drain voltage and positive gate voltage corresponding to the maximum device transconductance. In bipolar transistors, the base-emitter nonlinear capacitance represents the large diffusion capacitance in the active and saturation regions and much lower junction capacitance in the pinch-off region.

However, at higher frequencies, the device equivalent input circuit must include also a series resistance, base ohmic resistance for bipolar transistor or effective gate resistance consisting of the distributed channel and gate electrode resistances for MOSFET device. Let us consider the effect of a rectangular voltage drive with a duty cycle of 50% on the device input circuit shown in Fig. 2.15(*a*), where $R_{\text{in}}$ is the device input series resistance and $C_{\text{in}}$ is the device input capacitance. According to Kirchhoff voltage law, the algebraic sum of all voltage drops taken around any closed path is zero, which gives

$$v_{\text{R}} + v_{\text{C}} - v_{\text{in}} = 0, \tag{2.88}$$

where

$$v_{\text{R}} = i_{\text{dr}} R = R_{\text{in}} C_{\text{in}} \frac{dv_{\text{C}}(t)}{dt}, \tag{2.89}$$

and both the resistance $R_{\text{in}}$ and capacitance $C_{\text{in}}$ are assumed voltage-independent.

For a time period when $0 \leq t \leq 0.5T$,

$$v_{\text{in}} = V_{\max}, \tag{2.90}$$

where $V_{\max}$ is the input peak voltage corresponding to the device saturation conditions.

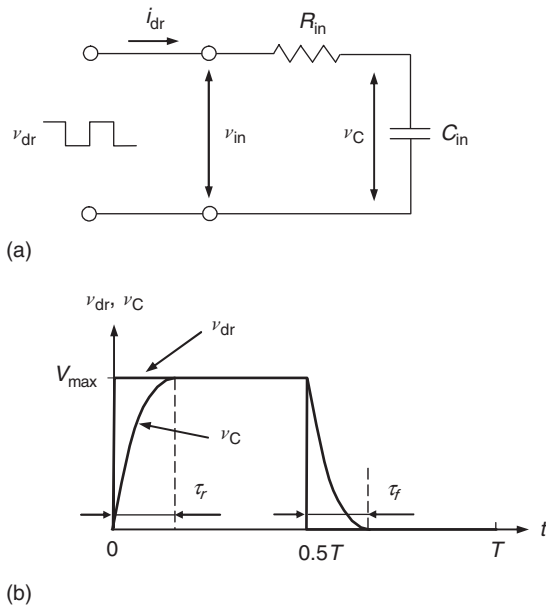



**Figure 2.15: Rectangular driving of equivalent input transistor circuit.**

Substituting Eqs. (2.89) and (2.90) into Eq. (2.88) yields

$$R_{\text{in}}C_{\text{in}}\frac{dv_{\text{C}}(t)}{dt}+v_{\text{C}}(t)=V_{\max}. \tag{2.91}$$

The general solution of the linear nonhomogeneous first-order differential equation under initial condition of $v_{\text{C}}(t)=0$ at $t=0$ when there is no energy stored in the input capacitance can be obtained by

$$\frac{v_{\text{C}}(t)}{V_{\max}}=1-\exp\left(-\frac{t}{R_{\text{in}}C_{\text{in}}}\right), \tag{2.92}$$

which determines the length of voltage rise time $\tau_{\text{r}}$ through the time constant $\tau_{\text{in}}=R_{\text{in}}C_{\text{in}}$ required the input capacitance to charge up to from 0 to $V_{\max}$.

Similarly, for a time period when $0.5T\le t\le T$,

$$v_{\text{in}}=0, \tag{2.93}$$

resulting in the linear homogeneous first-order differential equation

$$R_{\text{in}}C_{\text{in}}\frac{dv_{\text{C}}(t)}{dt}+v_{\text{C}}(t)=0. \tag{2.94}$$

Under initial condition of $v_C(t) = V_{max}$ when $t = 0.5T$, the solution of Eq. (2.94) can be written as

$$\frac{v_C(t)}{V_{max}} = \exp\left(-\frac{t}{R_{in}C_{in}}\right), \tag{2.95}$$

which determines the length of voltage fall time $\tau_f$ through the time constant $\tau_{in} = R_{in}\,C_{in}$ required the input capacitance to discharge down from $V_{max}$ to zero.

From Eqs. (2.92) and (2.95), it follows that the switching losses due to charging and discharging effects of the input capacitance are the same with voltage rise time $\tau_r$ and fall time $\tau_r$ equal both to $4\tau_{in}$ at the voltage level of 98% of $V_{max}$, which are shown in Fig. 2.15(*b*). Note that power requirement for the input drive is independent of the switching speed, and the switching speed is ultimately limited by the input resistance. Hence, there is an intrinsic limit

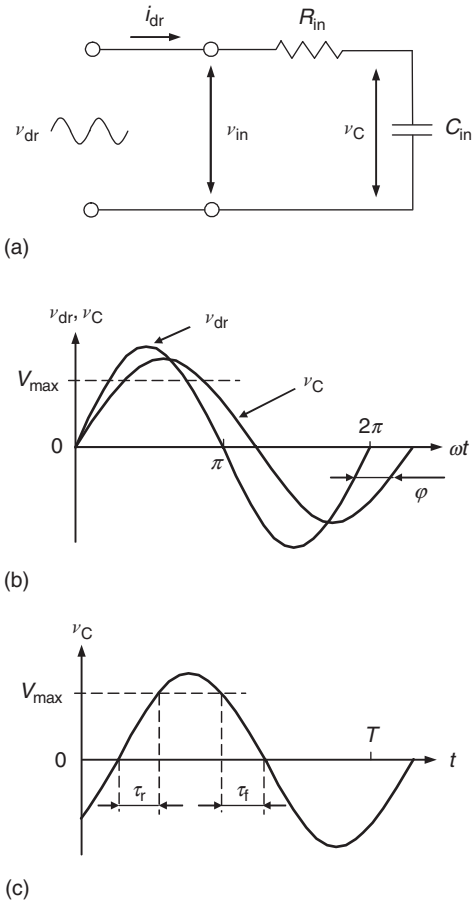



**Figure 2.16: Sinusoidal driving of equivalent input transistor circuit.**

to how fast the input capacitance can be charged, which becomes a serious factor as the operating frequency increases.

Now let us consider a response of the same circuit to a sinusoidal voltage driving and its effect on the power losses during the switching time. For the device input circuit shown in Fig. 2.16(*a*) with sinusoidal drive $v_{dr}(\omega t) = V_{dr}\sin(\omega t)$ we can write

$$R_{in}C_{in}\frac{dv_C(t)}{dt} + v_C(t) = V_{dr}\sin(\omega t), \tag{2.96}$$

where $V_{dr}$ is the voltage amplitude of the driving signal.

The general solution of the linear nonhomogeneous first order differential equation can be written as

$$v_C(t) = A\exp\left(-\frac{t}{\tau_{in}}\right) + \frac{V_{dr}}{1 + (\omega\tau_{in})^2}\left[\sin(\omega t) - \tau_{in}\cos(\omega t)\right]. \tag{2.97}$$

Let us assume that the driving voltage $v_{dr}(t)$ is zero at $t < 0$, so that the initial voltage across the input capacitance is zero. Then, under initial condition of $v_C(t) = 0$ at $t = 0$ required to determine the unknown coefficient $A$, Eq. (2.97) can be rewritten in a normalized form as

$$\frac{v_C(t)}{V_{dr}} = \frac{1}{\sqrt{1 + (\omega\tau_{in})^2}}\left[\sin\varphi\exp\left(-\frac{t}{\tau_{in}}\right) + \sin(\omega t - \varphi)\right], \tag{2.98}$$

where $\varphi = \tan^{-1}(\omega\tau_{in})$ is the phase shift. From Eq. (2.98), it follows that after a few time constants the natural response corresponding to the capacitance-charging process becomes negligible, and only the sinusoidal response with phase shift of $\varphi$ remains, as shown in Fig. 2.16(*b*). Then the circuit is operating in the sinusoidal steady-state mode with reduced amplitude.

The voltage rise time $\tau_r$ and fall time $\tau_f$ become longer with increasing input time constant $\tau_{in} = R_{in}C_{in}$, since the voltage amplitude across the capacitance reduces, becoming closer to the maximum amplitude $V_{max}$ required for a saturation mode of the transistor. Consequently, to minimize power losses, it is just necessary to increase the voltage amplitude of the driving signal. An advantage of the sinusoidal driving signal compared with rectangular drive is that there is no need to use a broadband input transformer, and all lead and leakage inductances in the gate-drive circuit can be absorbed into the input resonant circuit.

Generally, an exact analysis that includes transition waveforms and effects of elements of the complete device equivalent circuit is very complicated. This analysis of power losses can be substantially simplified by assuming that the resultant collector or drain voltage waveform of a complementary voltage-switching Class-D power amplifier is trapezoidal when the

transitions produce ramp voltage waveforms, as shown in Fig. 2.17 [2]. From Fig. 2.16(*c*), we can see that, under sinusoidal drive with increased voltage amplitude, the shape of the rise time $\tau_r$ and fall time $\tau_f$ are close to ramp. The transition time required by a single transistor to complete the entire switching process is shown in Fig. 2.17 as being converted to the angular time $\tau_s$. This time can include an effect of the output capacitance and other device parasitics. Both transistors are then assumed to have zero saturation resistances, and switching is completed within $2\tau_s$.

The fundamental-frequency collector voltage amplitude $V$ is obtained by a Fourier integral of the trapezoidal waveform taking into account the dc supply voltage of $2V_{cc}$ as

$$V = \frac{4}{\pi} V_{cc} \frac{\sin \tau_s}{\tau_s} \approx \frac{4}{\pi} V_{cc} \left(1 - \frac{\tau_s^2}{6}\right), \tag{2.99}$$

where the linear approximation is valid only for small values of $\tau_s$.

For the fundamental-frequency output power $P = 0.5V^2/R_L$ and dc current $I_0 = V_R/(\pi R_L)$, where $R_L$ is the load resistance, the collector efficiency can be calculated from

$$\eta = \frac{\pi}{2} \frac{V}{V_{cc}} = \frac{\sin \tau_s}{\tau_s}. \tag{2.100}$$

The same results may be obtained for the symmetrical current-switching and both voltage-switching and current-switching transformer-coupled Class-D power-amplifier configurations [11].

## 2.8 Practical Class-D Power-Amplifier Implementation

Fig. 2.18 shows the circuit schematic of a quasi-complementary voltage-switching Class-D power amplifier where the dc power supply is connected to the drain of the top device and the

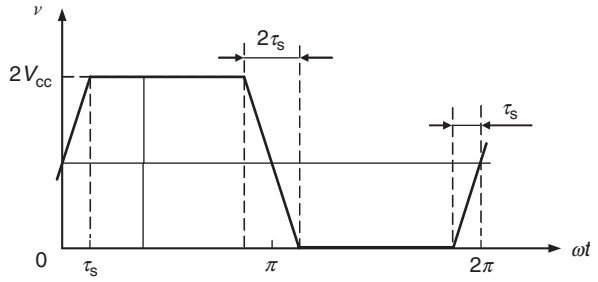



**Figure 2.17: Transition time in Class-D power amplifier.**

source of the other device is connected to the ground [12]. The devices are driven via a three-winding transformer with appropriate polarities on the output so that the same drive is used for both devices. The midpoint between the two devices is connected to the series resonant $L_0C_0$ circuit with a reasonable loaded quality factor of about 10, which can provide small impedance at the fundamental frequency and high impedances at the harmonic components. To design a 300 W Class-D power amplifier operating at 13.56 MHz from a 75 V dc supply voltage, it is necessary to provide the load resistance $R_L = 3.8\ \Omega$ and peak drain current $I_{max} = 12.56$ A in accordance with Eqs. (2.36) and (2.38) assuming zero device saturation resistance. To satisfy these requirements, the MOSFET devices IRF540 were chosen, which can operate under dc voltage and current conditions of 100 V and 25 A, respectively. This MOSFET device has a saturation resistance equal to 0.085 Ω, thus providing the conduction losses per device of 3.35 W. The output capacitance of the device is equal to 500 pF. Consequently, according to Eq. (2.82), the switching losses per device due to capacitance discharging process are equal to 38.14 W. As a result, the maximum expected drain efficiency can reach a value of 80%. However, it needs also to take into account the effect of the device input circuit with the time constant $\tau_{in} = 39$ ns for a gate voltage of 10 V to rectangular drive that makes the overall transition time even longer.

Applying a current-switching Class-D configuration enables us to eliminate switching losses due to the device output shunt capacitances. In this case, it is necessary to minimize the switching losses due to the parasitic series inductances, which can be represented by the lead inductances of the device package. However, by on-chip integration of the parallel *LC* resonator, it is possible to reduce the circuit complexity and eliminate parasitic reactance losses.

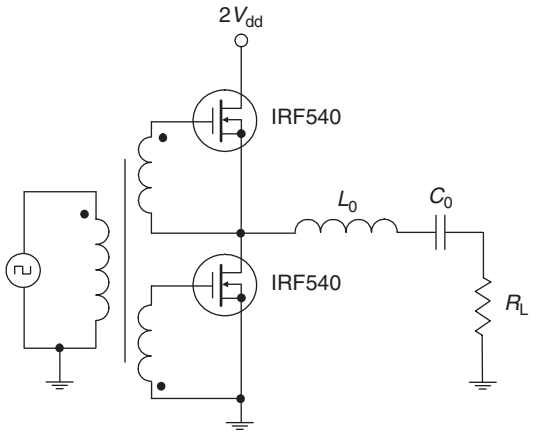



**Figure 2.18: MOSFET voltage-switching Class-D power amplifier.**

Fig. 2.19 shows the circuit schematic of a bipolar current-switching InGaP/GaAs HBT Class-D power amplifier where active devices represent 80 emitter fingers with emitter area of $2\,\mu\text{m} \times 20\,\mu\text{m}$ and peak current density of $0.11\,\text{mA}/\mu\text{m}^2$ [11]. A 180° input balun represented by a 50 Ω coaxial line generates differential input signals, while an 180° output balun converts the balanced output with out-of-phase output signals to a single-ended output signals. To maximize power gain, the input- and output-matching circuits in the form of high-pass *L*-sections are applied to each transistor. The *LC* resonator comprises a bond-wire inductor and a metal-insulator-metal (MIM) capacitor. Using a spiral inductor with lower quality factor reduces collector efficiency by 5%. At a supply voltage of 3.4 V, the transistor saturation resistance $r_{\text{sat}}$ and transition time $\tau_{\text{s}}$ were equal to 0.58 Ω and $0.1\pi$, respectively. The bases of both HBTs are biased to a turn-on voltage of 1.2 V for operation as switches. As a result, the current-switching Class-D power amplifier achieved a collector efficiency of 78.5% at an output power of 29.5 dBm with a maximum power-added efficiency of 68.5% at the operating frequency of 700 MHz. The best efficiency was achieved at a high drive level resulting in a power gain of about 9 dB. By using a similar approach with GaAs MESFET devices, the power-added efficiency of 75.6% with an output power of 28.6 dBm and power gain of 13.9 dB was achieved at the operating frequency of 900 MHz and supply voltage of 5 V [13].

Fig. 2.20 shows the current-switching Class-D power amplifier using PTF10135 LDMOSFET devices [14]. The input and output baluns are represented by the 180° rat-race hybrids built on

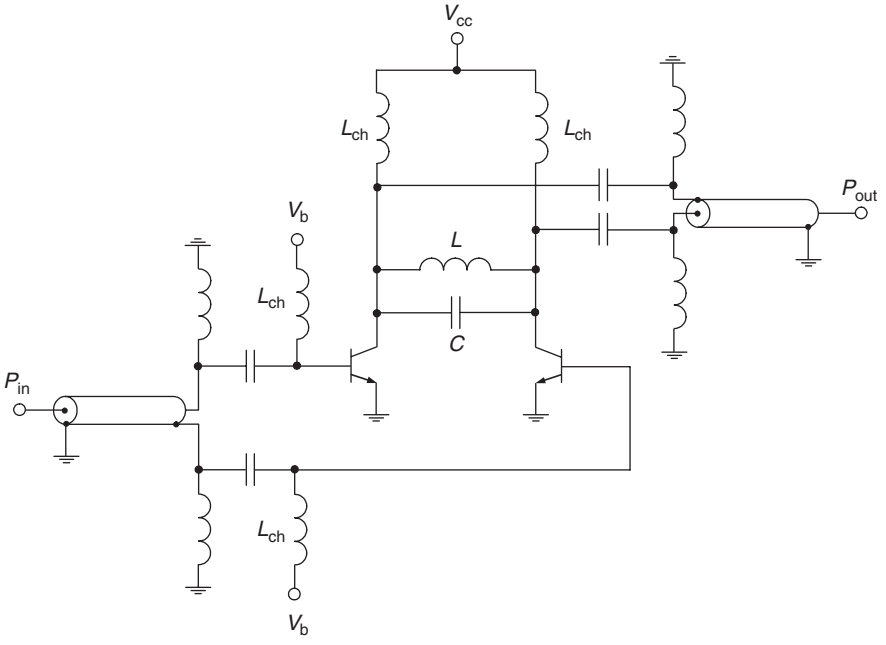



**Figure 2.19: Schematic of bipolar current-switching Class-D power amplifier.**

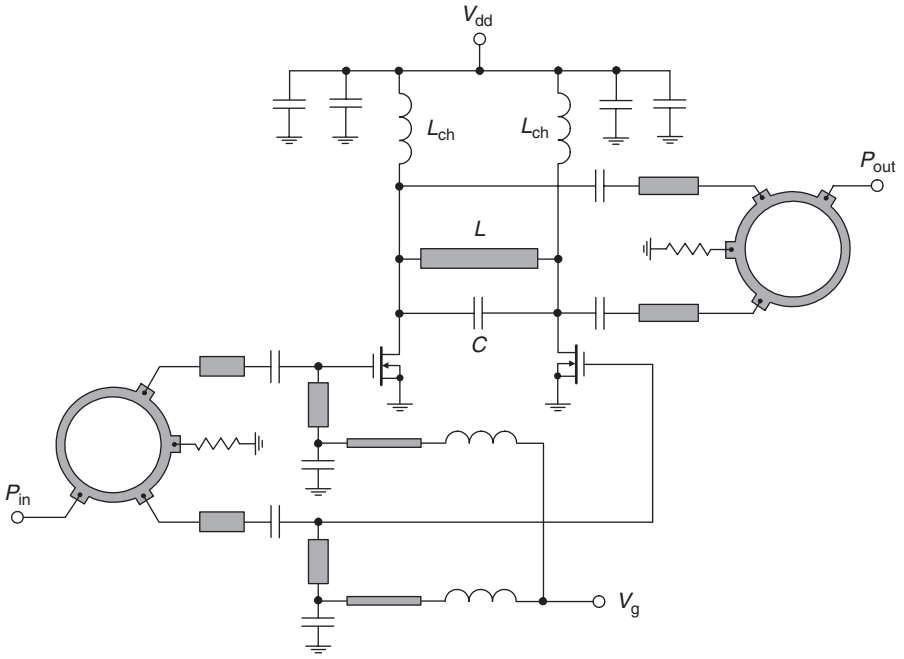



**Figure 2.20: Schematic of LDMOSFET current-switching Class-D power amplifier.**

high dielectric substrate to minimize the physical size. The input matching circuits are added between the input of each transistor and hybrid to reduce the return loss. The *LC* resonator was designed by converting the ideal inductor *L* and capacitor *C* to real microstrip line and parallel capacitor. The power amplifier begins operating in a switching mode beyond 25 dBm input power. As a result, a maximum output power of 13 W was observed with a drain efficiency of 60% and power gain of 14 dB.

## References

[1] I. A. Popov (Ed.), Transistor *Generators of Harmonic Oscillations in Switching Mode* (in Russian), Moskva: Radio i Svyaz, 1985.

[2] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons, 1980.

[3] A. D. Artym, *Class D Power Amplifiers and Switching Generators in Radio Communication and Broadcasting* (in Russian), Moskva: Svyaz, 1980.

[4] M. R. Osborne, ''Design of Tuned Transistor Power Amplifiers,'' *Electronic Eng*., vol. 40, pp. 436–443, August 1968.

[5] P. J. Baxandall, ''Transistor Sine Wave LC Oscillators, Some General Considerations and New Developments,'' *IEE Proc. Electric Power Appl.*, vol. 106, pp. 748–758, May 1959.

[6] W. J. Chudobiak and D. F. Page, ''Frequency Limitations of Class-D Transistor Amplifiers,'' *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 25–37, February 1969.

[7] F. H. Raab and D. J. Rupp, ''A Quasi-Complementary Class-D HF Power Amplifier,'' *RF Design*, vol. 15, pp. 103–110, September 1992.

[8] M. Kazimierczuk and J. S. Modzelewski, ''Drive-Transformerless Class-D Voltage-Switching Tuned Power Amplifier,'' *Proc. IEEE*, vol. 68, pp. 740–741, June 1980.

[9] M. K. Kazimierczuk, ''Class D Voltage-Switching MOSFET Power Amplifier,'' *IEE Proc. Electric Power Appl.*, vol. 138, pp. 285–296, November 1991.

[10] H. O. Granberg, ''Applying Power MOSFETs in Class D/E RF Power Amplifier Design,'' *RF Design*, vol. 8, pp. 42–47, June 1985.

[11] T.-P. Hung, A. G. Metzger, P. J. Zampardi, M. Iwamoto, and P. M. Asbeck, ''Design of High-Efficiency Current-Mode Class-D Amplifiers for Wireless Applications,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-53, pp. 144–151, January 2005.

[12] S.-A. El-Hamamsy, ''Design of High-Efficiency RF Class-D Power Amplifier,'' *IEEE Trans. Power Electronics*, vol. PE-9, pp. 297–308, May 1994.

[13] H. Kobayashi, J. M. Hinrichs, and P. M. Asbeck, ''Current-Mode Class-D Power Amplifiers for High-Efficiency RF Applications,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 2480–2485, December 2001.

[14] A. Long, J. Yao, and S. I. Long, ''A 13 W Current Mode Class D High Efficiency 1 GHz Power Amplifier,'' *45th Midwest Circuits and Systems Symp. Dig.*, vol. 1, pp. 33–36, 2002.

This page intentionally left blank

CHAPTER 3

# Class-F Power Amplifiers

Highly efficient operation of the power amplifier can be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multi-resonant circuit tuned to the odd harmonics of the fundamental frequency is added into the load network. An infinite number of odd-harmonic resonators results in an idealized Class-F mode with a square voltage waveform and a half-sinusoidal current waveform at the device output terminal. In Class-F power amplifiers analyzed in frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking to control the voltage and current waveforms at the device output to obtain maximum efficiency. In this chapter, different Class-F techniques, using lumped and transmission-line elements including a quarter-wave transmission line, are analyzed. The effect of the saturation resistance and parasitic shunt capacitance is demonstrated. The design examples and practical RF and microwave Class-F power amplifiers are described and discussed.

## 3.1 Biharmonic Operation Mode

In a Class-B operation mode, the maximum theoretical anode (collector or drain) efficiency achieves only 78.5% characterizing by the sinusoidal anode voltage waveform and half-sinusoidal current waveform. In real practical power-amplifier design, especially at high frequencies and low supply voltage, efficiency significantly degrades. Therefore, some design, solutions contributing to efficiency improvement were published a long time ago with regard to the vacuum-tube power amplifiers and were based on the harmonic tuning at the anode of the active device. To understand this basic approach, let us evaluate a contribution of each harmonic component to ideal half-sinusoidal current waveform and square voltage waveform. In this case, it is useful to calculate the partial Fourier series of current $i(\omega t)$ and voltage $v(\omega t)$ in normalized forms according to

$$\frac{i(\omega t)}{I_0} = 1 - \frac{\pi}{2}\sin\omega t - 2\sum_{\mathrm{n}=2,4,6,\ldots}^{N}\frac{\cos n\omega t}{n^2-1} \tag{3.1}$$

$$\frac{v(\omega t)}{V_0} = 1 + \frac{4}{\pi}\sin\omega t + \frac{4}{\pi}\sum_{\mathrm{n}=3,5,7,\ldots}^{N}\frac{\sin n\omega t}{n}, \tag{3.2}$$

where $I_0$ and $V_0$ are the dc current and voltage components, respectively.

Fig. 3.1 shows that the shapes of the voltage and current waveforms can be significantly changed with increasing fundamental voltage amplitude by adding even one additional harmonic component being properly phased. For example, the combination of the fundamental and third harmonic components being out-of-phase at center point results in a flattened voltage waveform with depression in its center. It is clearly seen from Fig. 3.1(*a*) that the proper ratio between the amplitudes of the fundamental and third-harmonic components can provide the flattened voltage waveform with minimum depression and maximum difference between its peak amplitude and amplitude of the fundamental harmonic. Similarly, the combination of the fundamental and second-harmonic components being in phase at the center point flattens the current waveform corresponding to the maximum values of the voltage waveform and sharpens the current waveform corresponding to the minimum values of the voltage waveform, as shown in Fig. 3.1(*b*). The optimum ratio between the amplitudes of the fundamental and second current harmonic components can maximize a peak value of the current waveform with its minimized value determined by the device saturation resistance in a practical circuit. Thus, power loss due to the active device can be minimized since the results of the integration over the period when minimum voltage corresponds to maximum current will give small value compared with the power delivered to the load. In a common case, the same result can be achieved by adding the second harmonic into the voltage waveform and third harmonic into the current waveform resulting in an inverse operation mode.

Ideally, the half-sinusoidal current waveform does not contain the third-harmonic component, as it follows from Eq. 3.1, because its third harmonic Fourier current coefficient is equal to zero, i.e., $\gamma_3(\theta) = 0$. However, a load-line analysis of a Class-B power amplifier with sinusoidal output-voltage waveform—under over-driven conditions when device operates in pinch-off, active, and voltage-saturation modes during one oscillation period—shows that operation in the saturation mode is characterized by a depression in the output-current waveform, as shown in Fig. 3.1. From Fourier analysis it follows that such a current waveform includes the third harmonic component, which is out-of-phase with the fundamental component at the point of symmetry of $\omega t = \pi/2$. Therefore, when an additional resonant circuit tuned to the third-harmonic is included into the anode circuit operating in a saturation mode, the voltage drop with opposite phase will appear across this resonant circuit resulting in a similar depressed voltage waveform shown in Fig. 3.1(*a*), solid line. Hence, for the increased fundamental voltage amplitude, the output power at the fundamental frequency and anode efficiency can be increased for the same input drive. Physically, an efficiency improvement can be explained by the fact that fundamental voltage or fundamental current has negative values during some part of the period corresponding to the negative power as an integration of a product of the instantaneous fundamental voltage and current. This means that the power loss on the active device is partly compensated by the reactive power provided by the harmonic resonator.

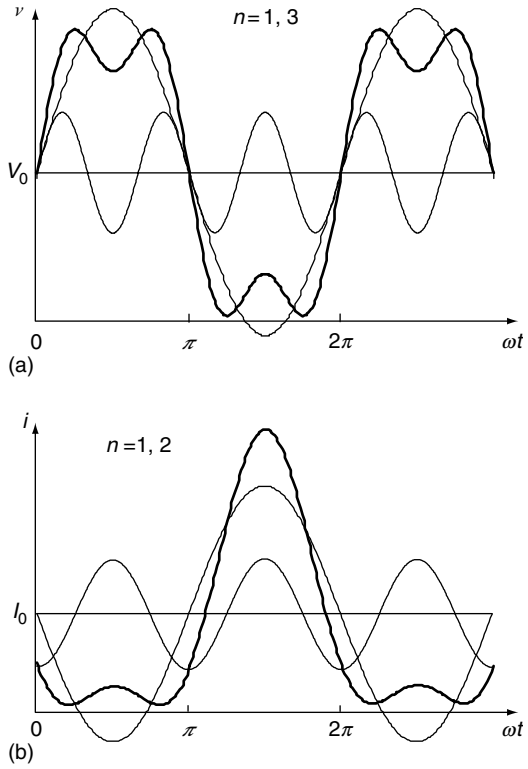



**Figure 3.1: Fourier voltage and current waveforms with third and second harmonics.**

Adding one or more high-order harmonic components can further improve the voltage or current waveform. Fig. 3.2(*a*) shows the voltage waveform with third and fifth harmonic peaking, which is close to an ideal rectangular waveform. Fig. 3.2(*b*) shows the current waveform with second and fourth harmonic peaking resulting in close to an ideal half-sinusoidal waveform.

The possibility to improve efficiency by approximation of the anode voltage waveform to square wave and to minimize the values of the saturation voltage compared to the supply voltage over half an entire interval $0 \leq \omega t \leq 2\pi$ was found a very long time ago [1]. The effect of the inclusion of the parallel resonant circuit tuned to the third harmonic component and located in series to the anode, as shown in Fig. 3.3(*a*), was described and analyzed [2, 3]. It was shown that the symmetrical anode voltage waveform and level of its depression can be provided with opposite phase conditions between the fundamental and third harmonic and optimum value of the ratio between their voltage amplitudes. Also, it was noted that high operation efficiency can be achieved even when impedance of the parallel circuit to third harmonic is equal or slightly greater than impedance of the tank circuit to the fundamental component. In addition,

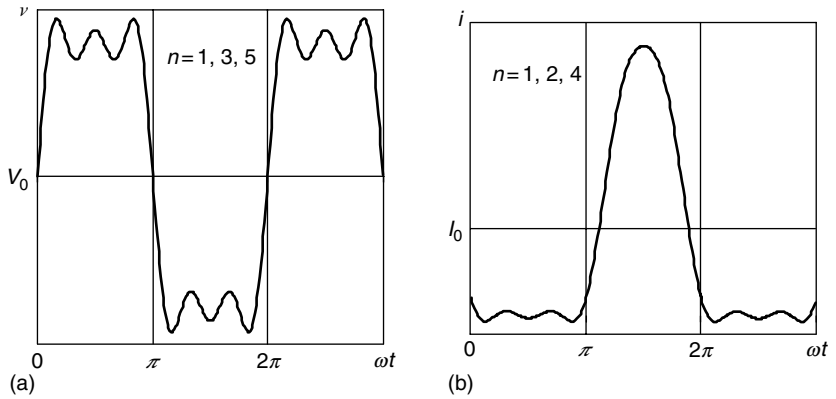



**Figure 3.2: Fourier voltage and current voltage waveforms with three harmonics.**

such an approach can slightly improve the modulation properties of the power amplifier using either grid or anode modulation techniques [2].

The parallel resonator tuned to the third harmonic can be replaced by a low-pass filter with two series inductors and a shunt capacitor, as shown in Fig. 3.3(*b*), designed to pass the third harmonic of the fundamental frequency, terminating in a parallel resonant circuit tuned to the fundamental [4]. However, impedances seen by the device anode can be arbitrary depending on the value of a filter cutoff frequency $\omega_c = 2/\sqrt{LC}$. In this case, the ratio between the series inductor $L/2$ and shunt capacitor $C$ can be chosen to resonate the third harmonic $\omega = 3\omega_0 = \sqrt{2}/\sqrt{LC} = \omega_c/\sqrt{2}$, thus providing ideally infinite impedance seen by the device

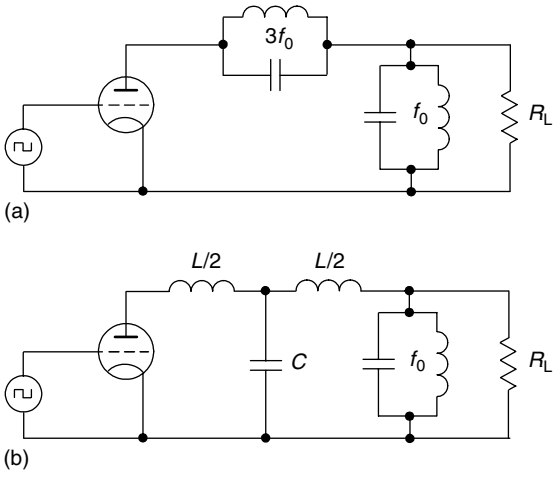



**Figure 3.3: Biharmonic power amplifiers.**

anode at the third harmonic when it is assumed an infinite $Q$ factor for the parallel fundamentally tuned resonant circuit.

To maximize efficiency of the vacuum-tube amplifier with a square voltage driving waveform, it was suggested to use an additional resonator tuned to the fifth harmonic, as shown in Fig. 3.4(*a*) [5]. However, generally, in view of the parasitic plate-cathode capacitance composed by the interelectrode and case capacitances and series plate inductance, the entire anode circuit should be tuned to the third harmonic, not only a single resonator. Such an anode circuit includes a parallel third harmonic resonator, which is slightly mistuned in this case, and an additional series LC circuit connected in parallel to the tube, which has a capacitive reactance at the fundamental frequency and inductive reactance at the third harmonic component tuned to the third harmonic resonance together with other elements of the anode circuit [6].

The parallel resonators tuned to the third and fifth harmonics can be replaced by a low-pass filter with three sections, as shown in Fig. 3.4(*b*), the elements of which are designed to pass the third and fifth harmonics of the fundamental frequency, terminating in a parallel resonant circuit tuned to the fundamental [4]. However, in this case, it is difficult to correctly specify the impedances at these harmonics seen by the anode circuit. This may result in a situation when a square-top anode voltage waveform cannot maintain its form in a circuit having inductive or capacitive reactance or both, even though, in the latter case, the reactive elements are so chosen that the circuit would be resonant for any one of the three frequencies including fundamental. The reactances cause phase shifting of the component waves with consequent distortion of the resultant wave and loss of efficiency.

In practice, the effective driving waveform may differ from the idealized square wave depending on what types of the harmonic resonators are located in the load network [7]. It was

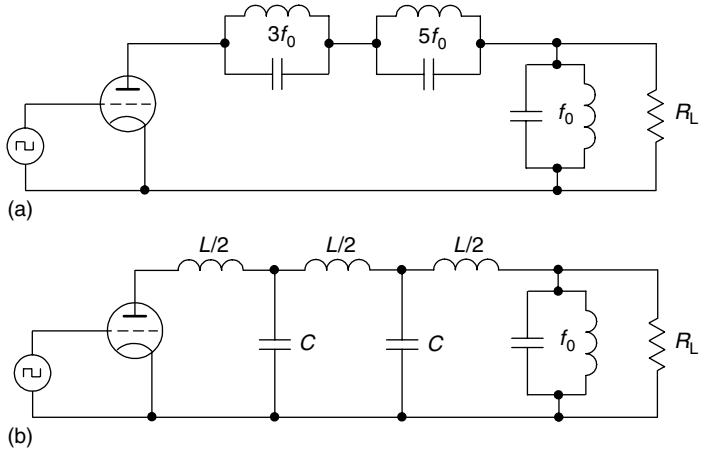



**Figure 3.4: Polyharmonic power amplifiers.**

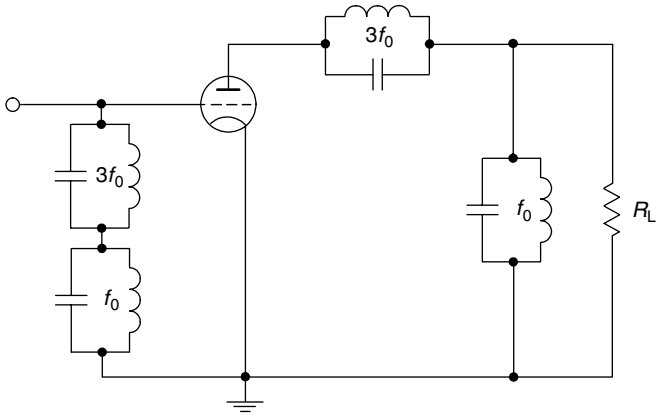



**Figure 3.5: Biharmonic power amplifier with input harmonic control.**

experimentally found that applying the biharmonic driving signal containing the fundamental and second harmonic components produces the signal amplification more efficiently because of the much steeper driving waveform [8]. In this case, the resultant driving waveform consists of the fundamental and second harmonic components being in phase at their maximum amplitudes, and the amplitude of the second harmonic is preferably chosen to have approximately one-quarter the amplitude of the fundamental. The detailed mathematical explanation of the effect of the biharmonic driving signal consisting of the fundamental and third harmonic component is given [9, 10]. Fig. 3.5 shows a simplified circuit of a vacuum-tube power amplifier containing the tank and third harmonic-resonant circuits both in grid and anode circuits.

Consider the effect of the biharmonic input signal on the MOSFET transistor, which simplified equivalent circuit is represented by an ideal voltage-controlled current source with transconductance $g_m$ only. The biharmonic signal in the voltage form can be written as

$$v_g = V_g + V_{g1}(\cos \omega t - a_n \cos n\omega t), \tag{3.3}$$

where $V_g$ is the gate-bias voltage and $a_n = V_{gn}/V_{g1}$ is the coefficient of $n$th harmonic injection.

Substituting Eq. (3.3) into the idealized device piecewise-linear transfer characteristic, we can write for output current

$$i = g_m(v_g - V_p) = I_0 + g_m V_{g1}(\cos \omega t - a_n \cos n\omega t), \tag{3.4}$$

where $I_0 = g_m(V_g - V_p)$ is the dc current and $V_p$ is the device pinch-off voltage. The output current $i(\omega t)$ takes a zero value when $\omega t = \theta$, where $\theta$ is one-half a conduction angle. Then,

$$I_0 = -g_m V_{g1}(\cos \theta - a_n \cos n\theta). \tag{3.5}$$

As a result, Eq. (3.4) can be rewritten in the form of

$$i = g_{\mathrm{m}} V_{\mathrm{g1}} [\cos \omega t - \cos \theta - a_{\mathrm{n}} (\cos n\, \omega t - \cos n\theta)]. \tag{3.6}$$

In this case, the Fourier current harmonic coefficients can be written as

$$\begin{aligned} \gamma_0'(\theta) &= \frac{1}{\pi} \left[ \sin \theta - \theta \cos \theta + a_{\mathrm{n}} \left( \theta \cos n\theta - \frac{\sin n\theta}{n} \right) \right] \\ &= \gamma_0(\theta) - \frac{a_{\mathrm{n}}}{n} \gamma_0(n\theta) \end{aligned} \tag{3.7}$$

$$\begin{aligned} \gamma_1'(\theta) &= \frac{1}{\pi} \left[ \theta - \frac{\sin 2\theta}{2} - n a_{\mathrm{n}} \left( \frac{\sin (n-1)\theta}{n-1} - \frac{\sin (n+1)\theta}{n+1} \right) \right] \\ &= \gamma_1(\theta) - n^2 a_{\mathrm{n}} \gamma_{\mathrm{n}}(\theta) \end{aligned} \tag{3.8}$$

$$\begin{aligned} \gamma_{\mathrm{n}}'(\theta) &= \frac{1}{\pi} \left[ \frac{\sin (n-1)\theta}{n(n-1)} - \frac{\sin (n+1)\theta}{n(n+1)} - a_{\mathrm{n}} \left( \theta - \frac{\sin 2n\theta}{2n} \right) \right], \\ &= \gamma_{\mathrm{n}}(\theta) - \frac{a_{\mathrm{n}}}{n} \gamma_1(n\theta) \end{aligned} \tag{3.9}$$

where $\gamma_{\mathrm{n}}(\theta)$ are the harmonic current coefficients of an idealized Class-C power amplifier with monoharmonic driving signal.

To compare the operation modes with the output cosinusoidal voltage $v = V_{\mathrm{dd}} - V \cos \omega t$ and biharmonic voltage $v = V_{\mathrm{dd}} - V_1(\cos \omega t - a_{\mathrm{n}} \cos n\omega t)$, where $a_{\mathrm{n}} = V_{\mathrm{n}}/V_1$ and $V_{\mathrm{dd}}$ is the supply voltage, let us assume the conduction angles and maximum output-current amplitudes are equal. The latter condition implies that the minimum values of the saturation voltages for both cases are equal, appearing however at different time moments depending on the number of injected harmonic components. Then, the maximum drain voltage peak factor of a biharmonic mode $\xi' = V_1/V_{\mathrm{dd}}$ can be given by [9]

$$\xi' = \frac{\xi}{\cos \frac{\pi}{2n}}, \tag{3.10}$$

where $\xi = V/V_{\mathrm{dd}}$ is the drain voltage peak factor corresponding to a cosinusoidal driving mode, when the voltage coefficient $a_{\mathrm{n}}$ takes an optimum value of

$$a_{\mathrm{n}}^0 = \frac{1}{n} \sin \frac{\pi}{2n}. \tag{3.11}$$

Generally, the drain efficiency $\eta$ is written through the fundamental power $P_1$ and dc power $P_0$ in a monoharmonic mode as

$$\eta = \frac{1}{2}\frac{P_1}{P_0} = \frac{1}{2}\frac{VI_1}{V_{dd}I_0} = \frac{1}{2}\xi\frac{\gamma_1(\theta)}{\gamma_0(\theta)}. \tag{3.12}$$

By using Eqs. (3.7) to (3.12), the drain efficiency $\eta'$ in a biharmonic mode can be calculated from

$$\eta' = \frac{1}{2}\frac{n^2}{\cos\frac{\pi}{2n}}\frac{\gamma_1(\theta) - n\gamma_n(\theta)\sin\frac{\pi}{2n}}{n^2\gamma_0(\theta) - \gamma_0(n\theta)\sin\frac{\pi}{2n}}\xi. \tag{3.13}$$

From Eq. (3.13), it follows that, in a Class-B biasing condition with $\theta = 90°$, the drain efficiency in a biharmonic mode with third harmonic injection, when $n = 3$, can achieve a value of

$$\eta' = (0.85 \div 0.86)\xi \tag{3.14}$$

resulting in a maximum efficiency of $(85 \div 86)\%$ in an ideal case of zero saturation voltage, when $\xi = 1$. Similar efficiency improvement of about 8% compared with a cosinusoidal driving signal was achieved for the case of third harmonic injection with $a_3 = 0.14$ [9]. Moreover, the drain efficiency $\eta'$ can be further improved by optimizing the conduction angle and voltage coefficient. For example, Eq. (3.14) can be rewritten as $\eta' = (0.95 \div 0.96)\xi$ for optimum values $\theta_{opt} \approx 63°$ and $a_n^0 \approx 0.205$ [9].

However, it is difficult to achieve an optimum value of the voltage coefficient $a_n$ in real practical conditions because its value significantly depends on the ratio between resonant circuit equivalent resistance $R_n$ at $n$th harmonic component and equivalent resistance $R_1$ at fundamental frequency; i.e.,

$$a_n = \frac{V_n}{V_1} = \frac{I_n R_n}{I_1 R_1} = \frac{\gamma_n'(\theta)}{\gamma_1'(\theta)}\frac{R_n}{R_1}. \tag{3.15}$$

From Eq. (3.15), it follows that, for a certain value of $n$ and an optimum value of $\theta$, the condition $a_n = a_n^0$ is satisfied with more accuracy for a greater ratio of $R_n/R_1$. As a rule of thumb, it is sufficient to choose their ratio equal or greater than 10. In this case, the worsening of the drain efficiency $\eta'$ will be equal to or less than 0.5%.

In previous input harmonic-control analysis, it was assumed that the active device represents an ideal voltage-controlled current source, which is a good approximation at sufficiently low frequencies for vacuum tubes or MOSFET devices. However, when using a high-frequency bipolar or MESFET transistor as an active element, it is necessary to take into account the significant nonlinearity of the device input capacitance. For example, the voltage-dependent input gate-source capacitance of a GaAs MESFET device can be modeled as a junction capacitance creating higher-order harmonics at the device input, each having a

different phase. In this case, the proper relationships between amplitudes and phases of the harmonics at the transistor input are needed to approximate the required symmetrical drain voltage and current waveforms [11]. The pHEMT device, in contrast to a conventional MESFET device, shows a very steep gradient in its gate-source capacitance versus gate-bias voltage. As a result, the efficiency increase up to 81% can be achieved for a microwave power amplifier with ideal Class-F load network by input termination of all harmonics when input signal is purely sinusoidal compared with a nonterminated case with severely distorted input-voltage waveform [12]. This situation appears as the simplest and effective alternative to multi-resonant input circuit, which is difficult to realize at very high frequencies, taking into account the active device parasitics.

Normally, the biharmonic-driving signal for the final stage is formed in previous amplifying stages by the proper harmonic tuning. However, if the driving signal source represents a sine wave output voltage, the formation of the biharmonic-driving signal can be done by subtracting, from the sinusoidal input voltage, the voltage of the same harmonic component as used in the anode circuit. Fig. 3.6(*a*) shows the biharmonic power amplifier, in which a resonator of low reactance compared with the anode resonator but tuned to the same third harmonic frequency component is inserted in the cathode circuit [7]. The high degree of negative feedback developed makes it impossible for any significant third harmonic current to develop, no matter what grid-voltage waveform is employed. In practice, with a sine wave

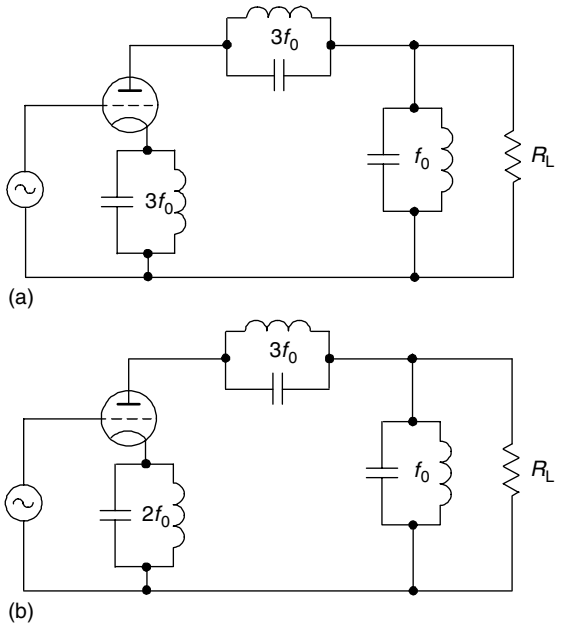



**Figure 3.6: Biharmonic power amplifiers with cathode harmonic control.**

input, correctly related in amplitude with the grid bias, the relative voltages developed between grid and cathode are self-adjusting to provide the flattened voltage waveforms.

Unfortunately, it is not always easy to realize the proper amplitude conditions because of the finite losses associated with two third harmonic resonators, since both resonators affect the voltage waveforms in the grid and anode circuits simultaneously. For example, the tubes with variable, weak, and small grid current characteristics cannot be used for such a biharmonic configuration. The effect of this problem can be significantly minimized, if the resonant circuit in the cathode circuit tuned to the second harmonic together with a third harmonic resonant circuit in the anode circuit is used, as shown in Fig. 3.6(*b*), resulting in the input-biharmonic voltage $v_g = V_{g1}\cos\omega t - V_2\cos 2\omega t$ and output voltage $v = V_1\cos\omega t + V_2\cos 2\omega t - V_3\cos 3\omega t$ [9]. In this case, the maximum available anode efficiency can reach values of $85 \div 88\%$.

## 3.2 Idealized Class-F Mode

Generally, an infinite number of odd-harmonic tank resonators can maintain a square voltage waveform, also providing a half-sinusoidal current waveform at the anode. Fig. 3.7(*a*) shows such a Class-F power amplifier with a multiple-resonator output filter to control the harmonic content of its collector (anode or drain) voltage and/or current waveforms, thereby shaping them to reduce dissipation and increase efficiency [13, 14].

To simplify an analysis of a Class-F power amplifier, a simple equivalent circuit of which is shown in Fig. 3.7(*b*), the following assumptions are introduced:

- Transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.

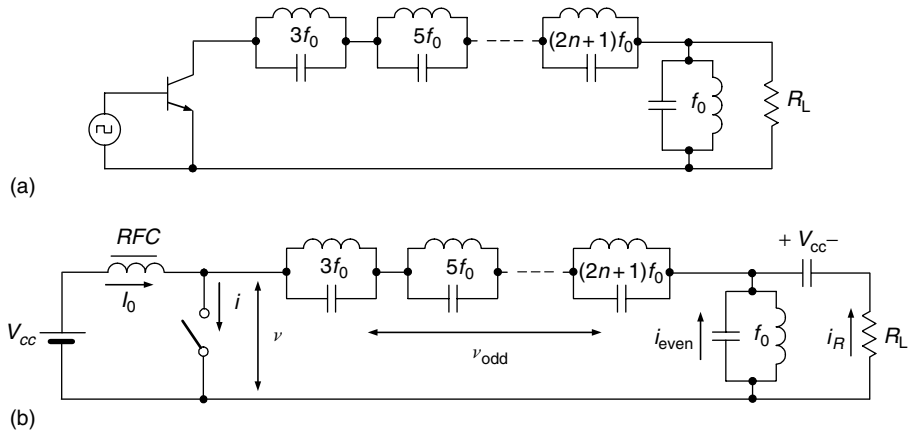



**Figure 3.7: Basic circuits of Class-F power amplifier with parallel resonant circuits.**

- RF choke allows only a dc current and has no resistance.
- Quality factors of all parallel resonant circuits have infinite impedance at the corresponding harmonic and zero impedance at other harmonics.
- There are no losses in the circuit except only into the load $R_L$.
- Operation mode with a 50% duty cycle.

To determine the idealized collector voltage and current waveforms, let us consider the distribution of voltages and currents in the load network assuming the sinusoidal fundamental current flowing into the load as $i_R(\omega t) = I_R \sin(\omega t)$, where $I_R$ is its amplitude. The voltage $v(\omega t)$ across the switch can be represented as a sum of the dc voltage $V_{cc}$, fundamental voltage $v_R = i_R R_L$ across the load resistor and voltage $v_{odd}$ across the odd-harmonic resonators, that is

$$v(\omega t) = V_{cc} + v_{odd}\,[(2n+1)\omega t] + v_R(\omega t). \tag{3.16}$$

Since the time moment $t$ was chosen arbitrarily, by introducing a phase shift of $\pi$, Eq. (3.16) can be rewritten for periodical sinusoidal functions as

$$v(\omega t + \pi) = V_{cc} - v_{odd}[(2n+1)\omega t] - v_R(\omega t). \tag{3.17}$$

Then, the summation of Eqs. (3.16) and (3.17) yields

$$v(\omega t) = 2V_{cc} - v(\omega t + \pi). \tag{3.18}$$

From Eq. (3.18), it follows that maximum value of the collector voltage cannot exceed a value of $2V_{cc}$ and the time duration with maximum voltage of $v = 2V_{cc}$ coincides with the time duration with minimum voltage of $v = 0$. Since the collector voltage is zero when the switch is closed, the only possible waveform for the collector voltage is a square wave composed of only dc, fundamental-frequency, and odd-harmonic components.

During the interval $0 < \omega t \leq \pi$ when switch is closed, the current $i(\omega t)$ flowing through the switch can be written as

$$i(\omega t) = I_0 + i_{even}(2n\,\omega t) + i_R(\omega t). \tag{3.19}$$

Whereas during the interval $\pi < \omega t \leq 2\pi$ when the switch is open, the current $i(\omega t + \pi)$ is equal to zero resulting in

$$0 = I_0 + i_{even}(2n\,\omega t) - i_R(\omega t). \tag{3.20}$$

Then, by substituting Eq. (3.20) into Eq. (3.19), we can rewrite Eq. (3.19) as

$$i(\omega t) = 2i_R(\omega t) = 2I_R \sin(\omega t), \tag{3.21}$$

from which it follows that the amplitude of the current flowing through the switch during interval $0 < \omega t \leq \pi$ is two times greater than the amplitude of the fundamental current. Thus, in a common case, Eq. (3.19) can be rewritten as

$$i(\omega t) = I_R(\sin \omega t + |\sin \omega t|), \tag{3.22}$$

which means that the switch current represents half-sinusoidal pulses with amplitude equal to double the load-current amplitude.

Consequently, for a purely sinusoidal current flowing into the load shown in Fig. 3.8(*a*), the ideal collector voltage and current waveforms can be represented by the appropriate normalized waveforms shown in Figs. 3.8(*b*) and 3.8(*c*), respectively. Here, a sum of odd harmonics approximates a square voltage waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. Such a condition, with symmetrical collector voltage and current waveforms, corresponds to an idealized Class-F operation mode with 100% collector efficiency.

A Fourier analysis of the current and voltage waveforms allows us to obtain the equations for the dc current, fundamental voltage, and current components in the collector voltage and current waveforms:

the dc current $I_0$ can be calculated from Eq. (3.22) as

$$I_0 = \frac{1}{2\pi} \int_0^{\pi} 2I_R \sin \omega t \, d\omega t = \frac{2I_R}{\pi}, \tag{3.23}$$

the fundamental current component can be calculated from Eq. (3.22) as

$$I_1 = \frac{1}{\pi} \int_0^{\pi} 2I_R \sin^2 \omega t \, d\omega t = I_R, \tag{3.24}$$

and the fundamental voltage component can be calculated using Eq. (3.18) as

$$V_1 = V_R = \frac{1}{\pi} \int_{\pi}^{2\pi} 2V_{cc} \sin(\omega t + \pi) \, d\omega t = \frac{4V_{cc}}{\pi}. \tag{3.25}$$

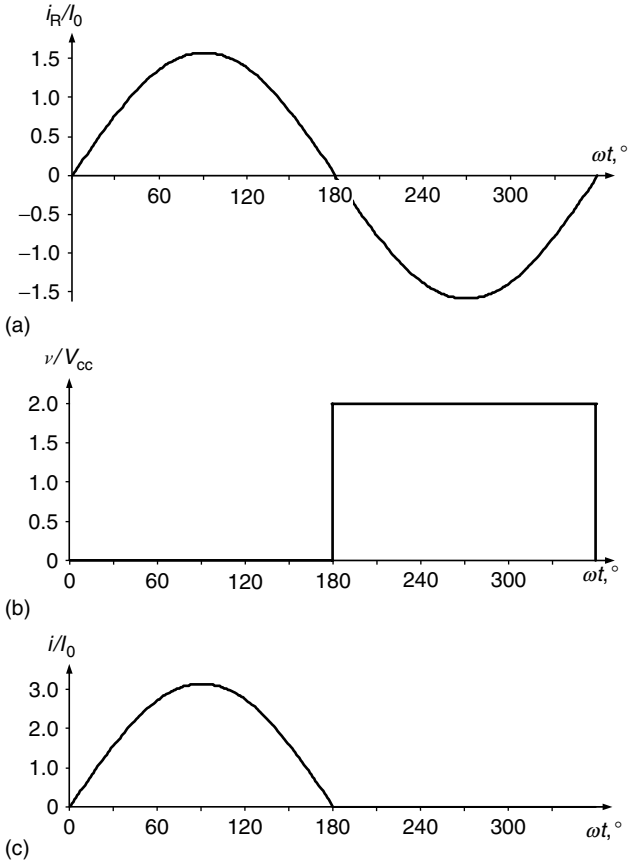



**Figure 3.8: Ideal waveforms of Class-F power amplifier.**

Then, the dc power and output power at the fundamental frequency are calculated from

$$P_0 = V_{cc} I_0 = \frac{2V_{cc} I_R}{\pi} \tag{3.26}$$

and

$$P_1 = \frac{V_1 I_1}{2} = \frac{2V_{cc} I_R}{\pi}, \tag{3.27}$$

resulting in a theoretical collector efficiency with maximum value of

$$\eta = \frac{P_1}{P_0} = 100\%. \tag{3.28}$$

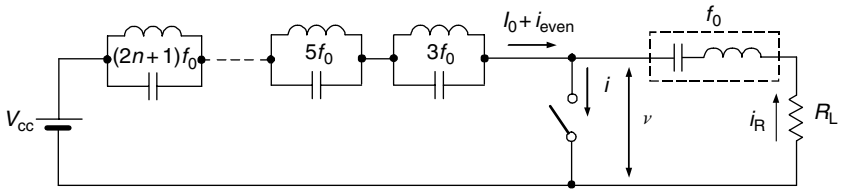



**Figure 3.9: Equivalent circuit of Class-F power amplifier with series filter.**

The impedance conditions seen by the device collector for idealized Class-F mode must be equal to

$$Z_1 = R_1 = \frac{8}{\pi^2}\frac{V_{cc}}{I_0} \tag{3.29}$$

$$Z_{2n} = 0 \quad \text{for even harmonics} \tag{3.30}$$

$$Z_{2n+1} = \infty \quad \text{for odd harmonics,} \tag{3.31}$$

which are similar to that derived from the limiting case of the optimum efficiency Class-B mode [15].

The collector square voltage and half-sinusoidal current waveforms can be similarly obtained by using a multiple-resonator circuit shown in Fig. 3.9, where the parallel resonators tuned to the third, fifth, and higher-order odd harmonics are located between the voltage supply and collector, while the series resonant circuit tuned to the fundamental frequency $f_0$ provides the sinusoidal current flowing into the load.

## 3.3 Class F with Maximally Flat Waveforms

Although it is impossible to realize the ideal harmonic-impedance conditions in real practice, the peaking of at least several current and voltage harmonic components should be provided to achieve high-efficiency operation of the power amplifier. The more the voltage waveform provided by higher-order harmonic components can be flattened, the less power dissipation due to flowing of the output current—when output voltage is extremely small—occurs. To understand common design principles and to numerically calculate power-amplifier efficiency according to the appropriate number of the frequency harmonic components of voltage and current waveforms, let us describe a design technique applied to Class-F approximation with maximally flat waveforms [16]. The output network is assumed ideal to deliver only the fundamental frequency power to the load without loss. The active device represents an ideal current source with zero saturation voltage and output capacitance. Flattening of the voltage and current waveforms to realize Class-F operation can be accomplished by using odd harmonic components to approximate a square voltage waveform, and even harmonic components to approximate a half-sinusoidal current waveform given by

$$v(\omega t) = V_{cc} + V_1 \sin \omega t + \sum_{n=3,5,7,\ldots}^{\infty} V_n \sin n\omega t \tag{3.32}$$

$$i(\omega t) = I_0 - I_1 \sin \omega t - \sum_{n=2,4,6,\ldots}^{\infty} I_n \cos n\omega t. \tag{3.33}$$

For the symmetrical flattened voltage waveforms shown in Fig. 3.10, the medium points where the voltage waveform reaches its maximum and minimum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Maximum flatness at the minimum voltage requires the even derivatives to be zero at $\omega t = 3\pi/2$. Since the odd-order derivatives are equal to zero because $\cos(n\pi/2) = 0$ for odd $n$, it is necessary to define the even-order derivatives of the voltage waveform given by Eq. (3.32). As a result, for a voltage spectrum including odd frequency components up to the seventh component, the second, fourth, and sixth derivatives are

$$\frac{d^2v}{d(\omega t)^2} = -V_1 \sin \omega t - 9V_3 \sin 3\omega t - 25V_5 \sin 5\omega t - 49V_7 \sin 7\omega t \tag{3.34}$$

$$\frac{d^4v}{d(\omega t)^4} = V_1 \sin \omega t + 81V_3 \sin 3\omega t + 625V_5 \sin 5\omega t + 2401V_7 \sin 7\omega t \tag{3.35}$$

$$\frac{d^6v}{d(\omega t)^6} = -V_1 \sin \omega t - 729V_3 \sin 3\omega t - 15625V_5 \sin 5\omega t - 117649V_7 \sin 7\omega t. \tag{3.36}$$

At the minimum points, these derivatives must be equal to zero,

$$\left.\frac{d^2v}{d(\omega t)^2}\right|_{\omega t=\frac{3}{2}\pi} = \left.\frac{d^4v}{d(\omega t)^4}\right|_{\omega t=\frac{3}{2}\pi} = \left.\frac{d^6v}{d(\omega t)^6}\right|_{\omega t=\frac{3}{2}\pi} = 0. \tag{3.37}$$

Consequently, a system of three equations to calculate the odd harmonic-voltage amplitudes ($V_3$, $V_5$, and $V_7$) through the dc component $V_{cc}$ and fundamental voltage amplitude $V_1$ can be written as

$$V_1 - 9V_3 + 25V_5 - 49V_7 = 0 \tag{3.38}$$

$$V_1 - 81V_3 + 625V_5 - 2401V_7 = 0 \tag{3.39}$$

$$V_1 - 729V_3 + 15625V_5 - 117649V_7 = 0. \tag{3.40}$$

For the third harmonic peaking when only the third harmonic component together with the fundamental one is present (assuming $V_5 = V_7 = 0$), Eq. (3.38) gives

$$V_3 = \frac{1}{9} V_1. \tag{3.41}$$

Then, from Eq. (3.32) at $\omega t = 3\pi/2$ when $v(\omega t) = 0$, the optimum amplitudes of the first and the third harmonics are defined by

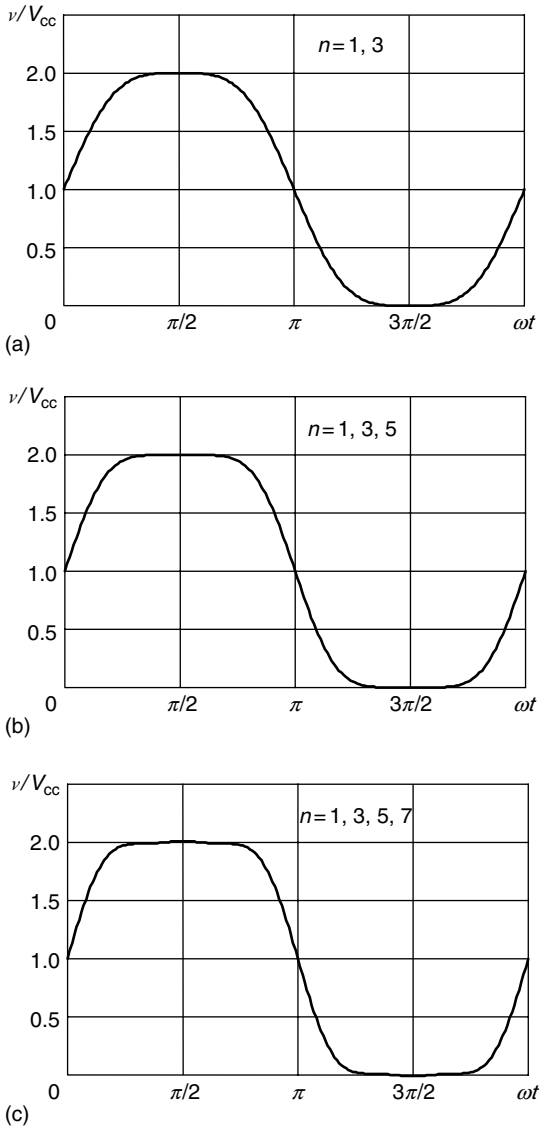



**Figure 3.10: Voltage waveforms for *n* harmonic peaking.**

$$V_1 = \frac{9}{8}V_{cc} \quad V_3 = \frac{1}{8}V_{cc}. \tag{3.42}$$

For the fifth harmonic peaking with third and fifth harmonic components (assuming $V_7 = 0$), the simultaneous solution of Eqs. (3.38) and (3.39) yields

$$V_3 = \frac{1}{6}V_1 \quad V_5 = \frac{1}{50}V_1 \tag{3.43}$$

and, consequently,

$$V_1 = \frac{75}{64}V_{cc} \quad V_3 = \frac{25}{128}V_{cc} \quad V_5 = \frac{3}{128}V_{cc}. \tag{3.44}$$

Similarly, for the seventh harmonic peaking with third, fifth, and seventh harmonic components, simultaneous solution of Eqs. (3.38) to (3.40) yields

$$V_3 = \frac{1}{5}V_1 \quad V_5 = \frac{1}{25}V_1 \quad V_7 = \frac{1}{245}V_1, \tag{3.45}$$

resulting for zero collector voltages in

$$\begin{aligned} V_1 &= \frac{1225}{1024}V_{cc} \quad V_3 = \frac{245}{1024}V_{cc} \\ V_5 &= \frac{49}{1024}V_{cc} \quad V_7 = \frac{5}{1024}V_{cc}. \end{aligned} \tag{3.46}$$

The voltage waveforms for the third-harmonic peaking ($n = 1, 3$), fifth harmonic peaking ($n = 1, 3, 5$), and seventh-harmonic peaking ($n = 1, 3, 5, 7$) are shown in Fig. 3.10.

For the symmetrical current waveforms shown in Fig. 3.11, the medium points where the current waveform reaches its minimum and maximum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Since the odd-order derivatives are equal to zero because $\cos(\pi/2) = 0$ and $\sin(n\pi/2) = 0$ for even $n$, it is sufficient to determine the even-order derivatives of the current waveform given by Eq. (3.33). Maximum flatness at the minimum current requires the even derivatives to be zero at $\omega t = \pi/2$. As a result, for a current spectrum including even frequency components up to the sixth component, the second, fourth, and sixth derivatives of the current waveform are

$$\frac{d^2 i}{d(\omega t)^2} = I_1 \sin \omega t + 4I_2 \cos 2\omega t + 16I_4 \cos 4\omega t + 36I_6 \cos 6\omega t \tag{3.47}$$

$$\frac{d^4 i}{d(\omega t)^4} = -I_1 \sin \omega t - 16I_2 \cos 2\omega t - 256I_4 \cos 4\omega t - 1296I_6 \cos 6\omega t \tag{3.48}$$

$$\frac{d^6 i}{d(\omega t)^6} = I_1 \sin \omega t + 64 I_2 \cos 2\omega t + 4096 I_4 \cos 4\omega t + 46656 I_6 \cos 6\omega t \tag{3.49}$$

At the minimum points, these derivatives must be equal to zero,

$$\left.\frac{d^2 i}{d(\omega t)^2}\right|_{\omega t=\frac{\pi}{2}} = \left.\frac{d^4 i}{d(\omega t)^4}\right|_{\omega t=\frac{\pi}{2}} = \left.\frac{d^6 i}{d(\omega t)^6}\right|_{\omega t=\frac{\pi}{2}} = 0. \tag{3.50}$$

Hence, a system of three equations to calculate the even harmonic current amplitudes ($I_2$, $I_4$, and $I_6$) through the dc component $I_0$ and fundamental current amplitude $I_1$ can be written as

$$I_1 - 4I_2 + 16I_4 - 36I_6 = 0 \tag{3.51}$$

$$I_1 - 16I_2 + 256I_4 - 1296I_6 = 0 \tag{3.52}$$

$$I_1 - 64I_2 + 4096I_4 - 46656I_6 = 0. \tag{3.53}$$

For the second harmonic peaking when only the second harmonic component together with the fundamental one is present (assuming $I_4 = I_6 = 0$), Eq. (3.51) gives

$$I_2 = \frac{1}{4} I_1. \tag{3.54}$$

Then, from Eq. (3.51) at $\omega t = \pi/2$ when $i(\omega t) = 0$, the optimum amplitudes are obtained by

$$I_1 = \frac{4}{3} I_0 \quad I_2 = \frac{1}{3} I_0. \tag{3.55}$$

For the fourth-harmonic peaking with second- and fourth-harmonic components (assuming $I_6 = 0$), simultaneous solution of Eqs. (3.51) and (3.52) yields

$$I_2 = \frac{5}{16} I_1 \quad I_4 = \frac{1}{64} I_1 \tag{3.56}$$

and, consequently,

$$I_1 = \frac{64}{45} I_0 \quad I_2 = \frac{4}{9} I_0 \quad I_4 = \frac{1}{45} I_0. \tag{3.57}$$

Similarly, for the sixth-harmonic peaking with second, fourth, and sixth harmonic components, simultaneous solution of Eqs. (3.51) to (3.53) yields

$$I_2 = \frac{175}{512} I_1 \quad I_4 = \frac{7}{256} I_1 \quad I_6 = \frac{1}{512} I_1 \tag{3.58}$$

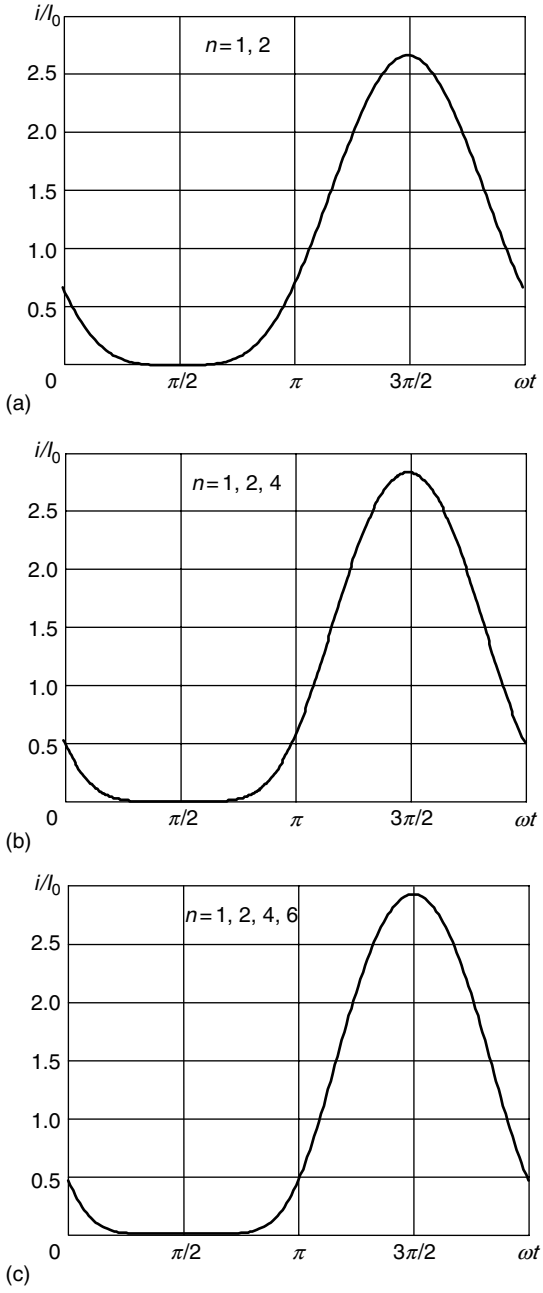



**Figure 3.11: Current waveforms for *n*-harmonic peaking.**

resulting for zero collector current in

$$I_1 = \frac{256}{175} I_0 \quad I_2 = \frac{1}{2} I_0$$
$$I_4 = \frac{1}{25} I_0 \quad I_6 = \frac{1}{350} I_0. \tag{3.59}$$

The current waveforms for the second-harmonic peaking ($n = 1, 2$), fourth-harmonic peaking ($n = 1, 2, 4$), and sixth-harmonic peaking ($n = 1, 2, 4, 6$) are shown in Fig. 3.11.

To compare the effectiveness of the operating modes with different voltage and current harmonic peaking, let us calculate the collector (drain) efficiency $\eta$ of each operating mode in accordance with

$$\eta = \frac{P_1}{P_0} = \frac{1}{2} \frac{I_1 V_1}{I_0 V_{cc}}. \tag{3.60}$$

The resultant efficiencies for various combinations of voltage and current harmonic components, as presented in Table 3.1, show that the efficiency increases with an increase in the number of voltage and current harmonic components. To increase efficiency, it is more desirable to provide harmonic peaking in consecutive numerical order—both for voltage and current harmonic components—than to increase the number of the harmonic components into only voltage or current waveforms. Class-F operation becomes mostly effective in comparison with Class-B operation if at least third voltage harmonic peaking and fourth harmonic current peaking are realized. An inclusion of fifth voltage harmonic component increases the efficiency to 83.3%. An additional inclusion of sixth harmonic component into the current waveform and seventh harmonic component into the voltage waveform leads to efficiencies up to 94%.

Maximum efficiency for a given set of harmonics can be additionally increased to fix the fundamental-frequency amplitude and then adjust the amplitude of the harmonics to minimize the downward excursion of the overall waveform [17]. Fixing the waveform minimum at zero gives the minimum supply voltage needed for full output power, thus maximizing efficiency. As a result, the maximum efficiency can be generally improved by 6–8% compared to those for maximally flat waveforms. Most Class-F power amplifiers employ a conduction angle of 180° when all of the odd harmonics of a half-sinusoidal current waveform are nulled, as are all of the even harmonics of a rectangular-voltage waveform. However, conduction angles other than 180° generally cause all harmonics to be present. A given harmonic is nulled at a specific conduction angle, but all or most of the others remain. Consequently, flattening of the voltage waveform during the time of conduction must be accomplished by the addition of a single harmonic [18]. For example, for a conduction angle of approximately 130°, the use of the fourth harmonic increases efficiency by about 6% compared with that of a conventional Class-C power amplifier.

**Table 3.1 Resultant Efficiencies for Various Combinations of Voltage and Current Harmonic Components**

| Current Harmonic Components | Voltage Harmonic Components | | | | |
|---|---|---|---|---|---|
| | 1 | 1, 3 | 1, 3, 5 | 1, 3, 5, 7 | 1, 3, 5, ..., $\infty$ |
| 1 | $1/2 = 0.500$ | $9/16 = 0.563$ | $75/128 = 0.586$ | $1225/2048 = 0.598$ | $2/\pi = 0.637$ |
| 1, 2 | $2/3 = 0.667$ | $3/4 = 0.750$ | $25/32 = 0.781$ | $1225/1536 = 0.798$ | $8/3\pi = 0.849$ |
| 1, 2, 4 | $32/45 = 0.711$ | $4/5 = 0.800$ | $5/6 = 0.833$ | $245/288 = 0.851$ | $128/45\pi = 0.905$ |
| 1, 2, 4, 6 | $128/175 = 0.731$ | $144/175 = 0.823$ | $6/7 = 0.857$ | $7/8 = 0.875$ | $512/175\pi = 0.931$ |
| 1, 2, 4, ..., $\infty$ | $\pi/4 = 0.785$ | $9\pi/32 = 0.884$ | $75\pi/256 = 0.920$ | $1225\pi/4096 = 0.940$ | $1 = 1.000$ |

## 3.4 Class F with Quarter-wave Transmission Line

Ideally, a control of an infinite number of the harmonics maintaining a square voltage waveform and a half-sinusoidal current waveform at the drain can be provided using a series quarter-wave transmission line and a parallel-tuned resonant circuit, as shown in Fig. 3.12. This type of Class-F power amplifier was initially proposed to be used at very high frequencies where implementation of the load networks with only lumped elements is difficult and the parasitic device output (lead or package) inductor is sufficiently small [13, 14]. In this case, the quarter-wave transmission line transforms the load impedance according to

$$R = \frac{Z_0^2}{R_L}, \tag{3.61}$$

where $Z_0$ is the characteristic impedance of a transmission line [19]. For even harmonics, the short circuit on the load side of the transmission line is repeated, thus producing a short circuit at the drain. However, the short circuit at the load produces an open circuit at the drain for odd harmonics with resistive load at the fundamental.

Generally, at low drive level, the active device acts as a current source (voltage-controlled in the case of MOSFETs or MESFETs and current-controlled in the case of bipolar

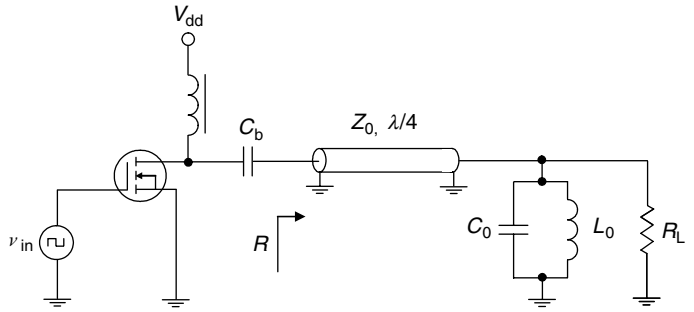



**Figure 3.12: Class-F power amplifier with series quarter-wave transmission line.**

transistors). As drive input increases, the active device enters voltage saturation resulting in a harmonic-generation process. Since the transmission line presents the high impedance conditions to all odd harmonics, all odd harmonics provide a proper contribution to the output-voltage waveform. As a result, at high drive level, the output voltage waveform becomes a complete square wave and the active device is voltage-saturated for a full half-cycle. In this case, the transistor acts as a switch rather than a saturating current source.

An alternative configuration of the Class-F power amplifier with a shunt transmission line located between the dc power supply and device collector is shown in Fig. 3.13(*a*). In this case, there is no need to use an RF choke and a series blocking capacitor because a series fundamentally tuned resonant circuit is used instead of a parallel fundamentally tuned resonant circuit. However, unlike the case with a series quarter-wave transmission line, such a Class-F load network configuration with a shunt quarter-wave transmission line does not provide an impedance transformation. Therefore, the load resistance $R$, which is equal to the active device output resistance at the fundamental, must then be transformed to the standard load impedance. Let us now derive analytically some basic fundamental properties of a quarter-wave transmission line. The transmission line in time domain can be represented as an element with finite delay time depending on its electrical length. Consider a simple load

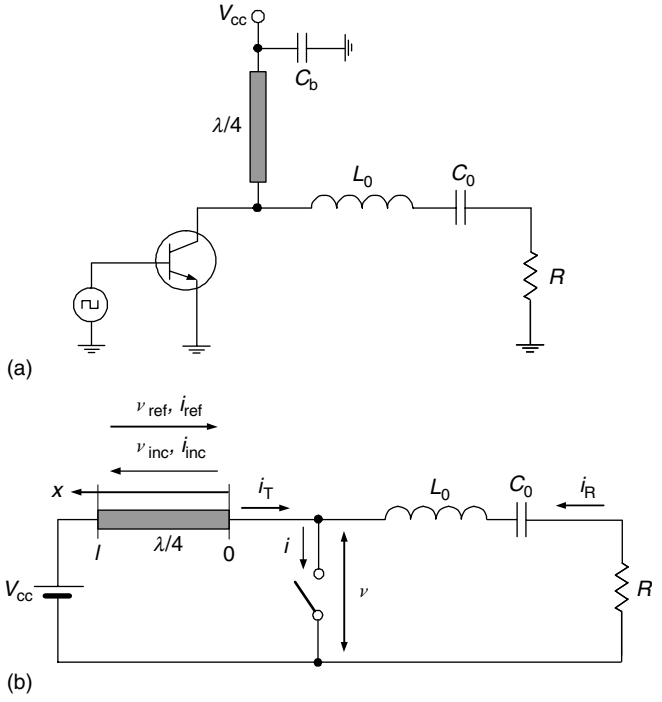



**Figure 3.13: Class-F power amplifier with shunt quarter-wave transmission line.**

network of the Class-F power amplifier shown in Fig. 3.13(*b*) consisting of a parallel quarter-wave transmission line grounded at the end through power supply, a series fundamentally tuned $L_0C_0$-circuit, and a load resistance $R$. In an idealized case, the intrinsic device output capacitance is assumed negligible to affect the power amplifier RF performance. The loaded quality factor $Q_L$ of the series resonant $L_0C_0$-circuit is high enough to provide the sinusoidal output current $i_R$ flowing into the load $R$.

To define the collector voltage and current waveforms, consider the electrical behavior of a homogeneous lossless quarter-wave transmission line connected to the dc voltage supply with RF grounding [20]. In this case, the voltage $v(t, x)$ in any cross section of such a transmission line can be represented as a sum of the incident and reflected voltages, $v_{inc}(\omega t - 2\pi x/\lambda)$ and $v_{refl}(\omega t + 2\pi x/\lambda)$, generally with an arbitrary waveform. When $x = 0$, the voltage $v(t, x)$ is equal to the collector voltage

$$v(\omega t) = v(t, 0) = v_{inc}(\omega t) + v_{refl}(\omega t). \tag{3.62}$$

At the same time, at another end of the transmission line when $x = \lambda/4$, the voltage is constant and equal to

$$V_{cc} = v(t, \pi/2) = v_{inc}(\omega t - \pi/2) + v_{refl}(\omega t + \pi/2). \tag{3.63}$$

Since the time moment $t$ was chosen arbitrarily, let us rewrite Eq. (3.63) using a phase shift of $\pi/2$ for each voltage by

$$v_{inc}(\omega t) = V_{cc} - v_{refl}(\omega t + \pi). \tag{3.64}$$

Substituting Eq. (3.62) into Eq. (3.60) yields

$$v(\omega t) = v_{refl}(\omega t) - v_{refl}(\omega t + \pi) + V_{cc}. \tag{3.65}$$

Consequently, for the phase shift of $\pi$, the collector voltage can be obtained by

$$v(\omega t + \pi) = v_{refl}(\omega t + \pi) - v_{refl}(\omega t + 2\pi) + V_{cc}. \tag{3.66}$$

For an idealized operation condition with a 50% duty cycle when during half a period the transistor is turned on and during another half a period the transistor is turned off with an overall period of $2\pi$, the voltage $v_{refl}(\omega t)$ can be considered the periodical function with a period of $2\pi$,

$$v_{refl}(\omega t) = v_{refl}(\omega t + 2\pi). \tag{3.67}$$

As a result, the summation of Eqs. (3.65) and (3.66) results in the expression for collector voltage in the form of

$$v(\omega t) = 2V_{cc} - v(\omega t + \pi). \tag{3.68}$$

From Eq. (3.68), it follows that the maximum value of the collector voltage cannot exceed a value of $2V_{cc}$, and the time duration with maximum voltage of $v = 2V_{cc}$ coincides with the time duration with minimum voltage of $v = 0$.

Similarly, an equation for the current $i_T$ flowing into the quarter-wave transmission line can be obtained as

$$i_T(\omega t) = i_T(\omega t + \pi), \tag{3.69}$$

which means that the period of a signal flowing into the quarter-wave transmission line is equal to $\pi$ because it contains only even harmonics, since a quarter-wave transmission line has an infinite impedance at odd harmonics.

Let the transistor operate as an ideal switch when it is closed during the interval $0 < \omega t \leq \pi$ where $v = 0$ and open during the interval $\pi < \omega t \leq 2\pi$, where $v = 2V_{cc}$ according to Eq. (3.68). During the interval $\pi < \omega t \leq 2\pi$ when the switch is open, the load is connected directly to the transmission line and $i_T = -i_R \sin - I_R \sin \omega t$. Consequently, during the interval $0 < \omega t \leq \pi$ when the switch is closed, $i_T \sin I_R \sin \omega t$ according to Eq. (3.68). Hence, the current flowing into the quarter-wave transmission line at any $\omega t$ can be represented by

$$i_T(\omega t) = I_R|\sin \omega t|, \tag{3.70}$$

where $I_R$ is the amplitude of current flowing into the load.

Since the collector current is defined as $i = i_T + i_R$, then

$$i(\omega t) = I_R(\sin \omega t + |\sin \omega t|), \tag{3.71}$$

which means that the collector current represents half-sinusoidal pulses with amplitude equal to double the load-current amplitude.

Consequently, for a purely sinusoidal current flowing into the load due to infinite loaded quality factor of the series fundamentally tuned $L_0C_0$ circuit shown in Fig. 3.8($a$), the ideal collector voltage and current waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms shown in Figs. 3.8($b$) and 3.8($c$), respectively, where $I_0$ is the dc current. Here, a sum of odd harmonics approximates a square voltage waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. The waveform corresponding to the normalized current flowing into the quarter-wave transmission line, shown in Fig. 3.14, represents a sum of even harmonics. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously.

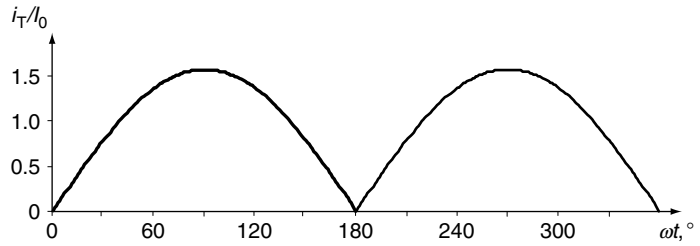



**Figure 3.14: Ideal current waveform in quater-wave transmission line.**

## 3.5 Effect of Saturation Resistance and Shunt Capacitance

In a real transistor, the saturation or on-resistance $r_{sat}$ is not equal to zero, and transistor dissipates some amount of power due to the collector current flowing through this resistance when the transistor is turned on. The simplified equivalent circuit of a Class-F power amplifier with a quarter-wave transmission line where the transistor is represented by a non-ideal switch with saturation resistance $r_{sat}$ and parasitic-output capacitance $C_{out}$ is shown in Fig. 3.15. During the interval $0 < \omega t \leq \pi$ when the switch is closed, the saturation voltage $v_{sat}$ due to the current $i(\omega t)$ flowing through the switch can be written as

$$v_{sat}(\omega t) = V_{sat} \sin \omega t = 2I_R r_{sat} \sin \omega t, \tag{3.72}$$

where, by using Eq. (3.25), the saturation voltage amplitude $V_{sat}$ can be obtained by

$$V_{sat} = 2V_R \frac{r_{sat}}{R} = \frac{8V_{cc}}{\pi} \frac{r_{sat}}{R}. \tag{3.73}$$

The collector current and voltage waveforms are shown in Fig. 3.16 where the half-sinusoidal current flowing through the saturation resistance $r_{sat}$ causes the deviation of the voltage waveform from the ideal square waveform. In this case, the bottom part of the voltage waveform becomes sinusoidal with the amplitude $V_{sat}$ during the interval $0 < \omega t \leq \pi$. From

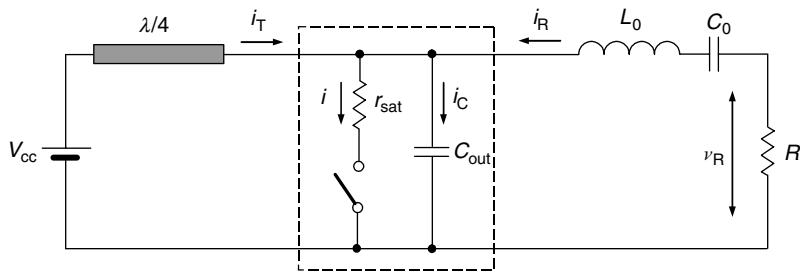



**Figure 3.15: Effect of parasitic on-resistance and shunt capacitance.**

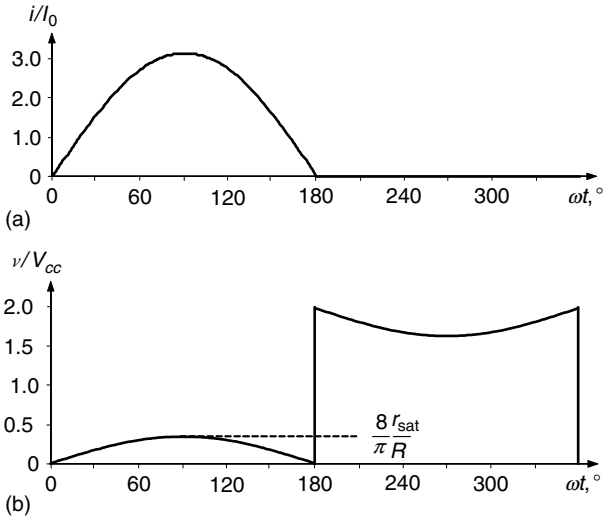



**Figure 3.16: Idealized collector current and voltage waveforms with non-zero on-resistance.**

Eq. (3.18), it follows that the same sinusoidal behavior will correspond to the top part of the voltage waveform during the interval $\pi < \omega t \leq 2\pi$.

Now let us evaluate the power losses and collector efficiency due to presence of the saturation resistance $r_{sat}$. Using Eqs. (3.21), (3.23), and (3.25) results in

$$\frac{P_{sat}}{P_0} = \frac{1}{2\pi}\int_0^{2\pi} \frac{i^2(\omega t) r_{sat}}{I_0 V_{cc}}\, d\omega t = \frac{r_{sat}}{2\pi I_0 V_{cc}}\int_0^{2\pi} (2I_R)^2 \sin^2 \omega t\; d\omega t$$
$$= \frac{r_{sat} I_R}{V_{cc}}\frac{I_R}{I_0} = \frac{r_{sat}}{R}\frac{I_R}{I_0}\frac{V_R}{V_{cc}} = \frac{2r_{sat}}{R}. \tag{3.74}$$

Hence, the collector efficiency can be calculated from

$$\eta = 1 - \frac{P_{sat}}{P_0} = 1 - \frac{2r_{sat}}{R}. \tag{3.75}$$

In practice, the idealized collector voltage and current waveforms can be realized at low frequencies when the effect of the device collector capacitance is negligible. At higher frequencies, the effect of the collector capacitance contributes to a non-zero switching time resulting in time periods when the collector voltage and collector current exist at the same time when $v > 0$ and $i > 0$. Consequently, such a load network with shunt capacitance cannot provide the switched-mode operation with an instantaneous transition from the device pinch-off to saturation mode. Therefore, during a non-zero time interval,

the device operates in active region as a current source with the reverse-biased collector-base junction and the collector current is provided by this current source.

The current flowing through the collector capacitance can be determined by differentiating both parts of Eq. (3.18), by taking into account that voltage $v$ is the voltage across the capacitance $C$, as

$$i_C(\omega t) = -i_C(\omega t + \pi), \tag{3.76}$$

that is, the current due to the capacitance-charging process is equal to the current due to the capacitance-discharging process with opposite sign, and the durations of the charging and discharging periods are equal.

From Fig. 3.15, it follows that the current flowing through the collector capacitance at the arbitrary time moment $t$ can be written as

$$i_C(\omega t) = i_T(\omega t) + i_R(\omega t) - i(\omega t), \tag{3.77}$$

whereas, at the time moment $(t + \pi/\omega)$, it can be obtained by

$$i_C(\omega t + \pi) = i_T(\omega t + \pi) + i_R(\omega t + \pi) - i(\omega t + \pi). \tag{3.78}$$

The output current flowing into the load is written as sinusoidal as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi), \tag{3.79}$$

where $\varphi$ is the initial phase shift due to the finite value of the collector capacitance.

Then, by taking into account Eqs. (3.69) and (3.76), from Eq. (3.78) it follows that

$$-i_C(\omega t) = i_T(\omega t) - i_R(\omega t) - i(\omega t + \pi). \tag{3.80}$$

Adding Eqs. (3.77) and (3.80) yields

$$i(\omega t) + i(\omega t + \pi) = 2i_T(\omega t), \tag{3.81}$$

specifying the relationship in the time domain between the collector current and current flowing into the transmission line.

The collector current and voltage waveforms are shown in Fig. 3.17 where the phase angle $\varphi_1$ corresponds to the beginning of the transistor saturation mode, and the phase angle $\varphi_2$ corresponds to the beginning of the active mode and collector capacitance-charging process start-up. During the saturation interval when $\varphi_1 < \omega t < \varphi_2$, the collector current $i$ can be defined using Eqs. (3.77), (3.79), and (3.80) by

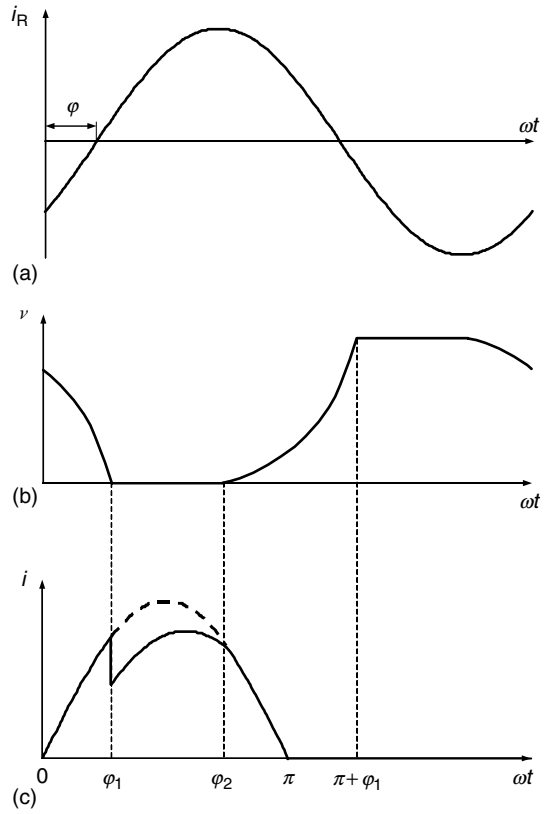



**Figure 3.17: Effect of shunt capacitance on voltage and current waveforms.**

$$i(\omega t) = i_T(\omega t) + i_R(\omega t) = 2i_R(\omega t) = 2I_R \sin(\omega t + \varphi). \tag{3.82}$$

In active region when $0 \leq \omega t \leq \varphi_1$ and $\varphi_2 \leq \omega t \leq \pi$, the collector current flowing into the load network is defined by the input driving signal and, for the conduction angle of 180°, represents the periodic half-sinusoidal pulses written as

$$i(\omega t) = I_{active}(\sin \omega t + |\sin \omega t|), \tag{3.83}$$

where the collector current amplitude $I_{active}$ in active region has a higher value than the one in saturation mode when $I_{sat} = 2I_R$ (see Eq. (3.82)) due to the shunting effect of the forward-biased collector-base diode junction when device is saturated. The moment of the opening of the collector-base junction corresponds to the time moment $\varphi_1$ with instantaneous reduction in the collector current waveform, as shown in Fig. 3.17(*c*). Physically, this effect can be explained by the carrier injection from the device collector to its base region as a result of forward-biasing of the collector-base junction. The saturation period is characterized by the diffusion capacitance of the forward-biased collector-base junction, whereas, in active or

pinch-off regions, the reverse-biased collector-base junction is described by the junction capacitance, which value is substantially smaller. The saturation period is ended at the time moment $\varphi_2$ corresponding to the beginning of the active mode, and collector junction capacitance charging process start-up.

By using Eqs. (3.70), (3.81), and (3.83), the current flowing into the transmission line $i_T$ and current flowing through the collector capacitance $i_C$ can be obtained by

$$i_T(\omega t) = I_{active}|\sin \omega t| \tag{3.84}$$

$$i_C(\omega t) = 2[I_R \sin(\omega t + \varphi) - I_{active} \sin \omega t]. \tag{3.85}$$

Power losses due to the charging and discharging processes of the device collector capacitance can be calculated from

$$P_{loss} = \frac{1}{2\pi} \int_0^{\varphi_1} v(\omega t) i(\omega t) d\omega t + \frac{1}{2\pi} \int_{\varphi_2}^{\pi} v(\omega t) i(\omega t) d\omega t, \tag{3.86}$$

where the collector voltage $v$ coincides with the voltage across the capacitance $C$. From Eq. (3.86), it follows that the longer active region due to the larger collector capacitance, the more power losses and less efficient operation of the power amplifier. From the results of numerical calculations, the maximum operating frequency where the collector efficiency of a Class-F power amplifier with the effect of the output capacitance $C_{out}$ is higher than the collector efficiency of a conventional Class-B power amplifier can be approximately calculated from

$$f_{max} \cong \frac{0.47}{RC_{out}}, \tag{3.87}$$

where the output capacitance $C_{out}$ is assumed a total collector capacitance (including the capacitances of the passive and active parts of the collector-base junction) corresponding to the dc bias operation points [20].

## 3.6 Load Networks with Lumped Elements

Theoretical results show that the proper control of the second and third harmonics only can significantly increase the collector efficiency of the power amplifier by flattening the output voltage waveform. Since practical realization of a multi-element high-order *LC*-resonant circuit can cause a serious implementation problem, especially at higher frequencies, it is sufficient to be confined to a three- or four-element resonant circuit composing the load network of the power amplifier. In addition, it is necessary to take into account that, in practice, both extrinsic and intrinsic transistor parasitic elements like output shunt capacitance

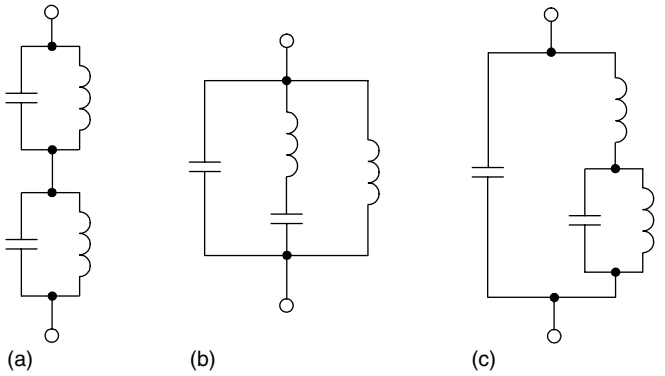



**Figure 3.18: Two-terminal reactive networks with series and parallel resonators.**

or serious inductance have a substantial effect on the efficiency. The output capacitance $C_{out}$ can represent the collector capacitance $C_c$ in the case of the bipolar transistor or drain-source capacitance plus gate-drain capacitance $C_{ds} + C_{gd}$ in the case of the FET device. The output inductance $L_{out}$ is generally composed of the bondwire and lead inductances for a packaged transistor, the effect of which becomes significant at higher frequencies. The typical two-terminal reactive networks with series and parallel resonators used in a practical design procedure, which provide ideally infinite impedances at the fundamental and third harmonics and zero impedance at the second harmonic, are shown in Fig. 3.18 [21, 22, 23].

At microwave and millimeter frequencies, it is required to minimize a number of elements to reduce the effect of any possible circuit parasitics. Fig. 3.19 shows the simple third harmonic peaking load network where $C_{ds}$ is the drain-source capacitance of the MESFET device tuned together with inductance $L_1$ and capacitance $C_1$ for a parallel resonance at the third harmonic, while the series combination of $L_1$ and $C_1$ provides a series resonance at the second harmonic [24]. The load network input impedance $Z_{net}$ can be written as

$$Z_{net} = j\frac{\omega^2 L_1 C_1 - 1}{\omega C_1 - \omega C_{ds}(\omega^2 L_1 C_1 - 1)}. \tag{3.88}$$

As a result, applying two harmonic-impedance conditions, open-circuited for the third harmonic $Z_{net}(3\omega_0) = \infty$ and short-circuited for the second harmonic $Z_{net}(2\omega_0) = 0$ where $\omega_0$ is the fundamental angular frequency, the values of load-network elements as a function of $C_{ds}$ can be calculated from

$$C_1 = \frac{5}{4}C_{ds} \tag{3.89}$$

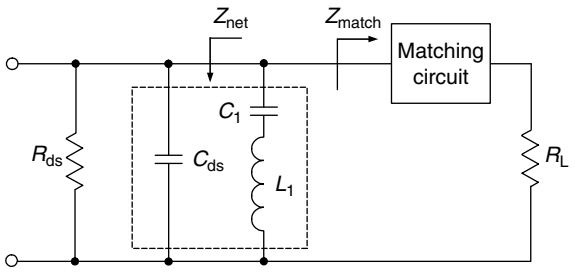



**Figure 3.19: Third-harmonic peaking Class-F load network.**

$$L_1 = \frac{1}{5\omega_0^2 C_{ds}}. \tag{3.90}$$

However, since the resulting impedance at the fundamental frequency is capacitive, it is necessary to compensate for the capacitive reactance by choosing the parameters of the matching circuit having an inductive reactance of its input impedance $Z_{match}$ at the fundamental and high impedance conditions at third and higher-order harmonic components.

By adding an additional element to a load network shown in Fig. 3.19, it is possible to compensate for the capacitive reactance at the fundamental frequency providing both high impedance at the fundamental and third harmonics and zero impedance at the second harmonic. Examples of such load networks with additional parallel and series resonant circuits located between the dc power supply and device output are shown in Fig. 3.20 [23, 25]. Here, the output circuit of the active device is represented by a multiharmonic current source, and $R_{out}$ is the resistance at the fundamental frequency defined as a ratio of the fundamental voltage at the device output to the fundamental current flowing into the device.

The reactive part of the output admittance or susceptance $B_{net} = \mathrm{Im}(Y_{net})$ of the load network with parallel resonant tank shown in Fig. 3.20($b$) including the device output capacitance $C_{out}$ can be written by

$$B_{net} = \omega C_{out} - \frac{1 - \omega^2 L_2 C_2}{\omega L_1 (1 - \omega^2 L_2 C_2) + \omega L_2}. \tag{3.91}$$

By applying three harmonic-impedance conditions $B_{net}(\omega_0) = B_{net}(3\omega_0) = \infty$ and $B_{net}(2\omega_0) = 0$ at the device collector or drain, that is, the open-circuited for fundamental and third harmonic components and short-circuited for second-harmonic components, Eq. (3.91) can be rewritten in the form of the following system of three equations:

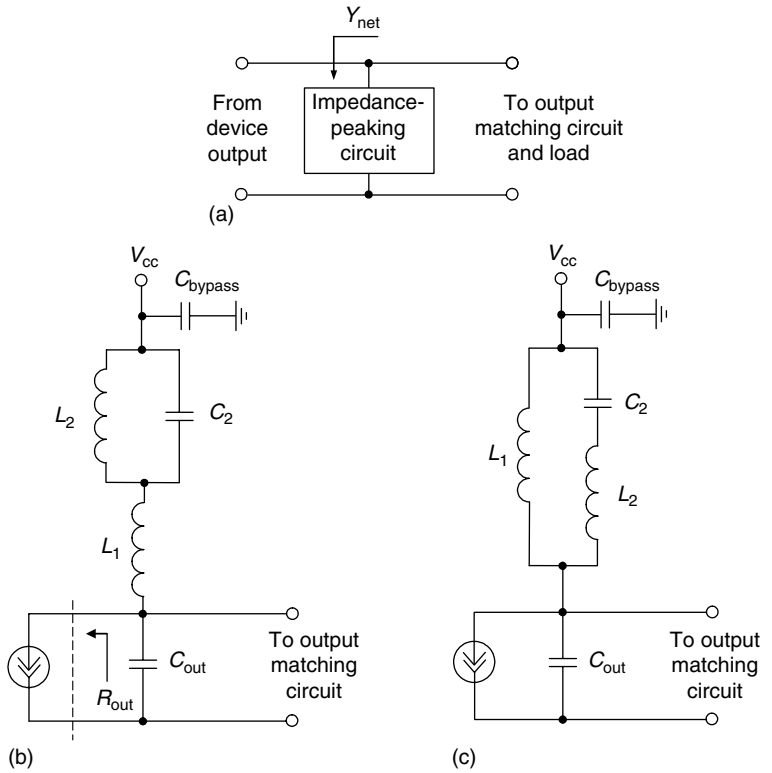



**Figure 3.20: Load networks with parallel and series resonant circuits.**

$$\begin{cases} (1-\omega_0^2 L_1 C_{\text{out}})(1-\omega_0^2 L_2 C_2) - \omega_0^2 L_2 C_{\text{out}} = 0 \\ L_1(1-4\omega_0^2 L_2 C_2) + L_2 = 0 \\ (1-9\omega_0^2 L_1 C_{\text{out}})(1-9\omega_0^2 L_2 C_2) - 9\omega_0^2 L_2 C_{\text{out}} = 0. \end{cases} \tag{3.92}$$

As a result, the ratios between elements of this impedance-peaking circuit are

$$L_1 = \frac{1}{6\omega_0^2 C_{\text{out}}} \tag{3.93}$$

$$L_2 = \frac{5}{3} L_1 \tag{3.94}$$

$$C_2 = \frac{12}{5} C_{\text{out}}, \tag{3.95}$$

where the sum of the reactance of the parallel resonant tank, consisting of an inductor $L_2$ and a capacitor $C_2$, and inductor $L_1$ create resonances at the fundamental and third harmonic

components, and the series capacitance of the tank circuit in series with $L_1$ creates a low-impedance series resonance at the second harmonic component [25].

Applying the same conditions for the load network with series-resonant circuit shown in Fig. 3.20($c$) results in the ratios between elements given by

$$L_1 = \frac{4}{9\omega_0^2 C_{\text{out}}} \tag{3.96}$$

$$L_2 = \frac{9}{15} L_1 \tag{3.97}$$

$$C_2 = \frac{15}{16} C_{\text{out}}, \tag{3.98}$$

where an inductance $L_2$ and a capacitance $C_2$ create a short-circuit condition at the second harmonic, and all elements create the parallel-resonant tanks for fundamental and third harmonic components [23].

To determine the amplitude characteristics of the load network in the frequency domain, it is best to represent the load network as shown in Fig. 3.20($a$) and simulate the small-signal $S$-parameters. Then, it is just necessary to plot a magnitude of $S_{21}$ in absolute values or in decibels. As an example, the frequency-response characteristic of the load network with a parallel-resonant circuit, whose parameters are calculated based on the chosen fundamental frequency $f_0 = 500\,\text{MHz}$, is depicted in Fig. 3.21. The circuit parameters are $C_{\text{out}} = 2.2\,\text{pF}$, $R_{\text{out}} = 200\,\Omega$, $C_2 = 5.3\,\text{pF}$, $L_1 = 7.7\,\text{nH}$, and $L_2 = 12.8\,\text{nH}$ with inductor quality factor $Q_{\text{ind}} = 20$. In this case, the power-amplifier efficiency will be effectively increased if the first

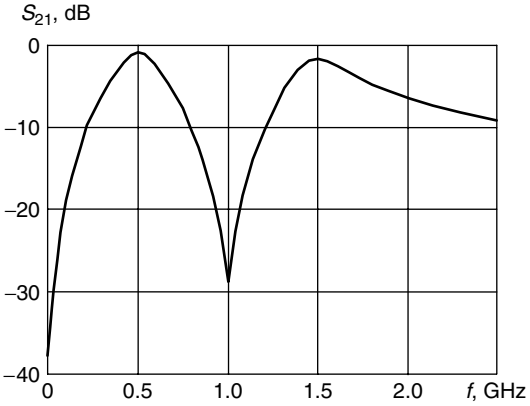



**Figure 3.21: Frequency response of load network with parallel-resonant circuit.**

element of the output matching circuit adjacent to the transistor output is series and inductive to provide high impedance at odd harmonics.

Careful design must be provided at higher frequencies or in the case of high-power mode when the transistor output resistance is sufficiently small. In this case, an effect of the output series inductance, including the bondwire and lead inductances for a packaged active device, becomes significant. The equivalent circuit of such an impedance-peaking circuit is shown in Fig. 3.22. Here, the series circuit consisting of an inductor $L_1$ and a capacitor $C_1$ creates a resonance at the third harmonic. Since the output inductor $L_{out}$ and capacitor $C_{out}$ are tuned to create an open-circuited condition at the third harmonic, the device collector sees resultant high impedance at the third harmonic.

To achieve a third-harmonic high impedance, an external inductance may be added to interconnect the device output inductance $L_{out}$ directly at the output terminal (collector or drain) if its value is not accurate enough. In addition, the parallel-resonant tank ($L_2$, $C_2$) is tuned to the second harmonic, while the series network ($L_1 + L_{out}$, $C_1$) is resonant at the second harmonic. As a result, the ratios between the network parameters are as follows [26]:

$$L_{out} = \frac{1}{9\omega_0^2 C_{out}} \tag{3.99}$$

$$L_1 = \frac{4}{5} L_{out} \tag{3.100}$$

$$C_1 = \frac{5}{4} C_{out} \tag{3.101}$$

$$L_2 = \frac{1}{4\omega_0^2 C_2}. \tag{3.102}$$

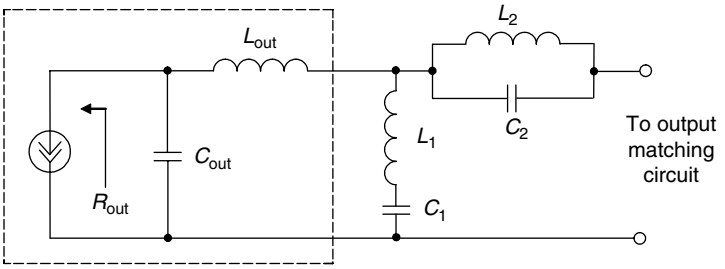



**Figure 3.22: Impedance-peaking circuit including device output inductance.**

As a first approximation for comparison between different operation modes, the output device resistance $R_{out}$ at the fundamental frequency required to realize a Class-F operation mode with third harmonic peaking can be estimated as the equivalent resistance determined at the fundamental frequency for an ideal Class-F operation, $R_{out} = R_1^{(F)} = V_1/I_1$, where $V_1$ and $I_1$ are the fundamental voltage and current at the device output. Assuming zero saturation voltage and using Eq. (3.25) yield

$$R_1^{(F)} = \frac{4}{\pi}\frac{V_{cc}}{I_1} = \frac{4}{\pi}R_1^{(B)}, \tag{3.103}$$

where $R_1^{(B)} = V_{cc}/I_1$ is the fundamental output resistance in an ideal Class B.

## 3.7 Load Networks with Transmission Lines

The ideal Class-F power amplifier with all even harmonic short-circuit termination and third-harmonic peaking achieves a maximum drain efficiency of 88.4%. Such an operation mode is easy to realize by using transmission lines in the load-network circuit. The load network impedance-peaking circuit topology of such a transmission-line power amplifier is shown in Fig. 3.23 [25, 26].

In this case, a quarter-wave transmission line $TL_1$ located between the dc power supply and drain terminal provides short-circuit termination for even harmonics. The electrical length $\theta_3$ of an open-circuit stub $TL_3$ is chosen to have a quarter wavelength at the third harmonic to realize short-circuit condition at the end of the series transmission line $TL_2$, whose electrical length $\theta_2$ should provide an inductive reactance to resonate with the device output capacitance $C_{out}$ at the third harmonic. As a result, the electrical lengths of the transmission lines on fundamental frequency can be obtained from

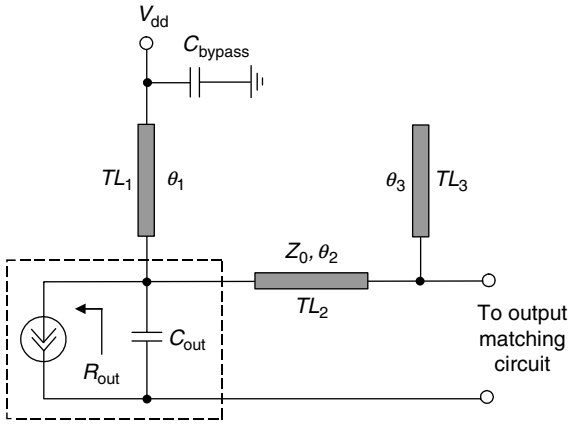



**Figure 3.23: Transmission-line impedance-peaking circuit.**

$$\theta_1 = \frac{\pi}{2} \tag{3.104}$$

$$\theta_2 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{\text{out}}}\right) \tag{3.105}$$

$$\theta_3 = \frac{\pi}{6}, \tag{3.106}$$

where $Z_0$ is the characteristic impedance of the series transmission line $TL_2$, and $\omega_0$ is the operating frequency. Fig. 3.24 shows an example of the frequency-response characteristic of the microstrip impedance-peaking circuit using alumina substrate for the device output resistance $R_{\text{out}} = 50\,\Omega$ and output capacitance $C_{\text{out}} = 2.2\,\text{pF}$, characteristic impedance of microstrip lines $Z_0 = 50\,\Omega$ and electrical length $\theta_2 = 15°$. From Fig. 3.24 it follows that if the short-circuited conditions for all even harmonics and third-harmonic peaking have taken place, an additional output impedance matching at the operating fundamental frequency $f_0 = 500\,\text{MHz}$ is required to compensate for the reactive part and to match the real part of the realized output impedance with the standard $50\,\Omega$ load impedance.

The close approximation to an ideal Class-F mode in microwave region can be achieved by using a load network shown in Fig. 3.25, where each open-circuit stub has a quarter wavelength at each higher-order harmonic of the fundamental frequency providing zero impedance at the higher harmonic at point $A$ [27]. The transmission line $TL_{11}$ having a quarter wavelength at the fundamental frequency transforms these zero impedances into open-circuit impedance at odd harmonics and short-circuit impedance at even harmonics seen from the device output. The quarter-wave transmission-line $TL_{12}$ is necessary for impedance matching at the fundamental frequency of the output impedance $Z_{\text{out}}$ with standard load $R_{\text{L}}$. To compensate for the reactive impedance at the fundamental frequency due to the open-circuit stubs

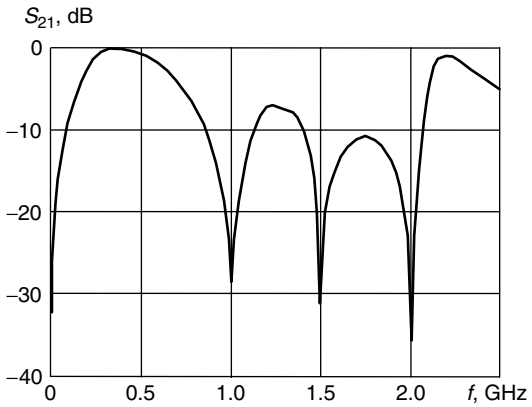



**Figure 3.24: Frequency response of microstrip impedance-peaking circuit.**

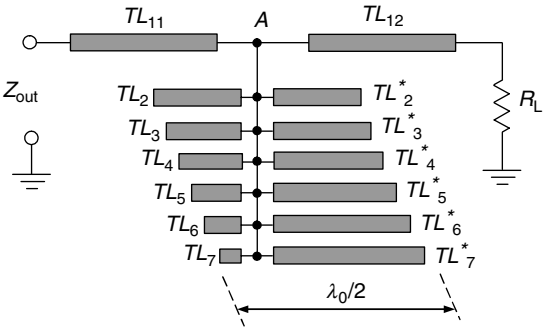



**Figure 3.25: Class-F load network with reactance compensation circuits.**

$TL_2, \ldots, TL_7$, the reactance compensation open-circuit stubs $TL_2^*, \ldots, TL_7^*$ are added in series to form an overall half wavelength for each stub. However, such a Class-F load network can be used effectively at low power levels when the device parasitic output capacitance $C_{\text{out}}$ is sufficiently small.

When the Class-F power amplifier is fabricated as a hybrid integrated circuit, the parasitic inductance from a bond wire exists at the drain port. The corresponding impedance-peaking circuit including the output series bond-wire inductance $L_{\text{out}}$ is shown in Fig. 3.26(*a*) [28]. In this case, the open-circuit condition at the drain for the third harmonic can be satisfied by modifying Eq. (3.105) as

$$\theta = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{\text{out}}} - \frac{3\omega_0 L_{\text{out}}}{Z_0}\right), \tag{3.107}$$

where $\theta$ is the electrical length of the series transmission line $TL_2$ (at the operating frequency $\omega_0$) with the characteristic impedance $Z_0$. However, the short-circuit condition for the second and higher-order even harmonics cannot be met and the performance of the Class-F power amplifier is adversely affected as the operating frequency increases. Therefore, the transistor drain voltage and current waveforms are not perfectly symmetrical and are characterized by significant transition times from a saturation region to a pinch-off region and vice versa, mainly due to the effect of the second harmonic having the certain phase shift provided by the series bond-wire inductance.

The more complicated impedance-peaking circuit to improve efficiency, including the output series parasitic inductance $L_{\text{out}}$, which can generally represent the bond-wire and package lead inductances, is shown in Fig. 3.26(*b*). Here, to create the second-harmonic short-circuited condition and third-harmonic peaking, it is convenient to use a combination of the open-circuit and short-circuit transmission-line stubs in the load network. The device output elements $L_{\text{out}}$ and $C_{\text{out}}$ must create a parallel resonance at the third harmonic of the fundamental frequency

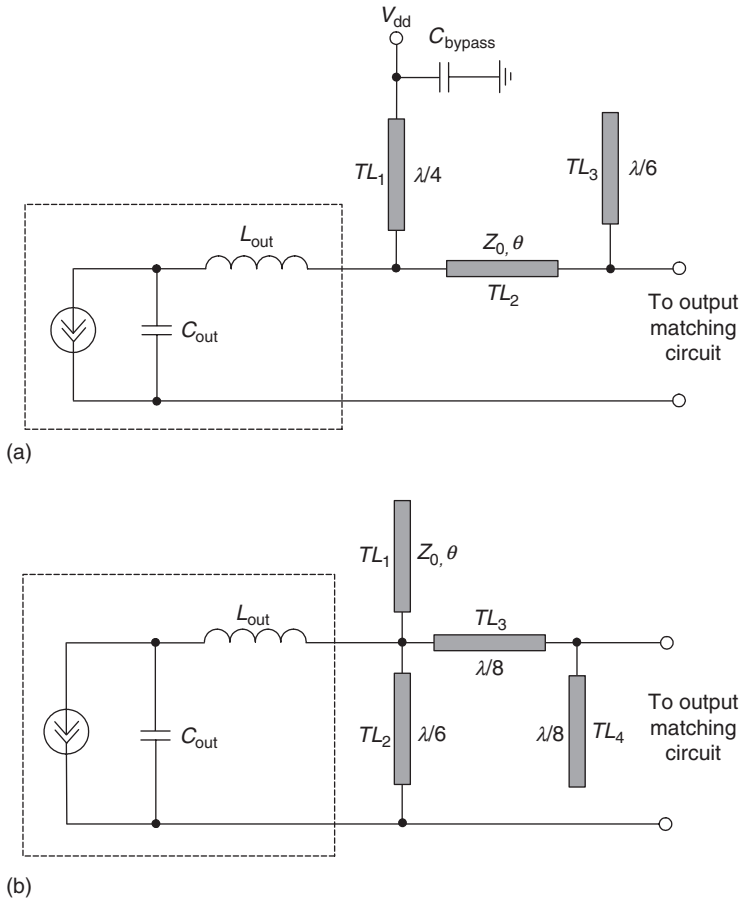



**Figure 3.26: Transmission-line impedance-peaking circuit including device bond-wire inductance.**

since the short-circuit stub $TL_2$ has a half wavelength at the third harmonic with short-circuited conditions at both its ends. It should be mentioned that the open-circuit stub having a quarter wavelength at the third harmonic of the fundamental frequency can be used instead of this short-circuit stub [29]. The electrical length $\theta$ of an open-circuit stub $TL_1$ is chosen to have less than a quarter wavelength at the second harmonic to realize an overall capacitive reactance together with the short-circuited transmission line $TL_2$ to be resonant with output inductance $L_{out}$ at the second harmonic of the fundamental frequency. The transmission lines $TL_3$ and $TL_4$ must be of quarter wavelengths at the second harmonic to provide the second harmonic high impedance condition at the input of $TL_3$. As a result, the ratios between the elements are as follows [26]:

$$L_{out} = \frac{1}{9\omega_0^2 C_{out}} \tag{3.108}$$

$$\theta = \frac{1}{2}\tan^{-1}\left(\frac{Z_0}{2\omega_0 L_{\text{out}}} - \frac{1}{\sqrt{3}}\right). \tag{3.109}$$

## 3.8 LDMOSFET Power-Amplifier Design Examples

The effectiveness of the Class-F circuit design technique can be demonstrated in the example of high-power LDMOSFET amplifiers. The small-signal equivalent circuit of the LDMOS device cell with gate length of 1.25 $\mu$m and gate width of 1.44 mm is shown in Fig. 3.27 [30]. The device model parameters were extracted from pulsed *I–V* and small-signal *S*-parameter measurements. The parameters of the small-signal equivalent circuit are given at a bias voltage for Class-AB bias conditions with a quiescent current $I_q = 15$ mA at a supply voltage $V_{dd} = 28$ V. The measured and modeled output voltage-ampere $I_{ds} - V_{ds}$ characteristics of the high power device with total gate width of $28 \times 1.44$ mm are shown in Fig. 3.28. Based on these characteristics, it is easy to choose the peak drain current, which allows us to maximize the drain efficiency by minimizing the saturation voltage. For example, choosing a peak current of 3.5 A results in a dc current of approximately $3.5/\pi \cong 1.1$ A according to Eqs. (3.21) and (3.23). In this case, a saturation voltage is about 4 V only. As a result, the maximum drain efficiency of about 80% providing a delivery of the output power of more than 20 W into the load can be achieved using a supply voltage of 24 V.

The equivalent circuit of the simulated 500 MHz single-stage lumped LDMOSFET power amplifier is shown in Fig. 3.29. In this particular case, the total gate width of a high-voltage LDMOSFET device is $7 \times 1.44$ mm. The drain efficiency and power gain of the amplifier versus input power $P_{in}$ for the case of ideal circuit inductors are given in Fig. 3.30(*a*). The obtained values of the drain efficiency more than 75% (curve 2) are due to a short-circuit condition at the second harmonic and open-circuit mode at the third harmonic. Also, an important issue is to provide high-impedance conditions at higher-order harmonics. This can be readily done by using an output matching circuit with the first series inductor. This shortens the switching time from pinch-off region to voltage-saturation region by better approximating the

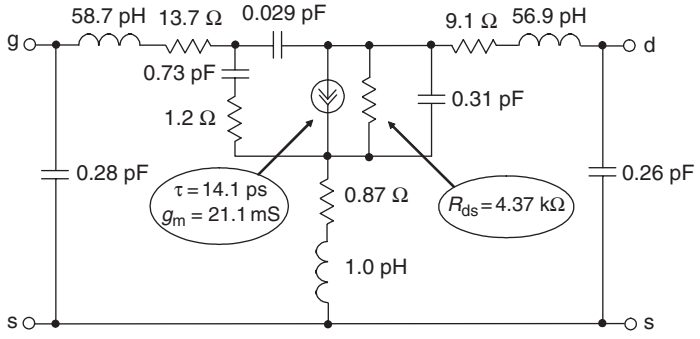



**Figure 3.27: Small-signal LDMOSFET equivalent circuit.**

idealized drain voltage square waveform (Fig. 3.31, solid line). It should be noted that the drain current waveform differs from a half-sinusoidal waveform because it includes higher-order odd harmonic components together with the current flowing through the device internal equivalent circuit capacitors (Fig. 3.31, dotted line).

As it follows from Eq. (3.32) for a symmetrical voltage waveform, the initial phases for the fundamental frequency and its harmonics should be equal, which is easy to realize by short-circuited and open-circuited conditions. However, according to Eq. (3.33) for a half-sinusoidal current waveform, the phases for any harmonic should differ from the phase for the fundamental frequency by 90°. This condition is easily realized in a Class-B load network where the fundamental component of the drain voltage is in phase with the fundamental

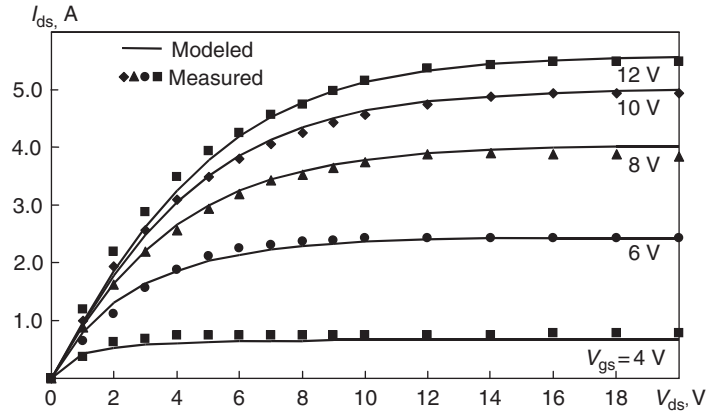



**Figure 3.28: Measured and modeled $I_{ds}-V_{ds}$ curves of high voltage LDMOSFET.**

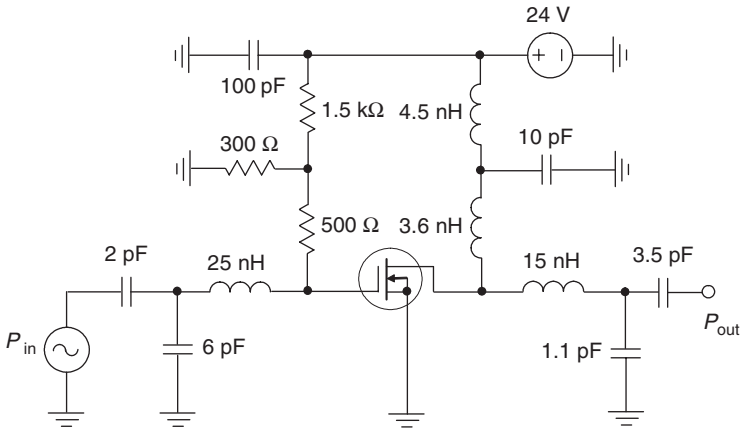



**Figure 3.29: Simulated lumped LDMOSFET Class-F power amplifier.**

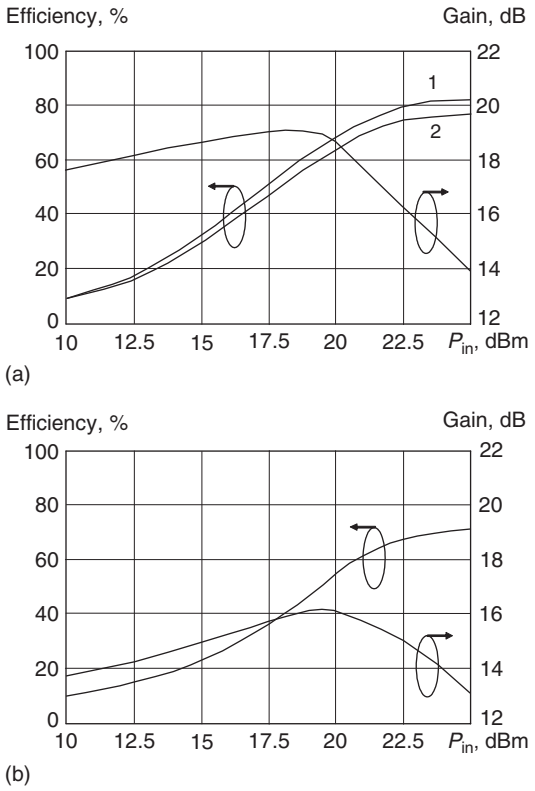



**Figure 3.30: Drain efficiency and power gain versus input power.**

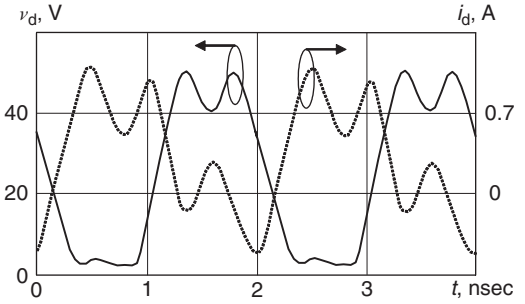



**Figure 3.31: Drain voltage and current waveforms.**

component of the drain current, but, for all higher-order current harmonics, the impedance of the resonant circuit will be capacitive since the drain current harmonics are mostly flowing through the shunt capacitor. Therefore, accurate harmonic phasing is very important to improve the effectiveness of a Class-F load network. The drain efficiency becomes higher than 80%, as shown in Fig. 3.30(*a*) by curve 1, if to ignore the effect of the device series drain resistance. However, the amplifier drain efficiency and power gain will be significantly

reduced when the values of the quality factor of load network inductors are sufficiently small. For example, the maximum value of the drain efficiency can be only 71% when an inductor quality factor at the fundamental frequency is $Q_{\text{ind}} = 30$, as shown in Fig. 3.30(*b*).

Therefore, at high power level, it is preferred to use load network circuits that employ microstrip lines. The equivalent circuit of a simulated 500 MHz single-stage microstrip LDMOSFET power amplifier using an active device with the same geometry is shown in Fig. 3.32. The input and output matching circuits represent a *T*-type matching circuit, and each consists of a series of microstrip line, a parallel open-circuit stub, and a series capacitor. To provide even harmonic termination and third harmonic peaking for a Class-F mode, an RF grounded quarter-wave microstrip line and a combination of the series microstrip line and open-circuit stub with electrical length of 30° at the fundamental frequency are used. Such an output-circuit configuration approximates the square drain voltage waveform with good accuracy (Fig. 3.33, solid line) and realizes a high drain efficiency of more than 75% with maximum output power $P_{\text{out}} = 8$ W, as shown in Fig. 3.34. The smaller value of the drain efficiency, in comparison with the theoretically achievable value, can be explained by the non-optimized impedances at higher harmonics since, unlike a lumped inductor, the transmission line exhibits an equidistant impedance performance in frequency domain with consecutive poles and zeros at the characteristic frequencies. This means that using a simple *T*-type transmission line transformer does not provide high impedance conditions at all higher-order harmonics simultaneously. Also, as seen from Fig. 3.33, the drain current waveform (dotted line) significantly differs from half-sinusoidal waveform because of the non-optimal magnitudes and phases of odd harmonic components at the device output.

It should be mentioned that, at frequencies close to the device transition frequency $f_{\text{T}}$, the drain (or collector) waveform becomes stretched due to a delay effect of the transistor input circuit with different and significant phase shifts $\omega\tau_{\text{in}} = \omega R_{\text{in}} C_{\text{in}}$ for higher-order harmonic

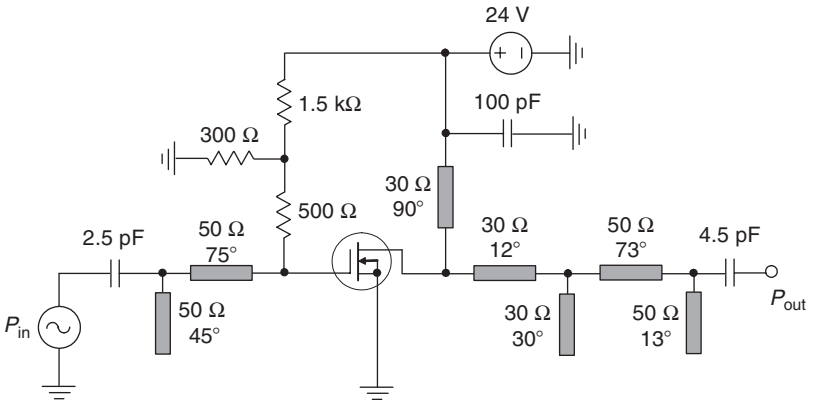



**Figure 3.32: Simulated microstrip LDMOSFET Class-F power amplifier.**

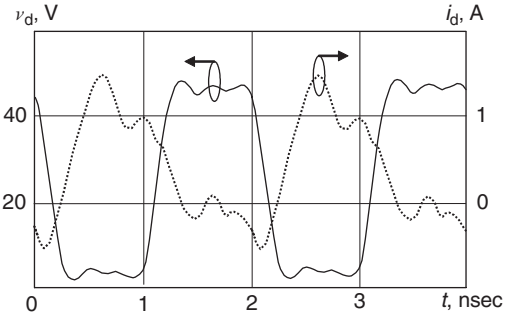



**Figure 3.33: Drain voltage and current waveforms.**

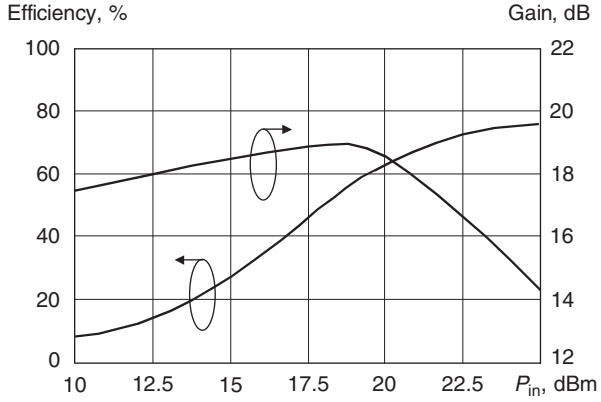



**Figure 3.34: Drain efficiency and power gain versus input power.**

components, where $R_{in}$ is the series input resistance (gate resistance for field-effect transistor or base resistance for bipolar transistor) and $C_{in}$ is the shunt input capacitance (gate-source capacitance for field-effect transistor or diffusion base-emitter capacitance for bipolar transistor). In this case, the concept of the low-frequency conduction angle is not valid anymore when the fundamental frequency and third harmonic component of the output voltage are out-of-phase only for conduction angles above $2\theta = 180°$. In other words, the low-frequency or external conduction angle considered at the input of the transistor is different from the high-frequency or internal conduction angle considered at the transistor junction directly due to a transient effect of the device input circuit. Thus, to achieve a 50% duty cycle of the collector voltage, the low-frequency conductance angles at the input may be significantly less than $2\theta = 180°$ [31]. In addition, it is necessary to introduce an additional phase shift at the third harmonic by tuning a third-harmonic tank circuit in the load network to make the collector-voltage waveform more symmetrical.

## 3.9 Practical RF and Microwave Class-F Power Amplifiers

A typical VHF high-efficiency bipolar power amplifier, which can provide output power of about 10 W with power-added efficiency of about 60% in a zero-bias Class-C operation, is shown in Fig. 3.35. Using a *T*-type output matching transformer with a series inductor creates high impedance conditions for the second and higher-order harmonic components at the collector terminal, thereby improving the collector efficiency. In this case, the collector current waveform is close to sinusoidal waveform, while the collector voltage waveform is characterized by a high value of its peak factor. To provide a reliable transistor operation when maximum collector voltage amplitude should be less than the collector-emitter breakdown voltage, it is necessary to reduce the collector supply voltage. Due to the small value of the transistor input impedance of about 1 Ω, the frequency bandwidth of such an amplifier is sufficiently narrow and does not exceed several percents at −3 dB output power level. The inductor $L_3$ is required to provide zero base-emitter biasing, while the inductor $L_1$ and bypass capacitor $C_b$ are necessary to isolate dc power supply from RF signal. Their values are sufficiently large to influence the amplifier matching conditions. Such an RF power amplifier in a slightly overdriven Class-B operation mode can provide 10 W output power with a power gain of 8 dB and a power-added efficiency close to 70% at an operating frequency of 250 MHz [15].

However, to improve the power-amplifier reliability by reducing a peak factor to a theoretical maximum value of 2, it is best to use an RF grounded quarter-wave transmission line instead of RF choke. This method realizes short-circuit conditions for even collector voltage harmonics, resulting in the square voltage and half-sinusoidal current waveform approximations typical for Class-F operation mode. To increase the impedance conditions for higher harmonic components, it is necessary to use the series high-*Q* resonant circuit tuned to the fundamental frequency and followed by the output matching circuit. The typical electrical schematic of such a high-efficiency Class-F VHF power amplifier is shown in Fig. 3.36. This design offers

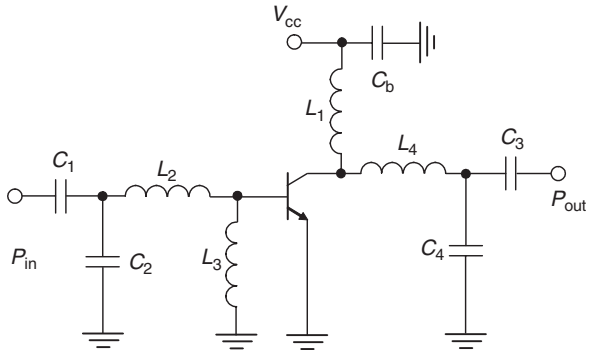



**Figure 3.35: Typical VHF high-efficiency bipolar power amplifier.**

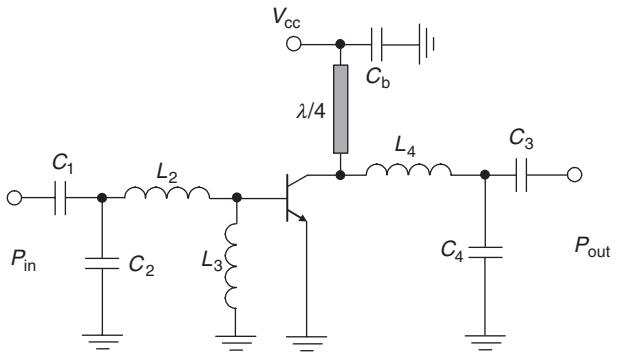



**Figure 3.36: High-efficiency Class-F VHF power amplifier with transmission line.**

the possibility that a collector efficiency approaching 90% for a 10 W hybrid power amplifier at 250 MHz can be achieved [30]. At higher frequencies when output-matching circuit is fabricated using the transmission line technology replacing a lumped inductor by a series microstrip line and a shunt capacitor by an open-circuit stub, its input impedance is optimized to realize high impedance condition at the third harmonic, taking into account also the active device parasitics [32].

The simplified circuit topology of a microstrip two-stage 900 MHz GaAs MESFET power amplifier is shown in Fig. 3.37(*a*) [33]. The microstrip line between MESFET and open-circuit stub with electrical length $\lambda_2/4$, where $\lambda_2$ is a second harmonic wavelength, is a compensation line for the equivalent device output reactance. The *T*-type impedance transformer, which consists of the series microstrip line, open-circuit microstrip stub, and series capacitor, provides an output impedance matching with load. The input and interstage matching circuits at fundamental frequency were designed using microstrip lines as well. As a result, with second harmonic control by a series microstrip line and microstrip open-circuit stub (included in dotted box), such a power amplifier demonstrates a drain efficiency of more than 80%, a power-added efficiency of 71%, and an output power of 2 W at a supply voltage of 6 V. Similar load network configuration of a single-stage 1.75 GHz MESFET power amplifier is shown in Fig. 3.37(*b*) [34, 35]. It consists of a short-circuited quarter-wave microstrip line $TL_2$, having high-impedance conditions at the fundamental and third-harmonic frequencies at its input, and an open-circuit stub $TL_4$ of a quarter wavelength at the third harmonic, having low impedance at the third-harmonic component at its input. To realize close to a square-wave voltage and half-sinusoidal current waveforms at the drain terminal, these short- and open-circuit conditions are transformed to the device output by the two series microstrip lines $TL_1$ and $TL_3$. This results in a drain efficiency of 75% and power gain of 11 dB at the output power of 24.5 dBm with a drain bias voltage of 3 V. To better optimize impedance at the second harmonic, an additional short-circuited quarter-wave line can be included further into the output matching circuit of the microwave power amplifier [36].

In monolithic integrated circuits design, the second harmonic short at the drain can be realized also by using a series resonant circuit connected to the ground, while the high impedance condition at the third harmonic is provided by a series spiral inductor being a part of the output matching circuit [37].

One of the most important factors for high-efficiency operation mode is the value of the device saturation resistance $r_{sat}$ (or on-resistance $r_{on}$), especially at low supply voltage. Here, $r_{sat}$ is the ratio of the drain-source voltage at saturated drain current to the saturated drain current. It is difficult to improve the efficiency of a small-scale MESFET with a narrow gate width when, in low voltage operation, the ratio $r_{sat}/R_{out}$ (where $R_{out}$ is the real part of the device output impedance) is not small enough. Realizing a high-efficiency operation mode of the power amplifier requires increasing this ratio as much as possible. For example, by decreasing $r_{sat}$ by half, the drain efficiency can be improved by about 10%. A MESFET, which has a saturation resistance $r_{sat}$ of about 1 Ω, can demonstrate a drain efficiency of 90% at a supply voltage of 6 V in a 900-MHz Class-F power amplifier [33].

By inputting a quasi-square voltage wave into the MESFET gate, the efficiency of the Class-F power amplifier can be increased. This quasi-square gate voltage contributes to the reduction of the voltage/current switching time at the drain and reduces power dissipation. Dissipation occurs when the drain voltage and current exist simultaneously. Fig. 3.38 shows a circuit schematic of a single-stage power amplifier with optimally terminated source and drain second-harmonic impedances $Z_{S2}$ and $Z_{L2}$, each of which is provided by a 50 Ω series microstrip line connected in series to a shunt capacitor [38]. The source and drain second-harmonic impedances $Z_{S2}$ and $Z_{L2}$ are optimized by varying the lengths of the quarter

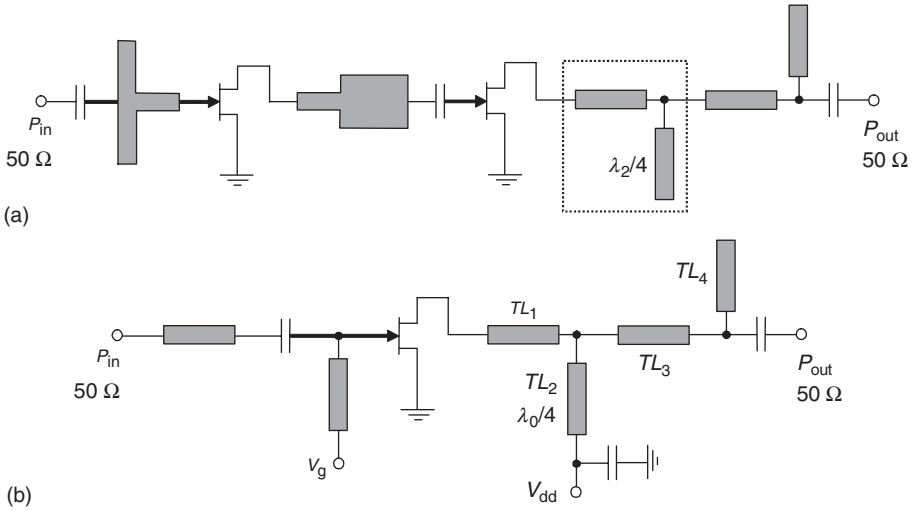



**Figure 3.37: Simplified schematic of microstrip Class-F power amplifier.**

wavelength shorted stubs to compensate for the device parasitics without affecting the values of the fundamental impedances. For example, the maximum efficiency is achieved at a phase of greater than 152° for $Z_{S2}$. Based on this approach, the power-added efficiency of 74% with output power of 31.4 dBm (1.4 W) at the operating frequency of 930 MHz and supply voltage of 3.5 V was obtained using a GaAs MESFET device of 12-mm gate width. In this case, applying the input second-harmonic control circuit improves the power-added efficiency by 5%.

The circuit schematic of a Class-F power amplifier implemented in a deep submicron 0.2 $\mu$m CMOS technology is shown in Fig. 3.39 [39]. Applying a Class-F operation mode has an advantage of substantially less drain voltage peak factor compared with a Class-E mode. This

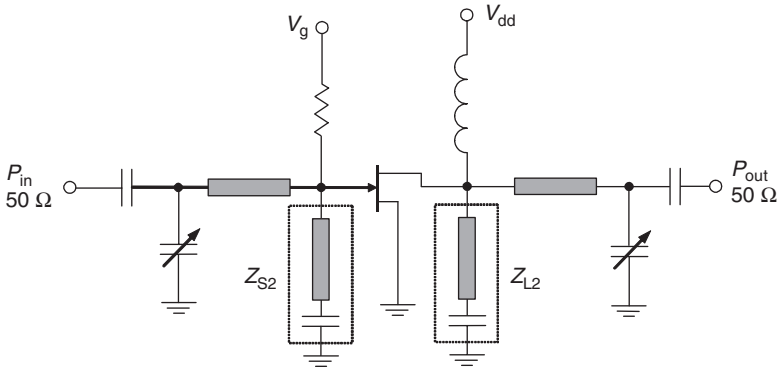



**Figure 3.38: Circuit diagram of Class-F power amplifier with optimally terminated source and drain second-harmonic impedances.**

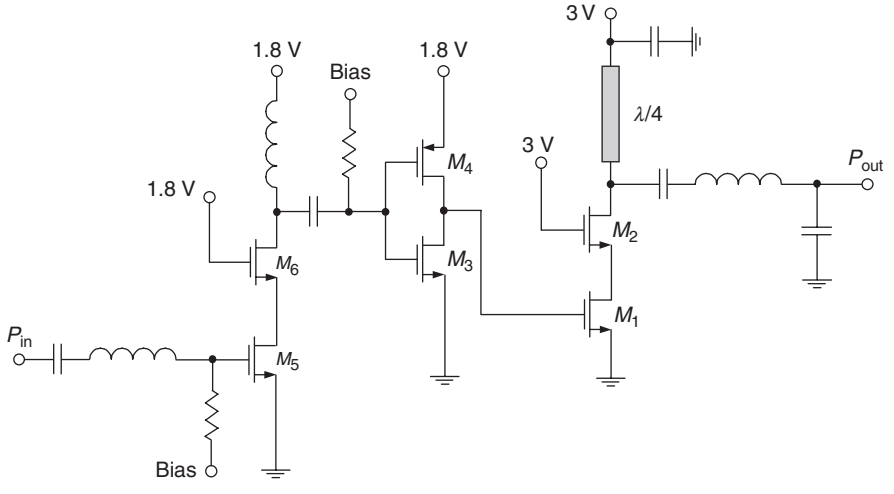



**Figure 3.39: Schematic of Class-F power amplifier with quater-wave transmission line.**

helps to overcome the problem of low oxide breakdown voltage, which limits the maximum output power and efficiency of the CMOS power amplifier because of lower supply voltage required for the device protection. The Class-F operation mode is achieved by using an external quarter-wave transmission line together with a series on-chip resonant circuit in the load network having high impedance at the second and higher harmonics. In cascode configuration of the final stage, the thin gate device $M_1$ is protected by a thick oxide (80 Å) device $M_2$ with no threat to oxide breakdown under supply voltage of 3 V. The driver stage based on a complementary nMOS and pMOS pair eliminates the problem of negative voltage swing across the gate of the cascode device $M_1$, which is normally the case for a single-ended nMOS device, and provides the driving signal waveform closer to a square wave. Being operated at 900 MHz, such a CMOS Class-F power amplifier can deliver a maximum output power of 1.5 W with power-added efficiency of 43%.

Fig. 3.40 shows the simplified schematic of a parallel-amplifier architecture implemented in a 0.25 $\mu$m CMOS technology and intended to provide high efficiency at backoff output power levels [40]. This architecture employs three binary weighted Class-F power amplifiers, the output powers of which are combined in a power-combining network based on using the quarter-wave transmission lines loaded on the parallel resonant circuit tuned to the fundamental frequency. The capability to turn off completely each individual power amplifier without interfering with the operation of other individual power amplifiers is provided by the addition of pMOS shorting switches resulting in high impedance at the end of the

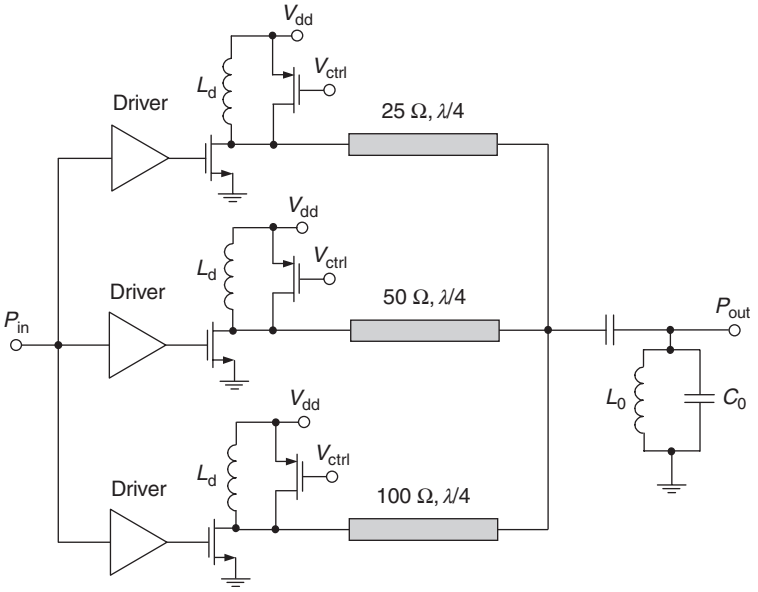



**Figure 3.40: Class-F parallel-power amplifier architecture.**

corresponding transmission line. The power-amplifier architecture operating at 1.4 GHz from 1.5 V power supply occupies an active die size of 0.43 $mm^2$ and achieves a power-added efficiency of 49% at maximum output power of 300 mW, while maintaining a power-added efficiency of greater than 43% over a lower output power range down to 100 mW. The transmission lines are implemented using the printed circuit board microstrip lines. On-chip transmission-line fabrication in CMOS technology by using *LC* ladders makes it significantly shorter. For example, the frequency response of 10 sections containing a series inductance and a shunt capacitance each can approximate that of the transmission line within 5% occupying the area of about 14 times shorter. In this case, it is enough to use a spiral inductor to implement both series inductance and shunt capacitance, which can be obtained with the bottom-plate parasitic capacitance of the spiral. However, the maximum power-added efficiency of the parallel on-chip power-amplifier architecture degrades by 10–15%.

An efficient Class-F operation mode can also be applied to a distributed power amplifier. Fig. 3.41 shows the simplified schematic of a modified Class-F single-ended dual-fed distributed MESFET power amplifier with device spacing of 180° at the center frequency for optimum operation [41]. The two-port output Class-F load network simultaneously provides

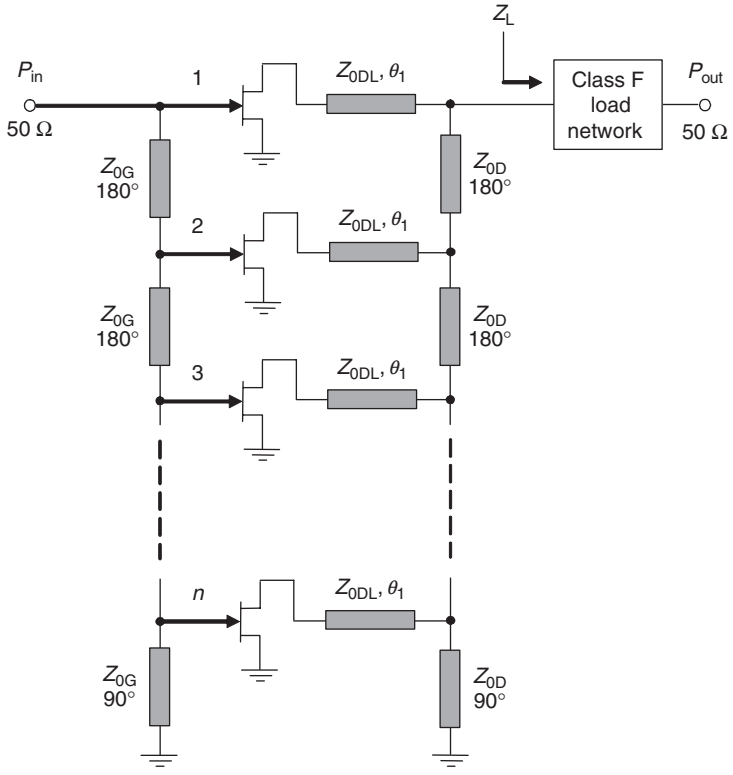



**Figure 3.41: Simplified schematic of microstrip Class-F distributed amplifier.**

impedance matching at the fundamental frequency, high impedance at the third and fifth harmonics, and low impedance at even harmonics. Namely, $Z_L$ is equal to $Z_{0D}$ at the fundamental but infinite at the third and fifth harmonics. The open-circuit and short-circuit terminations of the output line are applied directly to the drain of each device through the half-wave transmission lines. For an idealized Class-F optimum MESFET operation, the impedance $Z_L(\omega_0)$ seen from its drain at the fundamental frequency considering both forward and reverse traveling waves can be obtained by

$$Z_L(\omega_0) = Z_{0D} = \frac{8}{n\pi^2}\frac{V_{dd}}{I_0}, \tag{3.110}$$

where $V_{dd}$ is the drain-bias voltage, $I_0$ is the total dc current, and $n$ is the number of MESFETs. To compensate for the device parasitics, an extra transmission line is cascaded with each device drain port. The characteristic impedance $Z_{0DL}$ and electrical length $\theta_1$ of this transmission line are

$$Z_{0DL} = \sqrt{\frac{L_d}{C_{ds}}} \tag{3.111}$$

$$\theta_1 = \pi - \omega_0\sqrt{L_d C_{ds}}, \tag{3.112}$$

where $\omega_0$ is the fundamental angular frequency, $L_d$ is the series drain inductance, and $C_{ds}$ is the shunt drain-source capacitance. The combination of $L_d$ and $C_{ds}$ forming a simple low-pass filter and the extra transmission line will behave as a half-wave transmission-line transformer if $\omega\sqrt{L_d C_{ds}}$ is less than $36^\circ$ or one-tenth wavelength at least up to the third harmonic. Being fabricated using hybrid technology and employing Fujitsu FLK012WF devices, such a 2-FET ($n = 2$) Class-F distributed power amplifier enables us to achieve a drain efficiency of 71% at output power of 22 dBm at operating frequency of 1.75 GHz.

Modern wireless communication systems require feeding the signal with a non-constant envelope through the power amplifier. In this case, there is a trade-off between power-amplifier efficiency and linearity with improvement in one coming at the expense of the other. In a classical analog envelope elimination and restoration (EER) Kahn approach where special devices are required to separate amplitude (envelope) and RF phase-modulated signals, one type of power amplifier is responsible for envelope signal amplification, while another type of power amplifier is fed by a constant-envelope RF signal, as shown in Fig. 3.42. The constant-envelope RF signal can be amplified efficiently by a nonlinear power amplifier (PA) using Class-F operation mode. For example, at the operating frequency of 8.4 GHz, a Class-F power amplifier can provide the maximum instantaneous efficiency of 55% with output power of 610 mW using a Fujitsu FLK052WG MESFET device [42]. Amplitude modulation of the final stage of the power amplifier based on a Class-S modulator restores the envelope to the

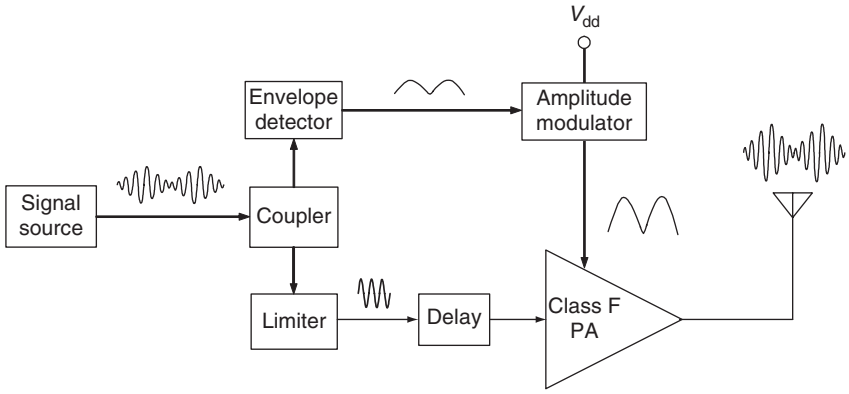



**Figure 3.42: Block diagrams of Kahn EER transmitter with Class-F power amplifier.**

phase-modulated carrier signal creating an amplitude replica of the input signal [13]. In contrast to linear power amplifiers, a Kahn EER transmitter operates with high efficiency over a wide dynamic range of back-off output power levels and, therefore, produces an average efficiency that is typically three to five times higher. To minimize misalignment between phase and amplitude, the delay line is required. In modern radio transmitters intended for wireless applications, both the envelope and phase-modulated signals can be easily generated separately using a digital signal processing (DSP) technique [30]. The average efficiency of 26.4% for a multi-carrier signal and 43.8% for a quadrature-amplitude modulation with better linearity can be achieved in *X*-band Class-F power amplifiers using the Kahn technique compared with 9.5% and 28.7% for a linear power-amplifier mode, respectively [42]. Average efficiency can even be increased by applying a modified Kahn technique using additional drive modulation when dynamic RF input amplitude varies proportionally to the signal envelope.

## References

[1] J. Zenneck and H. Rukop, *Lehrbuch der Drahtlosen Telegraphie*, Stuttgart: Ferdinand Enke, 1925.

[2] I. N. Fomichev, ''A New Method to Increase Efficiency of the Radio Broadcasting Station (in Russian),'' *Elektrosvyaz*, pp. 58–66, June 1938.

[3] R. I. Sarbacher, ''Power-Tube Performance in Class C Amplifiers and Frequency Multipliers as Influenced by Harmonic Voltage,'' *Proc. IRE*, vol. 31, pp. 607–625, November 1943.

[4] G. T. Royden, ''High-Frequency Amplifier,'' U.S. Patent 2,498,711, February 1950.

[5] H. J. Round, ''Wireless Telegraph and Telephone Transmission,'' U.S. Patent 1,564,627, December 1925.

[6] Z. I. Model, B. I. Ivanov, S. V. Person, and G. F. Soloviev, ''Increasing of the Efficiency of a High Power HF Vacuum-Tube Oscillator by Separating the Third Harmonic (in Russian),'' *Radiotekhnika,* vol. 2, pp. 15–23, April 1947.

[7] V. J. Tyler, ''A New High-Efficiency High-Power Amplifier,'' *Marconi Review*, vol. 21, pp. 96–109, Fall 1958.

[8] J. C. Shelleng, ''Amplifying System,'' U.S. Patent 1,484,967, February 1924.

[9] N. S. Fuzik, ''Biharmonic Modes of a Tuned RF Power Amplifier,'' *Telecommunications and Radio Engineering,* Part 2, vol. 25, pp. 117–124, July 1970.

[10] Z. Zivkovic and A. Marcovic, ''Third Harmonic Injection Increasing the Efficiency of High-Power HF Amplifiers,'' *IEEE Trans. Broadcasting*, vol. BC-31, pp. 34–39, June 1985.

[11] A. N. Rudyakova and V. G. Krizhanovski, ''Driving Waveforms for Class-F Power Amplifiers,'' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 473–476.

[12] P. M. White, ''Effect of Input Harmonic Terminations on High Efficiency Class-B and Class-F Operation of PHEMT Devices,'' *1998 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1611–1614.

[13] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons, 1980.

[14] F. H. Raab, ''An Introduction to Class-F Power Amplifiers,'' *RF Design*, vol. 19, pp. 79–84, May 1996, p. 14, July 1996.

[15] D. M. Snider, ''A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier,'' *IEEE Trans. Electron Devices*, vol. ED-14, pp. 851–857, December 1967.

[16] F. H. Raab, ''Class-F Power Amplifiers with Maximally Flat Waveforms,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-45, pp. 2007–2012, November 1997.

[17] F. H. Raab, ''Maximum Efficiency and Output of Class-F Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1162–1166, June 2001.

[18] F. H. Raab, ''Class-F Power Amplifiers with Reduced Conduction Angles,'' *IEEE Trans. Broadcasting*, vol. BC-44, pp. 455–459, December 1998.

[19] F. H. Raab, ''FET Power Amplifier Boosts Transmitter Efficiency,'' *Electronics*, vol. 49, pp. 122–126, June 1976.

[20] V. A. Borisov and V. V. Voronovich, ''Analysis of Switched-Mode Transistor Amplifier with Parallel Forming Transmission Line (in Russian),'' *Radiotekhnika i Elektronika*, vol. 31, pp. 1590–1597, August 1986.

[21] N. S. Fuzik, E. A. Sadykov, and V. I. Serguchev, ''Electrical Design of the Oscillatory Circuits of the Final Stage of a Radio Transmitter Operating in a Biharmonic Mode,'' *Telecommunications and Radio Engineering,* Part 2, vol. 25, pp. 141–145, January 1970.

[22] V. V. Voronovich and V. P. Galakh, ''Investigation of a Polyharmonic Bipolar Transistor Oscillator by Monoharmonic Excitation,'' *Journal of Communication Technology and Electronics*, vol. 42, pp. 102–108, January 1997.

[23] C. Trask, ''Class-F Amplifier Loading Networks: A Unified Design Approach,'' *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 351–354.

[24] W. S. Kopp and S. D. Pritchett, ''High Efficiency Power Amplification for Microwave and Millimeter Frequencies,'' *1989 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 857–858.

[25] A. V. Grebennikov, ''Effective Circuit Design Techniques to Increase MOSFET Power Amplifier Efficiency,'' *Microwave J.*, vol. 43, pp. 64–72, July 2000.

[26] A. V. Grebennikov, ''Circuit Design Technique for High Efficiency Class F Amplifiers,'' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 771–774.

[27] K. Honjo, ''A Simple Circuit Synthesis Method for Microwave Class-F Ultra-High-Efficiency Amplifiers with Reactance-Compensation Circuits,'' *Solid-State Electronics*, vol. 44, pp. 1477–1482, August 2000.

[28] S. Ko, W. Wu, J. Lin, S. Jang, F. Ren, S. Pearton, R. Fitch, and J. Gillespie, ''A High Efficiency Class-F Power Amplifier Using AlGaN/GaN HEMT,'' *Microwave and Optical Technology Lett.*, vol. 48, pp. 1955–1957, October 2006.

[29] J. E. Mitzlaff, ''High Efficiency RF Power Amplifier,'' U.S. Patent 4,717,884, January 1988.

[30] A. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[31] A. N. Rudiakova, ''BJT Class-F Power Amplifier Near Transition Frequency,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-53, pp. 3045–3050, September 2005.

[32] S. F. Ooi, S. Gao, A. Sambell, D. Smith, and P. Butterworth, ''A High Efficiency Class-F Power Amplifier Design Technology,'' *Microwave J.*, vol. 47, pp. 110–122, November 2004.

[33] K. Chiba and N. Kanmuri, ''GaAs FET Power Amplifier Module with High Efficiency,'' *Electronics Lett.*, vol. 19, pp. 1025–1026, November 1983.

[34] C. Duvanaud, S. Dietsche, G. Pataut, and J. Obregon, ''High-Efficient Class F GaAs FET Amplifiers Operating with Very Low Bias Voltages for Use in Mobile Telephones at 1.75 GHz,'' *IEEE Microwave and Guided Wave Lett.*, vol. 3, pp. 268–270, August 1993.

[35] S. Dietsche, C. Duvanaud, G. Pataut, and J. Obregon, ''Design of High Power-Added Efficiency FET Amplifiers Operating with Very Low Drain Bias Voltages for Use in Mobile Telephones at 1.7 GHz,'' *Proc. 23rd Europ. Microwave Conf.*, pp. 252–254, 1993.

[36] R. D. Boesch and J. A. Thompson, ''*X*-Band 0.5, 1, and 2 Watt Power Amplifiers with Marked Improvement in Power-Added Efficiency,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-38, pp. 707–711, June 1990.

[37] M. Maeda, M. Nishijima, H. Takehara, C. Adachi, H. Fujimoto, and O. Ishikawa, ''A 3.5 V, 1.3 W GaAs Power Multi-Chip IC for Cellular Phones,'' *IEEE J. Solid-State Circuits*, vol. SC-29, pp. 1250–1256, October 1994.

[38] M. Maeda, H. Masato, H. Takehara, M. Nakamura, S. Morimoto, H. Fujimoto, Y. Ota, and O. Ishikawa, ''Source Second-Harmonic Control for High Efficiency Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-43, pp. 2952–2958, December 1995.

[39] T. C. Kuo and B. B. Lusignan, ''A 1.5-W Class-F RF Power Amplifier in 0.2-$\mu$m CMOS Technology,'' *2001 IEEE Int. Solid-State Circuits Conf. Dig.*, pp. 154–155.

[40] A. Shirvani, D. K. Su, and B. Wolley, ''A CMOS RF Power Amplifier with Parallel Amplification for Efficient Power Control,'' *IEEE J. Solid-State Circuits*, vol. SC-37, pp. 684–693, June 2002.

[41] K. W. Eccleston, ''Modified Class-F Distributed Amplifier,'' *IEEE Microwave and Wireless Components Lett.*, vol. 14, pp. 461–483, October 2004.

[42] M. D. Weiss, F. H. Raab, and Z. Popovic, ''Linearity of *X*-Band Class-F Power Amplifiers in High-Efficiency Transmitters,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1174–1179, June 2001.

This page intentionally left blank

CHAPTER 4

# Inverse Class F

Highly efficient operation of the power amplifier can also be obtained by applying biharmonic or polyharmonic modes when an additional single-resonant or multi-resonant circuit tuned to the even harmonics of the fundamental frequency is added into the load network. An infinite number of even-harmonic resonators results in an idealized inverse Class-F mode with a half-sinusoidal voltage waveform and a square current waveform at the device output terminal. In inverse Class-F power amplifiers analyzed in frequency domain, the fundamental and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking to control the voltage and current waveforms at the device output to obtain maximum efficiency. In this chapter, different inverse Class-F techniques using lumped and transmission-line elements including a quarter-wave transmission line are analyzed. Design examples and practical RF and microwave inverse Class-F power amplifiers are described and discussed.

## 4.1 Biharmonic Operation Mode

Biharmonic operation mode can be realized using a second harmonic peaking when an additional parallel resonant circuit tuned to the second harmonic of the fundamental frequency is included in series into the load network. Similarly to the load network with the third harmonic peaking, the additional resonator creates a high impedance at the second harmonic resulting in an efficiency improvement. In this case, by limiting to a biharmonic operation condition, the partial Fourier series of current $i(t)$ and voltage $v(t)$ in normalized form can be respectively written as

$$\frac{v(\omega t)}{V_0} = 1 - \frac{\pi}{2}\sin\omega t - \frac{2}{3}\cos 2\omega t \tag{4.1}$$

$$\frac{i(\omega t)}{I_0} = 1 + \frac{4}{\pi}\sin\omega t + \frac{4}{3\pi}\sin 3\omega t, \tag{4.2}$$

where $V_0$ and $I_0$ are the dc voltage and current components, respectively. Note that an infinite number of voltage and current harmonics presented in a Fourier series results in the ideal half-sinusoidal voltage and square current waveforms.

Fig. 4.1 shows that the shapes of the voltage and current waveforms can be significantly transformed with increased voltage peak factor by adding even one additional harmonic being properly phased. For example, the combination of the fundamental and third harmonics being out of phase results in a flattened current waveform with depression in its center shown in Fig. 4.1(*a*), which can be minimized by using the proper ratio between the amplitudes of the fundamental and third harmonics. Similarly, the combination of the fundamental and second harmonics being in phase sharpens the voltage waveform corresponding to minimum values of the voltage waveform, as shown in Fig. 4.1(*b*). The optimum ratio between the amplitudes of the fundamental and second current harmonics can maximize the current waveform in one-half of the period and minimize the current waveform during the other half of the period determined by the device saturation resistance in a practical circuit. This means that the power loss due to the active device can be minimized since the results of the integration over the period when minimum current corresponds to maximum voltage will give small value compared with the power delivered to the load.

The effect of the inclusion of the parallel-resonant circuit tuned to the second harmonic and located in series at the anode, as shown in Fig. 4.2(*a*), was described and analyzed in [1, 2].

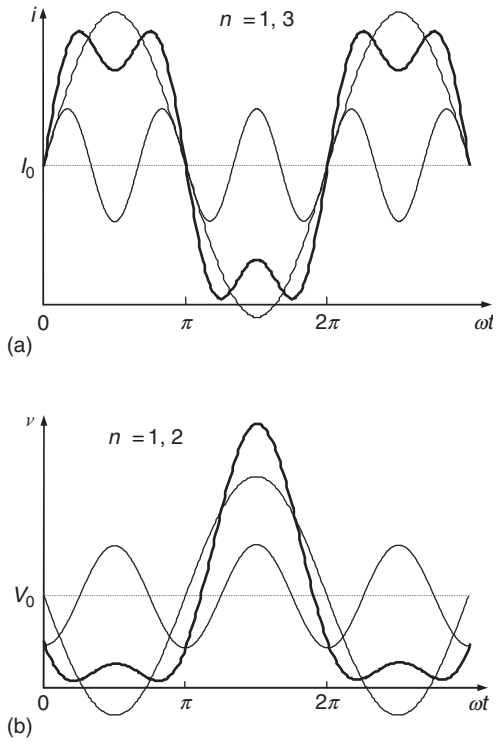



**Figure 4.1: Fourier current and voltage waveforms with third and second harmonics.**

It was shown that the symmetrical anode current waveform and level of its depression can be provided with the opposite phase conditions between the fundamental-frequency and second harmonic components and an optimum value of the ratio between their voltage amplitudes. It was noted that high operation efficiency can be achieved even when impedance of the parallel circuit to second harmonic is equal to or slightly greater than impedance of the tank circuit to fundamental frequency. In practical vacuum-tube power amplifiers intended for operation at very high frequencies, the peak output power and anode efficiency can be increased by 1.15–1.2 times [3]. In addition, such an approach can improve the modulation properties of the power amplifier when the phase of the second voltage harmonic becomes negative compared to that of the fundamental frequency [1]. It was suggested to use an additional resonator tuned to the fourth harmonic in a series with the second-harmonic resonator, as shown in Fig. 4.2(*b*), to maximize efficiency of the vacuum-tube amplifier with square voltage driving waveform [4]. However, generally, in view of the parasitic capacitance realized between anode and cathode, the entire anode circuit should be tuned to the second harmonic, not only a single resonator.

The efficiency improvement can be significant in a Class-C power amplifier even by using a single fourth harmonic resonator in anode circuit. In this case, the grid driving voltage can represent a simple sinusoidal waveform, since the current coefficients for the fundamental frequency component and fourth harmonic have opposite signs providing their out-of-phase voltage conditions at the anode. For an idealized active device which output is represented by the voltage-controlled current source only, the flattening of the anode voltage waveform can take place when the biharmonic signal including the fundamental and fourth harmonic at the anode can be written as

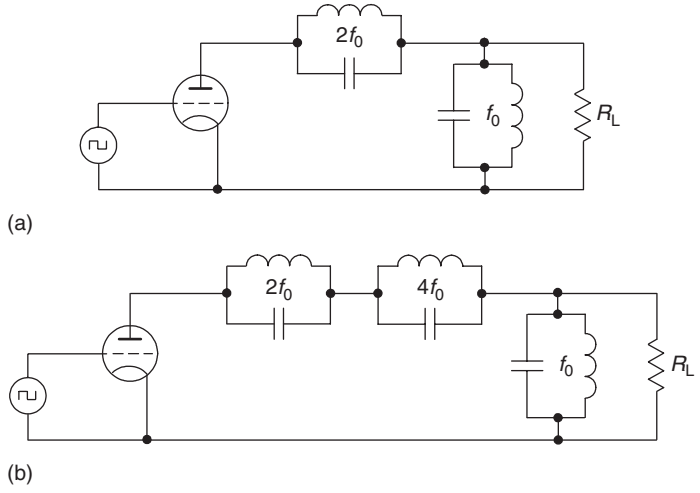



**Figure 4.2: Biharmonic and polyharmonic power amplifiers.**

$$v = V_a - V_{a1}\cos\omega t + V_{a4}\cos 4\omega t, \tag{4.3}$$

where $V_a$ is the anode dc voltage, $V_{a1}$ is the fundamental-component amplitude, and $V_{a4}$ is the fourth-harmonic amplitude. For a piecewise-linear approximation of the active device transfer voltage-current characteristic, the anode current will represent a sequence of pulses whose duration is defined by a conduction angle $2\theta$ determined by the grid dc-bias conditions. The opposite signs of the voltage amplitudes $V_{a1}$ and $V_{a4}$ cause the anode-voltage waveform to be bottom flattened, thus reducing the power losses during the time interval when anode current is high. Fig. 4.3 shows simplified schematics of both single-ended and push-pull biharmonic vacuum-tube high-power amplifiers, each having an additional harmonic resonator tuned to the fourth harmonic [5].

The ratio of the fundamental and fourth-harmonic amplitudes expressed through the anode-current coefficients $\gamma_1(\theta)$ and $\gamma_4(\theta)$ is defined by

$$\frac{V_{a1}}{V_{a4}} = \frac{I_{a1}}{I_{a4}}\frac{R_L}{R_{L4}} = \frac{\gamma_1(\theta)}{\gamma_4(\theta)}\frac{R_L}{R_{L4}}, \tag{4.4}$$

where $I_{a1}$ is the amplitude of the fundamental current, $I_{a4}$ is the amplitude of the fourth-harmonic current, $R_{L4}$ is the load resistance for the fourth-harmonic current due to a finite value of the quality factor of the fourth-harmonic resonator,

$$\gamma_1(\theta) = \frac{1}{\pi}\left(\theta - \frac{\sin 2\theta}{2}\right) \tag{4.5}$$

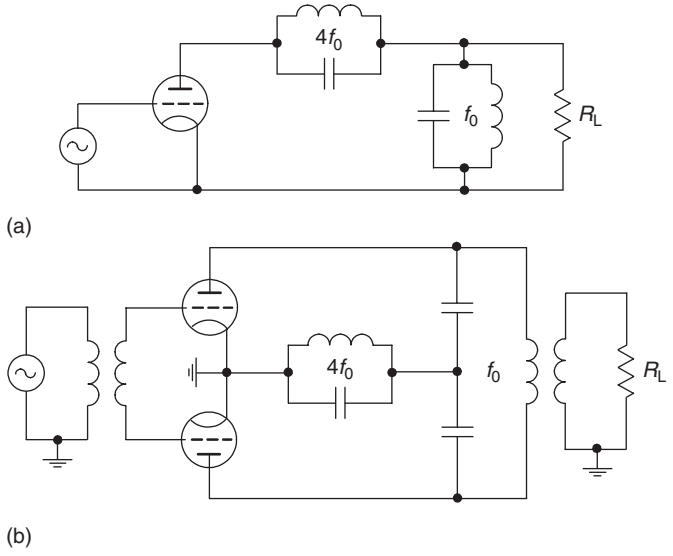



**Figure 4.3: Single-ended and push-pull power amplifiers with fourth-harmonic peaking.**

$$\gamma_4(\theta) = \frac{\sin 4\theta \cos\theta - 4\cos 4\theta \sin\theta}{30\pi} = -\frac{2}{15\pi}\sin\theta\left(6\cos^4\theta - 7\cos^2\theta + 1\right). \tag{4.6}$$

From Eqs. (4.5) and (4.6), it can be seen that the signs of the fundamental current coefficient $\gamma_1(\theta)$ and that of the fourth-harmonic current coefficient $\gamma_4(\theta)$ are opposite when

$$\cos^{-1}\frac{1}{\sqrt{6}} < \theta < \pi - \cos^{-1}\frac{1}{\sqrt{6}} \tag{4.7}$$

i.e., when $\theta$ is between 65.9° and 114.1°, thus satisfying the required relationship between $V_{a1}$ and $V_{a4}$ in Eq. (4.3). This means that the bottom flattening of the anode-voltage waveform can be achieved in Class-B or Class-C power amplifiers with a sinusoidal driving signal. Fig. 4.4(*a*) shows the anode voltage waveform when the amplitude of the fourth harmonic is one-eighth of the amplitude of the fundamental component, while the anode pulsed current waveform corresponding to a Class-C operation mode is shown in Fig. 4.4(*b*). The higher efficiency can be achieved in a deep Class-C mode when $\theta$ is significantly smaller than 90°, since the bottom flattening of the voltage waveform occurs during the time interval shorter than half a period.

To further increase efficiency of the biharmonic power amplifier, it is advisable to provide a biharmonic driving signal consisting of the fundamental frequency and its second harmonic

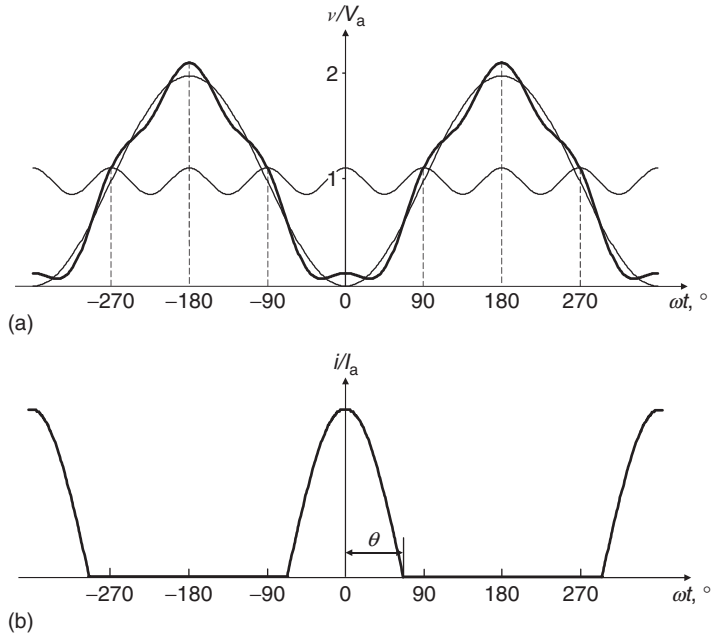



**Figure 4.4: Voltage and current waveforms of fourth harmonic power amplifier.**

component [6, 7]. In this case, the fundamental and second harmonic components must be out of phase at their maximum amplitudes, and the amplitude of the second harmonic is preferably chosen to have approximately three-eighths the amplitude of the fundamental. Fig. 4.5 shows a simplified circuit of a vacuum-tube power amplifier containing the fundamental tank and second harmonic resonant circuits both in grid and anode circuits. From Eq. (3.13) given in Chapter 3 it follows that, for optimum values $\theta_{\text{opt}} \approx 80^\circ$ and $a_{\text{n}}^0 \approx 0.41$, the anode efficiency in a biharmonic mode with second harmonic injection when $n = 2$ can be increased up to $\eta' = (0.950.96)\xi$ [6].

The simple solution to realize out-of-phase conditions between the voltage fundamental-frequency and second harmonic components at the device output is to use a second harmonic parallel resonator connected in series to the device input, as shown in Fig. 4.6 [1]. Such an approach gives a possibility to flatten the anode voltage waveform in active region avoiding the device saturation mode. In this case, the driver stage must operate in Class-B mode providing a half-sinusoidal output current waveform that includes the fundamental-frequency and even harmonic components only. The presence of the strong second harmonic component in the driver output current spectrum results in a second harmonic voltage drop across the resonator. The loaded quality factor of the second harmonic resonator must be high enough to neglect the voltage drop at the fundamental frequency. As a result, the second harmonic resonator has no effect on the voltage fundamental-frequency component, however it provides a phase shift of $180^\circ$ for the second harmonic component, since increasing in a voltage drop across the resonator results in decreasing of the voltage drop across the grid-cathode (base-emitter or gate-source) terminals.

Fig. 4.7(*a*) shows the combination of the fundamental-frequency component and second harmonic component shifted by $180^\circ$. In comparison with Fig. 4.1(*b*) where the fundamental-frequency and second harmonic components are in phase at maximum point of the

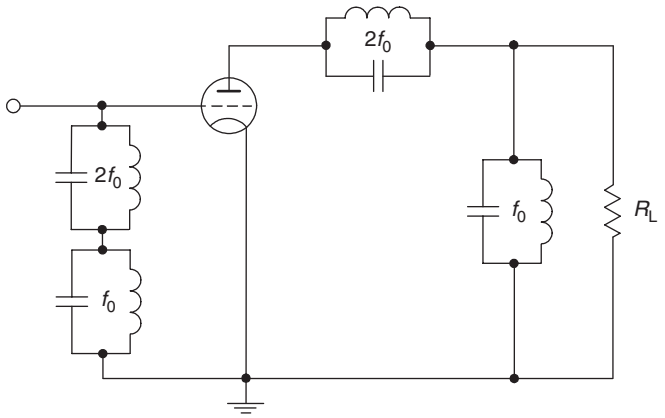



**Figure 4.5: Biharmonic power amplifier with input harmonic control.**

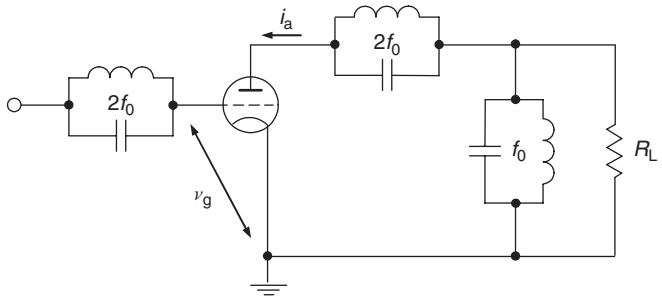



**Figure 4.6: Biharmonic power amplifier with input second harmonic resonator.**

fundamental-frequency component resulting in a waveform bottom flattening, this voltage waveform at the device input is characterized by its top flattening when the second harmonic has minimum value at maximum point of the fundamental-frequency component. Then, choosing the bias point $V_g$ equal to the device pinch-off voltage $V_p$, i.e., $V_g = V_p$, the selection of which corresponds to Class-B mode with the conduction angle of $180^\circ$ for monoharmonic operation, will result in the anode biharmonic current pulses with conduction angle $2\theta > 180^\circ$, as shown in Fig. 4.7(*b*). At the same time, using a second-harmonic resonator in the load network contributes to the anode voltage waveform, as shown Fig. 4.1(*b*).

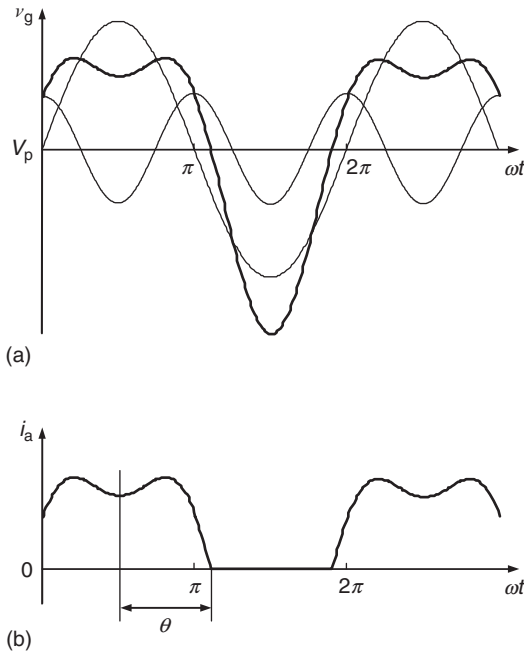



**Figure 4.7: Input and output voltage and current waveforms with second harmonic.**

Similar biharmonic approach to affect individually the fundamental frequency and second-harmonic conditions by using transmission-line technique can be applied to the two-stage transistor power amplifiers intended to operate at ultra-high and microwave frequencies. In this case, the proper amplitude and phase conditions for the fundamental-frequency and second harmonic components at the input of the final power stage separating from the driver stage output can be realized using the quarter-wave transmission lines in the form of the open-circuit and short-circuit stubs [8]. As a result, the drain efficiency of 77% can be achieved for a microstrip biharmonic GaAs MESFET power amplifier operated at the carrier frequency of 1.62 GHz with an output power of 27.9 dBm.

## 4.2 Idealized Inverse Class-F Mode

Generally, an infinite number of even-harmonic tank resonators can maintain a square current waveform, also providing a half-sinusoidal voltage waveform at the anode. Figs. 4.8(*a*) and (*b*) show such an inverse Class-F power amplifier with a multiple-resonator output filter to control the harmonic content of its collector (anode or drain) voltage and/or current waveforms, thereby shaping them to reduce dissipation and to increase efficiency.

The term ''inverse'' means that collector voltage and current waveforms are interchanged compared to a conventional case under the same idealized assumptions. Consequently, for a purely sinusoidal current flowing into the load shown in Fig. 4.9(*a*), the ideal collector current waveform is composed by a fundamental component and odd harmonics approximating a square waveform, as shown in Fig. 4.9(*b*). The collector voltage waveform is composed by the fundamental component and even harmonics approximating a half-sinusoidal waveform, as shown in Fig. 4.9(*c*). As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously similar to

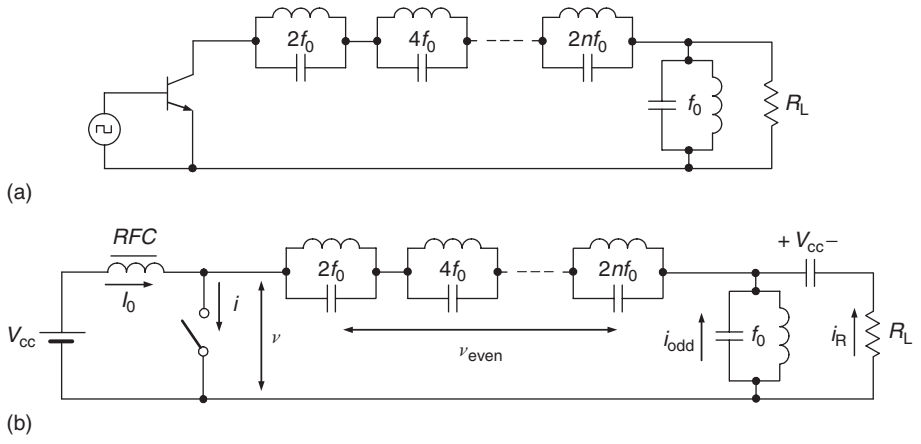



**Figure 4.8: Basic circuits of inverse Class-F power amplifier with parallel resonant circuits.**

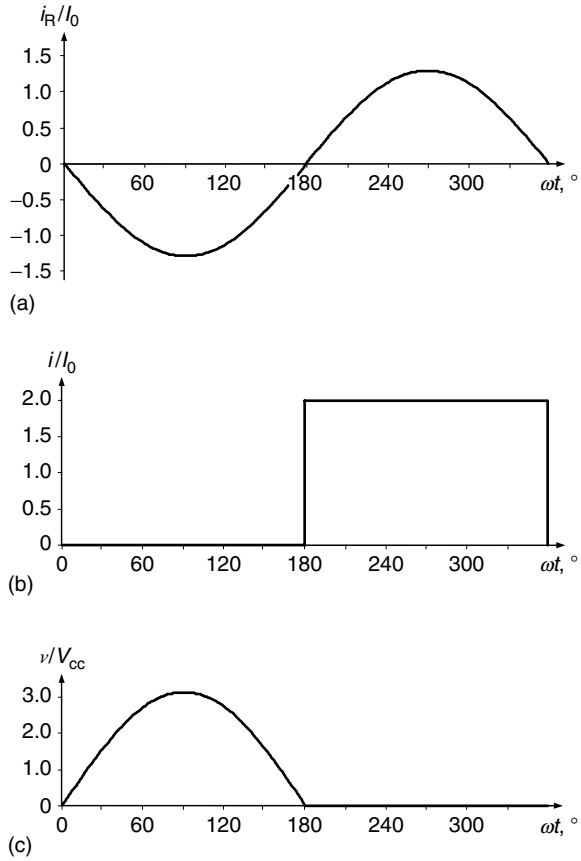



**Figure 4.9: Ideal waveforms of inverse Class-F power amplifier.**

a conventional Class-F mode. Such a condition, with symmetrical-collector voltage and current waveforms, corresponds to an idealized inverse Class-F operation mode with 100% collector efficiency.

By using Eqs. (3.18) and (3.22) given in Chapter 3 for a conventional Class-F mode, similar analysis of the distribution of voltages and currents in the inverse Class-F load network results in equations for the collector current and voltage waveforms as

$$i(\omega t) = 2I_0 - i(\omega t + \pi), \tag{4.8}$$

where $I_0$ is the dc current, and

$$v(\omega t) = V_R(\sin \omega t + |\sin \omega t|), \tag{4.9}$$

where $V_R$ is the fundamental-frequency amplitude. From Eq. (4.8) it follows that maximum value of the collector current cannot exceed a value of $2I_0$ and the time duration with maximum amplitude of $i = 2I_0$ coincides with the time duration with minimum amplitude of $i = 0$. Since the collector current is zero when switch is open, the only possible waveform for the collector current is a square wave composing of only dc, fundamental-frequency, and odd-harmonic components.

By using a Fourier analysis of the current and voltage waveforms, the following equations for the dc voltage, fundamental voltage and current components in the collector voltage and current waveforms can be obtained:

the fundamental current component can be calculated using Eq. (4.8) as

$$I_1 = I_R = \frac{1}{\pi}\int_{\pi}^{2\pi} 2I_0 \sin(\omega t + \pi) d\omega t = \frac{4I_0}{\pi}, \tag{4.10}$$

the dc voltage $V_{cc}$ can be calculated from Eq. (4.9) as

$$V_{cc} = \frac{1}{2\pi}\int_{0}^{\pi} 2V_R \sin \omega t \, d\omega t = \frac{2V_R}{\pi}, \tag{4.11}$$

the fundamental voltage component can be calculated from Eq. (4.9) as

$$V_1 = \frac{1}{\pi}\int_{0}^{\pi} 2V_R \sin^2 \omega t \, d\omega t = V_R. \tag{4.12}$$

Then, the ratio between the dc and output power at the fundamental frequency, $P_0$ and $P_1$, can be given by

$$P_1 = \frac{V_1 I_1}{2} = \frac{1}{2}\frac{\pi V_{cc}}{2}\frac{4I_0}{\pi} = P_0, \tag{4.13}$$

resulting in a theoretical collector efficiency with maximum value of 100%.

The impedance conditions seen by the device collector for an idealized inverse Class-F mode must be equal to

$$Z_1 = R_1 = \frac{\pi^2}{8}\frac{V_{cc}}{I_0} \tag{4.14}$$

$$Z_{2n+1} = 0 \quad \text{for odd harmonics} \tag{4.15}$$

$$Z_{2n} = \infty \quad \text{for even harmonics.} \tag{4.16}$$

## 4.3 Inverse Class F with Quarter-wave Transmission Line

An idealized inverse Class-F operation mode can also be represented by using a sequence of the series resonant circuits tuned to the fundamental and odd harmonics, as shown in Fig. 4.10(*a*). In this case, it is assumed that each resonant circuit has zero impedance at the corresponding fundamental frequency $f_0$ and its odd harmonic components $(2n + 1)f_0$ and infinite impedance at even harmonics realizing the idealized inverse Class-F square current and half-sinusoidal voltage waveforms at the device output terminal. As a result, the active device which is driven to operate as a switch sees the load resistance $R_L$ at the fundamental frequency, while the odd harmonics are shorted by the series resonant circuits.

An infinite set of the series resonant circuits tuned to the odd harmonics can be effectively replaced by a quarter-wave transmission line with the same operating capability. Such a circuit representation of an inverse Class-F power amplifier with a series quarter-wave transmission line loaded by the series resonant circuit tuned to the fundamental is shown in Fig. 4.10(*b*) [9, 10]. The series-tuned output circuit presents to the transmission line a load resistance at the frequency of operation. At the same time, the quarter-wave transmission line transforms the load impedance according to

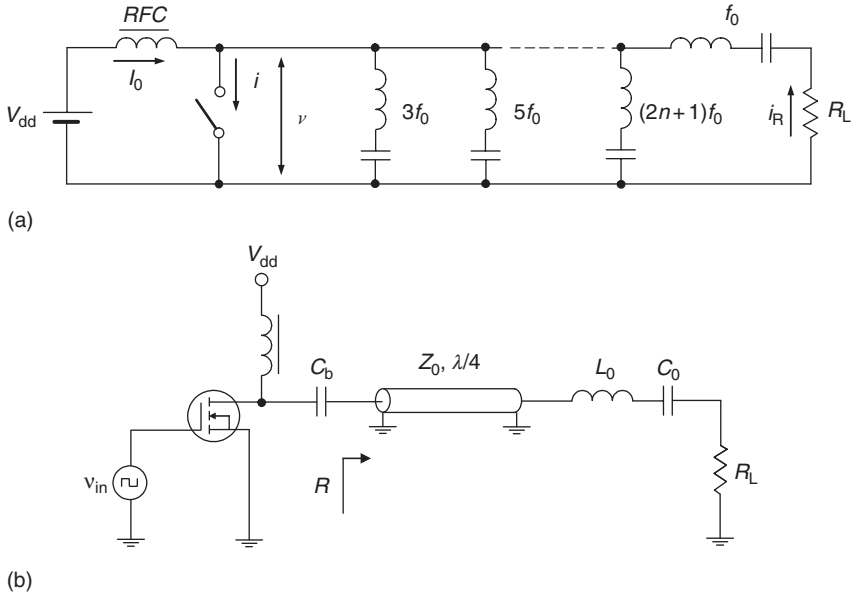



**Figure 4.10: Inverse Class-F power amplifier with series quater-wave transmission line.**

$$R = \frac{Z_0^2}{R_L}, \tag{4.17}$$

where $Z_0$ is the characteristic impedance of a transmission line. For even harmonics, the open circuit on the load side of the transmission line is repeated, thus producing an open circuit at the drain. However, the quarter-wave transmission line converts the open circuit at the load to a short circuit at the drain for odd harmonics with resistive load at the fundamental.

Consequently, for a purely sinusoidal current flowing into the load due to infinite loaded quality factor of the series fundamentally tuned circuit, the ideal drain current and voltage waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms shown in Figs. 4.9(*b*) and 4.9(*c*), respectively. Here, a sum of odd harmonics approximates a square current waveform and a sum of the fundamental and even harmonics approximates a half-sinusoidal drain voltage waveform. As a result, the shapes of the drain current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. The quarter-wave transmission line causes the output voltage across the load resistor $R_L$ to be phase-shifted by 90° relative to the fundamental-frequency components of the drain voltage and current.

## 4.4 Load Networks with Lumped Elements

Theoretical results show that the proper control of the second harmonic can significantly increase the collector efficiency of the power amplifier by flattening of the output-current waveform and minimizing the product of integration of the voltage and current waveforms. Practical realization of a multi-element high-order *LC* resonant circuit can cause a serious implementation problem, especially at higher frequencies and in monolithic integrated circuits, when only three harmonic components can be effectively controlled. Therefore, it is sufficient to be confined to the three or four element resonant circuit comprising the load network of the power amplifier. In this case, the operation with a second harmonic open-circuit and third-harmonic short-circuit is a promising concept for low-voltage power amplifiers [11].

In addition, it is necessary to take into account that, in practice, both extrinsic and intrinsic transistor-parasitic elements like output shunt capacitance or serious inductance have a substantial effect on the efficiency. The output capacitance $C_{out}$ can represent the collector capacitance $C_c$ in the case of the bipolar transistor or drain-source capacitance plus gate-drain capacitance $C_{ds} + C_{gd}$ in the case of the FET device. The output inductance $L_{out}$ is generally composed of the bondwire and lead inductances for a packaged transistor, effect of which becomes significant at higher frequencies. Fig. 4.11 shows the typical two-terminal lumped reactive networks with series and parallel resonators used in a practical design procedure,

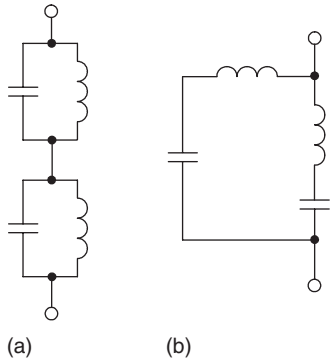



**Figure 4.11: Two terminal reactive network with series and parallel resonators.**

which provide ideally infinite impedances at the fundamental-frequency and second harmonic components.

The equivalent circuit of the second-harmonic impedance-peaking circuit is shown in Fig. 4.12. Here, the series circuit consisting of an inductor $L_1$ and a capacitor $C_1$ creates a resonance at the second harmonic. Since the device output inductor $L_{out}$ and capacitor $C_{out}$ are tuned to create an open-circuited condition at the second harmonic, the device collector sees resultant high impedance at the second harmonic. To achieve a second-harmonic high impedance, an external inductance may be added to interconnect the device output inductance $L_{out}$ directly at the output terminal (collector or drain) if its existing value (parasitic capacitance) is not accurate enough. As a result, the values of the network parameters are as follows:

$$L_{out} = \frac{1}{4\omega_0^2 C_{out}} \tag{4.18}$$

$$L_1 = \frac{1}{4\omega_0^2 C_1}. \tag{4.19}$$

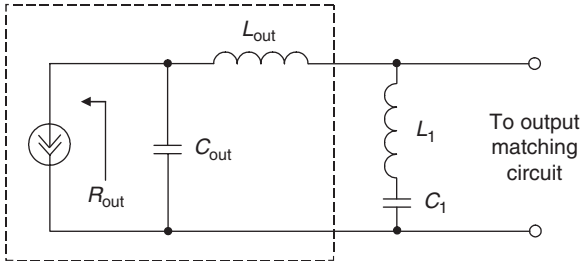



**Figure 4.12: Second-harmonic impedance-peaking circuit.**

As a first approximation for numerical calculation, the output device resistance $R_{\text{out}}$ at the fundamental frequency required to realize an inverse Class-F operation mode with second-harmonic peaking can be estimated as an equivalent resistance determined at the fundamental frequency for an ideal inverse Class-F operation, $R_{\text{out}} = R_1^{(invF)} = V_1/I_1$. Assuming zero saturation voltage and using Eq. (4.11) yield

$$R_1^{(invF)} = \frac{\pi}{2}\frac{V_{\text{cc}}}{I_1} = \frac{\pi^2}{8}R_1^{(\text{F})} = \frac{\pi}{2}R_1^{(B)} \tag{4.20}$$

where $R_1^{(F)}$ is the fundamental output resistance in a conventional Class-F mode and $R_1^{(B)} = V_{\text{cc}}/I_1$ is the fundamental output resistance in an ideal Class B.

## 4.5 Load Networks with Transmission Lines

The ideal inverse Class-F power amplifier cannot provide all voltage third and higher-order odd harmonic short-circuit termination by the use of a single parallel transmission line, as can be easily realized by a quarter-wave transmission line for even harmonics in the conventional Class-F power amplifier. In this case, with a sufficiently simple circuit schematic convenient for practical realization, applying the current second harmonic peaking and voltage third harmonic termination can result in a maximum drain efficiency of more than 80% [12, 13]. The equivalent output impedance-peaking circuit of such a microstrip power amplifier is shown in Fig. 4.13. This circuit schematic is similar to the one used to provide a conventional Class-F operation mode.

As it follows from Eq. (4.20), the equivalent output resistance for an ideal inverse Class-F mode is higher by more than 1.5 times compared to a conventional Class-B operation. Therefore, using an inverse Class-F operation mode simplifies the output matching circuit

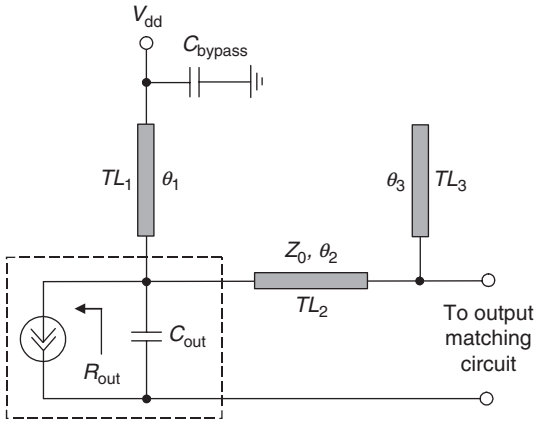



**Figure 4.13: Transmission-line impedance-peaking circuit.**

design by minimizing the impedance transformation ratio. This is very important for high output power level when the output resistance is sufficiently small. However, the maximum amplitude of the output voltage waveform can exceed the supply voltage by about three times. In practice, it requires increasing the device breakdown voltage or reducing the supply voltage. The latter is not desirable because of a decrease in power gain and efficiency.

For such an inverse Class-F microstrip power amplifier, it is necessary to provide the following electrical lengths for the transmission lines at the fundamental frequency:

$$\theta_1 = \frac{\pi}{3} \tag{4.21}$$

$$\theta_2 = \frac{1}{2}\tan^{-1}\left[\left(2Z_0\,\omega_0\,C_{\text{out}} - \frac{1}{\sqrt{3}}\right)^{-1}\right] \tag{4.22}$$

$$\theta_3 = \frac{\pi}{4} \tag{4.23}$$

where $Z_0$ is the characteristic impedance of the microstrip lines. The transmission line $TL_1$ with electrical length $\theta_1 = \pi/3$ provides a short circuit condition for the third harmonic, whereas the remaining two transmission lines, together with the device output capacitance, form a parallel resonant circuit to realize an open circuit condition for the second harmonic at the drain terminal. The open-circuit stub $TL_3$ with electrical length $\theta_3 = \pi/4$ creates a short-circuited condition at the end of the transmission line $TL_2$ at the second harmonic. Thus, the two short-circuited transmission lines having overall inductive reactance are tuned to the parallel resonance condition with the device output capacitance $C_{\text{out}}$.

As an example, Fig. 4.14 shows the frequency-response characteristic of the microstrip impedance-peaking circuit using an alumina substrate for the device output resistance $R_{\text{out}} = 50\,\Omega$ and output capacitance $C_{\text{out}} = 2.2\,\text{pF}$, characteristic impedance of microstrip lines $Z_0 = 50\,\Omega$ and electrical length $\theta_2 = 42^\circ$. From Fig. 4.14 it follows that, for the second-harmonic peaking and third-harmonic short-circuit termination, an additional output matching at the fundamental frequency $f_0 = 500\,\text{MHz}$ is required, taking into account the reactance introduced by the impedance-peaking circuit.

At higher frequencies, especially at microwaves, the effect of the output series inductance $L_{\text{out}}$, including a bond-wire inductance and lead inductance for a packaged active device, becomes significant. The equivalent circuit of such a transmission-line impedance-peaking circuit is shown in Fig. 4.15. Here, a combination of the series transmission line $TL_1$ and open-circuit stub $TL_2$ together with the output capacitance $C_{\text{out}}$ and inductance $L_{\text{out}}$ is used to provide an open-circuited condition seen by the device current source at the second harmonic. Since the

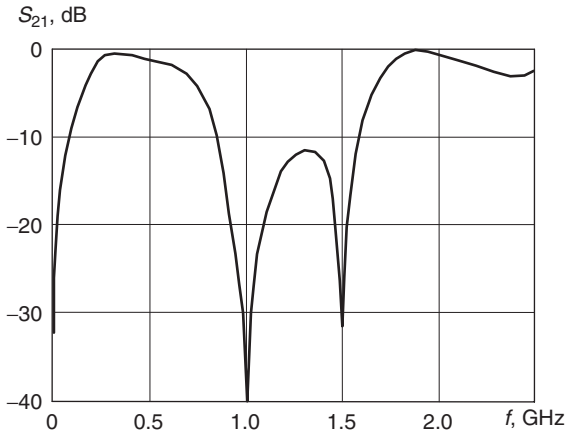



**Figure 4.14: Frequency response of the microstrip impedance-peaking circuit.**

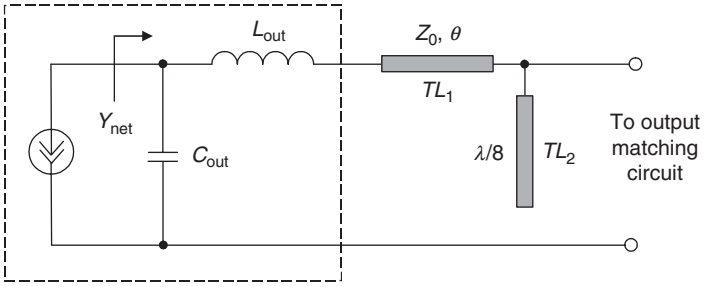



**Figure 4.15: Second harmonic resonant circuit with output lead inductance.**

open-circuit stub at the second harmonic has zero impedance, the network admittance at the second harmonic can be written as

$$Y_{\text{net}}(2\omega_0) = j2\omega_0 C_{\text{out}} + \frac{1}{j2\omega_0 L_{\text{out}} + jZ_0 \tan 2\theta}. \tag{4.24}$$

Hence, when $Y_{\text{net}}(2\omega_0) = 0$, the ratios between the parameters of the impedance-peaking circuit at the second harmonic are defined from

$$\theta = \frac{1}{2} \tan^{-1}\left(\frac{1 - 4\omega_0^2 L_{\text{out}} C_{\text{out}}}{2\omega_0 C_{\text{out}} Z_0}\right). \tag{4.25}$$

resulting in a parallel-resonant circuit consisting of the shunt capacitance $C_{\text{out}}$ and parallel inductance composed by the output inductance $L_{\text{out}}$ and transmission line $TL_1$.

Another configuration of the impedance-peaking circuit including the output lead inductance $L_{\text{out}}$ is shown in Fig. 4.16. Here, in order to create the third-harmonic short-circuit termination

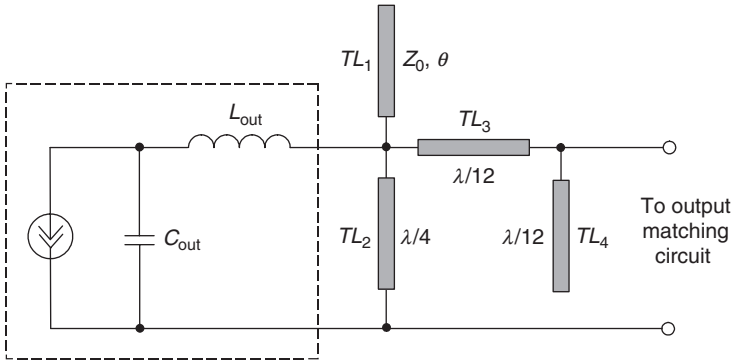



**Figure 4.16: Impedance-peaking circuit with output lead inductance.**

and second-harmonic peaking, it is convenient to use both the open-circuit and short-circuit microstrip stubs. The device output elements $C_{out}$ and $L_{out}$ (if necessary, an additional series inductor should be added) must create a parallel resonance at the second harmonic since a short-circuit stub $TL_2$ has a half wavelength at the second harmonic with short-circuited conditions at its both ends. The electrical length $\theta$ of an open-circuit stub $TL_1$ is chosen to have less than a quarter wavelength at the third harmonic to realize a capacitive reactance to be resonant with output inductance $L_{out}$ at the third harmonic of the fundamental frequency. The transmission lines $TL_3$ and $TL_4$ must be of quarter wavelengths at the third harmonic to provide a third harmonic high impedance condition at the input of $TL_3$. As a result, the ratios between the elements are as follows:

$$L_{out} = \frac{1}{4\omega^2 C_{out}} \tag{4.26}$$

$$\theta = \frac{1}{3}\tan^{-1}\left(\frac{Z_0}{3\omega_0 L_{out}}\right). \tag{4.27}$$

## 4.6 LDMOSFET Power-Amplifier Design Examples

The effectiveness of the circuit design technique for inverse Class-F application can be demonstrated by the example of a high-power LDMOSFET amplifier with the device of the same geometry as for a conventional Class-F mode. The equivalent circuit of the simulated 500 MHz single-stage microstrip inverse Class-F power amplifier is shown in Fig. 4.17. The schematic of the input and output matching circuits also represent *T*-section matching circuits with a series microstrip line, parallel open-circuit stub having a capacitive reactance and series capacitor. To provide the third harmonic termination and second harmonic peaking corresponding to an inverse Class-F operation mode, the short-circuited microstrip line with electrical length of 60° and combination of a series microstrip line and an open-circuit stub with electrical length of 45° for the second-harmonic termination are used.

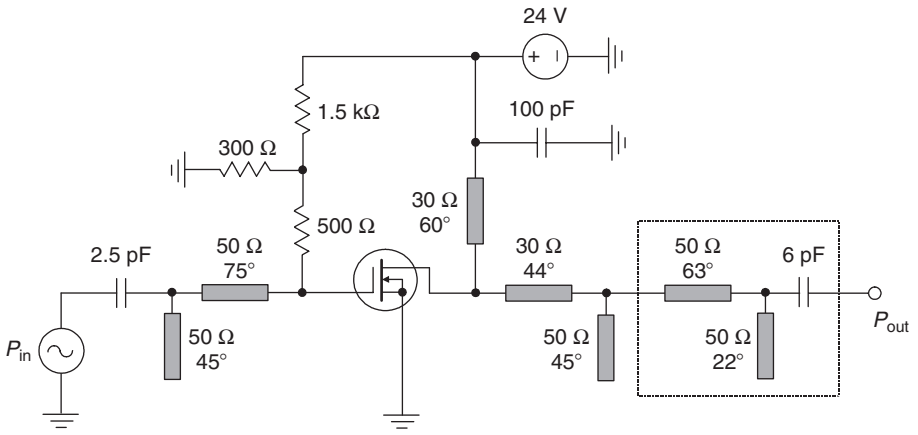



**Figure 4.17: Simulated 500 MHz single-stage microstrip power amplifier.**

Fig. 4.18 shows the drain-voltage waveform close to the half-sinusoidal one (solid line) and the drain-current waveform, which differs from the ideal square wave due to the effects of the higher-order harmonics (dotted line). Nevertheless, the drain efficiency of up to 71% with maximum output power $P_{out} = 8$ W was achieved, as shown in Fig. 4.19. In this case, the peak value of the drain voltage is more than two times greater than the drain supply voltage of 24 V (peak factor is approximately equal to $58/24 = 2.4$).

To minimize the number of circuit elements, the output-matching circuit of such a power amplifier can also be realized in the form of an *L*-transformer representing a high-pass filter section, as shown in Fig. 4.20 inside the dotted box (compare with a *T*-type output matching circuit inside the dotted box in Fig. 4.17). Simulation results indicate that, for this particular case, the length of a short-circuited parallel stub in the output matching circuit is close to a quarter-wavelength corresponding to a significant inductive reactance at the fundamental

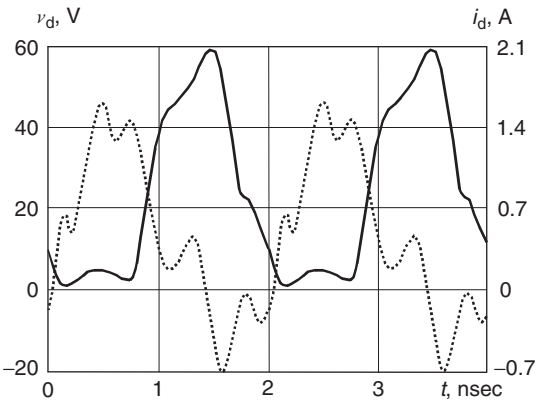



**Figure 4.18: Drain voltage and current waveforms.**

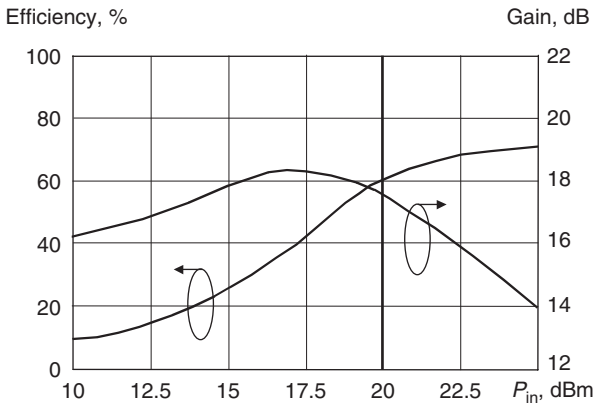



**Figure 4.19: Drain efficiency and power gain versus input power.**

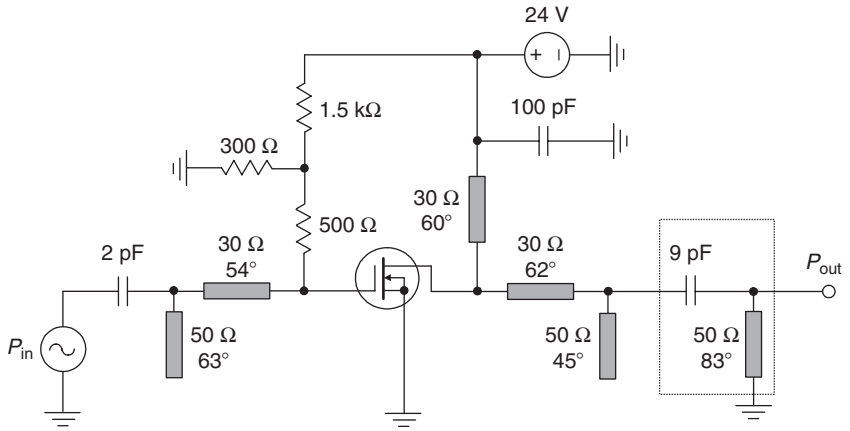



**Figure 4.20: Simulated 500-MHz microstrip power amplifier with *L*-transformer.**

frequency. Consequently, in this case, the load network designed to provide the second and third harmonic control can also perform a function of the matching circuit, together with the series capacitance also required for dc blocking. The equivalent circuit of the simulated 500-MHz single-stage microstrip inverse Class-F high-power amplifier with total LDMOSFET channel width of 28 × 1.44 mm is shown in Fig. 4.21. Drain efficiency of 78% for an output power of about 25 W with a power gain of 14 dB can be achieved, as shown in Fig. 4.22.

An analysis of the drain voltage and current waveforms plotted in Fig. 4.23 indicates that the operation mode obtained is close to an inverse Class-F mode where the current waveform is close to square one (dotted line), while the voltage waveform looks close to a half-sinusoidal. It should be noted that the negative current values are due to the current flowing through the internal drain-source and gate-drain capacitances when the device voltage-controlled current

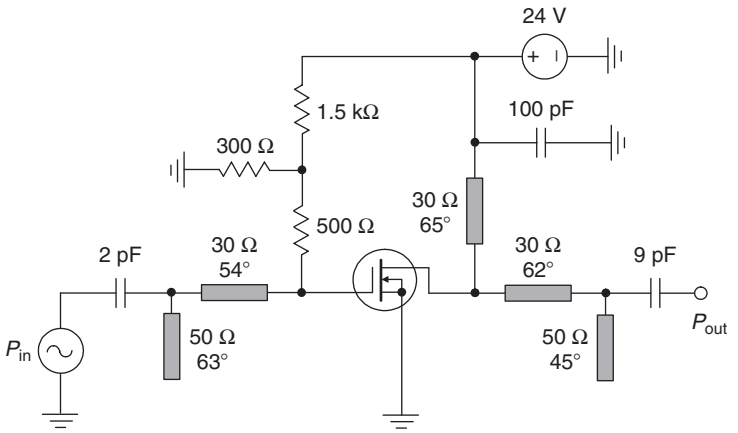



**Figure 4.21: Simulated 500 MHz single-stage microstrip high-power amplifier.**

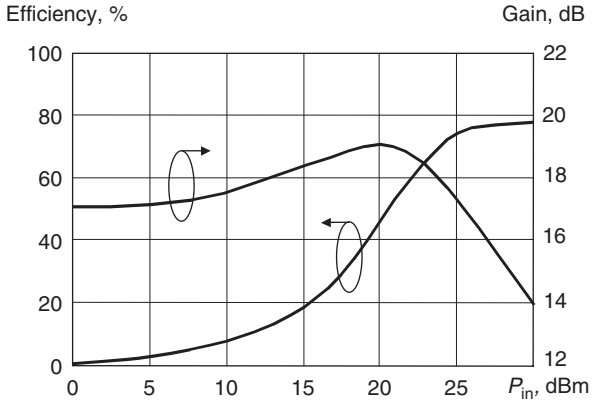



**Figure 4.22: Drain efficiency and power gain versus input power.**

source is pinched off. Also, there is a small phase shift between voltage and current waveforms due to uncompensated phases at the harmonics using such a simple load network incorporating matching properties as well. In this case, the maximum drain voltage amplitude does not reach even a value of 60 V.

Fig. 4.24 shows the (*a*) harmonic spectrum corresponding to the drain current waveform and (*b*) harmonic spectrum corresponding to the drain voltage waveform up to the fifth harmonic components. It can be seen that both the second harmonic of a current waveform and third harmonic of a voltage waveform are slightly increased than expected from the ideal waveforms. In addition, the higher-order harmonic components also make their contribution to the shapes of voltage and current waveforms. In practical design, it is possible to use chip capacitors instead of open-circuit microstrip stubs to minimize the overall size of a power-amplifier board. In this case, the presence of a parasitic series inductance of the chip capacitor

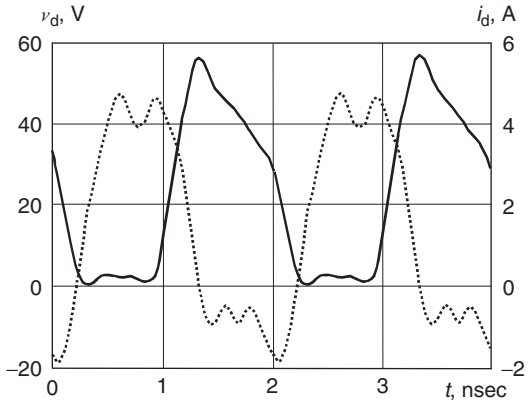



**Figure 4.23: Drain voltage and current waveforms.**

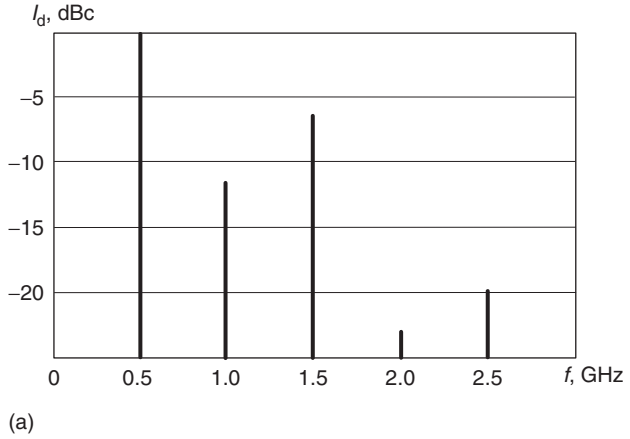



**Figure 4.24: Drain current and voltage waveform spectra.**

together with a parasitic via inductance can be useful to tune the capacitor series self-resonance condition to the second harmonic.

## 4.7 Practical Implementation

The inverse Class-F mode concept can be successfully used in low-voltage monolithic power amplifiers designed for wireless applications. Lower current consumption is preferable in RF CMOS design characterized by on-chip inductors with low-quality factors. Fig. 4.25 shows an inverse Class-F CMOS power amplifier with second harmonic peaking implemented in a 0.6 $\mu$m CMOS standard double-poly double-metal technology [14]. The MOSFET device has a gate length of 0.6 $\mu$m and a gate width of 1200 $\mu$m. The load network consists of the shunt on-chip capacitance $C_1$, the series bond-wire inductance $L_0$ and the shunt off-ship surface-mount device (SMD) capacitance $C_2$. At the second harmonic, the capacitance $C_2$ acts as a short circuit because of the self-resonance condition with its series parasitic inductance. At the same time, the capacitance $C_1$ and bond-wire inductance $L_0$ are tuned to the second harmonic providing a second-harmonic peaking at the device drain. To stabilize the power-amplifier operation, the feedback resistance $R_2$ is connected. The active device was biased at half the maximum expected drain current. As a result, at an operating frequency of 1.9 GHz and supply voltage of 3 V, a small-signal power gain of 10.5 dB, saturated output power of 22.8 dBm and maximum power-added efficiency of 42% were achieved.

However, the third-order intermodulation component $IM_3$, at high output power (approximately $-20$ dBc at $P_{out} = 18$ dBm), is large enough that this amplifier could not be used in an application that requires linear response to a varying-envelope signal. The theoretical analysis and measurements of the intermodulation distortion for Class-AB operation show that, for the small-signal conditions, $IM_3$ follows a well-known 3 dB output per dB input slope. As a result of the different contribution of the device transfer function components, there are two sweet spots where $IM_3$ is minimal [15]. The first sweet spot appears because of the turn-on knee region contribution, whereas the second sweet spot close to the output-power compression point is

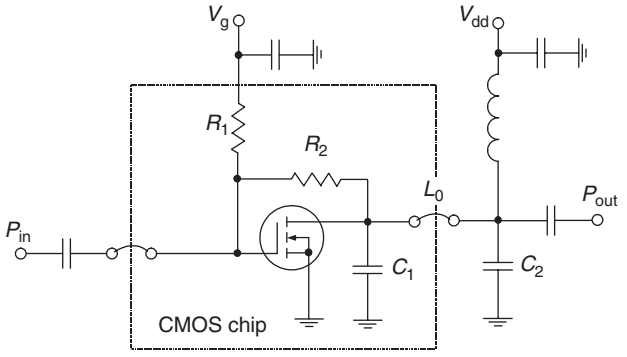



**Figure 4.25: RF CMOS inverse Class-F power-amplifier schematic.**

due to the combined effect of the quadratic-to-linear and compression transitions of the device transfer function.

Fig. 4.26 shows an inverse Class-F pulsed, bipolar power amplifier operated at 425 MHz with a peak output power of 50 W [16]. The transmission lines in the output matching circuit serve two purposes, one is to match the low impedance of the device collector to the standard 50 Ω output, and the other is to present the second-harmonic peaking required to produce the desired waveforms at the device collector for inverse Class-F operation. The electrical length $\theta$ of the first series microstrip line is calculated from Eq. (4.25) based on the value of the output device inductance $L_{out}$. The first open-circuit microstrip stub having zero impedance at the second harmonic is necessary to provide high impedance seen by the device internal current source at the second harmonic. The second open-circuit microstrip stub is necessary to maximize the suppression of the even-harmonic components. Both open-circuit stubs work as capacitors at the fundamental frequency realizing a two-section low-pass output-matching circuit. The inductor-resistor parallel circuit contains a ferrite core wire-wound inductor and 15 Ω resistor to provide a supply path while presenting an open circuit to the RF power. The right-hand capacitor on the dc-supply branch is a 1500 $\mu$F charge-storage capacitor to preserve the squareness of the current pulse at the collector by preventing pulse slump and poor rise time. The left-hand capacitor is a 100-nF parallel-plate bypass capacitor to bring RF ground to that node to prevent any RF power from entering the dc power supply.

In modern telecommunication systems operating in a frequency range of 225 MHz to 2.5 GHz, the silicon LDMOSFET devices are widely used in high-power transmitters due to their efficient and linear operation, simple bias-circuit realization, and cost-per-watt

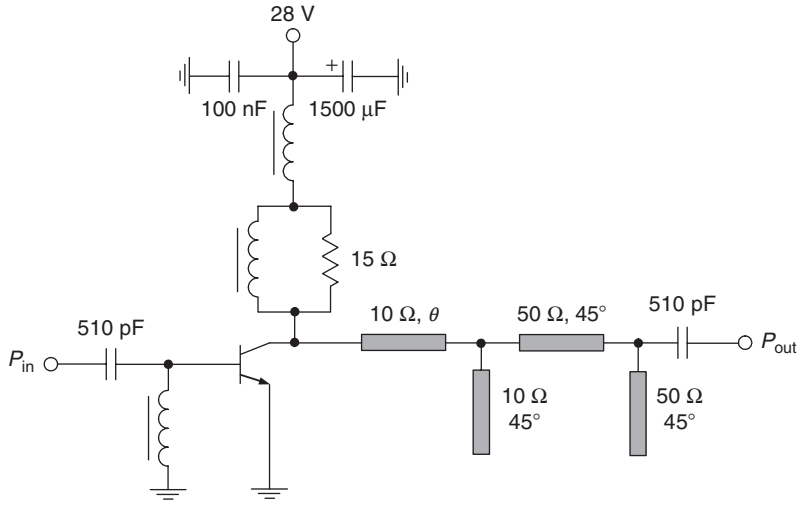



**Figure 4.26: Schematic of bipolar high-power amplifier.**

performance. Fig. 4.27 shows the schematic of a 1 GHz power amplifier using lumped resonators [17]. Such an inverse Class-F architecture provides high impedance at the second harmonic of the fundamental frequency, low impedance at the third harmonic, and provides conjugate matching of the output device impedance at the fundamental frequency to a standard 50 Ω load. By using an LDMOSFET MRF282 device with gate length of 0.8 $\mu$m and total gate width of 31.9 mm, a maximum drain efficiency of 77.8% with an output power of 12.4 W were achieved at a supply voltage of 28 V.

The 1.78 GHz power amplifier using the same LDMOSFET device, which schematic is shown in Fig. 4.28, is based on a quarter-wave transmission-line topology [17]. At the fundamental frequency, a quarter-wave transmission line works as an impedance transformer followed by a series $L_0C_0$-filter tuned to the fundamental frequency and an L-type output-matching circuit required to provide conjugate matching and additional harmonic suppression. For all harmonic components, the series filter presents an open circuit at the output of a quarter-wave transmission line. Hence, an open circuit is presented at the device output for any even harmonic and a short circuit is presented for any odd harmonic of the fundamental frequency due to the equidistant frequency properties of the input impedance of a loaded quarter-wave transmission line. The proper phasing of the second harmonic can be easily practically realized when the active device is driven into a slight saturation mode. As a result, an efficiency of 60% with an output power of 13 W and a power gain of 10 dB were achieved at a supply voltage of 26 V.

The experimental test structure of a single-stage high-voltage 500-MHz LDMOSFET power amplifier with the device gate length of 1.25 $\mu$m and total gate width of 28 × 1.44 mm is shown in Fig. 4.29 [18]. The two *T*-type impedance transformers with series microstrip lines and parallel variable capacitors are used for the input and output matching. The parameters of

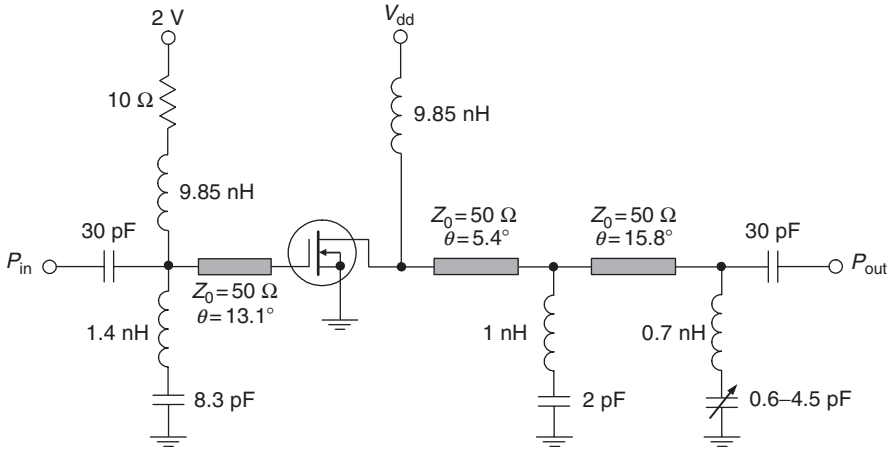



**Figure 4.27: Schematic of 1 GHz power amplifier with second harmonic resonator.**

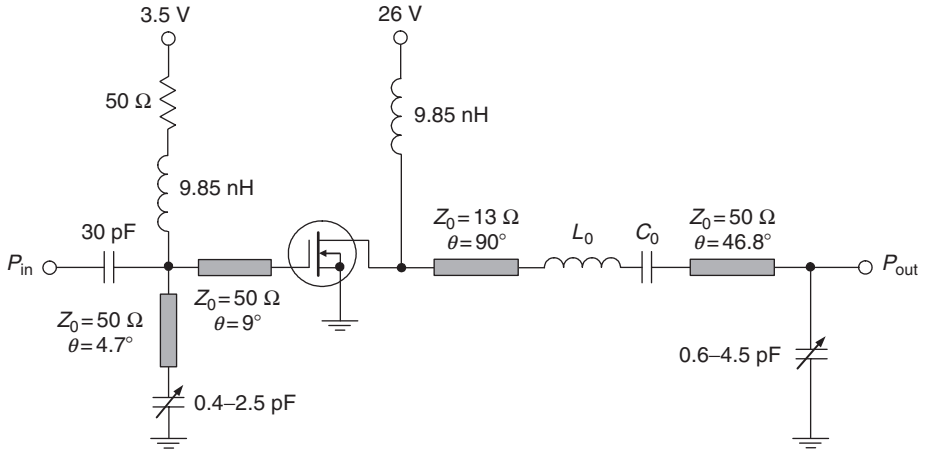



**Figure 4.28: Schematic of 1.78 GHz power amplifier with quater-wave transmission line.**

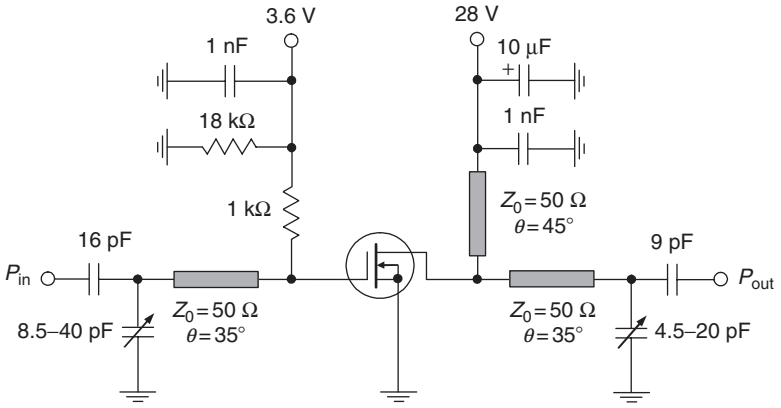



**Figure 4.29: Test structure of 500 MHz LDMOSFET high-power amplifier.**

the output-matching circuit are chosen to approximate an inverse Class-F mode. The matching circuits were fabricated on epoxy-glass copper-clad laminate substrate and the characteristic impedances of all microstrip lines are equal to 50 Ω. To avoid low-frequency parasitic oscillations, the electrolytic capacitor of 10 $\mu$F was connected in parallel to the drain voltage supply. The circuit parameters were chosen according to the results of the analytical calculation and final computer optimization for high-efficiency operating mode of this power amplifier. In this case, only small fine-tuning of the variable capacitors in the input and output matching circuits were needed to realize the excellent electrical characteristics of this high-voltage LDMOSFET power amplifier. Maximum level of the output power of 20 W with a power gain of 13 dB, drain efficiency of 76%, and dc drain current of 0.94 A was achieved. An appropriate choice of the input matching circuit elements to maximize the

amplifier frequency range contributed to providing an output-power ripple of less than 1 dB peak-to-peak within the frequency bandwidth of about 20%.

## References


[1] A. I. Kolesnikov, ''A New Method to Improve Efficiency and to Increase Power of the Transmitter (in Russian),'' *Master Svyazi*, pp. 27–41, June 1940.

[2] R. I. Sarbacher, ''Power-Tube Performance in Class C Amplifiers and Frequency Multipliers as Influenced by Harmonic Voltage,'' *Proc. IRE*, vol. 31, pp. 607–625, November 1943.

[3] E. S. Glazman, L. B. Kalinin, and Y. I. Mikhailov, ''Improving VHF Transmitter Efficiency by Using the Biharmonic Mode,'' *Telecommunications and Radio Engineering,* Part 1, vol. 30, pp. 46–51, July 1975.

[4] V. J. Tyler, ''A New High-Efficiency High-Power Amplifier,'' *Marconi Review*, vol. 21, pp. 96–109, Fall 1958.

[5] X. Lu, ''An Alternative Approach to Improving the Efficiency of High Power Radio Frequency Amplifiers,'' *IEEE Trans. Broadcasting*, vol. BC-38, pp. 85–89, June 1992.

[6] N. S. Fuzik, ''Biharmonic Modes of a Tuned RF Power Amplifier,'' *Telecommunications and Radio Engineering,* Part 2, vol. 25, pp. 117–124, July 1970.

[7] Z. Zivkovic and A. Marcovic, ''Increasing the Efficiency of the High-Power Triode HF Amplifier—Why Not with the Second Harmonic?'' *IEEE Trans. Broadcasting*, vol. BC-32, pp. 5–10, March 1986.

[8] B. Ingruber, W. Pritzl, D. Smely, M. Wachutka, and G. Magerl, ''A High-Efficiency Harmonic-Control Amplifier,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 857–862, June 1998.

[9] M. K. Kazimierczuk, ''A New Concept of Class F Tuned Power Amplifier,'' *Proc. 27th Midwest Circuits and Systems Symp.*, pp. 425–428, 1984.

[10] F. H. Raab, ''An Introduction to Class-F Power Amplifiers,'' *RF Design*, vol. 19, pp. 79–84, May 1996, p. 14, July 1996.

[11] P. Heymann, R. Doerner, and M. Rudolph, ''Harmonic Tuning of Power Transistors by Active Load-Pull Measurement,'' *Microwave J.*, vol. 43, pp. 22–37, June 2000.

[12] C. J. Wei, P. DiCarlo, Y. A. Tkachenko, R. McMorrow, and D. Bartle, ''Analysis and Experimental Waveform Study on Inverse Class-F Mode of Microwave Power FETs,'' *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 525–528.

[13] A. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[14] F. Fortes and M. J. Rosario, ''A Second Harmonic Class-F Power Amplifier in Standard CMOS Technology,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1216–1220, June 2001.

[15] C. Fager, J. C. Pedro, N. B. Carvalho, H. Zirath, F. Fortes, and M. J. Rosario, ''A Comprehensive Analysis of IMD Behavior in RF CMOS Power Amplifiers,'' *IEEE J. Solid-State Circuits*, vol. SC-39, pp. 24–34, January 2004.

[16] W. McCalpin, ''High Efficiency Power Amplification with Optimally Loaded Harmonic Waveshaping,'' *Proc. RF Tech. Expo '86* (Anaheim, CA), pp. 119–124, 1986.

[17] F. Lepine, A. Adahl, and H. Zirath, ''*L*-Band LDMOS Power Amplifiers Based on an Inverse Class-F Architecture,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-53, pp. 2007–2012, June 2005.

[18] A. V. Grebennikov, ''Effective Circuit Design Techniques to Increase MOSFET Power Amplifier Efficiency,'' *Microwave J.*, vol. 43, pp. 64–72, July 2000.

This page intentionally left blank

CHAPTER 5

# Class E with Shunt Capacitance

The switched-mode Class-E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency operation. Their load network configuration consists of the shunt capacitance, series inductance, and series filter tuned to the fundamental frequency to provide a high level of harmonic suppression. In the Class-E power amplifier, the transistor operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition when the high current and the high voltage do not overlap simultaneously that minimizes the power dissipation and maximizes the power-amplifier efficiency. In this chapter, the historical aspect and modern trends of a Class-E power-amplifier design are presented. Different circuit configurations and load network techniques using the push-pull mode, lumped, and transmission-line elements are analyzed. The effect of the device saturation resistance, finite switching time, and nonlinear shunt capacitance is described. The practical RF and microwave Class-E power amplifiers and their applications are given and discussed.

## 5.1 Effect of Detuned Resonant Circuit

Using resonant circuits tuned to the odd or even harmonics of the fundamental frequency in the load network by realizing biharmonic or polyharmonic operation modes of the vacuum-tube power amplifiers is very effective to increase their operating efficiency. This implies ideally the in-phase or out-of-phase harmonic conditions when symmetrical flattened voltage or current waveforms can be formed. However, as it turned out, this is not the only way to improve the power-amplifier efficiency. Fig. 5.1 shows the circuit schematic of the vacuum-tube power amplifier with a parallel-tuned LC-circuit inserted between the anode and the output matching circuit, which has a resonant frequency equal to about 1.5 times the carrier frequency of the signal to be amplified [1]. In other words, if the carrier signal is transmitting at a fundamental frequency $f_0$, the parallel resonant circuit will have a resonant frequency of about $1.5f_0$ followed by a filter or output matching circuit to suppress the harmonics of the fundamental frequency and to maximize the output power at the fundamental frequency delivered to the standard load. As a result, an efficiency of 89% was achieved for a 3.2 MHz vacuum-tube high-power amplifier. Although it was assumed that such a parallel resonant circuit introduces considerable impedance to its own second harmonic, which is the third

harmonic $3f_0$ of the carrier frequency and can result in a flattened anode voltage waveform, another interesting and nontrivial conclusion can be derived from this circuit topology. In this case, provided the output π-type-matching circuit has purely resistive impedance at the fundamental frequency and capacitive reactances at the harmonic components, the anode of the device sees inductive impedance at the fundamental frequency and capacitive reactances at the second and higher-order harmonic components. This means that the voltage and current waveforms are not symmetrical anymore representing an alternative mechanism of the efficiency improvement. Such an effect of increasing efficiency when the output resonant circuit of the vacuum-tube Class-C power amplifier is detuned relative to the carrier frequency was described earlier [2]. The anode efficiencies of about 92–93% were achieved for the phase angles of the output load network in limits of 30°–40° resulting in the inductive reactance at the fundamental frequency and capacitive reactances at the harmonic components seen by the anode of the active device.

At the same time, it was discovered that very high efficiencies can be obtained with a series resonant *RLC* circuit connected to the transistor, as shown in Fig. 5.2(*a*) [3]. The reasons for this high efficiency are due to a proper choice of transistor and circuit parameters, the transistor operates in a pure switching mode, and the voltage across the transistor and the current flowing through it can both be made equal to zero during the switching transient interval. To satisfy this condition, the current and voltage must be zero at the time just prior to the conduction interval when transistor goes to the saturation mode and the series-tuned circuit, consisting of a capacitor $C_0$ and an inductor $L$, must appear inductive at the operating frequency. In this case, a loaded quality factor $Q_L$ of the series-tuned circuit of about 10 will give a good sinusoidal shape to the load current. As a result, a 20 W 500 kHz bipolar power amplifier was built having a collector efficiency of 94% with a conduction angle of 180°.

To realize high operation efficiency of the power amplifier, the ideal switch should represent the transistor, and the impedance seen from the collector into the matched circuit should not correspond to a short circuit for the second harmonic over the whole frequency range [4].

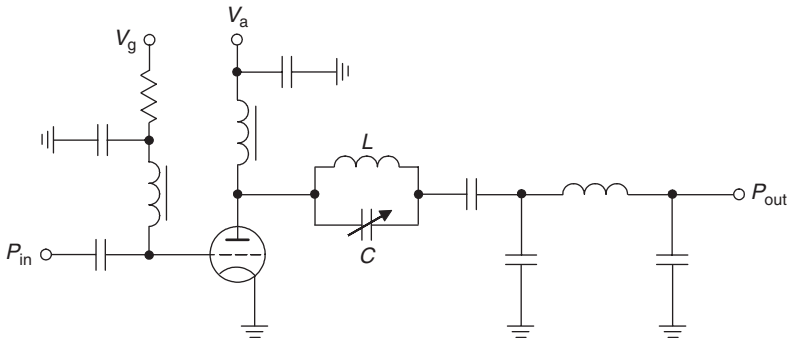



**Figure 5.1: Class-C power amplifier with detuned resonant circuit.**

The simplified collector circuit of the switched-mode power amplifier is shown in Fig. 5.2(*b*), where $C$ is a collector-emitter capacitance assumed independent of voltage, $C_0$ is the dc blocking capacitor, $L$ is the series inductor, and $R$ is the load resistor. When the voltage across $C$ crosses zero, the switch will close. The basic switching operation can be described by the two sets of linear first-order differential equations, one set for the on-state and another for the off-state, with an approximate solution. It was assumed that high collector efficiency is a result of a zero collector-emitter voltage at the end of the off-state cycle due to transient without need for any current when only a little power is dissipated in the switching slopes. The collector efficiencies up to 85% were achieved in the frequency range from 48–70 MHz.

The exact theoretical analysis of the operation conditions of a single-ended switched-mode power amplifier using its simplified equivalent circuit shown in Fig. 5.2(*b*) with the calculation of the circuit parameters [5, 6]. Here, the active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is on and by the transient response of the load network when the switch is off. To simplify a theoretical analysis, the following assumptions were introduced:

- Transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless (except when discharging the shunt capacitance).

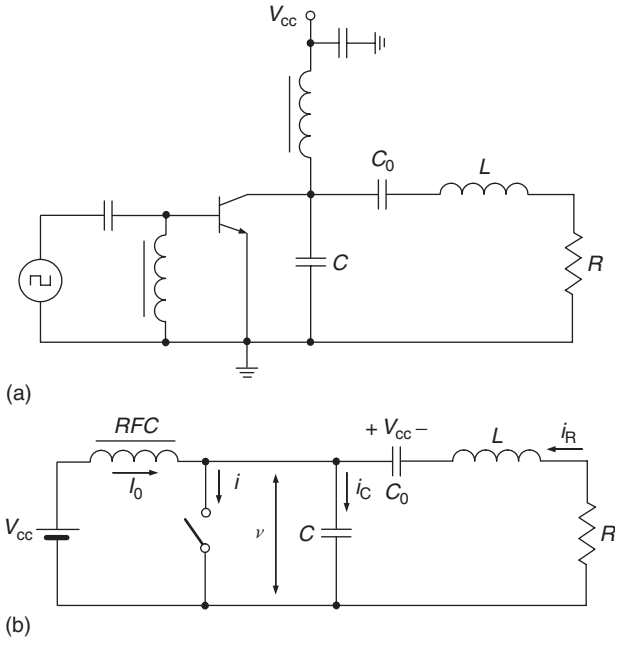



**Figure 5.2: Basic circuits of switched-mode power amplifier with non-sinusoidal output voltage.**

- Total shunt capacitance is independent of the collector and is assumed linear.
- RF choke allows only a constant dc current and has no resistance.
- There are no losses in the circuit except into the load $R$.

For a lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch at turn-on time moment $t = T$, when transistor is saturated:

$$v(t)\big|_{t=T} = 0 \tag{5.1}$$

$$\left.\frac{dv(t)}{dt}\right|_{t=T} = 0 \tag{5.2}$$

where $T$ is the period of input driving signal, and $v(t)$ is the voltage across the switch. The second condition means that the collector current $i(t)$ has no jump and is equal to zero at this moment since the collector capacitor $C$ is completely discharged.

The derivation of the load network parameters is based on the consideration of the processes during on-state and off-state transistor operation modes separately [6, 7]. When the switch is turned on, the equivalent amplifier system is described by a system of differential equations in the form of

$$V_{cc} = L\frac{di_R(t)}{dt} + i_R(t)R \tag{5.3}$$

$$i(t) = I_0 + i_R(t), \tag{5.4}$$

where the voltage $V_{cc}$ is applied to the plates of the blocking capacitor $C_0$. By taking into account the initial condition $i(0) = 0$, the current $i(t)$ flowing through the switch can be obtained by

$$i_s(t) = \frac{V_{cc} + I_0R}{R}\left[1 - \exp\left(-\frac{R}{L}t\right)\right]. \tag{5.5}$$

When at the time moment $t = t_1$ switch is turned off, another system of differential equations can be written by

$$V_{cc} = v(t) + L\frac{di_R(t)}{dt} + i_R(t)R \tag{5.6}$$

$$C\frac{dv(t)}{dt} = I_0 + i_R(t) \tag{5.7}$$

with the initial conditions $i_R(t_1) = i(t_1) - I_0$ and $v(t_1) = 0$.

Hence, the voltage $v(t)$ across the switch can be obtained from

$$v(t) = (V_{cc} + I_0R)\left[1 + \frac{1}{\omega}\sqrt{d^2 + \omega^2}\ \exp(-\delta t)\sin(\omega t + \varphi)\right], \tag{5.8}$$

where

$$\omega_0 = 1/\sqrt{LC} \quad \delta = \frac{R}{2L} = \frac{\omega_0}{2Q_L}$$

$$d = \frac{i(t_1)}{(V_{cc} + I_0R)}\frac{1}{C} - \delta$$

$$\varphi = \tan^{-1}\left(\frac{\omega}{d}\right) \quad \omega = \sqrt{\omega_0^2 - \delta^2}.$$

In optimum operation mode when the collector voltage current waveforms shown in Fig. 5.3 (a) and (b) do not overlap each other resulting in a zero power loss on the transistor, the voltage $v(t)$ in Eq. (5.8) should satisfy the conditions given by Eqs. (5.1) and (5.2). As a result, the analytical relationships between the load network components can be obtained whose values for different duty cycle or saturation time $\tau_{sat} = \omega t_1$ are given in Table 5.1, were $P_{out} = I_0V_{cc}$ is the output power corresponding to the idealized lossless operation conditions [8].

However, to provide such an idealized switching operation mode, the loaded quality factor of this L-type circuit should be sufficiently small, for example, $Q_L = 2.8656$ for a 50% duty cycle increasing at smaller duty cycles. This leads to the variation of the harmonic coefficient from 15% at $\tau_{sat} = 216°$ to 3% at $\tau_{sat} = 144°$. As a result, such a switched-mode bipolar power amplifier designed to operate at 1 MHz and supply voltage of 15 V with total output power of 3 W could provide collector efficiency of 95.9% under optimum conditions with 50% duty cycle [8].

## 5.2 Load Network with Shunt Capacitor and Series Filter

For additional harmonic suppression, it is necessary to connect the load through the series filter tuned to the fundamental frequency, for example, a simple $L_0C_0$ filter as shown in Fig. 5.4(*a*) [5, 9]. The loaded quality factor $Q_L$ of the series resonant circuit consisting of an inductor $L_0$ and a capacitor $C_0$ tuned to the fundamental frequency $\omega_0 = 1/\sqrt{L_0C_0}$ should be sufficiently high in order for the output current to be sinusoidal. The single-ended switched-mode

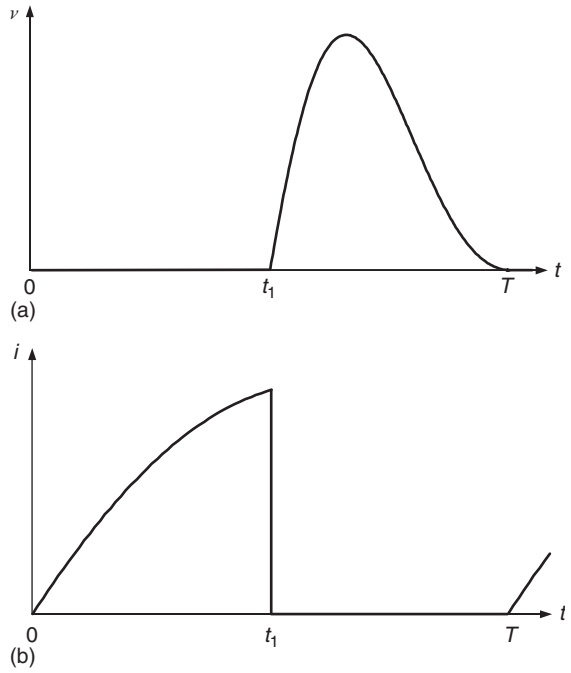



**Figure 5.3: Idealized collector voltage and current waveforms of switched-mode power amplifier with non-sinusoidal output voltage.**

power amplifier with a shunt capacitor (such as a Class-E power amplifier) was introduced by Sokals in 1975 and has found widespread application due to its design simplicity and high operation efficiency [10, 11]. This type of high-efficiency power amplifiers is widely used in different frequency ranges and output power levels ranging from several kilowatts at low RF frequencies up to about one watt at microwaves [12].

The characteristics of a Class-E power amplifier can be determined by finding its steady-state collector voltage and current waveforms. The simplified equivalent circuit of a Class-E power amplifier with a shunt capacitance is shown in Fig. 5.4(*b*) where the load network consists of a capacitor *C* shunting the transistor, a series inductor *L*, a series fundamentally tuned

**Table 5.1: Load Network Parameters of Switched-Mode Power Amplifier**

| Parameters | $\tau_{sat}$, degree | | | | |
|---|---|---|---|---|---|
| | 108° | 144° | 180° | 216° | 252° |
| $\frac{\omega L}{R}$ | 3.4872 | 2.4083 | 1.7879 | 1.3494 | 0.9887 |
| $\omega CR$ | 0.2063 | 0.2280 | 0.2177 | 0.1865 | 0.1437 |
| $\frac{P_{out}R}{V_{cc}^2}$ | 0.0732 | 0.1788 | 0.3587 | 0.6622 | 1.1953 |

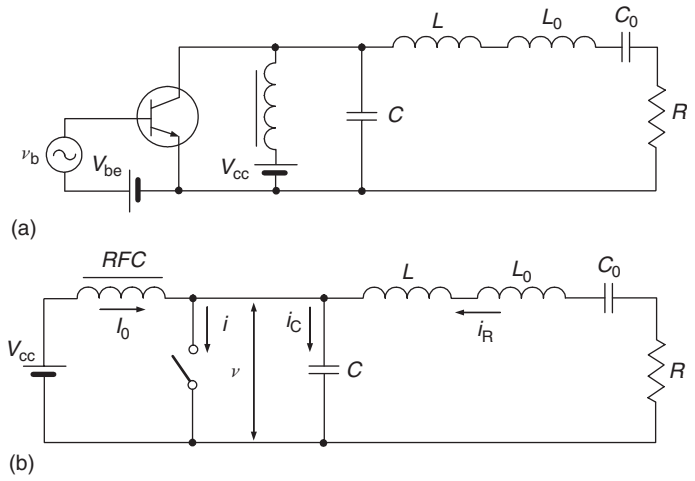



**Figure 5.4: Basic circuits of Class-E power amplifier with shunt capacitance.**

$L_0C_0$ circuit and a load resistor $R$. In a common case, a shunt capacitor $C$ can represent the intrinsic device output capacitor and external circuit capacitor added by the load network. The collector of the transistor is connected to the supply voltage by an RF choke with high reactance at the fundamental frequency. The active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off.

To simplify an analysis of a Class-E power amplifier, the following several assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed linear.
- The RF choke allows only a constant dc current and has no resistance.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant $L_0C_0$ circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except only in the load $R$.
- For an optimum operation mode, a 50% duty cycle is used.

For a lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch (just prior to the start of switching on) at the moment $\omega t = 2\pi$, when the transistor is saturated:

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{5.9}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0, \tag{5.10}$$

where $v(\omega t)$ is the voltage across the switch.

The detailed theoretical analysis of a Class-E power amplifier with shunt capacitance for any duty cycle [13], where the load current is assumed sinusoidal, is given as

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi), \tag{5.11}$$

where $\varphi$ is the initial phase shift.

When switch is on for $0 \leq \omega t < \pi$, the current through the capacitance

$$i_{\mathrm{C}}(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0 \tag{5.12}$$

and, consequently,

$$i(\omega t) = I_0 + I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{5.13}$$

under the initial on-state condition $i(0) = 0$. Hence, the dc current can be defined as

$$I_0 = -I_{\mathrm{R}} \sin\varphi \tag{5.14}$$

and the current through the switch can be rewritten by

$$i(\omega t) = I_{\mathrm{R}}[\sin(\omega t + \varphi) - \sin\varphi]. \tag{5.15}$$

When the switch is off for $\pi \leq \omega t < 2\pi$, the current through the switch $i(\omega t) = 0$, and the current flowing through the capacitor $C$ can be written as

$$i_{\mathrm{C}}(\omega t) = I_0 + I_{\mathrm{R}} \sin(\omega t + \varphi), \tag{5.16}$$

producing the voltage across the switch by the charging of this capacitor according to

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_C(\omega t)d\omega t$$
$$= -\frac{I_R}{\omega C}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi]. \tag{5.17}$$

Applying the first optimum condition given by Eq. (5.9) enables the phase angle $\varphi$ to be determined as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482^{\circ}. \tag{5.18}$$

Consideration of trigonometric relationships shows that

$$\sin\varphi = \frac{-2}{\sqrt{\pi^2+4}} \quad \cos\varphi = \frac{\pi}{\sqrt{\pi^2+4}}. \tag{5.19}$$

Then, the steady-state voltage waveform across the switch using Eqs. (5.14) and (5.19) can be obtained in the form of

$$v(\omega t) = \frac{I_0}{\omega C}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right). \tag{5.20}$$

Using Fourier-series expansion, the expression to determine the supply voltage $V_{cc}$ can be written as

$$V_{cc} = \frac{1}{2\pi}\int_{0}^{2\pi} v(\omega\, t)\, d\omega t = \frac{I_0}{\pi\omega C}. \tag{5.21}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{5.22}$$

$$\frac{i(\omega t)}{I_0} = \frac{\pi}{2}\sin\omega t - \cos\omega t + 1. \tag{5.23}$$

Fig. 5.5 shows the normalized (*a*) load current, (*b*) collector voltage waveform, and (*c*) collector current waveforms for an idealized optimum Class E with shunt capacitance. From collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and the current *i* consisting of the load sinusoidal current

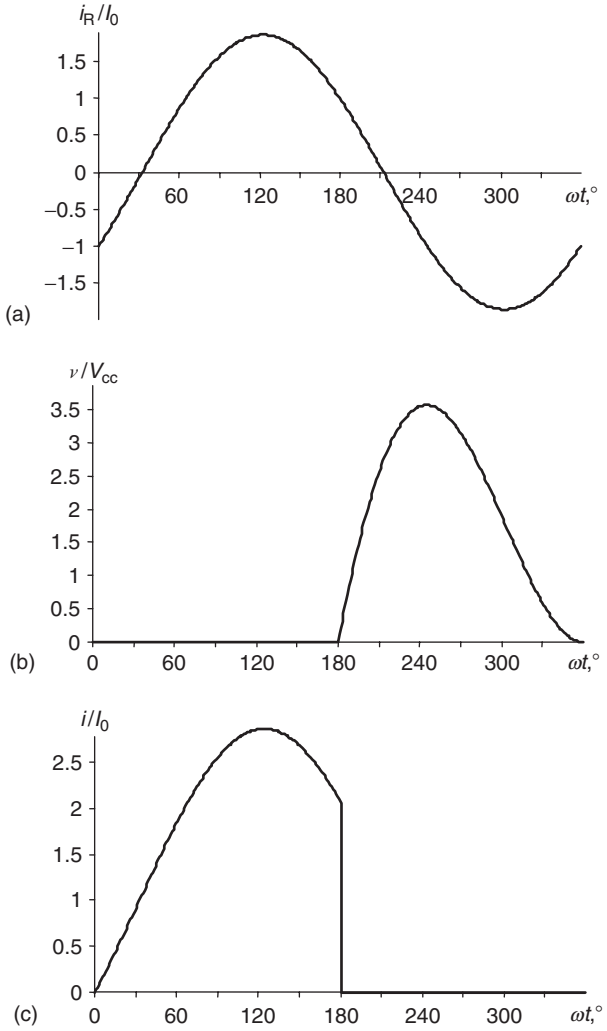



**Figure 5.5: Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum Class E with shunt capacitance.**

and dc current flows through the device. However, when the transistor is turned off, this current flows through the shunt capacitance $C$. The jump in the collector current waveform at the instant of switching off is necessary to obtain nonzero output power at the fundamental frequency delivered to the load, which can be defined as an integration of the product of the collector voltage and current derivatives over the entire period [14]. Therefore, $dv/dt$ and $di/dt$ must both be nonzero during at least one of the switching transitions.

As a result, there is no nonzero voltage and current simultaneously, which means a lack of the power losses gives an idealized collector efficiency of 100%. This implies that the dc power and fundamental-frequency output power delivered to the load are equal,

$$I_0 V_{cc} = \frac{I_R^2}{2} R. \tag{5.24}$$

Consequently, the value of dc supply current $I_0$ can be determined using Eqs. (5.14) and (5.19) by

$$I_0 = \frac{V_{cc}}{R} \frac{8}{\pi^2 + 4} = 0.577 \frac{V_{cc}}{R}. \tag{5.25}$$

Then, the amplitude of the output voltage $V_R = I_R R$ can be obtained from

$$V_R = \frac{4V_{cc}}{\sqrt{\pi^2 + 4}} = 1.074\ V_{cc}. \tag{5.26}$$

The peak collector voltage $V_{max}$ and current $I_{max}$ can be determined by differentiating the appropriate waveforms given by Eqs. (5.22) and (5.23), respectively, and setting the results equal to zero, which gives

$$V_{max} = -2\pi\varphi\ V_{cc} = 3.562\ V_{cc} \tag{5.27}$$

and

$$I_{max} = \left( \frac{\sqrt{\pi^2 + 4}}{2} + 1 \right) I_0 = 2.8621\ I_0. \tag{5.28}$$

The fundamental-frequency voltage $v_1(\omega t)$ across the switch consists of two quadrature components, as shown in Fig. 5.6, whose amplitudes can be found using Fourier formulas and Eq. (5.22) by

$$V_R = -\frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin(\omega t + \varphi) d(\omega t) = \frac{I_R}{\pi\omega C} \left( \frac{\pi}{2} \sin 2\varphi + 2\cos 2\varphi \right) \tag{5.29}$$

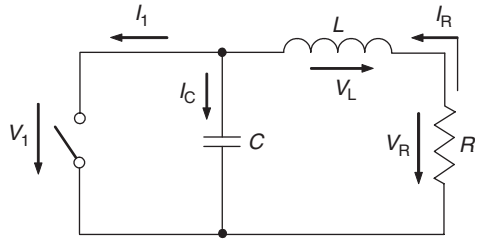



**Figure 5.6: Equivalent Class-E load network at fundamental frequency.**

$$V_L = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t+\varphi)d\omega t = -\frac{I_R}{\pi\omega C}\left(\frac{\pi}{2}+\pi\sin^2\varphi+2\sin 2\varphi\right). \tag{5.30}$$

As a result, the optimum series inductance $L$ and shunt capacitance $C$ can be calculated from

$$\frac{\omega L}{R} = \frac{V_L}{V_R} = 1.1525 \tag{5.31}$$

$$\omega CR = \frac{\omega C}{I_R}V_R = 0.1836. \tag{5.32}$$

The optimum load resistance $R$ can be obtained using Eqs. (5.24) and (5.26) for the supply voltage $V_{cc}$ and fundamental-frequency output power delivered to the load $P_{out}$ as

$$R = \frac{8}{\pi^2+4}\frac{V_{cc}^2}{P_{out}} = 0.5768\frac{V_{cc}^2}{P_{out}}. \tag{5.33}$$

Finally, the phase angle of the load network seen by the switch and required for an idealized optimum Class E with shunt capacitance can be determined through the load network parameters using Eqs. (5.31) and (5.32) by

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1-\frac{\omega L}{R}\omega CR}\right) = 35.945^\circ. \tag{5.34}$$

When realizing an optimum Class-E operation mode, it is very important to know up to which maximum frequency such an idealized efficient operation mode can be extended. In this case, it is advisable to establish a relationship between a maximum frequency $f_{max}$, a parallel shunt capacitance $C$, and a supply voltage $V_{cc}$. As a result, substituting Eq. (5.32) into Eq. (5.25) gives

$$I_0 = \pi\omega C V_{cc}. \tag{5.35}$$

Then, by taking into account the relationship between $I_0$ and $I_{max}$ given in Eq. (5.28), the maximum frequency of an optimum Class-E power amplifier using a load network with shunt capacitance can be evaluated from

$$f_{max} = \frac{1}{\pi^2}\frac{1}{\sqrt{\pi^2+4}+2}\frac{I_{max}}{C_{out}V_{cc}} = \frac{I_{max}}{56.5C_{out}V_{cc}}, \tag{5.36}$$

where $C = C_{out}$ is the device output capacitance limiting the maximum operation frequency of an ideal Class-E circuit [15].

The high $Q_L$ assumption for the series resonant $L_0C_0$ circuit can lead to considerable errors if its value is substantially small in real circuits [16]. For example, for a 50% duty cycle, the values of the circuit parameters for the loaded quality factor less than unity can differ by several tens of percents. At the same time, for $Q_L \geq 7$, the errors are found to be less than 10% and become less than 5% for $Q_L \geq 10$. A detailed overview of Class-E power amplifiers with shunt capacitance including explicit design equations, applicable frequency range, optimization principles, and experimental results is given (see reference [17]).

In optimum Class-E operation, the load network discharges the device output capacitance prior to turn-on of the device, producing ideally 100% efficiency. Below the maximum frequency, at which the shunt susceptance required for optimum operation is provided by the device output capacitance only, it is generally possible to adjust the series load reactance to achieve 100% efficiency. For example, optimum operation can be achieved by adding external shunt capacitance to the device output. However, above the maximum frequency, it is impossible to achieve an ideal 100% efficiency by varying the series load network parameters. As frequency increases, the collector voltage waveform approaches the ramp produced by dc charging of the shunt capacitor. Consequently, the maximum achievable collector (drain) efficiency decreases as the frequency of operation is increased above the maximum frequency. The maximum possible efficiency $\eta_{max}$ and the normalized circuit parameter $\omega L/R$ required to produce it, along with the normalized peak voltage $V_{max}/V_{cc}$, for a fixed supply voltage $V_{cc}$ are shown in Table 5.2 [18].

From Table 5.2 it follows that, above the maximum frequency, efficiency can be maximized by proper selection of the series inductance and load resistance when it looks reasonable. For example, at operating frequency $f = 2.512f_{max}$, the collector efficiency of an ideal Class-E mode still high being even higher than that for a Class-F mode with control of three collector voltage and three collector current harmonic components. The collector efficiency of an ideal

**Table 5.2: Suboptimum Operation above Maximum Frequency**

| $f/f_{max}$ | $\omega L/R$ | $V_{max}/V_{cc}$ | $\eta_{max}$, % |
|---|---|---|---|
| 1.000 | 1.152 | 3.562 | 100.00 |
| 1.259 | 1.330 | 3.198 | 99.59 |
| 1.585 | 1.053 | 2.981 | 96.96 |
| 1.995 | 0.852 | 2.789 | 92.16 |
| 2.512 | 0.691 | 2.632 | 85.62 |
| 3.162 | 0.561 | 2.519 | 77.87 |

Class-E power amplifier drops at $f = 3.162 f_{max}$ to the 77.87%, which approximately corresponds to the maximum ideal collector efficiency of an ideal Class-B power amplifier of 78.5%.

The small load variation has no significant effect on the efficiency of an ideal Class-E power amplifier. For example, efficiency varies gradually, remaining at 95% or more for variations in the load resistance $R$ of $+55\%$ to $-37\%$ relative to its optimum value [19]. Generally, the minimum efficiency for a given output *VSWR* (voltage standing wave ratio) decreases almost linearly, as shown in Table 5.3 [20]. For the usual design requirement of operation with *VSWR* $\leq 2$, efficiency is no lower than 89 percent. However, for some load impedance of any specified *VSWR*, it is possible to achieve the maximum collector efficiency of 100%, which is realized at phase angles of the complex reflection coefficient $\Gamma$ equal to $+65^\circ$ and $-115^\circ$. Consequently, the contour of $\eta = 100\%$ on a Smith chart is a straight line. The contours for lower values of efficiency are curved, but symmetrical about the contour of $\eta = 100\%$. These results are very helpful in practical implementation. Since 100% efficiency can be achieved along a line that goes through the center of the Smith chart, a single tuning element is generally sufficient to transform any specified load impedance into an impedance on the line corresponding to $\eta = 100\%$. The specified output power can then be obtained by adjusting the supply voltage.

## 5.3 Matching with Standard Load

For the most practical applications, it is necessary to match the required Class-E optimum load resistance $R$ with a standard load resistance $R_L = 50\,\Omega$. Fig. 5.7($a$) shows the equivalent circuit of a Class-E power amplifier with shunt capacitance where the series $L_0C_0$ filter is followed by an L-type low-pass matching circuit consisting of a series inductor $L_1$ and a shunt capacitor $C_1$ [21]. Such a connection of this matching circuit when its shunt capacitance $C_1$ is connected in parallel to a load resistor $R_L$ assumes that $R < R_L$. This is normally the case for the high-power or low-voltage power amplifiers. The main goal of the matching circuit is to provide a maximum delivery of the output power at the fundamental frequency $\omega_0$ to the

**Table 5.3: Minimum Efficiency for Different *VSWR***

| *VSWR* | $V_{max}/V_{cc}$ | $\eta_{min}$, % |
|---|---|---|
| 1.0 | 3.5621 | 100.00 |
| 1.5 | 3.0133 | 96.00 |
| 2.0 | 2.6814 | 88.88 |
| 2.5 | 2.4449 | 81.63 |
| 3.0 | 2.2615 | 74.99 |

standard load of 50 Ω, since it is assumed that a series $L_0C_0$ filter has sufficiently high $Q$-factor to suppress the harmonic components of the fundamental frequency.

In this case, the Class-E optimum resistance $R$ generally can be defined through the parameters of the L-type low-pass matching circuit and the load resistance as

$$R = \frac{R_L}{1 + (\omega_0 R_L C_1)^2} + j\left[\omega L_1 - \frac{\omega_0 C_1 R_L^2}{1 + (\omega_0 R_L C_1)^2}\right]. \tag{5.37}$$

Since it is necessary to provide the conjugate matching conditions to maximize the output power in the load, the imaginary part of Eq. (5.37) must be equated to zero. Then, Eq. (5.37) can be resolved separately for the real and imaginary parts as

$$R_L = R(1 + Q_L^2) \tag{5.38}$$

$$\frac{1}{\omega_0 C_1} = \omega_0 L_1 (1 + Q_L^{-2}), \tag{5.39}$$

where $Q_L = \omega_0 C_1 R_L = \omega_0 L_1 / R$ is the loaded quality factor that is equal for both the series and parallel circuits at the fundamental frequency.

As a result, the loaded quality factor $Q_L$ can be expressed through the load resistances $R$ and $R_L$ as

$$Q_L = \sqrt{\frac{R_L}{R} - 1}, \tag{5.40}$$

while the matching circuit parameters can be calculated from

$$L_1 = \frac{RQ_L}{\omega_0} \tag{5.41}$$

$$C_1 = \frac{Q_L}{\omega_0 R_L}. \tag{5.42}$$

The series high $Q_L$ filter and L-type matching circuit can be combined into a π-type matching circuit with two shunt capacitors and series $L_2C_2$ circuit where $L_2 = L + L_0 + L_1$ and $C_2 = C_0$, as shown in Fig. 5.7(*b*). Generally, a tandem connection of any type of low-pass or band-pass matching sections can be used for different ratios between a required optimum Class-E load resistance $R$ and a standard load resistance $R_L$. In this case, to simplify the matching design procedure, it is best to cascade the low-pass L-type matching sections with equal values of their $Q_L$ factors [22, 23].

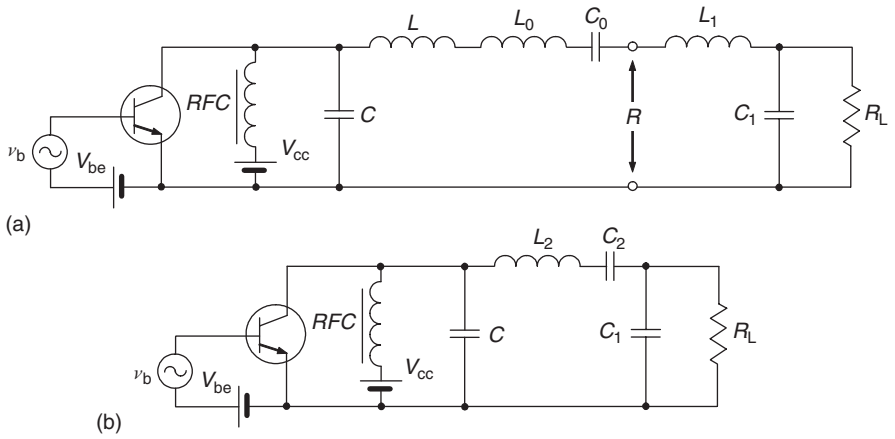



**Figure 5.7: Class-E power amplifiers with matching circuits.**

In the case of monolithic implementation of the Class-E power amplifier, the large value of inductor $L_0$ results in the significant ohmic losses and low self-resonant frequency that is crucial at microwave frequencies. Therefore, to minimize the inductance value of the monolithically implemented spiral inductor, the Class-E load network can represent the alternative topology shown in Fig. 5.8 with optimized second-harmonic peaking and simultaneous impedance transformation at the fundamental frequency [24]. Here, the parallel tank formed by a capacitor $C_2$ and an inductor $L_2$ is designed to resonate at $2f_0$. The net impedance of the second-harmonic resonator must represent an inductive reactance at the fundamental frequency $f_0$ similar to the contribution of an inductance's $L$ in the Class-E load network shown in Fig. 5.7($a$). In this case, it is assumed the capacitive reactances of the parallel tank at the third and higher-order harmonic components are relatively high compared with that provided by the shunt capacitance $C$.

Consequently, by using Eq. (5.31), the design equations for the load network elements $L_2$, $C_1$, and $C_2$ in Fig. 5.8 can be written as

$$L_2 = \frac{3R}{4\omega_0}(Q_L + 1.1525) \tag{5.43}$$

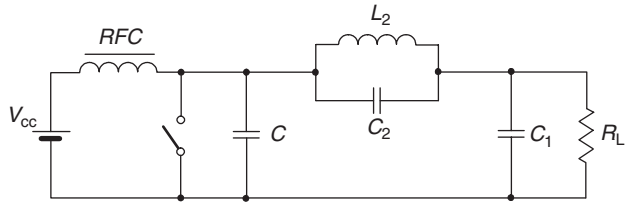



**Figure 5.8: Class-E power amplifier with second-harmonic peaking.**

$$C_2 = \frac{1}{4\omega_0^2 L_2} \tag{5.44}$$

$$C_1 = \frac{Q_L}{\omega_0 R_L}, \tag{5.45}$$

where $Q_L$ is obtained from Eq. (5.40).

## 5.4 Effect of Saturation Resistance

In practical power-amplifier design, especially when a value of the supply voltage is sufficiently small, it is very important to predict the overall degradation of power-amplifier efficiency due to the finite value of the transistor saturation resistance. Fig. 5.9 shows the simplified equivalent circuit of a Class-E tuned power amplifier with shunt capacitance including the on-resistance or saturation resistance $r_{sat}$ connected in series to the ideal switch. To obtain a quantitative estimate of the losses due to the contribution of $r_{sat}$, the saturated output power $P_{sat}$ can be obtained with a simple approximation when the current $i(\omega t)$ flowing through the saturation resistance $r_{sat}$ is determined in an ideal case by Eq. (5.23).

An analytical expression to calculate the power losses due to the saturation resistance $r_{sat}$, which value is assumed constant, can be represented in the normalized form according to

$$\frac{P_{sat}}{P_0} = \frac{r_{sat}}{2\pi I_0 V_{cc}} \int_0^{\pi} i^2(\omega t)\, d(\omega t), \tag{5.46}$$

where $P_0 = I_0 V_{cc}$ is the dc power. As a result, by using a linear approximation of the collector current waveform for the Class-E load network with one inductor and one capacitor which equivalent circuit without saturation resistance $r_{sat}$ is shown in Fig. 5.2(*b*), the averaged dissipated power $P_{sat}$ normalized to the dc power $P_0$ can be evaluated by

$$\frac{P_{sat}}{P_0} = \frac{8}{3} \frac{r_{sat} P_0}{V_{cc}^2} \tag{5.47}$$

for the required dc power and supply voltage [21].

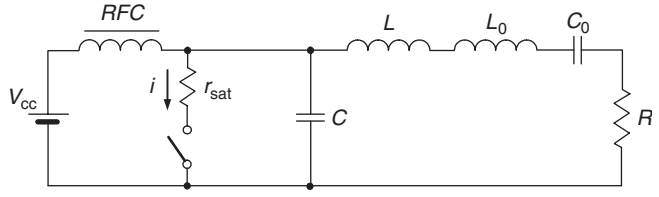



**Figure 5.9: Equivalent Class-E load network with saturation resistance.**

For a Class-E power amplifier with shunt capacitance, which equivalent circuit is shown in Fig. 5.9, by taking into account that

$$\int_0^{\pi} \left(\frac{\pi}{2}\sin\omega t - \cos\omega t + 1\right)^2 d(\omega t) = \frac{\pi}{8}(\pi^2 + 28)I_0^2, \tag{5.48}$$

Eq. (5.46) can be finally rewritten using Eq. (5.25) by

$$\frac{P_{\text{sat}}}{P_0} = \frac{r_{\text{sat}}}{2\pi}\frac{I_0}{V_{\text{cc}}}\frac{\pi}{8}(\pi^2 + 28) = \frac{r_{\text{sat}}}{2R}\frac{\pi^2 + 28}{\pi^2 + 4} = 1.365\frac{r_{\text{sat}}}{R}. \tag{5.49}$$

The collector efficiency $\eta$ can be calculated from

$$\eta = \frac{P_{\text{out}}}{P_0} = \frac{P_0 - P_{\text{sat}}}{P_0} = 1 - \frac{P_{\text{sat}}}{P_0}. \tag{5.50}$$

The presence of the saturation resistance results in the finite value of the saturation voltage $V_{\text{sat}}$ which can be defined from

$$\frac{V_{\text{sat}}}{V_{\text{cc}}} = 1 - \frac{1}{1 + 1.365\frac{r_{\text{sat}}}{R}}, \tag{5.51}$$

being normalized to the dc collector voltage $V_{\text{cc}}$ [25].

In optimum switching mode when both conditions given by Eqs. (5.9) and (5.10) are satisfied, the second optimum condition is equivalent to

$$\left.\frac{di(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0 \tag{5.52}$$

when the collector current at the end of each period must start with zero derivative, since $\nu(\omega t) = r_{\text{sat}}\, i(\omega t)$. Fig. 5.10 shows the collector voltage and current waveforms by solid lines corresponding to an optimum operation mode [9]. Here, the shape of the saturation voltage shown in Fig. 5.10(*a*) is determined by the collector current waveform. However, if the first optimum condition is not satisfied when it can be assumed, for example, some positive value of the collector voltage at the time instant when transistor is turned on, this results in the switching losses accompanied by the proper transient response of the current waveform shown in Fig. 5.10(*b*) by dashed line in the impulse form with a finite amplitude which duration is determined by the time constant $\tau_{\text{s}} = r_{\text{sat}}C$ [26]. In this case, the peak collector voltage reduces compared to the optimal case.

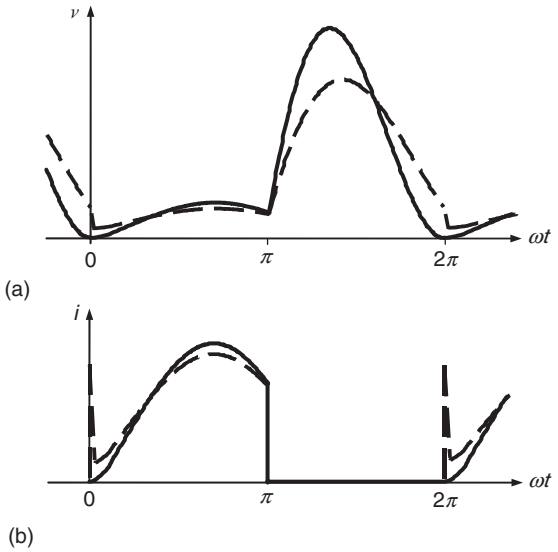



**Figure 5.10: Collector voltage and current waveforms for idealized Class E with saturation resistance.**

More detailed theoretical analysis of the time-dependent behavior of the collector voltage and current waveforms shows that, for a finite value of the saturation resistance $r_{sat}$, the optimum conditions for idealized operation mode given by Eqs. (5.9) and (5.10) do not correspond anymore to the minimum dissipated power losses, and there are optimum nonzero values of the collector voltage and its derivative at switching time instant corresponding to minimum overall power losses [27]. For example, even for small losses with the normalized loss parameter $\omega C r_{sat} = 0.1$ for a duty cycle of 50%, the optimum series inductance $L$ is almost two times greater while the optimum shunt capacitance $C$ is about 20% greater than those obtained under optimum conditions given by Eqs. (5.9) and (5.10). However, for collector efficiencies of 90% and greater, both the optimum inductance and optimum capacitance differ by less than 20% from their optimum values for $r_{sat} = 0$ [26]. It should be noted that, if the first condition is satisfied, the power losses close to minimum can be achieved with zero second condition, since the positive voltage derivative results in positive current jump, which requires greater driving amplitude, while the negative voltage derivative with negative current jump demonstrates reduction in power loss by only 3% [28]. Thus, generally the switching conditions given by Eqs. (5.9) and (5.10) can be considered optimum only for an idealized case of a Class-E load network with zero saturation resistance providing the switched-mode transistor operation when it operates in pinch-off and saturation regions only. However, they can be considered as a sufficiently accurate initial guess for further design and optimization of the real high-efficiency power-amplifier circuits.

Besides the saturation resistance $r_{sat}$, the power losses in the elements of the load network are very important for predicting efficiency of the Class-E power amplifier. The contribution of each circuit element to the overall power loss and drain efficiency was experimentally validated on the example of a 300 W MOSFET Class-E power amplifier developed to operate at a switching frequency of 7.29 MHz and a supply voltage of 130 V with a sinusoidal driving signal [29]. Being calculated at 42.5% duty ratio, the individual component losses of the elements of the equivalent Class-E load network shown in Fig. 5.11 are listed in Table 5.4. An IRFP440 power MOSFET device was used as a switch and its saturation resistance $r_{sat}$ was obtained from the manufacturer data sheet. As a result, the total calculated power loss was 29.3 W resulting in a drain efficiency of 91.1%, which value is very close to the measured drain efficiency of 90.1%. As it was expected, more than 40% in a total power loss is contributed by the power device due to its finite value of the saturation resistance.

## 5.5 Driving Signal and Finite Switching Time

An analysis of the idealized operation of the Class-E power amplifier is based on a preliminary assumption of instant device switching of the saturation mode with zero on-resistance to the pinch-off mode with zero collector current. However, real transistors have non-zero transition times when switching time may be a significant part of the period, especially at high frequencies. In this case, there are different contributions of the non-zero switching conditions during the on-to-off and off-to-on transitions. If the power loss during the off-to-on transition is negligible because the collector voltage drops to zero at the end of pinch-off mode with collector or drain current starting from zero value, the power loss becomes significant during the on-to-off transition since the collector or drain current must decrease instantly to zero from a significant value it has at the end of saturation mode. Physically the finite switching time can be explained by the device inertia when the base charge reduces to zero value with some finite time delay $\tau_s$. Due to the device inertia mostly owing to the time delay in its input circuit, there is an active state, where the collector or drain current is determined by the base or channel charge process, but not by the load network.

The input-port characteristics of bipolar, MOSFET, and MESFET devices are so different that generally a different driver circuit should be used for each type of transistor. The best

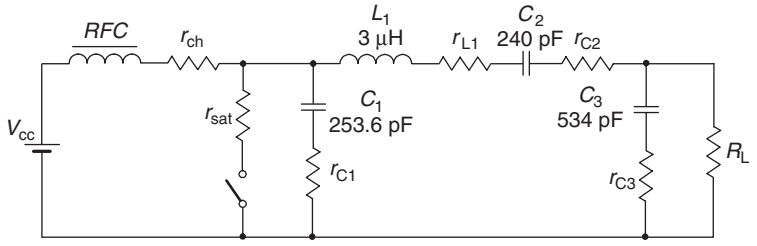



**Figure 5.11: Equivalent Class-E load network with lossy elements.**

**Table 5.4: Component Resistance and Predicted Power Loss**

| Component | Resistance, Ω | Predicted Power Loss, W |
|---|---|---|
| $r_{sat}$ | 0.85 | 12.75 |
| $r_{c2}$ | 0.42 | 6.29 |
| $r_{L1}$ | 0.28 | 4.19 |
| $r_{C3}$ | 0.42 | 3.77 |
| $r_{C1}$ | 0.23 | 1.22 |
| $r_{ch}$ | 0.2 | 1.07 |

gate-voltage drive is a trapezoidal waveform, with the falling transition occupying 30% or less of the period. Shorter transition time is difficult to achieve because of the effect of the device equivalent circuit parameters among which the most important are a gate-resistance $R_g$, a gate-source capacitance $C_{gs}$, and a gate-drain capacitance $C_{gd}$ providing an input time delay $\tau_{in} = R_g(C_{gs} + C_{gd})$. For both MOSFET and MESFET devices, the optimum drive minimizes the sum of the output-stage power dissipation and the driver-stage power consumption. The peak of the drive waveform should be safely below the device maximum gate-source voltage rating. For MESFET devices, it should be less than the gate-source voltage at which the gate-source diode conducts enough current to cause either of two undesired effects:

- Metal migration of the gate metallization at an undesirably rapid rate making the transistor operating lifetime shorter than desired
- Enough power dissipation to reduce the overall efficiency more than the efficiency is increased by the lower dissipation in the lower on-resistance that results from a higher upper level of the drive waveform

The lower level of the trapezoid should be low enough to result in a satisfactorily small current during off-state of the transistor operation. A sine wave is usable approximation to the trapezoidal waveform, although not optimum. To obtain the transistor switching ratio of 50% that is usually the best choice, the zero level of the sine wave should be positioned slightly above the device turn-on threshold voltage. It is a better approximation to remove the part of the sine waveform that goes below the value of the gate-source bias voltage that ensures fully off-state operation, replacing it with a constant voltage at that gate-source bias voltage. This reduces the input drive power by slightly less than 50%, almost doubling the power gain.

Fig. 5.12 shows the simplified equivalent transistor model where both the capacitances $C_{in}$ and $C_{out}$ include the feedback base-collector (or gate-drain) capacitance. Despite the simplification, such a model can describe with sufficient accuracy the behavior of the bipolar, MOSFET, or MESFET device up to approximately $0.1f_T$, where $f_T$ is the transition frequency.

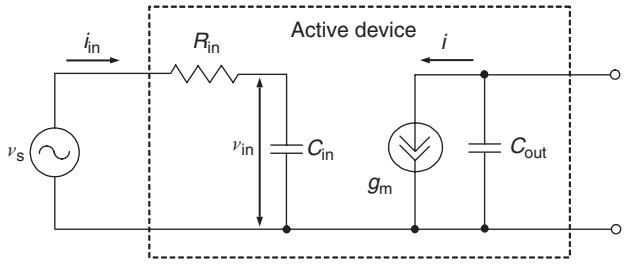



**Figure 5.12: Simplified equivalent transistor model.**

Moreover, for a MOSFET device, the gate-source capacitance varies insignificantly over a wide range of the gate-source bias voltages, whereas the feedback gate-drain capacitance is sufficiently small, normally by an order of less than the gate-source capacitance. Let us assume that the transistor is driven from the signal source with the sinusoidal voltage

$$v_S(\omega t) = V_0 + V_S \sin(\omega t + \psi_0), \tag{5.53}$$

where $V_0$ is the base-emitter or gate-source bias voltage, and $\psi_0$ is the initial phase shift.

For the input transistor circuit, the linear first-order differential equation can be written in the form of

$$\omega C_{in} \frac{dv_{in}}{dt} = \frac{v_S - v_{in}}{R_{in}}. \tag{5.54}$$

Taking into account that $i = g_m v_{in}$, where $g_m$ is the device transconductance (assuming it is constant when device is turned on and is equal to zero when device is turned off), Eq. (5.54) can be rewritten as

$$\frac{di}{d\omega t} + \frac{i}{\omega \tau_{in}} - \frac{V_0 + V_S \sin(\omega t + \psi_0)}{\omega \tau_{in}} = 0, \tag{5.55}$$

whose general solution can be obtained by

$$i(\omega t) = C_0 \exp\left(-\frac{\omega t}{\omega \tau_{in}}\right) + A_1 \sin(\omega t + \psi_0) + A_2 \cos(\omega t + \psi_0) + A_3, \tag{5.56}$$

where $\tau_{in} = R_{in} C_{in}$.

The coefficients $A_1$, $A_2$, and $A_3$ are defined by substituting Eq. (5.56) into Eq. (5.55) and equating the appropriate correct components. Then, by setting the boundary conditions

$i(0) = i(\pi) = 0$ to determine the remaining unknown coefficient $C_0$ and bias voltage $V_0$, we can finally write

$$i(\omega t) = \frac{g_m V_S}{\sqrt{1+(\omega\tau_{in})^2}}\left[\frac{1-2\exp\left(-\frac{\omega t}{\omega\tau_{in}}\right)+\exp\left(-\frac{\pi}{\omega\tau_{in}}\right)}{\exp\left(-\frac{\pi}{\omega\tau_{in}}\right)-1}\right.$$

$$\left.\times\sin(\psi-\psi_0)+\sin(\omega t-\psi+\psi_0)\right], \tag{5.57}$$

where $\psi = \tan^{-1}(\omega\tau_{in})$ is the phase angle. It should be noted that the collector (or drain) current waveforms can be different, depending on the boundary conditions, initial phase shift, and the base-emitter (or gate-source) bias voltage. For example, a 50% duty cycle of the input signal is realized with the bias voltage calculated from

$$V_0 = -\frac{V_S}{\sqrt{1+(\omega\tau_{in})^2}}\frac{1+\exp\left(-\frac{\pi}{\omega\tau_{in}}\right)}{1-\exp\left(-\frac{\pi}{\omega\tau_{in}}\right)}\sin(\psi-\psi_0), \tag{5.58}$$

which can take positive, zero, and negative values when the transistor can be biased for Class-AB, Class-B, or Class-C operation modes, respectively, depending on its input circuit parameters.

The resulting collector (or drain) current waveforms for several values of parameter $\omega\tau_{in}$ are plotted in Fig. 5.13(*b*), for the sinusoidal input voltage with initial phase $\psi_0 = 30^\circ$ shown in Fig. 5.13(*a*). From Fig. 5.13(*b*) it follows that, generally, the collector current waveforms are asymmetrical, and the degree of this asymmetry depends on the input circuit phase angle $\psi$. A more or less symmetrical waveform can be obtained with $\omega\tau_{in} = 0.6$. At higher frequencies, the waveform asymmetry is shifted to the right-hand side, thus contributing to the shorter switching time of the active device. However, the larger value of $\omega\tau_{in}$ (i.e., the time delay due to input *RC* circuit) the smaller output current amplitude with the appropriately smaller fundamental-frequency component resulting in a power gain reduction. The input voltage amplitude $V_{in}$ across the capacitance $C_{in}$ can be defined as a function of frequency by

$$\frac{V_{in}}{V_S} = \frac{1}{\sqrt{1+(\omega\tau_{in})^2}}. \tag{5.59}$$

From Eq. (5.59), it follows that, for the same input capacitance $C_{in}$, the voltage across the capacitance $C_{in}$ reduces with the increase of $R_{in}$ or $\tau_{in}$, thus resulting in a smaller output fundamental current. For zero input resistance $R_{in}$ when there is no power loss in the device input circuit, the power gain is infinite. The input power for a finite value of $R_{in}$ can be calculated from

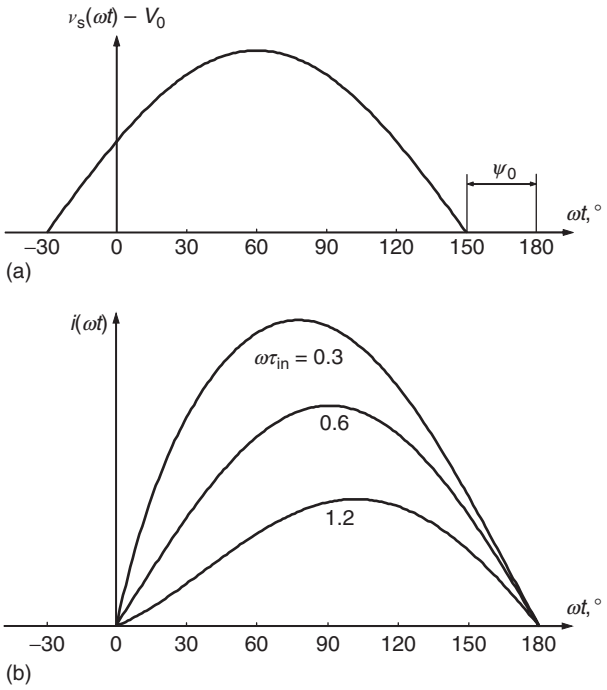



**Figure 5.13: Collector current waveforms versus input parameter $\omega\tau_{in}$.**

$$P_{in} = \frac{I_{in}^2 R_{in}}{2} = \frac{(\omega\tau_{in})^2}{1 + (\omega\tau_{in})^2} \frac{V_S^2}{2R_{in}}, \tag{5.60}$$

where $I_{in}$ equals the input current amplitude.

Generally, the switching time is sufficiently small. Certainly, for an ideal active device without any memory effects due to intrinsic phase delays, the switching time is equal to zero when the rectangular input drive results in a rectangular output response with the required amplitude, as shown in Fig. 5.14(*a*) by curve 1, where curve 2 corresponds to the ideal Class-E collector current waveform. Such an ideal case assumes zero feedback capacitance and zero input resistance $R_{in}$. Otherwise, if $R_{in}$ is not equal to zero, the input low-pass $R_{in}C_{in}$-filter section provides the suppression of high-order harmonics of the fundamental frequency resulting in the finite rising and falling times of the driving rectangular pulse in time domain. This means that, during these finite on-time and off-time operation conditions, an active device cannot be instantly switched from the saturation mode to the pinch-off mode and operates in the active region when simultaneously output current and output voltage are positive with the output power dissipation within the device.

However, in a real situation, especially at higher frequencies, it is very difficult to realize the driving signal close to the rectangular form as it leads to the significant circuit complexity and

requires the minimum device input delay ($R_{in}$ should be as small as possible) and transition frequency $f_T = g_m/2\pi C_{in}$ to be as high as possible ($C_{in}$ should be as small as possible). Fortunately, to realize high-efficiency operation conditions, it is sufficient to drive the power amplifier simply with a sinusoidal signal. The finite-time transition from the saturation mode to the pinch-off mode through the device active mode takes place at the point of the intersection of the curve corresponding to the base (or channel) charge process (curve 1) and the curve corresponding to the required ideal collector current waveform provided by the load network (curve 2), as shown in Fig. 5.14(*b*). To minimize the switching time interval, it is sufficient to slightly overdrive the active device with signal amplitude by 20–30% higher than is required

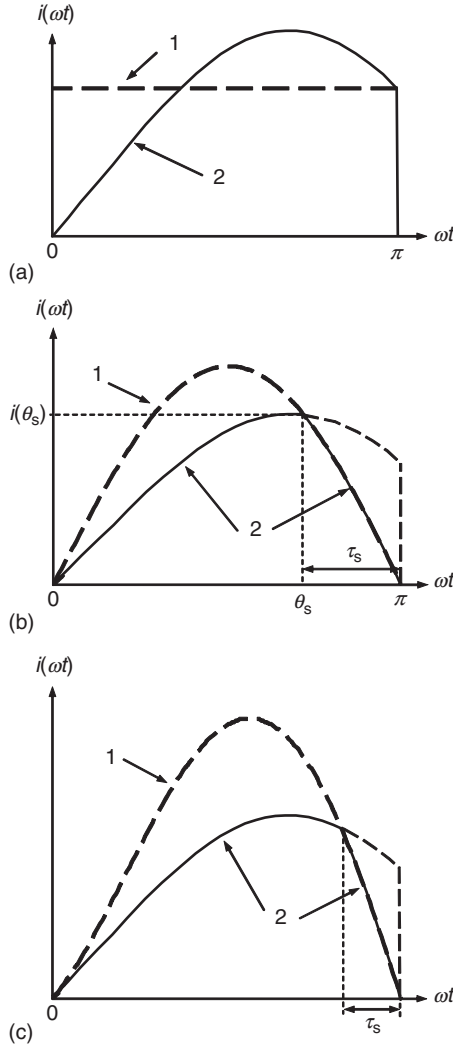



**Figure 5.14: Collector current waveforms due to finite switching time.**

for a conventional Class-B power amplifier, as shown in Fig. 5.14(*c*). As an alternative, the second harmonic component (approximation of a half-sinusoidal waveform) or third harmonic component (approximation of a rectangular waveform with close to trapezoidal waveform) with proper phasing can be added to the input driving signal. In both cases, the overall driving signal amplitude will be increased compared with simply sinusoidal driving signal, thus resulting in a faster switching operation time.

The power dissipated during this on-to-off transition can be calculated assuming zero on-resistance as

$$P_s = \frac{1}{2\pi}\int_{\theta_s}^{\pi} i(\omega t)\, v(\omega t)\, d\omega t, \tag{5.61}$$

where the collector voltage during the transition time $\tau_s = \pi - \theta_s$ is given by

$$v(\theta_s) = \frac{1}{\omega C}\int_{\theta_s}^{\pi} i_C(\omega t)\, d\omega t. \tag{5.62}$$

The short duration of the switching time and the proper behavior of the resulting collector (or drain) waveform allow us to make an additional assumption of a linearly decreasing collector current during fall time $\tau_s = \pi - \theta_s$ starting at $i(\theta_s)$ at time $\theta_s$ and decaying to zero at time $\pi$, which can be written by

$$i(\omega t) = i(\theta_s)\left(1 - \frac{\omega t - \theta_s}{\tau_s}\right), \tag{5.63}$$

where $i(\theta_s)$ corresponds to the peak collector current shown in Fig. 5.14(*b*) [21, 25]. In this case, the capacitor charging current $i_C(\omega t) = i(\theta_s) - i(\omega t)$, being zero during saturation mode, varies linearly between zero and $i(\theta_s)$ during on-to-off transition according to

$$i_C(\omega t) = i(\theta_s)\frac{\omega t - \theta_s}{\tau_s}. \tag{5.64}$$

The collector voltage produces a parabolic voltage waveform during the switching interval according to Eq. (5.62) given by

$$v(\omega t) = \frac{i(\theta_s)}{2\omega C \tau_s}(\omega t - \theta_s)^2. \tag{5.65}$$

As a result, the power dissipated during transition according to Eq. (5.61) is then

$$P_s = \frac{i^2(\theta_s)\tau_s^2}{48\pi\omega C}. \tag{5.66}$$

As a result, for an optimum power amplifier by assuming that, in view of a short transition time, $i(\theta_s) = i(\pi)$, from Eq. (5.23) it follows that $i(\pi) = 2I_0$, hence

$$P_s = \frac{I_0^2\tau_s^2}{12\pi\omega C}. \tag{5.67}$$

Taking into account Eq. (5.35), the switching loss power $P_s$ normalized to the dc power $P_0$ can be obtained from

$$\frac{P_s}{P_0} = \frac{I_0\tau_s^2}{12\pi\omega C V_{cc}} = \frac{\tau_s^2}{12}. \tag{5.68}$$

The collector efficiency $\eta$ can be estimated as

$$\eta = 1 - \frac{P_s}{P_0} = 1 - \frac{\tau_s^2}{12}. \tag{5.69}$$

As follows from Eq. (5.68), the power losses due to the finite switching time are sufficiently small and, for example, for $\tau_s = 0.35$ or $20^\circ$ they are only about 1%, whereas for $\tau_s = 60^\circ$ they are approximately equal to 10%. A more exact analysis assuming a linear variation of the collector current during on-to-off transition results in similar results when efficiency degrades to 97.72% for $\tau_s = 30^\circ$ and to 90.76% for $\tau_s = 60^\circ$ [30]. Considering an exponential collector current decay rather than linear during the fall time shows the similar result for $\tau_s = 30^\circ$ when $\eta = 96.8\%$, but the collector efficiency degrades more significantly at longer fall times when, for example, $\eta = 86.6\%$ for $\tau_s = 60^\circ$ [31].

It should be noted that all these results were obtained for a particular case of the infinite $Q_L$ factor of the series-tuned resonant circuit. However, for the loaded quality factors $Q_L$ having finite and sufficiently small values with the assumption of harmonic distortion in the output signal, the collector efficiency increases by several percent [32]. As a result, in terms of efficiency and linearity, the most desirable range of $Q_L$ is 5 to 10. In terms of practical implementation, the smaller size of the transistor, the lower fall-time angles can be expected and the loaded quality factor becomes of less importance for collector efficiency. For example, by using a 0.6 $\mu$m CMOS device, the lower decay time with the drain efficiency greater by about 10% than that when using a 0.8 $\mu$m CMOS device can be achieved [32]. Similarly, using the 1 $\mu$m $\times$ 150 $\mu$m GaN/AlGaN HEMT device results in the output power of 93 mW and drain efficiency 72% at the operating frequency of 1 GHz, whereas the output power of 130 mW and drain efficiency of 82% can be achieved with the 0.12 $\mu$m $\times$ 100 $\mu$m GaN/AlGaN HEMT device [33].

## 5.6 Effect of Nonlinear Shunt Capacitance

At high operating frequencies close to the maximum switching frequency $f_{max}$, the shunt capacitance $C$ required for an ideal switched-mode operation will be fully represented by the output capacitance of the active device. However, the intrinsic output device capacitance (collector capacitance of a bipolar device or drain-source capacitance of a field-effect transistor) is generally nonlinear. If its contribution to the overall shunt capacitance is significant, it is necessary to take into account the nonlinear nature of this capacitance. Fig. 5.15 shows the equivalent Class-E load network with a nonlinear shunt capacitor $C$.

The nonlinear device capacitance can be represented as a junction capacitance by

$$C(v) = \frac{C_0}{\left(1 + \frac{v}{V_{bi}}\right)^{\gamma}}, \tag{5.70}$$

where $v$ is the reverse voltage over the diode junction, $V_{bi}$ is the built-in potential, $\gamma$ is the junction sensitivity or gradual coefficient ($\gamma = 1/3$ for gradient junction and $\gamma = 1/2$ for abrupt junction), and $C_0 = C(0)$ is the collector capacitance at $v = 0$, which can be defined through the supply voltage $V_{cc}$ as

$$C(0) = C(V_{cc})\left(1 + \frac{V_{cc}}{V_{bi}}\right)^{\gamma}. \tag{5.71}$$

The nonlinear capacitance has an effect only during the time period when the transistor is turned off. Therefore, the collector current during the time period when the transistor is turned on can be determined by Eq. (5.23). Then, the collector voltage due to the current flowing through the nonlinear capacitance

$$i_C(\omega t) = \omega C(v)\frac{dv(\omega t)}{d\omega t} \tag{5.72}$$

can be calculated by substituting Eq. (5.70) and Eq. (5.16) into Eq. (5.72) and integrating both its parts as

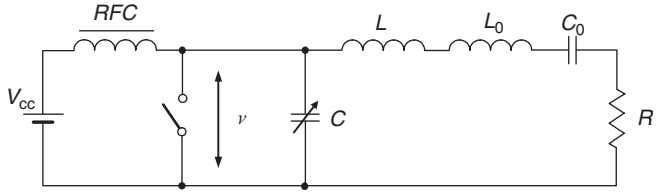



**Figure 5.15: Equivalent Class-E load network with nonlinear shunt capacitance.**

$$\int_0^v \frac{C_0}{\left(1+\frac{v}{V_{bi}}\right)^{\gamma}}\,dv = \frac{1}{\omega}\int_{\pi}^{\omega t} i_C(\omega t)\,d\omega t. \tag{5.73}$$

As a result,

$$\frac{V_{bi}}{1-\gamma}\left[\left(1+\frac{v}{V_{bi}}\right)^{1-\gamma}-1\right] = \frac{I_0}{\omega C_0}\left(\omega t-\frac{3\pi}{2}-\frac{\pi}{2}\cos\omega t-\sin\omega t\right) \tag{5.74}$$

or

$$v = V_{bi}\left\{\left[\frac{I_0}{\omega C_0}\frac{1-\gamma}{V_{bi}}\left(\omega t-\frac{3\pi}{2}-\frac{\pi}{2}\cos\omega t-\sin\omega t\right)+1\right]^{\frac{1}{1-\gamma}}-1\right\}. \tag{5.75}$$

Since the optimum load phase angle, dc current, and output voltage are not affected by the capacitance nonlinearity [34], Eq. (5.74) can be rewritten by using Eq. (5.35) as

$$\frac{V_{bi}}{1-\gamma}\left[1+\frac{v}{V_{bi}}-\left(1+\frac{v}{V_{bi}}\right)^{\gamma}\right] = V_{cc}\pi\left(\omega t-\frac{3\pi}{2}-\frac{\pi}{2}\cos\omega t-\sin\omega t\right), \tag{5.76}$$

which represents a nonlinear algebraic equation with respect to the collector voltage $v(\omega t)$ for any type of the device junction. For abrupt diode junction with $\gamma = 0.5$, it can be simplified to the quadratic equation and solved analytically. The optimum small-signal value of the shunt capacitance $C_0$ can then be calculated from Eq. (5.70) by taking into account Eqs. (5.32) and (5.33).

Fig. 5.16 shows the difference between the collector voltages of a circuit with nonlinear capacitance (dotted waveform) and one with linear capacitance (solid waveform). The nonlinear nature of this capacitance must be taken into account when specifying the breakdown voltage of the transistor. For example, the collector voltage waveform will rise in the case of the shunt capacitance described by abrupt diode junction in comparison with the linear capacitance, and its maximum voltage can be greater by about 20% for a 50% duty cycle [9, 34]. However, stronger nonlinearity of the shunt capacitance causes the peak voltages to be higher [35]. At the same time, the deviations of the optimum load network parameters are insignificant, less than 5% in a wide range of supply voltages. Since the nonlinear capacitance is largest at zero voltage, the collector waveform will rise more slowly than in the linear case. As the collector voltage increases, the capacitance will decrease, and hence the voltage should begin to rise more quickly than in the linear case. If the shunt capacitance consists of both nonlinear and linear capacitances, the collector voltage waveform is intermediate (dashed waveform) and located between the two extreme cases of entirely

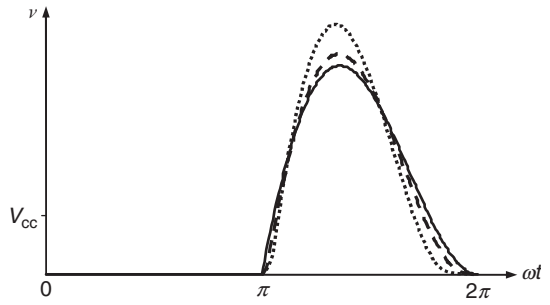



**Figure 5.16: Collector voltage waveforms due to nonlinear shunt capacitance.**

nonlinear or linear capacitance [36]. In some cases when the manufacturer provides with the device intrinsic capacitances at a specified bias value, the output capacitance can be considered an equivalent linear shunt capacitance specified at the operating bias point and expressed as a function of the supply voltage [37].

## 5.7 Push-Pull Operation Mode

The push-pull configuration offers a possibility of combining powers from two power amplifiers to obtain a larger overall output power. The switched-mode tuned power amplifiers can also be configured to operate in a push-pull mode. The simplest way is to use a push-pull power amplifier with resistive load by adding either a series or a parallel LC circuit. In a push-pull power amplifier shown in Fig. 5.17(*a*), the rectangular pulses of voltage $V_{cc} \pm V_{cc}$ drive the series resonant LC circuit. Therefore, it is called a switched-mode tuned power amplifier with switching voltage. In a push-pull power amplifier shown in Fig. 5.17(*b*), the rectangular pulses of current $I_0 \pm I_0$ drive the parallel resonant LC circuit. Therefore, it is called a switched-mode tuned power amplifier with switching current.

With high-$Q_L$ resonant circuits tuned to the fundamental frequency, these power amplifiers operate as switched-mode Class-D power amplifiers with a sinusoidal load current. However, when the low-$Q_L$ resonant LC circuit shown in Fig. 5.17(*b*) is mistuned to the frequency of about $1.5f_0$, where $f_0$ is the fundamental frequency, the collector voltage waveform will resemble the typical Class-E collector waveform with zero voltage and zero voltage-derivative conditions [26]. In this case, the load current will not contain even harmonics of the fundamental frequency. However, to provide a purely sinusoidal load current, the remaining third and higher-order harmonic components can be eliminated by using an additional high-$Q_L$ filter tuned to the fundamental frequency.

Fig. 5.18 shows the push-pull configuration of an optimally tuned Class-E power amplifier with a series-resonant filter representing an open-circuit for harmonic components of the fundamental frequency, where the input transformer provides the device driving

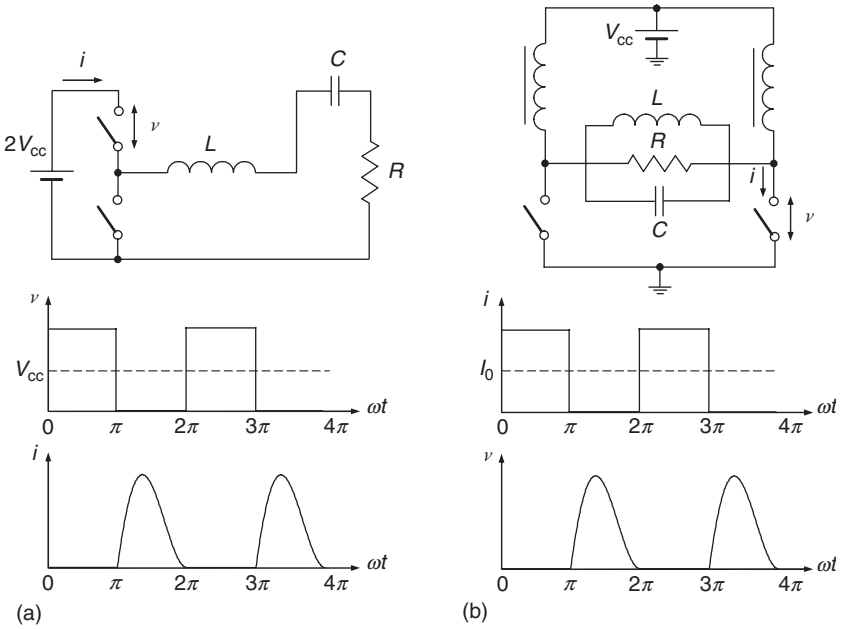



**Figure 5.17: Basic circuits of push-pull switched-mode power amplifiers.**

signals with opposite phases [13, 38]. Each device, however, operates as if it were a single-ended Class-E power amplifier. When a given transistor is driven on, it provides a ground connection on the primary winding of the output transformer, causing the dc current and transformed sinusoidal output current to charge the capacitor shunting the other transistor. The dc power is supplied to the switching devices through the center tap of the primary winding of the output transformer. The voltage appearing on the secondary winding of the output transformer contains both positive and negative Class-E collector-voltage waveforms. Consequently, it has a fundamental-frequency component that has twice the amplitude of the fundamental-frequency component of either collector waveform. The resulting impedance seen by either half of the power amplifier looking into primary winding of the output transformer depends on the squared ratio between the number of turns of the primary winding and the secondary winding. The sinusoidal load voltage will be shifted in phase relative to the collector voltage by the same phase shift as for the case of a single-ended Class-E power amplifier.

The push-pull Class-E power amplifier can be designed based on a balanced circuit topology with symmetrical Class-E load networks with shunt capacitances, connected to a common load. Fig. 5.19(*a*) shows a bipolar push-pull Class-E power amplifier with series load resistor [39]. Here, both bipolar transistors operate as switches with opposite 180° phases to each other when the even harmonics can be significantly suppressed in the load resistance. To provide the transition from balanced-to-unbalanced load, an additional transformer or balun can be used.

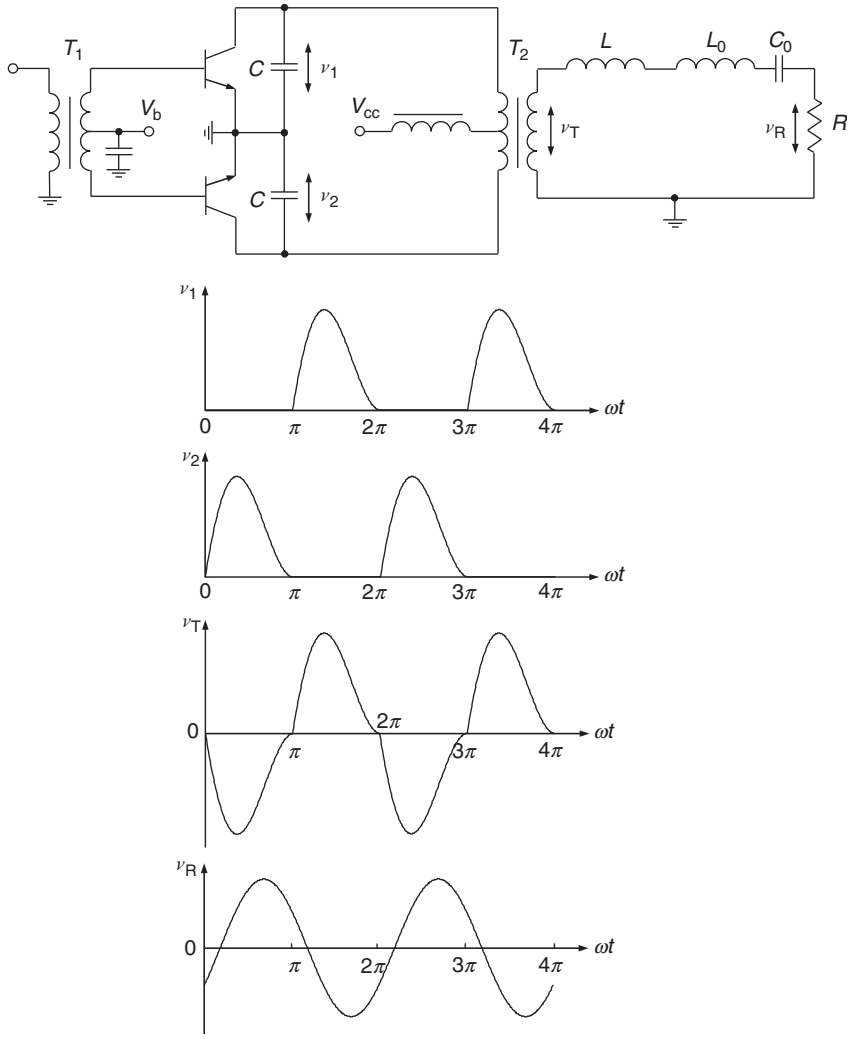



**Figure 5.18: Basic concept of Class-E push-pull operation.**

Being designed to operate at a carrier frequency of 100 kHz with a 50% duty cycle using two bipolar transistors MRF559, such a push-pull Class-E power amplifier achieved power-added efficiency of 82.2% with an output power of 1.89 W at a supply voltage of 5 V.

A symmetrically driven push-pull Class-E power amplifier using high-power MOSFET devices is shown in Fig. 5.19(*b*) [40]. In this circuit, the load resistance is connected in parallel to the series capacitance. For a symmetrically driven Class-E power amplifier, the switches are driven on and off within each of the half-operating period. The duty ratio of the switches is adjusted to realize zero voltage and zero voltage-derivative conditions. However, the optimum Class-E operation mode can only be maintained for relatively low loaded quality factors

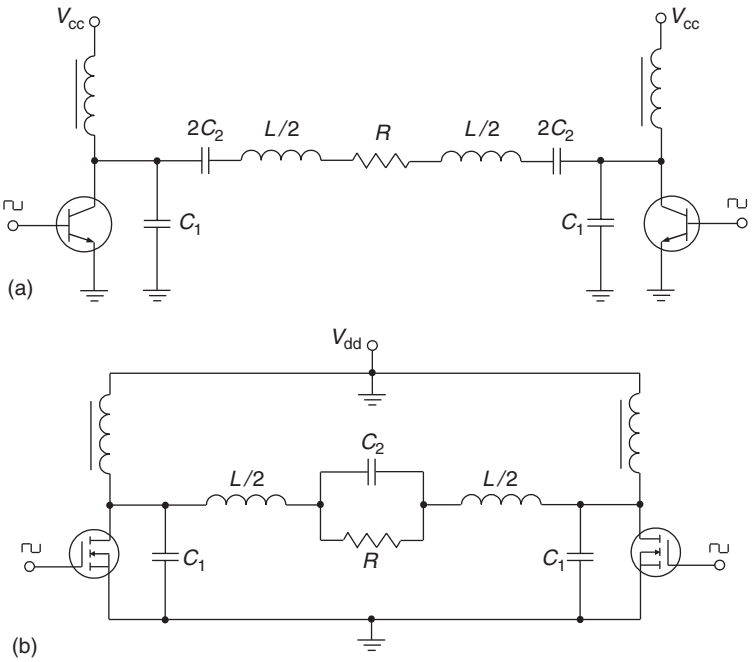



**Figure 5.19: Symmetrically driven push-pull Class-E power amplifiers.**

below 2, which is a design constraint for this symmetrically driven push-pull Class-E power amplifier. Although the use of low $Q_L$ factors has an advantage of low component stress, the harmonic content of the output signal may be significant. As a result, the measured drain efficiency of about 85% with a $Q_L$ factor of 1.9 was achieved within the ranges of output power from 30 to 150 W and supply voltages from 15 to 32 V at a switching frequency of about 1 MHz. Note that, in view of the non-zero device saturation voltage, the zero voltage and zero voltage-derivative conditions are not optimum to provide maximum operating efficiency.

At microwave frequencies, push-pull Class-E power amplifiers can be designed by using transmission-line power dividers and combiners. Fig. 5.20(*a*) shows the circuit schematic of a monolithic *X*-band push-pull pHEMT power amplifier including the input power divider and output power combiner based on slotlines and coplanar waveguides [41]. The input balun separates the input signal into two differential signals that are 180° out-of-phase, while the output balun is reverse-oriented to the input one. The input matching and output matching circuits consist of the series coplanar waveguides providing inductive impedances and shunt coplanar waveguides providing capacitive reactances at the fundamental frequency. The Class-E load network, which is followed by the output matching circuit, includes the internal device shunt capacitance and part of the series coplanar

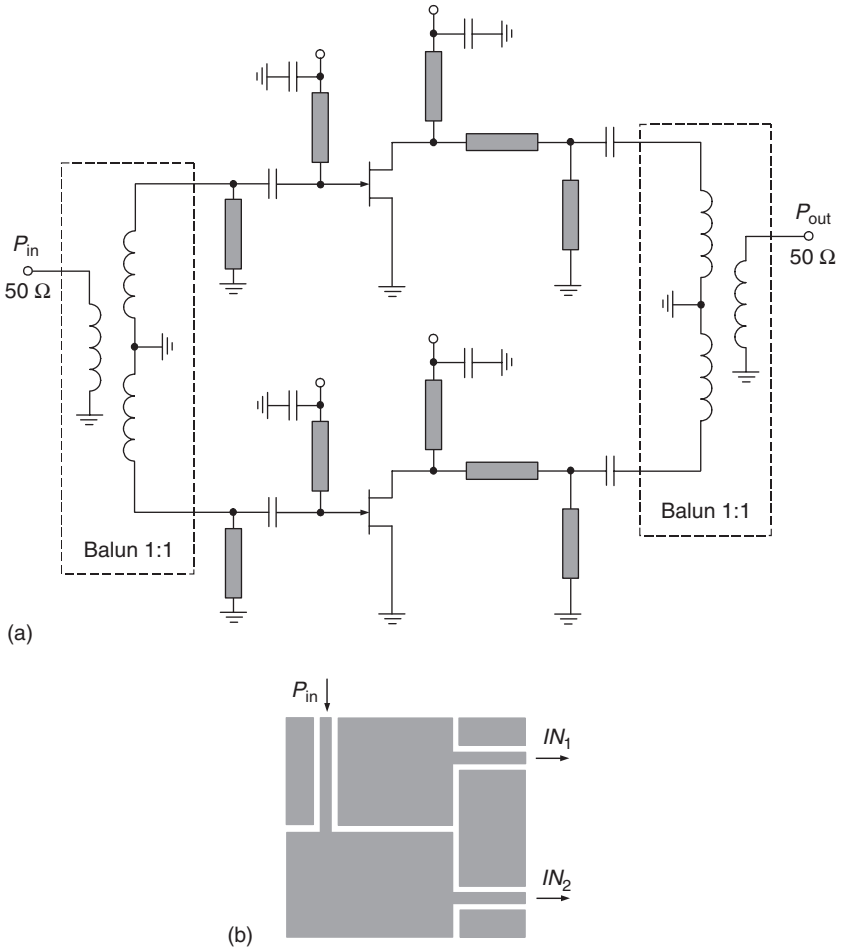



**Figure 5.20: Microwave push-pull Class-E power amplifier.**

waveguide. The input transmission-line balun shown in Fig. 5.20(*b*) provides first the balanced-to-unbalanced signal transformation by transition from the waveguide coplanar with left open-circuit end to slotline, then followed by the slotline *T*-junction, and finally connected to the two differential paths based on the coplanar waveguides with open-circuit terminations at each of their ends. The *X*-band power amplifier based on these baluns with broadband performance and compact size and pHEMT transistors with gate geometry of $0.3\,\mu\text{m} \times 600\,\mu\text{m}$ can achieve power-added efficiency close to 60% in a frequency band of 9 to 10 GHz with output powers of several hundred miliwatts.

## 5.8 Load Network with Transmission Lines

At ultrahigh and microwave frequencies, transmission lines are often preferred over lumped inductors because of the convenience of their practical implementation, more predictable performance, less insertion loss, and less effect of parasitic elements. For example, the matching circuit can be composed with any types of transmission lines including open-circuit or short-circuit stubs to provide the required matching and harmonic-suppression conditions. In this case, to approximate the idealized Class-E operation mode of the microwave power amplifier, it is necessary to design the transmission-line load network satisfying the required idealized optimum impedances at the fundamental-frequency and harmonic components. Generally, the device output capacitance can represent the required shunt capacitance which optimum value is defined by Eq. (5.32). Consequently, the main problem is to satisfy the optimum requirements on the fundamental-frequency impedance $Z_L(\omega_0)$ shown in Fig. 5.21($a$) and harmonic component impedances $Z_L(n\omega_0)$ shown in Fig. 5.21($b$), which are expressed by using Eq. (5.31) at fundamental frequency $f_0$ as

$$Z_L(\omega_0) = R + j\omega L = R\left(1 + j\frac{\omega L}{R}\right) = R(1 + j\tan 49.052^\circ) \tag{5.77}$$

and at harmonic components $nf_0$, where $n = 2, 3, \ldots, \infty$, as

$$Z_L(n\omega_0) = \infty. \tag{5.78}$$

Generally, it is practically impossible to realize these conditions for an infinite number of harmonic components by using only transmission lines. However, as it turned out from the Fourier-series analysis, a good approximation to Class-E mode can be obtained with the dc, fundamental-frequency, and second-harmonic components of the voltage waveform across the switch [15, 42]. The drain efficiency will be the same as that of a maximum-efficiency Class F with second-harmonic control [43]. Fig. 5.21($c$) shows the collector (drain) voltage waveform containing these two harmonic components (dotted line) plotted along with an ideal voltage waveform (solid line). In this case, the Class-E load network designed for microwave applications will include the series microstrip line $l_1$ and open-circuit stub $l_2$, as shown in Fig. 5.22($a$). The electrical lengths of lines $l_1$ and $l_2$ are chosen to be about 45° at the fundamental frequency to provide an open-circuit condition seen from the device output at the second harmonic, according to Eq. (5.78). Their characteristic impedances are calculated to satisfy the required inductive-impedance condition at the fundamental frequency given by Eq. (5.77). In the case of a packaged active device, its output lead inductance can be accounted for by shortening the length of $l_1$.

In some cases, a value of the device output capacitance exceeds the required optimum value for a Class-E mode with shunt capacitance. In this situation, it is possible to approximate Class-E mode with high efficiency by setting an adequate optimum load at the fundamental frequency

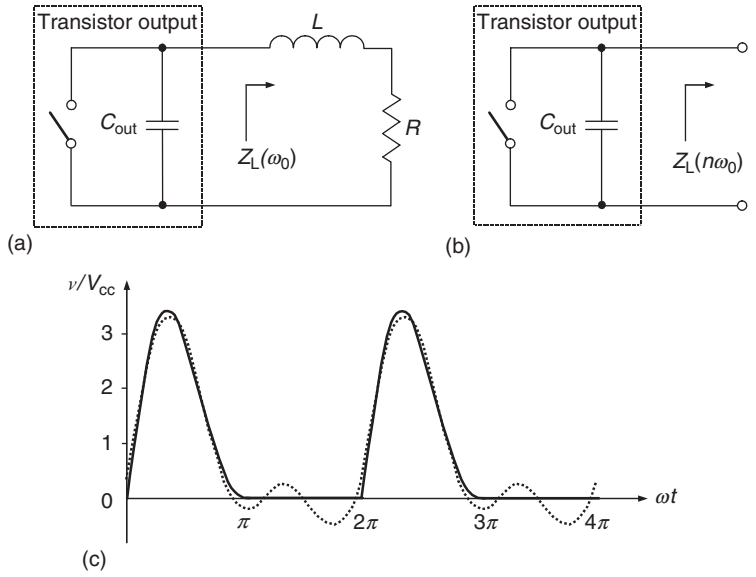



**Figure 5.21: Optimum load impedance and two harmonic Class-E voltage waveform.**

and strongly reactive load at the second and third harmonic components [44]. Such a harmonic-control network consists of open-circuit quarter-wave stubs at the second and third-harmonic components separately, as shown in Fig. 5.22(*b*), where the third-harmonic quarter-wave stub is located before the second harmonic quarter-wave stub. As a result, very high collector efficiency can be achieved even with values of the device output capacitance higher than is conventionally required at the expense of lower output power, keeping the load at the second and third harmonics strictly inductive. A collector efficiency of over 90% with output power of 1.5 W for a test power amplifier using the commercial bipolar transistor MRF557 was measured at a carrier frequency of 900 MHz.

An analysis of an optimum Class-E mode in the frequency domain shows that the combined effect of the saturation resistance $r_{sat}$ and second-harmonic loading is characterized by a shift of the optimum load fundamental-frequency impedance [45]. Besides, parasitic effects due to packaging and microstrip junction discontinuities may upset the transmission-line open-circuit requirement. Therefore, it is practically important to predict the power-amplifier performance due to non-ideal harmonic terminations. For example, the voltage peak factor increases when the second-harmonic load varies from capacitive to inductive, and excessive current flow can be realized under capacitive load reactance. It appears that, while a capacitive second-harmonic load achieves higher output power, an inductive second-harmonic load provides better efficiency. In this case, to approximate a switched-mode Class-E operation mode, the maximum collector efficiency with lower output power is achieved for nonzero collector voltage and negative collector voltage-derivative conditions [46]. Generally, by providing the

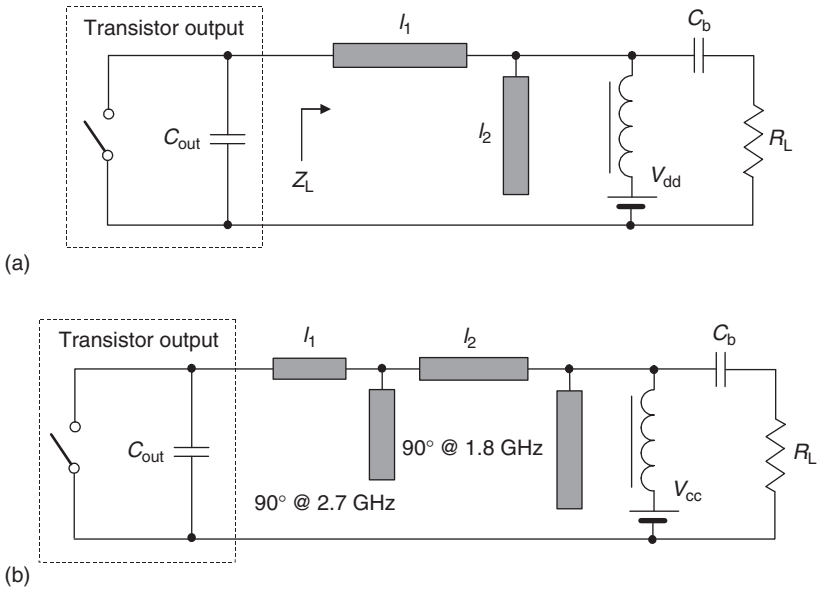



**Figure 5.22: Equivalent circuits of Class-E power amplifiers with transmission lines.**

open-circuit termination of the second- and third-harmonic components, the collector efficiency can be increased by 10% [47]. The variation of the second-harmonic load reflection coefficient by 10% in magnitude from 1 to 0.9 and $\pm 20^\circ$ in phase angle results in an insignificant efficiency variation of only 1%.

The resultant transmission-line topology of the Class-E load network including also the matching properties can be designed based on a lumped circuit prototype [48]. The design procedure includes the following steps:

1. Calculation of the optimum Class-E load network parameters (shunt capacitance $C$, series inductance $L$ and load resistance $R$) based on the specified supply voltage $V_{cc}$ and power delivered to the load $P_L$.

2. Design of the lumped-element circuit to match the optimum load resistance $R$ with standard load resistance of $50\,\Omega$ at the fundamental frequency, also providing the adequate harmonic suppression.

3. Transformation of the lumped-element circuit into a transmission-line circuit carefully observing the impedances at the higher harmonics.

4. Circuit simulation to validate its operation and component parameters to obtain Class-E approximation.

5. Transformation of the transmission-line equivalent circuit into a distributed microstrip layout.

Fig. 5.23(*a*) shows the lumped-element Class-E load network with impedance transformation for a 1-GHz power amplifier delivering 1 W to a 50 Ω resistive load. It is assumed that the MESFET device has a saturation resistance of 1 Ω and output shunt capacitance of around 2 pF. Taking into account the drain breakdown voltage of 15 V, the maximum supply voltage would be limited to $V_{max} = 15/3.562 = 4.2$ V according to Eq. (5.27). In this case, to achieve an output power of 1 W, an ideal value of $R = 0.5768 \times (4.2)^2 = 10\,\Omega$ is required according to Eq. (5.33). The inductive reactance $X = \omega L = 11.5\,\Omega$ is chosen providing a load phase angle 49.052°. The required switch shunt capacitance is $C = 0.1836/(2 \times \pi \times 10) = 2.92$ pF according to Eq. (5.32). To achieve the required impedance transformation from 10 Ω to 50 Ω, and to provide a satisfactory harmonic suppression in the load, a two-stage cascaded low-pass L-type transformer was chosen. The first *L*-section transforms from 10 Ω to 22 Ω, and the second stage transforms from 22 Ω to 50 Ω.

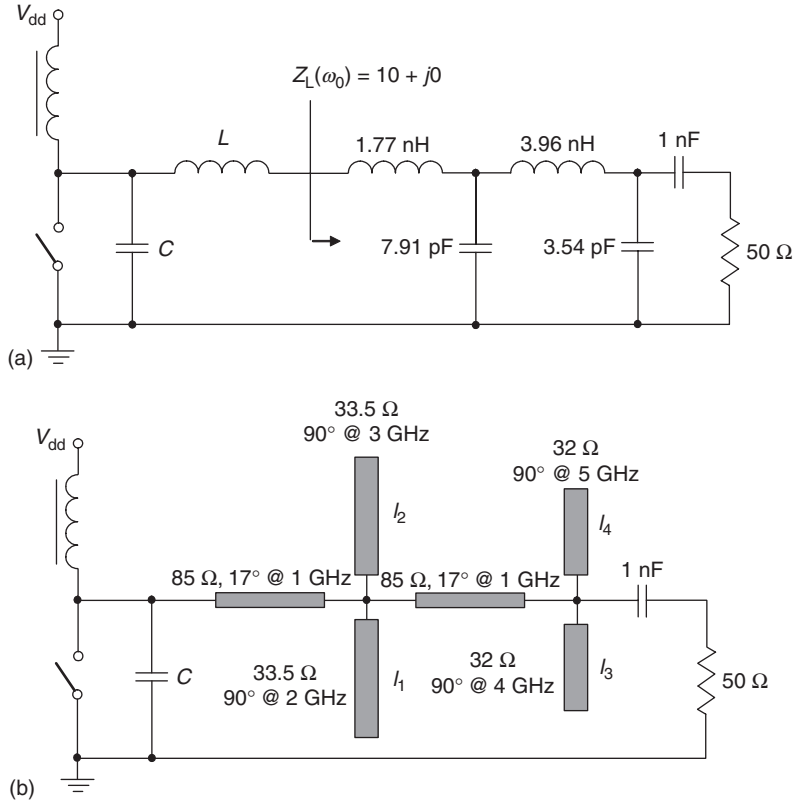



**Figure 5.23: Equivalent circuits of Class-E power amplifiers with transmission lines.**

The conversion of the lumped-element circuit involves replacing the series inductances and shunt capacitances with equivalent transmission-line elements. The series inductances can be realized by short sections with electrical length $\theta \leq \lambda/8$ of a high-impedance line according to $L = (Z_0 \tan\theta)/\omega$, where $Z_0$ is the characteristic impedance of the line, while shunt capacitances are replaced by low-impedance open-circuit stubs with electrical length of $\theta \leq \lambda/8$ according to $C = \tan\theta/(\omega Z_0)$ [23]. The electrical parameters of the capacitive stubs (characteristic impedance and electrical length) can be optimized to provide simultaneously the correct reactance at the fundamental frequency $f_0$, and provide enhanced suppression of harmonics reaching the load by arranging the stub lengths to have low input impedance at selected harmonics, i.e., short circuiting these harmonics to ground. This is achieved by choosing the stub length such that its electrical length is exactly 90° at the particular harmonic one would like to suppress. The characteristic impedance of the stub is then chosen to provide the desired capacitive reactance at the fundamental frequency.

Fig. 5.23(*b*) shows the resultant transmission-line topology of a 1-GHz Class-E power amplifier where each shunt capacitor is replaced by two stubs, providing for harmonic suppression at four frequencies [48]. The capacitive stubs were chosen to have an electrical length of 90° at frequencies $2f_0$, $3f_0$, $4f_0$, and $5f_0$. Table 5.5 lists the first three frequencies suppressed by each of the four harmonic stubs. By using a printed circuit board with a relative dielectric permittivity of 2.2, a loss tangent of 0.009 at 10 GHz, and dielectric thickness of 0.381 mm for microstrip realization of this Class-E load network, a drain efficiency of 72% at 950 MHz with an output power of 458 mW and a harmonic suppression of more than 40 dB at a drain supply voltage of 3.53 V were achieved. The equivalent output capacitance of the MESFET ATF8140 was approximately 2.5 pF, which is 0.6 pF less than the required switch capacitance of 3.1 pF. The additional 0.6 pF capacitance was made up of two short capacitive stubs attached at the point where the device drain is connected to the load network.

For a packaged high-power transistor with large output capacitance, additionally a series capacitor can be used to compensate for the package parasitic inductance followed by the shunt short-circuited transmission line, which is required to compensate for excessive device output capacitance [49]. In this case, power-added efficiency of 73.6% and power gain of

**Table 5.5: First Three Frequencies Suppressed by Each of Four Harmonic Stubs**

| Harmonic Stub | Suppressed Frequency | | |
|---|---|---|---|
| $l_1$ | $2f_0$ | $6f_0$ | $10f_0$ |
| $l_2$ | $3f_0$ | $9f_0$ | $15f_0$ |
| $l_3$ | $4f_0$ | $12f_0$ | $20f_0$ |
| $l_4$ | $5f_0$ | $15f_0$ | $25f_0$ |

14.8 dB were measured at an output power of 39.1 dBm for a 1-GHz LDMOSFET Class-E power amplifier using Motorola MRF282 device biased with a gate voltage of 3.2 V and drain voltage of 21.4 V.

## 5.9 Practical RF and Microwave Class-E Power Amplifiers and Applications

High output power with very high operation efficiency can be easily achieved in Class-E mode by using high-voltage power MOSFET devices at sufficiently low frequencies. Fig. 5.24 shows the circuit schematic of a 13.56-MHz 400-W Class-E power amplifier providing a drain efficiency of 82% with an input drive of 12 W at a supply voltage of 120 V [50]. The series inductor $L_s$ and capacitor $C_s$ form the resonant network that produces the rising and falling voltage waveform required for a Class-E operation. The series tank circuit at the load composed of a capacitor $C_1$ and an inductor $L_1$ is a trap for the second-harmonic component, which contributes to the overall level of harmonic suppression of more than 40 dB below the carrier. Since at the fundamental frequency this second-harmonic resonant circuit represents a capacitive reactance, together with a part of the series inductance $L_s$ it transforms the standard load of 50 Ω to around 13 Ω required for an optimum Class-E mode. The impedance of the gate is small with a real part of about 3 Ω and an inductive reactance of about 4 Ω. The input transformer with a voltage transformation ratio of 6:1 is used to step up from the input gate impedance to the driving source impedance of 50 Ω. This transformer also sets the dc gate bias to zero volts and ensures the transistor is turned off when it is not driven, as this is far below the threshold voltage of 4 V. The capacitor $C_g$ with the variable inductor $L_g$ is used to compensate for the input inductive reactance of the transistor, providing an input voltage standing wave ratio (*VSWR*) of 1.6:1.

Fig. 5.25 shows the circuit schematic of a 27.12-MHz 500-W Class-E MOSFET power amplifier with a drain efficiency of 83% at a supply voltage of 125 V [51]. The input ferrite transformer provides the 2:1 transformation voltage ratio to match the gate impedance, which is represented by the parallel equivalent circuit composed of a capacitance of 2200 pF and a resistance of 210 Ω. Use of the external parallel resistor of 25 Ω simplifies the matching procedure and improves the amplifier stability conditions. The transformer secondary winding provides an inductance of 19 nH, which is required to compensate for the device input capacitance at the operating frequency. High-quality factor passive components are necessary for use in the L-type output network. The quality factor of the bare copper wire inductance was 375. The series blocking capacitor consists of three parallel disc ceramic capacitors. To realize Class-E operation with shunt capacitance, it is sufficient to be limited to only the output device capacitance with a value of 125 pF. This is just slightly larger than that required to obtain the optimum drain voltage and current Class-E waveforms.

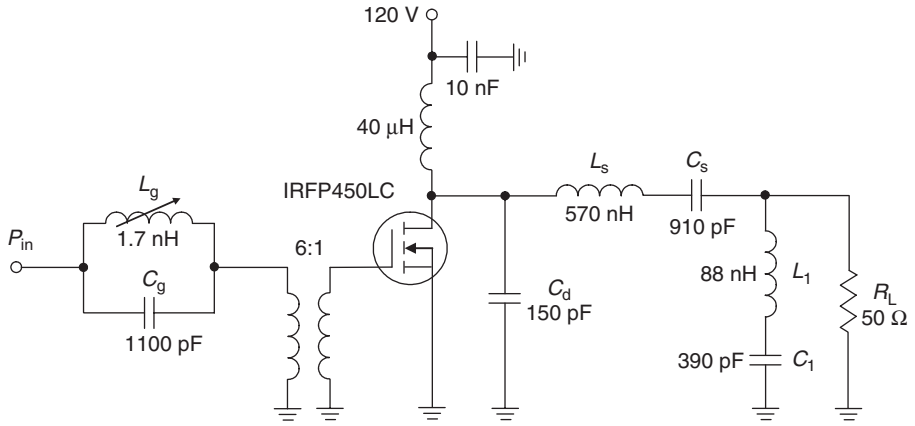



**Figure 5.24: High power 13.56-MHz Class-E MOSFET power amplifier [50].**

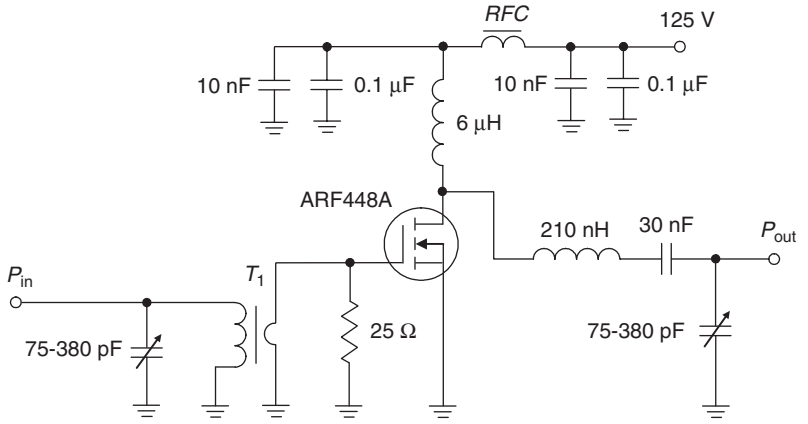



**Figure 5.25: High power 27.12-MHz Class-E MOSFET power amplifier [51].**

Silicon LDMOSFET devices made it possible in Class-E operation to achieve a high output power level with sufficiently high efficiency at higher frequencies. By using a Motorola MRF183 device, it is possible to achieve a drain efficiency of 70% for maximum output power of 54 W at operating frequency of 144 MHz when the input drive is set to 5 W [52]. The drain efficiency can be increased to 88% if the output power level is reduced to 14 W by an appropriate increase of the series inductance in the load network. The simplified circuit schematic of such a high power LDMOSFET amplifier is shown in Fig. 5.26. The input-device impedance is sufficiently low; therefore, a ferrite transformer and a series inductance are used at the input. At the output, the standard load impedance of 50 Ω is transformed to the load resistance of 1.5 Ω required for an optimum Class-E mode by a lumped elements *L*-transformer with a series inductance and a shunt capacitance of 100 pF. The series inductance is included with

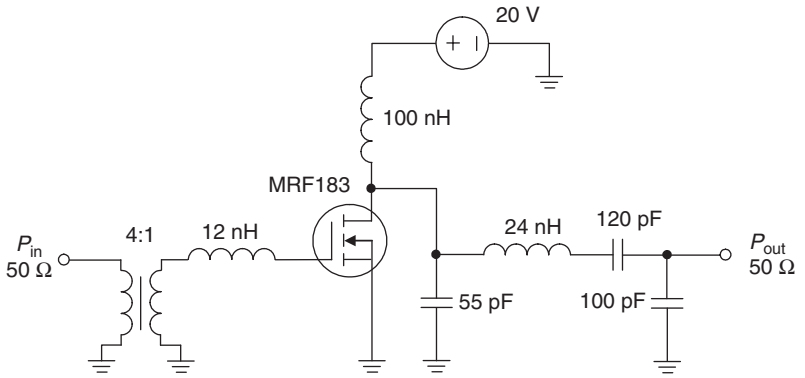



**Figure 5.26: High-power 144-MHz Class-E LDMOSFET power amplifier [52].**

the inductance of 24 nH. The required value of a shunt switching capacitance is provided by the values of the intrinsic device output capacitance of 38 pF and external capacitance of 55 pF. The loaded quality factor of the resonant circuit was chosen at about five, being sufficiently low, to provide some frequency bandwidth operation and to reduce the sensitivity of amplifier performance to the values of resonant circuit elements. To reduce the loss in the load network, the inductor was fabricated by using a 5-mm wide copper ribbon that provides the inductor quality factor of 150–250, depending on the distance to the ground plane. By inserting a spacer between the ribbon and the ground plane, the inductance can be tuned at least by a factor of two.

A transmission-line Class-E power-amplifier topology is shown in Fig. 5.27. The electrical lengths of microstrip lines $l_3$ and $l_4$ in the load network must be close to 45° so that an approximate open circuit at the second harmonic will be presented to the switch shunt capacitor, which is an equivalent output-device capacitance. Microstrip lines with the characteristic impedances of 50 Ω each were fabricated using a substrate with thickness of 2.54 mm and dielectric permittivity $\varepsilon_r = 10.5$. For a Siemens CLY5 MESFET device having a drain-source capacitance $C_{ds} = 2.4$ pF, a power-added efficiency of 80% was achieved at 0.5 GHz with output power of 0.55 W [42]. In this case, the electrical lengths of microstrip lines are $l_1 = 73°$, $l_2 = 79°$, $l_3 = 58°$, $l_4 = 46°$. The power-added efficiency remains above 75% over a 10% bandwidth and above 50% over a 26% bandwidth. Moreover, a power-added efficiency of 73% can be realized at 1.0 GHz with output power of 0.94 W. Using a Fujitsu FLK052WG MESFET makes it possible to use a Class-E power amplifier at higher frequencies [15]. Such a power amplifier can deliver the output power of 0.61 W, 1-dB compressed power gain of 7.6 dB, drain efficiency of 81%, and power-added efficiency of 72% at 5 GHz. The power amplifier was fabricated on a substrate with thickness of 0.508 mm and $\varepsilon_r = 2.2$. As a result, the lengths of 50 Ω microstrip lines (1.6 mm wide) are 9 mm for $l_1$, 1.8 mm for $l_2$, 5.3 mm for $l_3$, and 6.2 mm for $l_4$, respectively. The power-added

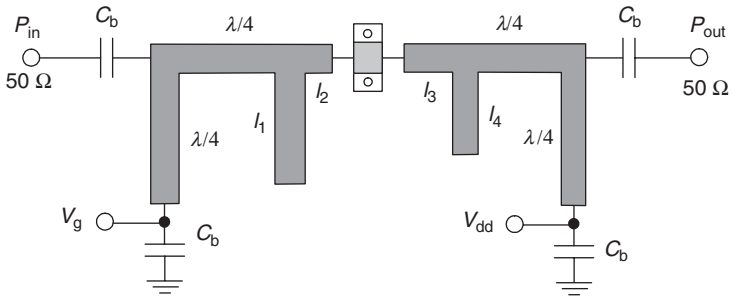



**Figure 5.27: Transmission-line Class-E power-amplifier topology.**

efficiency is greater than 70% over a 5% bandwidth and greater than 60% over a 10% bandwidth. A similar design approach can be used to design a monolithic Class-E power amplifier in *X*-band. As a result, the measured performance of a monolithic power amplifier that employs a $0.3\,\mu\text{m} \times 600\,\mu\text{m}$ pHEMT device showed a peak power-added efficiency of 63% at 10.6 GHz and a constant output power of greater than 24 dBm together with a power gain of 10 dB over frequency range of 9 GHz to 11 GHz [53].

Fig. 5.28 shows the schematic diagram of an experimental 1.8-GHz transmission-line Class-E power amplifier using a commercially available pHEMT device LP1500P100, which can offer a power gain over 12 dB for up to 15 GHz at a supply voltage of 3 V [45]. The gate and drain biasing are accomplished through the quarter-wave stubs printed on a substrate with thickness of 0.79 mm and $\varepsilon_r = 2.33$. In this case, the input quarter-wave stub provides a short-circuit termination of the second harmonic at the device input. The load impedance at the second harmonic is made nearly an open circuit by using microstrip line $l_3$ having an electrical length of 45° at the fundamental frequency. Fundamental input and output matching are achieved through microstrip lines $l_1$, $l_2$, $l_4$, $l_5$, and $l_6$, which were made adjustable by using high-quality copper foil. Initially, the device output capacitance $C_{out}$ of 0.3 to 0.5 pF and

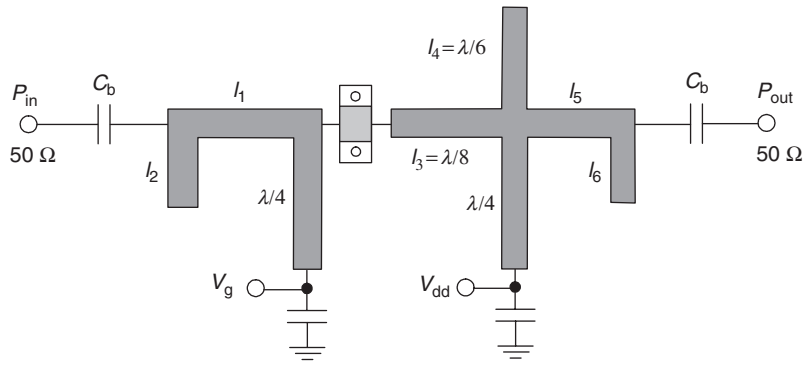



**Figure 5.28: Schematic diagram of 1.8 GHz pHEMT Class-E power amplifier.**

saturation resistance $r_{sat}$ of 1 to 2 Ω were assumed and $l_4$ was set to 60°. The transistor was biased near pinch-off with a quiescent current of 5 mA, which is about 5% of the maximum dc drain current. The amplifier exhibited a maximum saturated power of 22 dBm, a maximum drain efficiency of 93%, and a maximum power-added efficiency of 88%.

The transmission-line Class-E load network can also be realized by using a single-frequency equivalence between the lumped and distributed elements where a lumped inductance can be represented by a short-length transmission line and a lumped capacitance can be represented by an open-circuit stub [23]. Such an approach becomes useful when a matching circuit in the form of L- or T-type transformer is used instead of the series filter. Fig. 5.29(*a*) shows the schematic of a Class-E power amplifier with T-type output matching circuit [54]. Here, a small-size 0.8 μm pHEMT ATF-34143 is chosen for low-voltage broadband Class-E design. As the output capacitance is too small, it was increased by using an external shunt capacitance to optimize the efficiency and bandwidth of the power amplifier. It should be

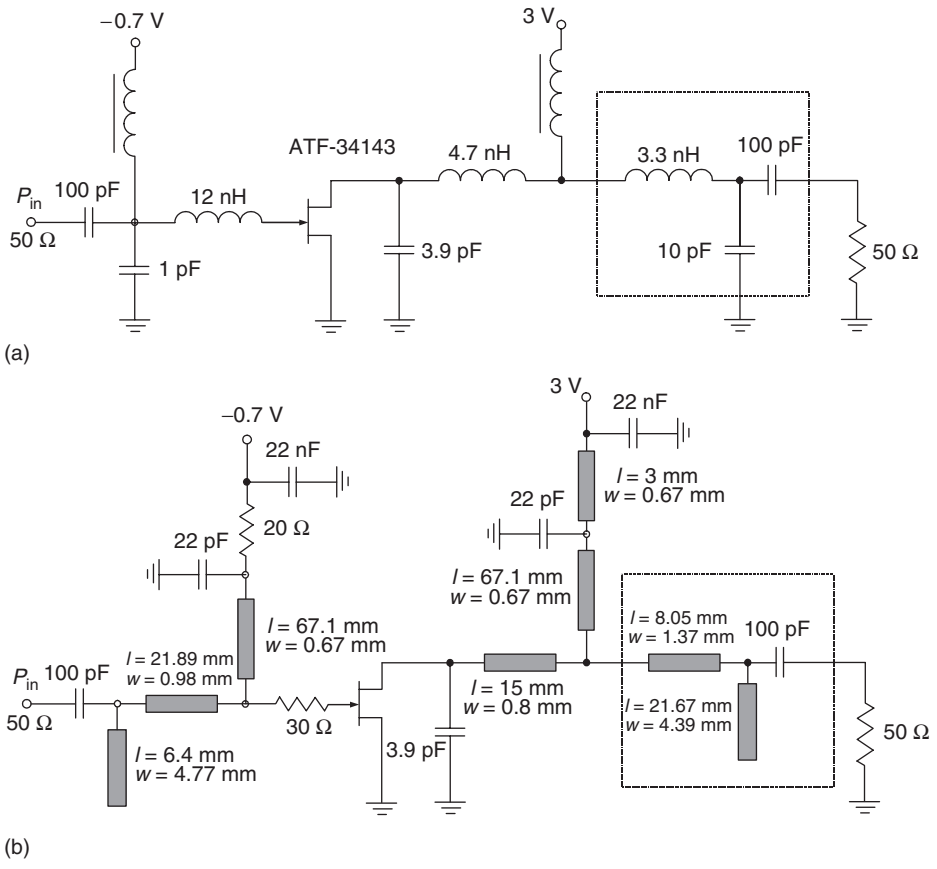



**Figure 5.29: Equivalent circuits of Class-E power amplifiers with *T*-transformer.**

noted that a simple L-transformer offers wider frequency bandwidth because of smaller loaded quality factor for the same impedance transformation ratio [23]. Therefore, a value of the series capacitance in an output T-transformer is chosen high enough, about 100 pF, to have a low capacitive reactance at the carrier frequency, about $2\,\Omega$, compared to the standard load resistance of $50\,\Omega$. The complex-conjugate matching technique is used for designing the input matching network. Due to the finite switching-time effect, the gate-bias point has to be moved slightly from Class B to Class C. To maximize efficiency over frequency bandwidth with minimum output power variations, load-pull simulation can be used to carefully transform the $50\,\Omega$ load to the optimal Class-E load resistance.

Fig. 5.29(*b*) shows the transmission-line topology of the lumped Class-E power amplifier whose electrical schematic is given in Fig. 5.29(*a*) [54]. Here, low-loss microstrip lines were fabricated on Rogers Duroid 5880 substrate with a dielectric permittivity of 2.33 and thickness of 0.79 mm, instead of using lumped inductors and capacitors. Two quarter-wave microstrip lines with high characteristic impedances are used instead of RF chokes. The two resistors used in the bias circuit and input-matching circuit are necessary to provide stable operation of the power amplifier. As a result, the maximum power-added efficiency of 66.5% was measured at 740 MHz with an output power of 22.7 dBm and a power gain of 10.7 dB. This power amplifier achieved a power-added efficiency above 50% within a frequency range between 540 and 890 MHz with an output power variation of about 2.5 dB.

To increase the overall efficiency of a two-stage power amplifier, it may be assumed that it is worthwhile to optimize both amplifying stages to operate in Class-E mode. For example, for a hybrid microwave GaAs MESFET Class-E power amplifier using the same AFM04P2 devices in both stages, the maximum two-stage power-added efficiency was achieved as high as 52% (including connector loss) with a corresponding power gain of 16 dB and an output power of 20 dBm at a carrier frequency of 10 GHz and a supply voltage of 4.2 V [55]. However, due to Class-E operation mode of the driver stage, the overall power gain is small enough to affect the overall efficiency. Therefore, by using a Class-AB driver stage, similar efficiency can be achieved with substantially higher power gain. As a result, for a monolithic microwave two-stage high-efficiency InP DHBT power amplifier where the driver stage operates in Class-AB mode and the output stage operates in Class-E mode, a power-added efficiency of 52% with output power of 24.6 dBm and power gain of 24.6 dB was achieved at a carrier frequency of 8 GHz and a supply voltage of 4 V [55]. The total emitter area of the driver-stage device was chosen to be $90\,\mu m^2$, providing a power-added efficiency of the driver stage of above 40% and an adequate power to push the output stage deep into compression as required for switched-mode operation. The output stage consists of two active devices with a total emitter area of $360\,\mu m^2$ combined in parallel reactively, taking care to provide odd-mode instability suppression resistors between the base and collector of each transistor [55]. The power-added efficiency is maintained greater than 40% over a frequency range of 7.7–10.5 GHz.

Recent progress in CMOS technology has shown their promising future for RF power application. Much progress has been achieved at the research level, and the obvious possibility to minimize cost and size of the integrated circuits for RF handset transmitters, especially power-amplifier MMICs, makes CMOS technology very feasible and brings considerable economic benefits. However, realizing high-efficiency operation of power amplifiers is limited by some technology issues like high value of the device saturation resistance, low value of breakdown voltage, and lossy silicon substrate. Therefore, it is vital to apply high-efficiency techniques in the design of CMOS power amplifiers. Fig. 5.30(*a*) shows a typical design structure of a two-stage CMOS Class-E power amplifier in which biasing inductors are used to provide dc-level shifting since the device threshold voltage is positive for the nMOS devices [56]. Note that these inductors should have extremely low parasitic resistance in order to reduce the metal power loss. To further reduce the power loss in passive components, bond-wire inductors can be used instead of low-$Q$ on-chip inductors, which especially makes sense under high-current conditions.

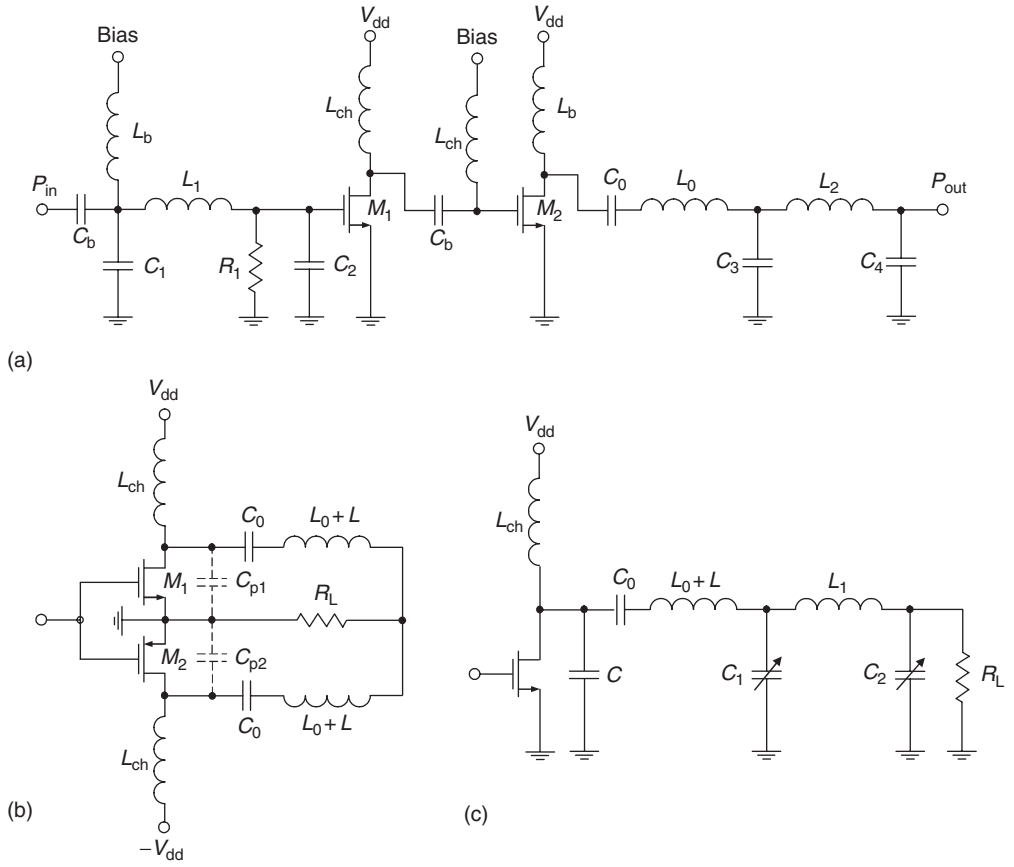



**Figure 5.30: Schematics of CMOS Class-E power amplifiers.**

A square driving waveform can be realized by using a high-pass interstage-matching section, employing a high-frequency filter to minimize the second harmonic of the driving signal or by overdriving the final stage with a large driving signal provided there is sufficient power gain.

While most Class-E power amplifiers use a single-ended topology due to practical implementation issues and available power devices, a differential counterpart, which exhibits smaller harmonic distortion since even harmonics cancel each other in a purely symmetrical structure, can be easily implemented using CMOS technology with nMOS and pMOS devices. The simplified topology of a Class-E complementary CMOS power amplifier is shown in Fig. 5.30(*b*) [57]. To minimize the saturation resistance of the devices, it is necessary to use devices with large gate width resulting in large, output capacitances. In some cases, the device output parasitic capacitances $C_{p1}$ and $C_{p2}$ can fully represent the shunt capacitances required for an optimum Class-E operation mode. The identical series resonant circuits are composed of a high-$Q_L$ series $L_0C_0$ filter and an optimum Class-E inductor $L$. As a result, the ideal Class-E switching conditions are provided for MOS devices, while the current flowing into the load $R_L$ is free from the even harmonics.

Modern wireless communication systems require the power amplifier to amplify linearly an input signal whose RF amplitude varies with time. In this case, there is a tradeoff between power-amplifier efficiency and linearity with improvement in one coming at the expense of the other. In addition, the power amplifiers in communications systems like GSM/EDGE, WCDMA, or CDMA2000 are required to cover linearly a dynamic range of the transmitter-output power up to 80 dB. As a result, being designed for the highest power level with maximum available efficiency, the power amplifier tends to operate less efficiently at lower power levels, which leads to shortening the battery life and the available time. In this case, to maximize efficiency of the power-amplifier operation, the load resistance for different output power levels should be different in order to provide a collector voltage amplitude close to the value of the supply voltage. Despite the fact that the shunt capacitance stays constant under different load conditions resulting in a non-optimum Class-E operation, the efficiency at a lower output-power level can be increased significantly. Fig. 5.30(*c*) shows the architecture of the power-controllable Class-E power amplifier whose matching network consists of two electrically tunable shunt capacitors and a series inductor [58]. This $\pi$-type matching circuit can transform the standard load of 50 $\Omega$ into different loads whose resistance values are greater than the optimum Class-E load.

Another possibility to improve efficiency of the power amplifier for RF signals with non-constant envelope is to use a traditional analog envelope elimination and restoration (EER) approach combined with digital processing system (DSP), whose polar architecture is shown in Fig. 5.31. Here, the two separate signals, one with amplitude (envelope) and the other with phase information only, are generated by DSP. The phase signal, in which the amplitude variations are canceled, modulates the phase of the phase-locked loop (PLL). Then, the output

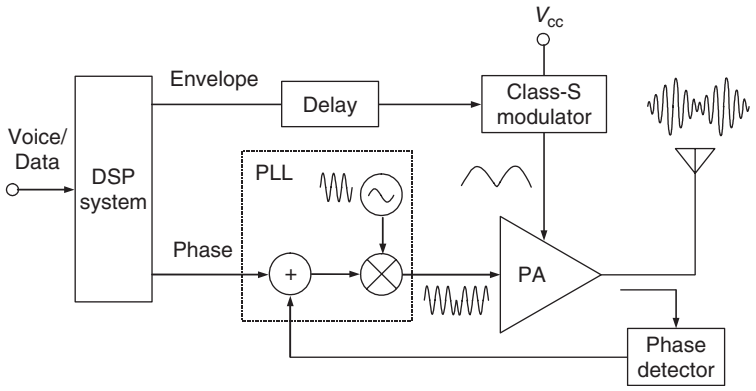



**Figure 5.31: Polar transmitter architecture.**

signal of the PLL is amplified by the highly efficient Class-E power amplifier. The amplitude signal is fed to a Class-S modulator to effectively vary the supply voltage according to the varying signal envelope amplitude. A Class-S modulator is a high-efficiency low-frequency power amplifier based on pulse-width modulation, and its output is a baseband envelope signal including a dc component. To minimize misalignment between phase and amplitude, the delay line is required. Adding the output-phase feedback circuit allows the intermodulation distortion to be reduced. The measured results from a prototype test chip operating at 835 MHz indicate that phase correcting feedback reduces the 30° phase distortion of the Class-E power amplifier down to 4° when it delivers an output power of 443 mW to the load at a supply voltage of 2.4 V, and the total power efficiency of the linearized Class-E power amplifier is 65% [56].

Generally, the dependence of the output voltage on the dc supply voltage is linear enough so that amplitude modulation can be achieved by linearly varying the supply voltage, both for bipolar and MESFET devices [59, 60]. Variations from perfect linearity can be caused by variations in the transistor saturation voltage being a function of the supply voltage, input-to-output feedthrough of the driving signal via the feedback capacitance, and voltage-variable output capacitance of the transistor. In addition, the size of a Class-S modulator can be too large for MMIC implementation, and the modulator can be inefficient at high frequencies. Note that, for such a polar architecture, a high degree of amplitude and phase tracking is required to achieve high depth of modulation. For instance, a combination of 0.2 dB amplitude and 3° of phase tracking error will result in a maximum modulation dynamic range of only 20 dB. There should be a trade-off between the switching frequency in a Class-S modulator and the order of a low-pass filter to minimize the intermodulation distortion.

A high-efficiency linear RF power amplifier using an improved EER (now, frequently called ‘‘polar’’) architecture is described in U.S. Patent 3,900,823 issued to Nathan O. Sokal and Alan D. Sokal on August 19, 1975. An experimental HF amplifier operating at 3.9 MHz, with

26 W peak envelope power (PEP), had intermodulation distortion (in a two-equal-tones test) that was too small to be detectable with the then-available test equipment. Nathan Sokal estimated that the distortion was smaller than −40 dB referenced to the PEP. The overall drain efficiency was 90% (95% in the Class-E RF power amplifier, and 95% in the 1-MHz dc-dc converter that supplied the time-varying collector supply voltage to the RF power amplifier). All harmonics in the RF output were −60 dBc or smaller.

## References

[1] J. W. Wood, ''High Efficiency Class C Amplifier,'' U.S. Patent 3,430,157, February 1969.

[2] E. P. Khmelnitsky, *Operation of Vacuum-Tube Generator on Detuned Resonant Circuit* (in Russian), Moskva: Svyazizdat, 1962.

[3] G. D. Ewing, *High-Efficiency Radio-Frequency Power Amplifiers*, Ph.D. Dissertation, Oregon State University, June 1964.

[4] D. R. Lohrmann, ''Amplifier Has 85% Efficiency while Providing up to 10 Watts Power over a Wide Frequency Band,'' *Electronic Design*, vol. 14, pp. 38–43, March 1966.

[5] A. D. Artym, ''Switching Mode of High Frequency Power Amplifiers (in Russian),'' *Radiotekhnika*, vol. 24, pp. 58–64, June 1969.

[6] V. V. Gruzdev, ''Calculation of Circuit Parameters of Single-Ended Switching-Mode Tuned Power Amplifier (in Russian),'' Trudy MEIS, vol. 2, pp. 124–128, 1969.

[7] A. Grebennikov, ''Class E High-Efficiency Power Amplifiers: Historical Aspect and Future Prospect,'' *Applied Microwave & Wireless*, vol. 14, pp. 64–71, July 2002, pp. 64–72, August 2002.

[8] M. Kazimierczuk, ''Class E Tuned Power Amplifier with Nonsinusoidal Output Voltage,'' *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 575–581, August 1986.

[9] V. B. Kozyrev, ''Single-Ended Switching-Mode Tuned Power Amplifier with Filtering Resonant Circuit (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Svyazi*, vol. 6, pp. 152–166, 1971.

[10] N. O. Sokal and A. D. Sokal, ''Class E—A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers,'' *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168–176, June 1975.

[11] N. O. Sokal and A. D. Sokal, ''High-Efficiency Tuned Switching Power Amplifier,'' U.S. Patent 3,919,656, November 1975.

[12] N. O. Sokal, ''Class E High-Efficiency Power Amplifiers, from HF to Microwave,'' *1998 IEEE MTT-S Int. Microwave Sym. Dig.*, vol. 2, pp. 1109–1112.

[13] F. H. Raab, ''Idealized Operation of the Class E Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-24, pp. 725–735, December 1977.

[14] B. Molnar, ''Basic Limitations on Waveforms Achievable in Single-Ended Switching-Mode Tuned (Class E) Power Amplifiers,'' *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 144–146, February 1984.

[15] T. B. Mader, E. W. Bryerton, M. Marcovic, M. Forman, and Z. Popovic, ''Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 1391–1398, October 1998.

[16] M. Kazimierczuk and K. Puczko, ''Exact Analysis of Class E Tuned Power Amplifier at any *Q* and Switch Duty Cycle,'' *IEEE Trans. Circuits and Systems*, vol. CAS-34, pp. 149–158, February 1987.

[17] N. O. Sokal, ''Class-E High-Efficiency RF/Microwave Power Amplifiers: Principles of Operation, Design Procedure, and Experimental Verification,'' in J. H. Huijsing, M. Steyaert, and A. van Roermund (Eds.), *Analog Circuit Design: Scalable Analog Circuit Design, High Speed D/A Converters, RF Power Amplifiers*, The Netherlands: Kluwer Academic Publishers, 2002, pp. 269–301.

[18] F. H. Raab, ''Suboptimum Operation of Class-E Power Amplifiers,'' *Proc. RF Technology Expo '89*, Santa Clara, CA, pp. 85–98, February 1989.

[19] F. H. Raab, ''Effects of Circuit Variations on the Class E Tuned Power Amplifier,'' *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 239–246, April 1978.

[20] F. H. Raab, ''Effects of VSWR upon the Class-E RF-Power Amplifier,'' *Proc. RF Expo East '88*, Philadelphia, PA, pp. 299–309, October 1988.

[21] I. A. Popov, ''Switching Mode of Single-Ended Transistor Power Amplifier (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Svyazi*, vol. 5, pp. 15–35, 1970.

[22] A. V. Grebennikov, ''A Simplified CAD Approach to Analyzing Lumped Elements,'' *RF Design*, vol. 23, pp. 22–38, June 2000.

[23] A. V. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[24] R. Negra and W. Bachtold, ''Lumped-Element Load-Network Design for Class-E Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-54, pp. 2684–2690, June 2006.

[25] F. H. Raab and N. O. Sokal, ''Transistor Power Losses in the Class E Tuned Power Amplifier,'' *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 912–914, December 1978.

[26] I. A. Popov (Ed.), *Transistor Generators of Harmonic Oscillations in Switching Mode* (in Russian), Moskva: Radio i Svyaz, 1985.

[27] A. N. Bruevich, ''About Optimum Parameters of Switching-Mode Tuned Power Amplifier with Filtering Resonant Circuit (in Russian),'' *Poluprovodnikovaya Elektronika v Tekhnike Svyazi*, vol. 18, pp. 43–48, 1977.

[28] V. B. Kozyrev and V. V. Shkvarin, ''Optimum Operation Mode of Single-Ended Switching-Mode Tuned Power Amplifier with Forming Resonant Circuit (in Russian),'' *Radiotekhnika*, vol. 37, pp. 90–93, October 1982.

[29] D. J. Kessler and M. K. Kazimierczuk, ''Power Losses and Efficiency of Class-E Power Amplifier at Any Duty Ratio,'' *IEEE Trans. Circuits and Systems–I: Regular Papers*, vol. CAS-I-51, pp. 1675–1689, September 2004.

[30] M. Kazimierczuk, ''Effect of the Collector Current Fall Time on the Class E Tuned Power Amplifier,'' *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 181–193, April 1983.

[31] J. A. Blanchard and J. S. Yuan, ''Effect of Collector Current Exponential Decay on Power Efficiency for Class E Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems–I: Fundamental Theory Appl.*, vol. CAS-I-41, pp. 69–72, January 1994.

[32] S. H.-L. Tu and C. Toumazou, ''Effect of the Loaded Quality Factor on Power Efficiency for CMOS Class-E RF Tuned Power Amplifiers,'' *IEEE Trans. Circuits and Systems–I: Fundamental Theory Appl.*, vol. CAS-I-46, pp. 628–634, May 1999.

[33] S. S. Islam and A. F. M. Anwar, ''High Frequency GaN/AlGaN HEMT Class-E Power Amplifier,'' *Solid-State Electronics*, vol. 46, pp. 1621–1625, October 2002.

[34] M. J. Chudobiak, ''The Use of Parasitic Nonlinear Capacitors in Class E Amplifiers,'' *IEEE Trans. Circuits and Systems– I*: *Fundamental Theories Appl.*, vol. CAS-I-41, pp. 941–944, December 1994.

[35] P. Alinikula, K. Choi, and S. I. Long, ''Design of Class E Power Amplifier with Nonlinear Parasitic Output Capacitance,'' *IEEE Trans. Circuits and Systems–II: Analog and Digital Signal Process*, vol. CAS-II-46, pp. 114–119, February 1999.

[36] T. Suetsugu and M. K. Kazimierczuk, ''Analysis and Design of Class E Amplifier with Shunt Capacitance Composed of Nonlinear and Linear Capacitances,'' *IEEE Trans. Circuits and Systems–I: Regular Papers*, vol. CAS-I-51, pp. 1261–1268, July 2004.

[37] T. Suetsugu and M. K. Kazimierczuk, ''Comparison of Class-E Amplifier with Nonlinear and Linear Shunt Capacitance,'' *IEEE Trans. Circuits and Systems–I: Fundamental Theory Appl.*, vol. CAS-I-50, pp. 1089–1097, August 2003.

[38] D. W. Cripe, ''Resonant Push-Pull Switching Power Amplifier,'' U.S. Patent 5,327,337, July 1994.

[39] S.-W. Ma, H. Wong, and Y.-O. Yam, ''Optimal Design of High Output Power Class E Amplifier,'' *Proc. 4th IEEE Int. Caracas Conf. Devices Circuits Syst.*, pp. 012-1–012-3, 2002.

[40] S.-C. Wong and C. K. Tse, ''Design of Symmetrical Class E Power Amplifiers for Very Low Harmonic-Content Applications,'' *IEEE Trans. Circuits and Systems–I: Regular Papers*, vol. CAS-I-52, pp. 1684–1690, August 2005.

[41] R. Tayrani and C. W. Meyers, ''Efficiency Broadband Switching-Mode Amplifier,'' U.S. Patent 6,949,978, September 2005.

[42] T. B. Mader and Z. B. Popovic, ''The Transmission-Line High-Efficiency Class-E Amplifier,'' *IEEE Microwave and Guided Wave Lett.*, vol. 5, pp. 290–292, September 1995.

[43] F. H. Raab, ''Class-E, Class-C, and Class-F Power Amplifiers Based Upon a Finite Number of Harmonics,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1462–1468, August 2001.

[44] F. J. Ortega-Gonzalez, J. L. Jimenez-Martin, A. Asensio-Lopez, and G. Torregrosa-Penalva, ''High-Efficiency Load-Pull Harmonic Controlled Class-E Power Amplifier,'' *IEEE Microwave and Guided Wave Lett.*, vol. 8, pp. 348–350, October 1998.

[45] Y.-B. Choi and K.-K. M. Cheng, ''Generalised Frequency-Domain Analysis of Microwave Class-E Power Amplifiers,'' *IEE Proc. Microwave Antennas Propag.*, vol. 148, pp. 403–409, December 2001.

[46] P. Watson, R. Neidhard, L. Kehias, R. Welch, T. Quach, R. Worley, M. Pacer, R. Pappaterra, R. Schweller, and T. Jenkins, ''Ultra-High Efficiency Operation Based on an Alternative Class-E Mode,'' *2000 IEEE GaAs IC Symp. Dig.*, pp. 53–56.

[47] T. K. Quach, P. M. Watson, W. Okamura, E. N. Kaneshiro, A. Gutierrez-Aitken, T. R. Block, J. W. Eldredge, T. J. Jenkins, L. T. Kehias, A. K. Oki, D. Sawdai, R. J. Welch, and R. D. Worley, ''Ultra-High Efficiency Power Amplifier for Space Radar Applications,'' *IEEE J. Solid-State Circuits*, vol. SC-37, pp. 1126–1134, September 2002.

[48] A. J. Wilkinson and J. K. A. Everard, ''Transmission-Line Load-Network Topology for Class-E Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1202–1210, June 2001.

[49] J. Lee, S. Kim, J. Nam, J. Kim, I. Kim, and B. Kim, ''Highly Efficient LDMOS Power Amplifier Based on Class-E Topology,'' *Microwave and Optical Technology Lett.*, vol. 48, pp. 789–791, April 2006.

[50] J. F. Davis and D. B. Rutledge, ''A Low-Cost Class-E Power Amplifier with Sine-Wave Drive,'' *1998 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 1113–1116.

[51] R. Frey, ''500 W, Class E 27.12 MHz Amplifier Using a Single Plastic MOSFET,'' *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 359–362.

[52] H. Zirath and D. Rutledge, ''An LDMOS VHF Class E Power Amplifier Using a High Q Novel Variable Inductor,'' *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 367–370.

[53] R. Tayrani, ''A Monolithic X-Band Class-E Power Amplifier for Space Based Radar Systems,'' *RF Design*, vol. 26, pp. D14–D19, November 2003.

[54] Y. Qin, S. Gao, A. Sambell, and E. Korolkiewicz, ''Design of Low-Cost Broadband Class-E Power Amplifier Using Low-Voltage Supply,'' *Microwave and Optical Technology Lett.*, vol. 44, pp. 103–106, January 2005.

[55] S. Pajic, N. Wang, P. M. Watson, T. K. Quach, and Z. Popovic, ''*X*-Band Two-Stage High-Efficiency Switched-Mode Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-53, pp. 2899–2907, September 2005.

[56] S. H.-L. Tu, ''Class-E RF-Tuned Power Amplifiers in CMOS Technologies: Theory and Circuit Design Considerations,'' *IEEE Communications*, vol. 42, pp. S6–S11, September 2004.

[57] S. H.-L. Tu and C. Toumazou, ''Low-Distortion CMOS Complementary Class-E RF-Tuned Power Amplifiers,'' *IEEE Trans. Circuits and Systems–I: Fundamental Theory Appl.*, vol. CAS-I-47, pp. 774–779, May 2000.

[58] S. H.-L. Tu and C. Toumazou, ''Design of Highly-Efficient Power-Controllable CMOS Class-E RF-Power Amplifier,'' *1999 IEEE Int. Symp. Circuits and Systems Dig.*, vol. 2, pp. 602–605.

[59] T. Sowlati, C. Andre, T. Salama, J. Sitch, G. Rabjohn, and D. Smith, ''Low Voltage, High Efficiency GaAs Class E Power Amplifiers for Wireless Transmitters,'' *IEEE J. Solid-State Circuits*, vol. SC-30, pp. 1074–1080, October 1995.

[60] M. Kazimierczuk, ''Collector Amplitude Modulation of the Class E Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-31, pp. 543–549, June 1984.

CHAPTER 6

# Class E with Finite dc-Feed Inductance

In this chapter, the switched-mode second-order Class-E configurations with one capacitor and one inductor and generalized load network including the finite dc-feed inductance, shunt capacitance, and series reactance are discussed and analyzed. The results of the Fourier analysis and derivation of the equations governing the operation in an idealized operation mode are presented. Based on these equations, the required voltage and current waveforms and load-network parameters are determined for both general case and particular circuits corresponding to the subharmonic Class E, parallel-circuit Class E, and even-harmonic Class-E modes. The effect of the device output bond-wire inductance on the optimum circuit parameters is demonstrated. The possibilities to realizing a Class-E approximation with transmission lines and broadband Class-E load networks are shown and discussed. The operating power gain achieved with a parallel-circuit Class-E power amplifier is evaluated and compared with the operating power gain of a conventional Class-B power amplifier. The circuit-design examples and practical implementations of the Class-E power amplifiers using a CMOS technology are given as well.

## 6.1 Class E with One Capacitor and One Inductor

The Class-E load network with a shunt capacitor and a series inductor represents the simplest load network used for a switched-mode operation because it can be analytically described by a first-order differential equation resulting in exact values for the load-network parameters. However, a switching-mode tuned Class-E power amplifier can also be realized with only one inductor and one capacitor connected in parallel in the load network [1, 2, 3, 4]. In this case, the load network topology is the same as in the classical current-source Class-C power amplifier, but the operation of the two circuits is entirely different. In a Class-C power amplifier, the tank circuit provides sinusoidal voltage on the device collector, being tuned to the fundamental frequency. In a Class-E power amplifier, this circuit is tuned between the fundamental frequency and second harmonic providing a non-sinusoidal collector-voltage waveform to minimize overlapping between the collector current and voltage waveforms, thus reducing the power losses on the device and increasing the collector efficiency.

The basic circuit of a switched-mode Class-E power amplifier with one parallel LC circuit is shown in Fig. 6.1(*a*). The load network consists of a parallel inductance $L$, a parallel

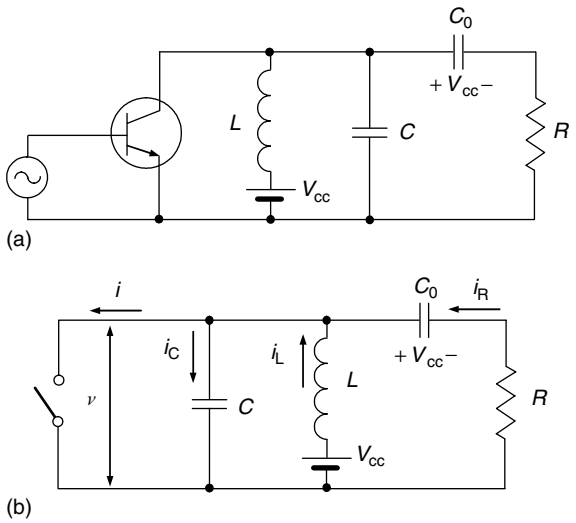



**Figure 6.1: Basic circuits of Class-E power amplifier with one capacitor and one inductor.**

capacitance $C$, a dc-blocking capacitance $C_0$, and a load $R$. In a common case, the parallel capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation modes. As a result, the collector voltage waveform is determined by the transient response of the load network when the switch is off.

To simplify an analysis of a parallel-circuit Class-E power amplifier, a simple equivalent circuit is shown in Fig. 6.1($b$), it is advisable to use the same assumptions as for the Class E with shunt capacitance:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-state resistance, and its switching action is instantaneous and lossless.
- The total parallel capacitance is independent of the collector-emitter voltage and is assumed linear.
- There are no losses in the circuit except only into the load $R$.
- For an optimum operation mode, a 50% duty cycle is used (other values can also be used if desired, as part of a trade-off among several performance parameters).

For an idealized theoretical analysis, it is best to replace an active device by the ideal switch, as shown in Fig. 6.1($b$). Let the moments of switch-on be $t = 0$ and switch-off be $t = \pi/\omega$ with period of repeatability of $T = 2\pi/\omega$ determined by the drive input to the power amplifier.

For lossless operation, it is necessary to provide the following optimum conditions for voltage across the switch just prior to the start of switch-on at the moment $t = 2\pi/\omega$ when the transistor is voltage-saturated:

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{6.1}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0, \tag{6.2}$$

where $v$ is the voltage across the switch.

The term ''optimum'' for the conditions given by Eqs. (6.1) and (6.2) means that the voltage across the switch should be equal to zero and there are no current jumps through the capacitor $C$ (capacitor must be discharged) at the moment when the switch is turned on with further instant transitions from off-state to on-state modes, thus resulting in a maximum achievable collector efficiency. Otherwise, if current starting to flow through the switch at this moment is not equal to zero, the device cannot be considered an ideal switch because of the appearance of the active operation mode of the device between its pinch-off and saturation modes. In this case, the collector current and voltage waveforms overlap each other reducing the collector efficiency because of the power dissipation in the device. The *optimum conditions* given by Eqs. (6.1) and (6.2) for a lossless operation mode with ideal switch can also be called the *nominal conditions*.

When the switch is turned on for $0 \leq \omega t < \pi$, the voltage across the switch $v(\omega t)$ and the current $i_C(\omega t)$ flowing through the capacitance $C$ are equal to zero, i.e.

$$v(\omega t) = V_{cc} - v_L(\omega t) = 0 \tag{6.3}$$

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)} = 0. \tag{6.4}$$

The current $i_R$ flowing into the load $R$ can generally be determined by

$$i_R(\omega t) = \frac{V_{cc}}{R} \exp\left(-\frac{t}{\tau}\right), \tag{6.5}$$

where $\tau = RC_0$. However, for $\tau \to \infty$ when the series capacitor $C_0$ serves as a dc-blocking capacitor with a large value of $C \to \infty$, the current $i_R$ can be simply rewritten as $i_R(\omega t) = V_{cc}/R$. Then, to describe the circuit operation in the time domain, the following system of equations can be obtained:

$$V_{cc} = \omega L \frac{di_L(\omega t)}{d\omega t} \tag{6.6}$$

$$i = i_{\mathrm{L}} + i_{\mathrm{R}}. \tag{6.7}$$

Taking into account that $i(0) = 0$ and

$$i_{\mathrm{L}}(\omega t) = \frac{1}{\omega L}\int_{0}^{\omega t} v_{\mathrm{L}}(\omega t)d\omega t + i_{\mathrm{L}}(0), \tag{6.8}$$

where $v_{\mathrm{L}} = V_{\mathrm{cc}}$ and $i_{\mathrm{L}}(0) = -V_{\mathrm{cc}}/R$, the current $i(\omega t)$ flowing through the switch can be defined by

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}\omega t. \tag{6.9}$$

When the switch is turned off for $\pi \leq \omega t < 2\pi$, the following system of equations can be written:

$$V_{\mathrm{cc}} = \omega L\frac{di_{\mathrm{L}}(\omega t)}{d\omega t} \tag{6.10}$$

$$i_{\mathrm{C}} = i_{\mathrm{L}} + i_{\mathrm{R}}, \tag{6.11}$$

where the current $i_{\mathrm{C}}(\omega t) = i_{\mathrm{L}}(\omega t) + i_{\mathrm{R}}(\omega t)$ flowing through the capacitance $C$ can be rewritten as

$$\omega C\frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L}\int_{\pi}^{\omega t}[V_{\mathrm{cc}} - v(\omega t)]d(\omega t) + i_{\mathrm{L}}(\pi) + \frac{V_{\mathrm{cc}} - v(\omega t)}{R} \tag{6.12}$$

under the initial off-state conditions: $v(\pi) = 0$ and

$$\omega C\left.\frac{dv}{d\omega t}\right|_{\omega t=\pi} = i(\pi) = \frac{V_{\mathrm{cc}}\pi}{\omega L}.$$

In [5], the solution of the integro-differential equation given by Eq. (6.12) was found by applying the Laplace transform method. Another approach is to apply the methods of solving the differential equations directly. As a result, Eq. (6.12) can be represented in the form of the linear non-homogeneous second-order differential equation given by

$$\omega^2 LC\frac{d^2v(\omega t)}{d(\omega t)^2} + \frac{\omega L}{R}\frac{dv(\omega t)}{d\omega t} + (\omega t) = V_{\mathrm{cc}} \tag{6.13}$$

the general solution of which can be obtained in the form of

$$v(\omega t) = \exp(a\omega t)[C_1\cos(b\omega t) + C_2\sin(b\omega t)] + V_{\mathrm{cc}}, \tag{6.14}$$

where

$$a = -\frac{1}{2Q} \qquad b = \frac{1}{2Q}\sqrt{(2Qq)^2 - 1}$$

$$q = \frac{1}{\omega\sqrt{LC}} \qquad Q = \omega RC.$$

The coefficients $C_1$ and $C_2$ are determined from the initial off-state conditions by

$$C_1 = -V_{cc}\exp(-a\pi)\left[\cos b\pi + \frac{\pi q^2 + a}{b}\sin b\pi\right] \tag{6.15}$$

$$C_2 = -V_{cc}\exp(-a\pi)\left[\sin b\pi - \frac{\pi q^2 + a}{b}\cos b\pi\right]. \tag{6.16}$$

To solve Eq. (6.14) with regard to two unknown parameters $q$ and $Q$, it is necessary to use the two optimum conditions given by Eqs. (6.1) and (6.2). Let us consider the oscillatory case of $2Qq > 1$ for a second-order differential equation. As a result, the numerical solution gives the following values:

$$q = 1.542 \tag{6.17}$$

$$Q = 1.025. \tag{6.18}$$

Thus, the optimum values of a parallel inductance and a parallel capacitance corresponding to the switched-mode Class-E load network with only one inductor and one capacitor can be calculated from

$$L = 0.41\frac{R}{\omega} \tag{6.19}$$

$$C = \frac{1.025}{\omega R}, \tag{6.20}$$

which are similar to those obtained in [2, 3].

The optimum load $R$ and phase shift $\varphi$ for the fundamental-frequency component can be determined using the load network impedance at the fundamental seen by the switch, which phase angle $\phi$ can be represented as a function of the load network elements by

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = \tan^{-1}[Q(q^2 - 1)] = 54.729^\circ. \tag{6.21}$$

On the other hand, the fundamental-frequency current $i_1(\omega t)$ flowing through the switch consists of two quadrature components, active $i_{R1}$ and reactive $i_{X1}$, which amplitudes can be found using Fourier formulas and Eq. (6.9) by

$$I_{R1} = \frac{1}{\pi}\int_0^{2\pi} i(\omega t)\sin(\omega t + \varphi)\, d(\omega t) = \frac{V_{cc}}{\pi\omega L}(\pi\cos\varphi - 2\sin\varphi) \tag{6.22}$$

$$I_{X1} = -\frac{1}{\pi}\int_0^{2\pi} i(\omega t)\cos(\omega t + \varphi)\, d(\omega t) = \frac{V_{cc}}{\pi\omega L}(\pi\sin\varphi + 2\cos\varphi), \tag{6.23}$$

where $\varphi$ is the initial phase shift of the fundamental-frequency current.

Hence,

$$\tan\phi = \frac{I_{X1}}{I_{R1}} = \frac{\pi\sin\varphi + 2\cos\varphi}{\pi\cos\varphi - 2\sin\varphi} \tag{6.24}$$

and the phase shift $\varphi$ can be finally calculated as

$$\varphi = \tan^{-1}\left(\frac{\pi\tan\phi - 2}{2\tan\phi + \pi}\right) = 22.25^\circ. \tag{6.25}$$

The dc supply current $I_0$ can be obtained using the Fourier formula from Eq. (6.9) as

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d(\omega t) = \frac{\pi V_{cc}}{4\omega L}. \tag{6.26}$$

By using Eq. (6.22), the optimum load resistance $R$ for the specified values of supply voltage $V_{cc}$ and output power $P_1$ at the fundamental frequency can be written as

$$R = \frac{2P_1}{I_{R1}^2} = 2\left(\frac{\pi\omega L}{V_{cc}}\right)^2 \frac{P_1}{(\pi\cos\varphi - 2\sin\varphi)^2}. \tag{6.27}$$

Then, by taking into account Eqs. (6.19) and (6.25), it can be simplified to

$$R = 1.394\frac{V_{cc}^2}{P_1}. \tag{6.28}$$

Fig. 6.2 shows the normalized (*a*) fundamental-frequency load current (not including the harmonic components), (*b*) collector voltage, and (*c*) collector current waveforms for an

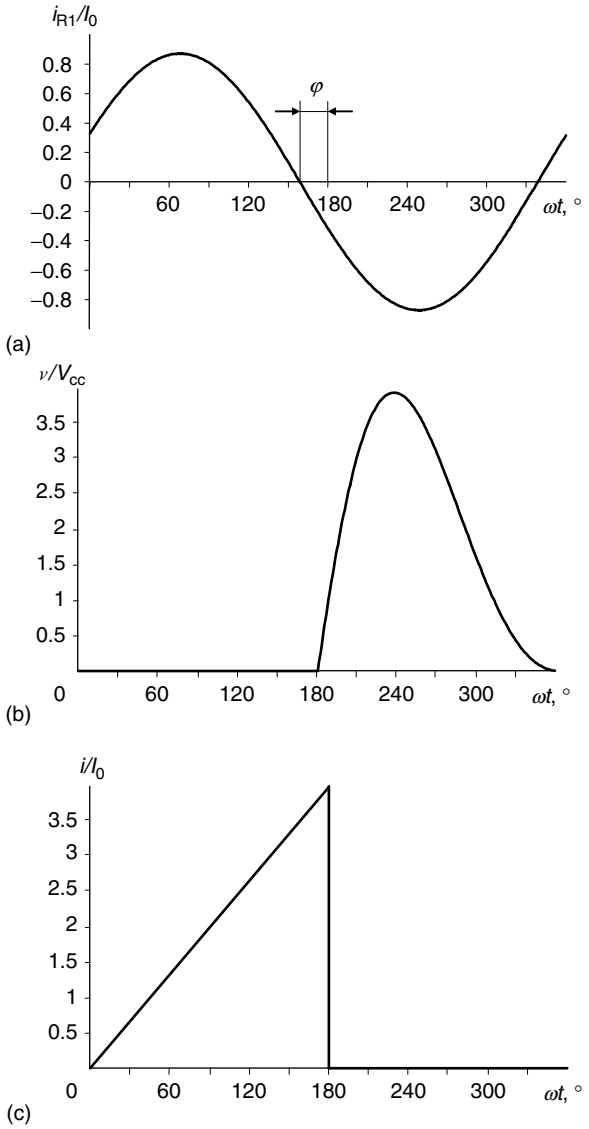



**Figure 6.2: Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum Class E with one capacitor and one inductor.**

idealized optimum Class-E mode. From the collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and current $i(\omega t)$ consisting of the total load current and inductor current flows through the switch. However, when the transistor is turned off, this current now flows through the shunt capacitor. As a result there is no nonzero voltage and current simultaneously, which means a lack of the power losses and gives an idealized collector efficiency of 100%. The normalized currents flowing

through the ($a$) shunt capacitor $C$, ($b$) parallel inductor $L$ and ($c$) load resistor $R$ for an idealized optimum operation mode are given in Fig. 6.3.

The peak collector current $I_{\max}$ can be directly determined from Eq. (6.9) using Eq. (6.26), while the peak collector voltage $V_{\max}$ is calculated numerically from Eq. (6.14) which gives

$$I_{\max} = 4.000 I_0 \tag{6.29}$$

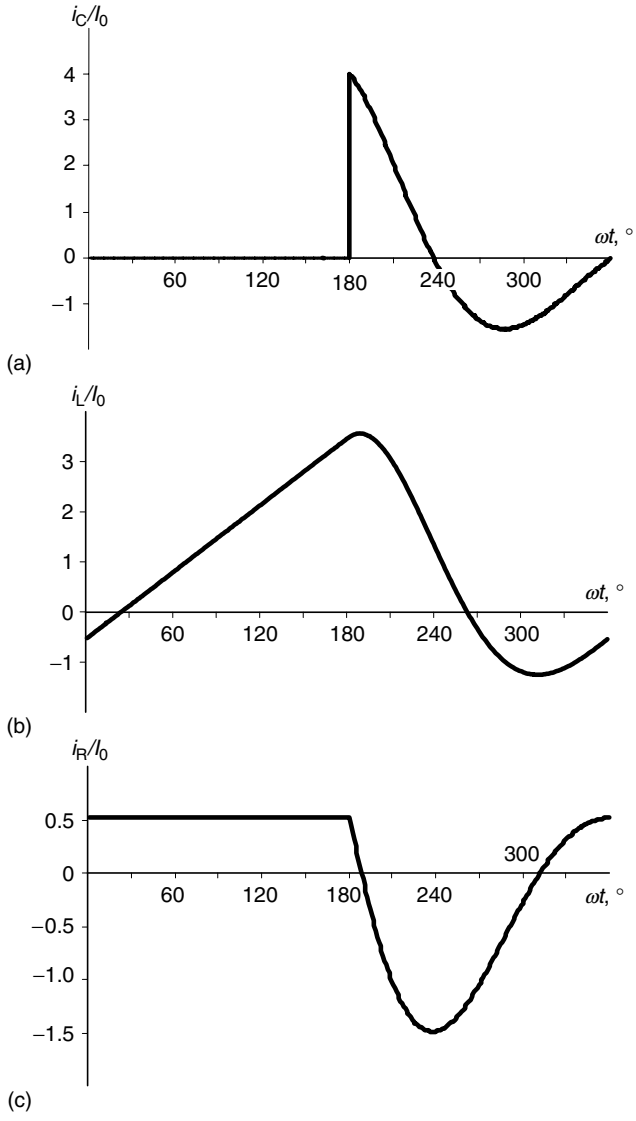



**Figure 6.3: Normalized currents flowing through ($a$) shunt capacitor, ($b$) parallel inductor, and ($c$) load resistor.**

$$V_{max} = 3.849 V_{cc}. \tag{6.30}$$

The numerical calculation shows that the harmonic level of the output signal spectrum is significant. The ratio of the fundamental-frequency output power $P_1$, second-harmonic output power $P_2$, and third-harmonic output power $P_3$ is

$$P_1 : P_2 : P_3 = 1 : 0.3156 : 0.0405, \tag{6.31}$$

which shows that the suppressions of the second and third harmonics relative to the fundamental-frequency component in the output power spectrum are approximately $-5$ dBc and $-14$ dBc, respectively [2]. Note that the harmonic level in the output power spectrum in the Class-E power amplifier with shunt capacitor and series inductor of Fig. 5.2 is lower than that in the Class E with one capacitor and one inductor of Fig. 6.1, being less than 10% of the fundamental-frequency power [5, 6]. Therefore, this version of the Class-E load network is suitable for applications, in which the power delivered to the load $R$ is allowed to have a fairly large harmonic content and phase-modulation noise because of the absence of any additional filtering. However, this circuit can be effectively used as a test bench for extracting the parameters of a simple, active device output-port model like saturation resistance and output capacitance [7]. This approach can provide the designers with a quick way to find out if a transistor will be useful in a Class-E operation and with what maximum operating frequency.

## 6.2 Generalized Class-E Load Network with Finite dc-Feed Inductance

In real practice, it is impossible to realize an RF choke with infinite impedance at the fundamental frequency and its harmonic components. Moreover, using a finite dc-feed inductance has an advantage of minimizing size, cost, and complexity of the overall circuit. The detailed approach to analyze the effect of a finite dc-feed inductance on the idealized Class-E mode with shunt capacitance and series filter was first described in 1987 [8]. It was based on the Laplace-transform technique to solve a second-order differential equation describing the behavior of a Class-E load network with finite dc-feed inductance. Later, this approach was extended to the load network with finite $Q_L$-factor of the series filter and finite device saturation resistance [9, 10]. The obtained results can be summarized as follows [10]:

- For a smaller dc-feed inductance, smaller detuning of a series-tuned circuit is necessary, which is very attractive for radio-transmitter applications where the amplitudes of the two sidebands should not be substantially different.
- Using a small dc-feed inductance is attractive when both the dc voltage and load resistance are specified and higher output power is needed.

- $Q_L$-factor of a series filter affects the power-amplifier performance less when the dc-feed inductance is small.

- Maximum output power increases as a dc-feed inductance decreases for large values of $Q_L$-factor and behaves oppositely for small values of $Q_L$-factors.

- Device saturation resistance $r_{sat}$ should be taken into account, especially when it is larger than $0.1R$, where $R$ is an optimum Class-E load resistance.

However, since the results of excessive analytical and numerical calculations are given only for a few particular cases, it is difficult to figure out the basic behavior of the load network elements and define simple equations for their parameters. Generally, based on the composing of the circuit equations in the form of a system of first-order differential equations for currents and voltages and setting the design specifications, the optimum Class-E load network parameters can be numerically calculated taking into account the finite dc-feed inductance, drain-current fall time, finite $Q_L$-factor, nonzero device saturation resistance, and nonlinear operation of any passive element simultaneously, [11]. More physical insight into Class-E load network specifics has been given [12], where the Class-E load network with finite dc-feed inductance was analyzed for a duty cycle of 50% based on the Class-E optimum conditions. It was analytically shown that the series excess reactance can be either inductive or capacitive depending on the values of the dc-feed inductance and shunt capacitance. A similar detailed analytical derivation procedure with particular examples is presented [13], where the finite device saturation resistance is taken into account to predict the power losses on the active device. Based on a certain number of cases, a Lagrange-polynomial interpolation was used to obtain explicit directly usable design equations for an idealized Class E with finite dc-feed inductance and series inductive reactance [14].

Now let us consider a general case of the Class-E load network with finite dc-feed inductance. The main goal is to demonstrate an analytical design procedure in a clear mathematical form and to represent the design equations in a simple explicit analytical or graphical form with special highlighting of the specific particular cases. The generalized second-order load network of a switched-mode Class-E power amplifier with finite dc-feed inductance is shown in Fig. 6.4(*a*) [15]. The load network consists of a shunt capacitance $C$, a series inductance $L_b$, a parallel inductance $L$, a series reactance $X$, a series resonant $L_0C_0$ circuit tuned to the fundamental frequency, and a load resistance $R$. In a common case, a shunt capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network, a series inductance $L_b$ can be considered as a bond-wire and lead inductance, a parallel inductance $L$ represents the finite dc-feed inductance, and a series reactance $X$ can be positive (inductance), or negative (capacitance), or zero depending on the Class-E mode. The active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector

voltage waveform is determined by the transient response of the load network when the switch is off.

To simplify an analysis of the general-circuit Class-E power amplifier, a simplified equivalent circuit of which is shown in Fig. 6.4(*b*), it is advisable to introduce the preliminary assumptions similar to those for the Class-E power amplifier with shunt capacitance. The moment of switch-on is $t = 0$ and switch-off is $t = \pi/\omega$ with a period of repeatability of input driving signal $T = 2\pi/\omega$ determined by the input drive to the power amplifier. Assume the losses in the reactive circuit elements are negligible and the loaded quality factor of the series $L_0C_0$ circuit is sufficiently high. For lossless operation, it is necessary to provide the optimum zero voltage and zero voltage-derivative conditions for voltage $v(\omega t)$ across the switch just prior to the start of switch on at the moment $t = 2\pi/\omega$, when transistor is saturated, given by Eqs. (6.1) and (6.2).

The output current flowing through the load is written as sinusoidal by

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi), \tag{6.32}$$

where $I_{\mathrm{R}}$ is the load current amplitude and $\varphi$ is the initial phase shift.

When switch is on for $0 \leq \omega t < \pi$, the voltage on the switch is

$$v(\omega t) = V_{\mathrm{cc}} - v_{\mathrm{L_b}}(\omega t) - v_{\mathrm{L}}(\omega t) = 0, \tag{6.33}$$

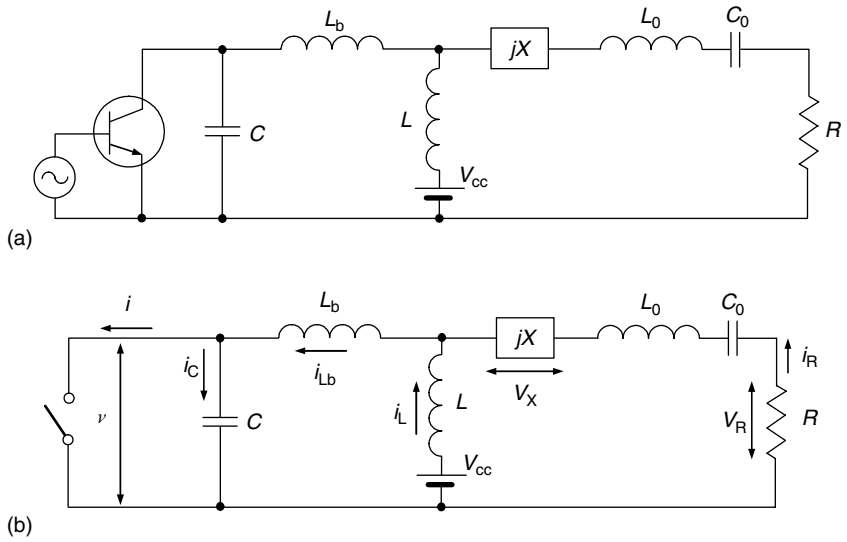



**Figure 6.4: Equivalent circuits of the Class-E power amplifiers with generalized load network.**

where

$$v_{L_b}(\omega t) = \omega L_b \frac{di(\omega t)}{d(\omega t)} \tag{6.34}$$

$$v_L(\omega t) = \omega L \frac{di_L(\omega t)}{d(\omega t)}. \tag{6.35}$$

Since the current flowing through the capacitance $C$

$$i_C(\omega t) = \omega C \frac{dv(\omega t)}{d(\omega t)} = 0, \tag{6.36}$$

the current flowing through the switch can be written using Eqs. (6.32), (6.33), and (6.35) as

$$\begin{aligned} i(\omega t) &= i_L(\omega t) + i_R(\omega t) \\ &= \frac{1}{\omega L} \int_0^{\omega t} [V_{cc} - v_{L_b}(\omega t)]\, d(\omega t) + i_L(0) + I_R \sin(\omega t + \varphi). \end{aligned} \tag{6.37}$$

Substituting Eq. (6.34) into Eq. (6.37) results in

$$i(\omega t) = \frac{V_{cc}}{\omega(L + L_b)} \omega t + \frac{\omega L}{\omega(L + L_b)} [i_L(0) + I_R \sin(\omega t + \varphi)]. \tag{6.38}$$

Since $i(0) = 0$, the initial value for the current $i_L(\omega t)$ flowing through the dc-feed inductance $L$ at $\omega t = 0$ can be found using Eq. (6.32) by

$$i_L(0) = i(0) - i_R(0) = -I_R \sin \varphi. \tag{6.39}$$

As a result,

$$i(\omega t) = \frac{V_{cc}}{\omega(L + L_b)} \omega t + \frac{\omega L I_R}{\omega(L + L_b)} [\sin(\omega t + \varphi) - \sin \varphi]. \tag{6.40}$$

When the switch is off for $\pi \leq \omega t < 2\pi$, the current $i(\omega t) = 0$ and the current $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$ flowing through the capacitance $C$ can be rewritten as

$$\begin{aligned} i_C(\omega t) &= \omega C \frac{dv(\omega t)}{d(\omega t)} = \omega C \frac{d[V_{cc} - v(\omega t) - v_{L_b}(\omega t)]}{d(\omega t)} \\ &= \frac{1}{\omega L} \int_{\pi}^{\omega t} [V_{cc} - v(\omega t) - v_{L_b}(\omega t)] d(\omega t) + i_L(\pi) + I_R \sin(\omega t + \varphi) \end{aligned} \tag{6.41}$$

under the initial off-state conditions $v(\pi) = 0$ and

$$i_{\mathrm{L}}(\pi) = i(\pi) - i_{\mathrm{R}}(\pi) = \frac{V_{\mathrm{cc}}\pi - \omega L I_{\mathrm{R}} \sin\varphi}{\omega(L + L_{\mathrm{b}})}.$$

Since the voltage $v_{\mathrm{L_b}}(\omega t)$ across the inductor $L_{\mathrm{b}}$ can be obtained from

$$v_{\mathrm{L_b}}(\omega t) = \omega L_{\mathrm{b}} \frac{di_{\mathrm{C}}(\omega t)}{d(\omega t)} = \omega^2 L_{\mathrm{b}} C \frac{d^2 v(\omega t)}{d(\omega t)^2}, \tag{6.42}$$

Eq. (6.41) can be rewritten in the form of

$$\begin{aligned} \omega C \frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L} \int_{\pi}^{\omega t} \left[ V_{\mathrm{cc}} - v(\omega t) - \omega L_{\mathrm{b}} C \frac{d^2 v(\omega t)}{d(\omega t)^2} \right] d(\omega t) \\ + i_{\mathrm{L}}(\pi) + I_{\mathrm{R}} \sin(\omega t + \varphi). \end{aligned} \tag{6.43}$$

As a result, by differentiating both sides of Eq. (6.43) and combining similar terms, it can be represented in the form of the linear non-homogeneous second-order differential equation as

$$\omega^2 (L + L_{\mathrm{b}}) C \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{\mathrm{cc}} - \omega L I_{\mathrm{R}} \cos(\omega t + \varphi) = 0, \tag{6.44}$$

the general solution of which can be obtained in the normalized form of

$$\frac{v(\omega t)}{V_{\mathrm{cc}}} = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1 - q^2} \cos(\omega t + \varphi), \tag{6.45}$$

where

$$q = \frac{1}{\omega\sqrt{(L + L_{\mathrm{b}})C}} \tag{6.46}$$

$$p = \frac{\omega L I_{\mathrm{R}}}{V_{\mathrm{cc}}} \tag{6.47}$$

and the coefficients $C_1$ and $C_2$ are determined from the initial off-state conditions by

$$C_1 = -(\cos q\pi + q\pi \sin q\pi) - \frac{qp}{1 - q^2} \left[ q \cos\varphi \cos q\pi - (1 - 2q^2) \sin\varphi \sin q\pi \right] \tag{6.48}$$

$$C_2 = (q\pi\cos q\pi - \sin q\pi) - \frac{qp}{1-q^2}[q\cos\varphi\sin q\pi + (1-2q^2)\sin\varphi\cos q\pi]. \tag{6.49}$$

The dc supply current $I_0$ can be found using Fourier formula and Eq. (6.40) by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\,d(\omega t) = \frac{I_R}{2\pi}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right)\Big/\left(1+\frac{L_b}{L}\right). \tag{6.50}$$

In an idealized Class-E operation mode, there is no nonzero voltage and current simultaneously that means a lack of the power losses and gives an idealized collector efficiency of 100%. This implies that the dc power and fundamental output power are equal,

$$I_0 V_{cc} = \frac{V_R^2}{2R}, \tag{6.51}$$

where $V_R = I_R R$ is the fundamental voltage amplitude across the load resistance $R$.

As a result, by using Eqs. (6.50) and (6.51) and taking into account that $R = V_R^2/2P_{out}$, the optimum load resistance $R$ for the specified values of a supply voltage $V_{cc}$ and a fundamental output power $P_{out}$ can be obtained by

$$R = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2\frac{V_{cc}^2}{P_{out}}, \tag{6.52}$$

where

$$\frac{V_R}{V_{cc}} = \frac{1}{\pi}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right)\Big/\left(1+\frac{L_b}{L}\right). \tag{6.53}$$

The normalized load network inductance $L$ and capacitance $C$ as a function of the ratio $L_b/L$ can be appropriately defined using Eqs. (6.46), (6.47), and (6.50) by

$$\frac{\omega L}{R} = p\left(1+\frac{L_b}{L}\right)\Big/\left(\frac{\pi}{2p} + \frac{2}{\pi}\cos\varphi - \sin\varphi\right) \tag{6.54}$$

$$\omega CR = 1/q^2\left(1+\frac{L_b}{L}\right)\frac{\omega L}{R}. \tag{6.55}$$

The series reactance $X$, which may have an inductive, capacitive, or zero reactance in special particular cases, depending on the load-network parameters, can be generally calculated using the two quadrature fundamental-frequency voltage Fourier components of

$$V_{\mathrm{R}} = -\frac{1}{\pi}\int_{0}^{2\pi}[v(\omega t) + v_{\mathrm{L_b}}(\omega t)]\ \sin(\omega t + \varphi)\, d(\omega t) \tag{6.56}$$

$$V_{\mathrm{X}} = -\frac{1}{\pi}\int_{0}^{2\pi}[v(\omega t) + v_{\mathrm{L_b}}(\omega t)]\ \cos(\omega t + \varphi)\, d(\omega t). \tag{6.57}$$

Generally, Eq. (6.45) for a normalized collector voltage contains the three unknown parameters $q$, $p$, and $\varphi$, which must be determined. In a common case, the parameter $q$ can be considered a variable, and the other two parameters $p$ and $\varphi$ are determined from a system of the two equations resulting from applying the two optimum zero voltage and zero voltage-derivative conditions given by Eqs. (6.1) and (6.2) to Eq. (6.45). Fig. 6.5 shows the dependencies of the optimum parameters $p$ and $\varphi$ versus $q$ for a Class E with finite dc-feed inductance with $L_{\mathrm{b}} = 0$.

However, there is a specific point of $q = 1$ in Eq. (6.45) when the denominator of its last term becomes zero. Therefore, it is necessary to define the optimum parameters corresponding to this special point separately. Such a case when $q = 1$ means that the parallel circuit comprising a dc-feed inductor $L$ and a shunt capacitor $C$ is tuned to the fundamental frequency. This implies in turn that the imaginary fundamental-frequency collector-current component is of equal to zero. Generally, the fundamental-frequency current flowing through the switch consists

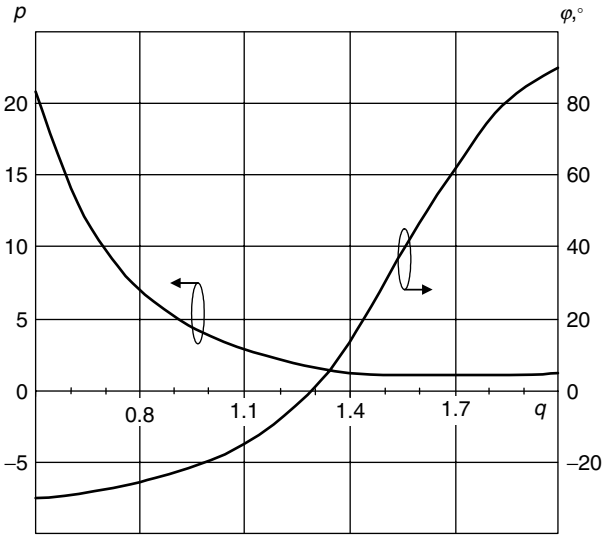



**Figure 6.5: Optimum parallel-circuit Class-E parameters $p$ and $\varphi$ versus $q$.**

of the two quadrature components, the amplitudes of which can be found using Fourier formulas and Eq. (6.40) by

$$I_{\mathrm{R}} = \frac{1}{\pi}\int_{0}^{2\pi} i(\omega t)\sin(\omega t+\varphi)\,d(\omega t)$$
$$= \frac{I_{\mathrm{R}}}{\pi}\left[\frac{\pi\cos\varphi - 2\sin\varphi}{p} + \frac{\pi}{2} - \sin 2\varphi\right] \tag{6.58}$$

$$I_{\mathrm{X}} = -\frac{1}{\pi}\int_{0}^{2\pi} i(\omega t)\cos(\omega t+\varphi)\,d(\omega t)$$
$$= \frac{I_{\mathrm{R}}}{\pi}\left[\frac{\pi\sin\varphi + 2\cos\varphi}{p} - 2\sin^2\varphi\right] = 0. \tag{6.59}$$

Hence, the optimum parameters $p$ and $\varphi$ can be calculated as

$$p = -\frac{4}{\pi\sin\varphi} = 3.84 \tag{6.60}$$

$$\varphi = \tan^{-1}\left(-\frac{2\pi}{\pi^2+8}\right) = -19.4^{\circ}. \tag{6.61}$$

Based on the calculated optimum parameters $p$ and $\varphi$ as functions of $q$, the optimum load-network parameters of the Class-E load network with a finite dc-feed inductance can be determined using Eqs. (6.52) to (6.55). The series reactance $X$ can be calculated through the ratio of the two quadrature fundamental-frequency voltage Fourier components given in Eqs. (6.56) and (6.57) as

$$\frac{X}{R} = \frac{V_{\mathrm{X}}}{V_{\mathrm{R}}}. \tag{6.62}$$

The dependencies of the normalized optimum dc-feed inductance $\omega L/R$ and series reactance $X/R$ are shown in Fig. 6.6($a$), while the dependencies of the normalized optimum shunt capacitance $\omega CR$ and load resistance $RP_{\mathrm{out}}/V_{\mathrm{cc}}^2$ are plotted in Fig. 6.6($b$). Here, we can see that the subharmonic case of $q = 0.5$ is very close to a Class-E mode with shunt capacitance since the value of the normalized inductance $\omega L/R$ is sufficiently high and the variations of normalized values of $\omega CR$ and $RP_{\mathrm{out}}/V_{\mathrm{cc}}^2$ are insignificant. The value of the series reactance $X$ changes its sign from positive to negative, which means the inductive reactance is followed by the capacitive reactance. As a result, there is a special case of a load network with a parallel circuit and a load resistance only when $X = 0$ at $q = 1.412$. In this case, the maximum value of

the optimum load resistance $R$ is provided for the same supply voltage and output power, thus simplifying the matching with the standard load of 50 Ω. Also, the values of a dc-feed inductance $L$ become smaller, making Class E very attractive for monolithic applications. The maximum operation frequency $f_{max}$ is realized at $q = 1.468$ where the normalized optimum shunt capacitance $\omega CR$ reaches its maximum.

The graphical solutions for the optimum load network parameters can be replaced by the analytical design equations represented in terms of the simple second-order and third-order polynomial functions given in Tables 6.1 and 6.2 for different ranges of the parameter $q$ [16].

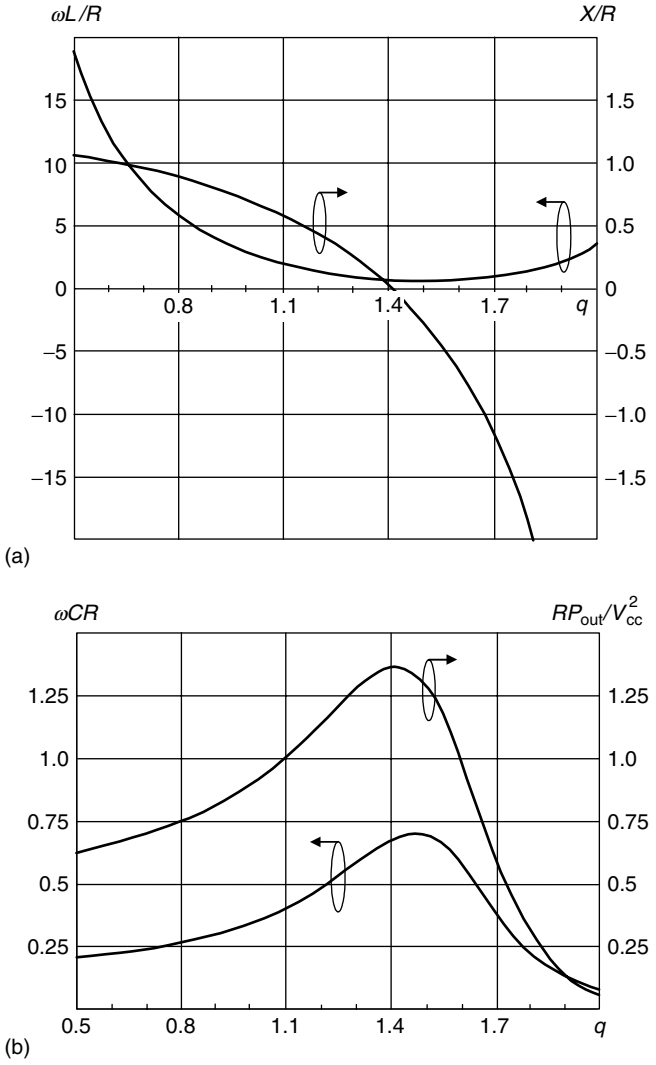



**Figure 6.6: Normalized optimum parallel-circuit Class-E load network parameters.**

**Table 6.1: Load Network Parameters for $0.6 < q < 1.0$**

| Parameter | Design Equation |
|---|---|
| $\frac{\omega L}{R}$ | $44.93q^2 - 94.32q + 52.46$ |
| $\omega CR$ | $0.426q^2 - 0.379q + 0.3$ |
| $\frac{X}{R}$ | $-0.73q^2 + 0.411q + 1.03$ |
| $\frac{P_{out}R}{V_{cc}^2}$ | $0.74q^2 - 0.6q + 0.76$ |

**Table 6.2: Load Network Parameters for $1.0 < q < 1.65$**

| Parameter | Design Equation |
|---|---|
| $\frac{\omega L}{R}$ | $8.085q^2 - 24.53q + 19.23$ |
| $\omega CR$ | $-6.97q^3 + 25.93q^2 - 31.071q + 12.48$ |
| $\frac{X}{R}$ | $-2.9q^3 + 8.8q^2 - 10.2q + 5.02$ |
| $\frac{P_{out}R}{V_{cc}^2}$ | $-11.9q^3 + 42.753q^2 - 49.63q + 19.7$ |

The maximum difference between the polynomial approximations and exact numerical solutions given in the graphic form is about 2%.

Now let us consider the particular cases of the Class-E operation mode like subharmonic Class E with $q = 0.5$, parallel-circuit Class E with $X = 0$, and even-harmonic Class E with $q = 2n$ assuming $L_b = 0$, which can be easily and explicitly described analytically. Then, the effect of a bond-wire inductor $L_b$ on the parameters of a Class-E load network will be described in the example of a parallel-circuit Class E.

## 6.3 Subharmonic Class E

The basic circuit of a switched-mode subharmonic Class-E power amplifier is shown in Fig. 6.7. The load network consists of a parallel inductance $L$, a shunt capacitance $C$, a series $L_0C_0$-resonant circuit tuned on the fundamental, and a load $R$. The condition of a subharmonic tuning implies that the inductance $L$ resonates with the capacitance $C$ at half a fundamental frequency $f_0$. In this case, to provide an inductive reactance at the fundamental frequency seen by the device collector, it is necessary to include a series inductance $L_X$. Hence, the first unknown parameter $q$ can be set to

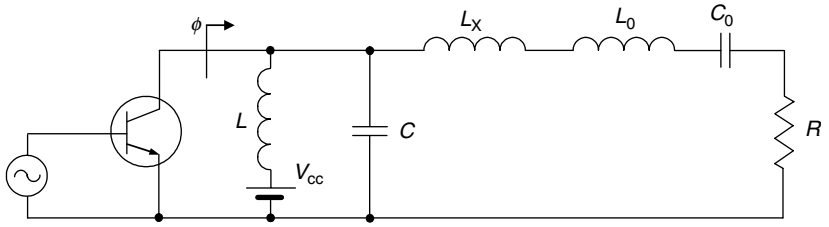



**Figure 6.7: Equivalent circuit of the subharmonic Class-E power amplifier.**

$$q = 0.5. \tag{6.63}$$

The coefficients $C_1$ and $C_2$ are determined from

$$C_1 = -\frac{\pi}{2} + \frac{p}{3}\sin\varphi \tag{6.64}$$

$$C_2 = -1 - \frac{p}{3}\cos\varphi. \tag{6.65}$$

Then, the other two parameters $\varphi$ and $p$ can be found by applying the optimum Class-E condition given by Eqs. (6.1) and (6.2) to Eq. (6.45) and using Eqs. (6.64) and (6.65) as

$$\varphi = \tan^{-1}\left(-\frac{\pi + 4}{2\pi + 6}\right) = -30.2^\circ \tag{6.66}$$

$$p = \frac{3\pi + 9}{\cos\varphi} = 21.3. \tag{6.67}$$

Fig. 6.8 shows the normalized collector (*a*) voltage and (*b*) current waveforms for idealized optimum subharmonic Class-E mode. From collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch, and current $i(\omega t)$ consisting of the load sinusoidal and inductive current flows through the device. The collector voltage and current waveforms are very similar to those of a Class E with shunt capacitance.

As a result, for a subharmonic Class-E mode, the optimum load resistance $R$, finite dc-feed inductance $L$, and shunt capacitance $C$ using Eqs. (6.52) to (6.55) can be obtained by

$$R = 0.635\frac{V_{cc}^2}{P_{out}} \tag{6.68}$$

$$L = 18.9\frac{R}{\omega} \tag{6.69}$$

$$C = \frac{0.212}{\omega R}. \tag{6.70}$$

To define the phase-shifting series inductance $L_X$, it is necessary to solve Eq. (6.57) for an imaginary component of the fundamental-frequency voltage amplitude $V_X$, which can be simplified to

$$\frac{V_X}{V_{cc}} = \frac{4}{3\pi}[(C_1 - C_2)\sin\varphi + 0.5(C_1 + C_2)\cos\varphi] - \frac{2\sin\varphi}{\pi} + \frac{p}{6}. \tag{6.71}$$

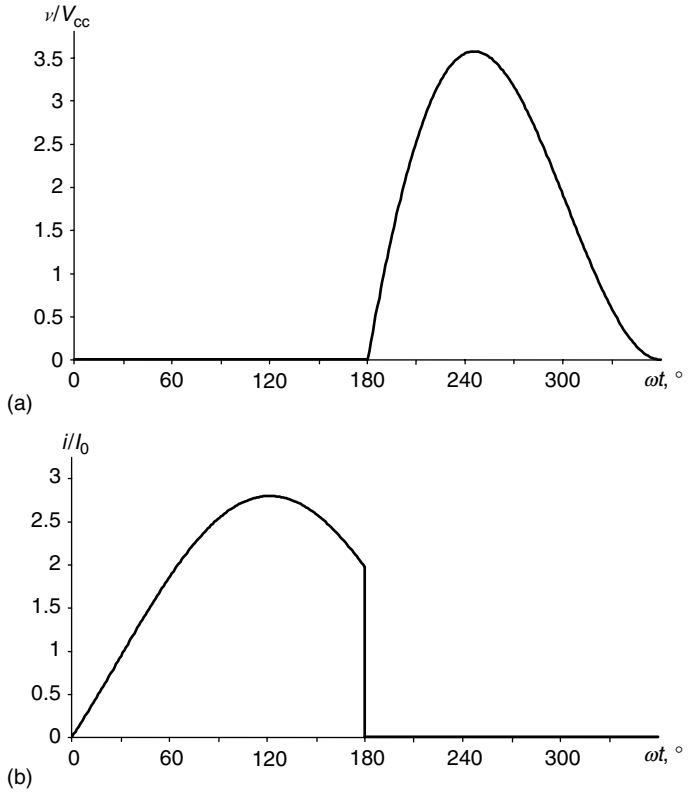



**Figure 6.8: Normalized collector (*a*) voltage and (*b*) current waveforms for idealized optimum subharmonic Class E.**

Thus, using Eqs. (6.53), (6.64), and (6.65) yields

$$L_X = \frac{V_X}{V_R}\frac{R}{\omega} = 1.058\frac{R}{\omega}. \tag{6.72}$$

The peak collector current $I_{max}$ and peak collector voltage $V_{max}$ can be determined from Eqs. (6.40), (6.45), and (6.50) as

$$I_{max} = 2.843I_0 \tag{6.73}$$

$$V_{max} = 3.571V_{cc}. \tag{6.74}$$

From Eqs. (6.68), (6.70), and (6.72) it follows that reducing a value of the dc-feed inductance to the case when it resonates with the shunt capacitance at half the fundamental frequency contributes to the causing of small variations of the optimum load network parameters $C$, $L_X$, and $R$ derived for a Class E with shunt capacitance, within approximately only 10% .

## 6.4 Parallel-Circuit Class E

The theoretical analysis of a switched-mode parallel-circuit Class-E power amplifier using a series filter with the calculation of the voltage and current waveforms and some graphical results was done by V. B. Kozyrev [17, 18]. Let us analyze the parallel-circuit Class-E mode in more detail. The basic circuit of a switched-mode parallel-circuit Class-E power amplifier is shown in Fig. 6.9(*a*). The load network consists of a finite dc-feed inductor $L$, a shunt capacitor $C$, a series $L_0C_0$-resonant circuit tuned to the fundamental frequency, and a load resistor $R$. In this case, the switch sees a parallel connection of the load resistor $R$ and parallel LC circuit at the fundamental frequency as shown in Fig. 6.9(*b*), where also the real and imaginary collector fundamental-frequency current components $I_X$ and $I_R$ and real collector fundamental-frequency voltage component $V_R$ are indicated.

For a subharmonic Class-E mode, to compensate for the resulting phase shift provided by the finite dc-feed inductance and shunt capacitance tuned to half of the fundamental frequency, it is required to include an additional series phase-shifting inductance $L_X$. In the case of a parallel-circuit Class-E load network without series phase-shifting reactance, since the parameter $q$ is unknown, generally it is necessary to solve a system of three equations to define the three unknown parameters $q$, $p$, and $\varphi$. The two equations are the result of applying the two optimum zero voltage and zero voltage-derivative conditions given by Eqs. (6.1) and (6.2) to Eq. (6.45). Since the fundamental-frequency collector voltage is fully applied to the load, this means that its reactive part must have zero value resulting in an additional equation

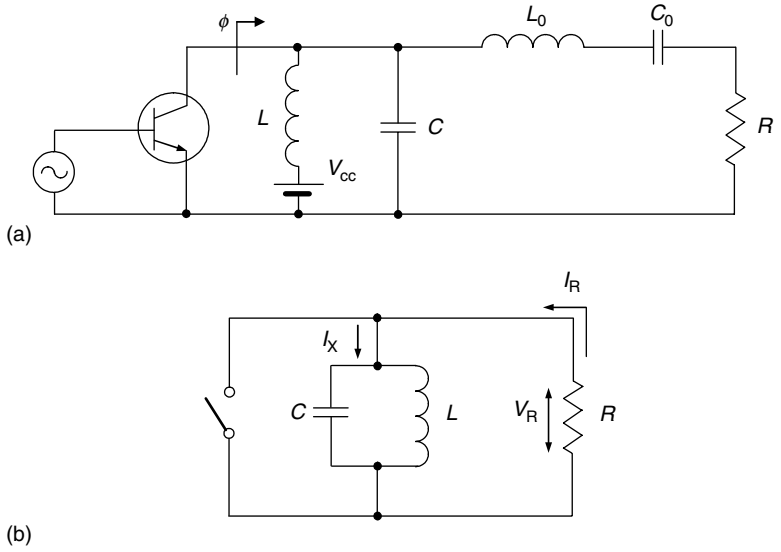



**Figure 6.9: Equivalent circuits of the parallel-circuit Class-E power amplifier.**

$$V_X = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)\, d(\omega t) = 0. \tag{6.75}$$

Solving the system of three equations with three unknown parameters numerically gives the following values [19, 20]:

$$q = 1.412 \tag{6.76}$$

$$p = 1.210 \tag{6.77}$$

$$\varphi = 15.155^\circ. \tag{6.78}$$

Fig. 6.10 shows the normalized (*a*) load current and collector, (*b*) voltage, and (*c*) current waveforms for an idealized optimum parallel-circuit Class-E operation. From collector voltage and current waveforms it follows that, similar to other Class-E subclasses, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized collector efficiency of 100% is achieved. The normalized currents flowing through the load network (*a*) shunt capacitance $C$ and (*b*) finite dc-feed inductance $L$ for an idealized optimum parallel-circuit Class-E operation mode are given in Fig. 6.11.

By using Eqs. (6.52) to (6.55), the optimum load resistance $R$, parallel inductance $L$, and parallel capacitance $C$ can be appropriately obtained by

$$R = 1.365\frac{V_{cc}^2}{P_{out}} \tag{6.79}$$

$$L = 0.732\frac{R}{\omega} \tag{6.80}$$

$$C = \frac{0.685}{\omega R}. \tag{6.81}$$

The dc supply current $I_0$ can be calculated from Eq. (6.50) as

$$I_0 = 0.826 I_R. \tag{6.82}$$

The phase angle $\phi$ seen from the device collector at the fundamental frequency can be represented either through the two quadrature fundamental-frequency current Fourier components $I_X$ and $I_R$ or as a function of load network elements by

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = 34.244^\circ. \tag{6.83}$$

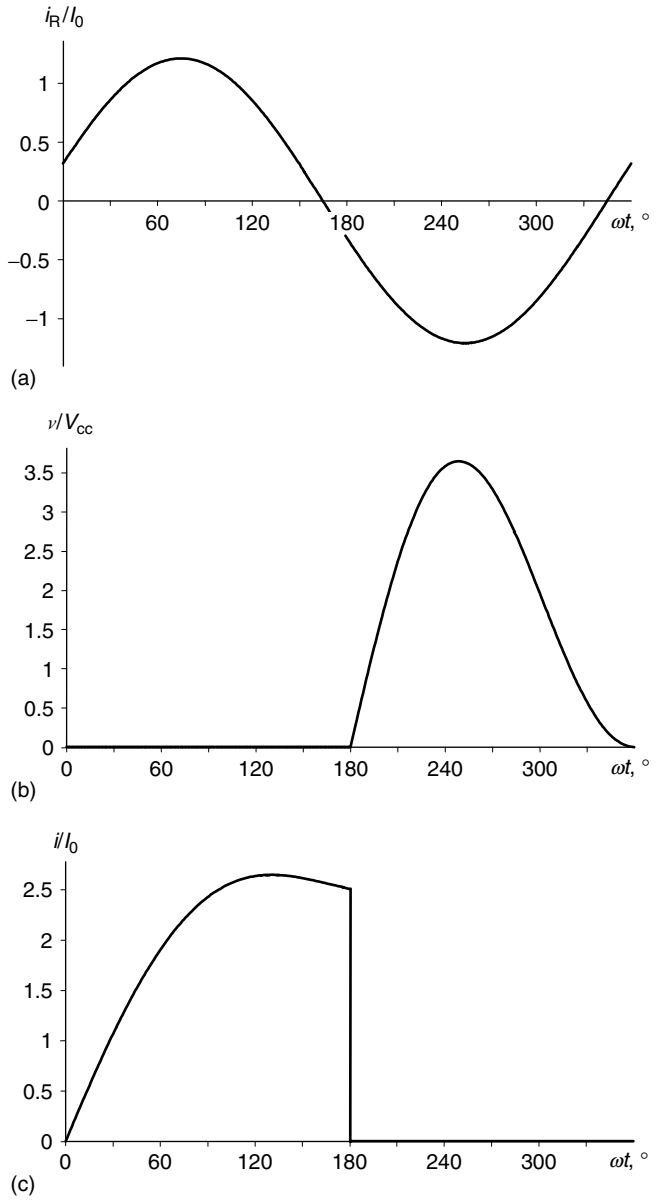



**Figure 6.10: Normalized (*a*) load current and collector, (*b*) voltage, and (*c*) current waveforms for idealized optimum parallel-circuit Class E.**

If the calculated value of the optimum Class-E resistance $R$ is too small or differs significantly from the required load impedance, it is necessary to use an additional matching circuit to deliver maximum output power to the load. It should be noted that, among a family of the Class-E load networks, a parallel-circuit Class-E load network offers the largest value of $R$,

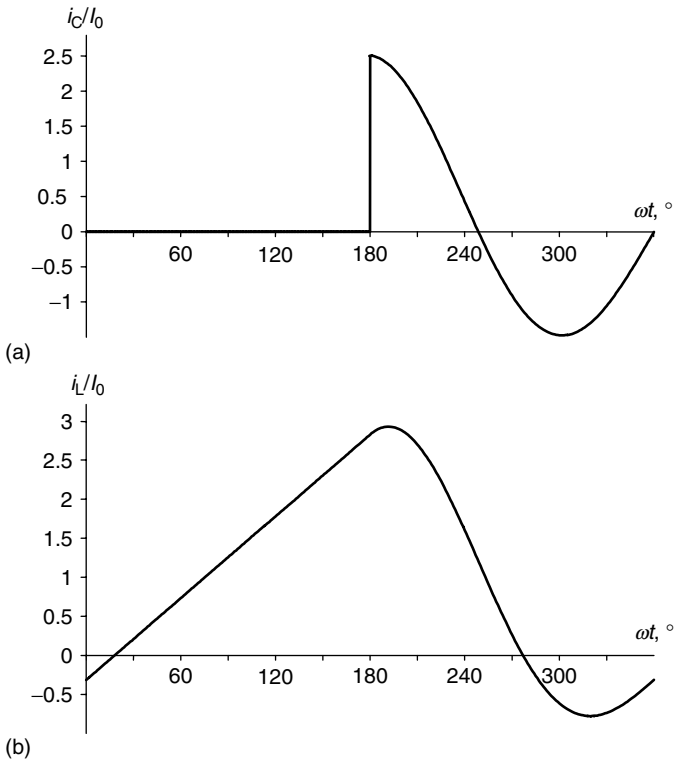



**Figure 6.11: Normalized currents flowing through load network parallel (*a*) capacitance and (*b*) inductance for idealized optimum parallel-circuit Class E.**

thus simplifying the final matching design procedure. In this case, the first series element of such matching circuits should be the inductor to provide high impedance conditions for harmonics, as shown in Fig. 6.12.

The peak collector current $I_{max}$ and peak collector voltage $V_{max}$ can be determined from Eqs. (6.40), (6.45), and (6.82) as

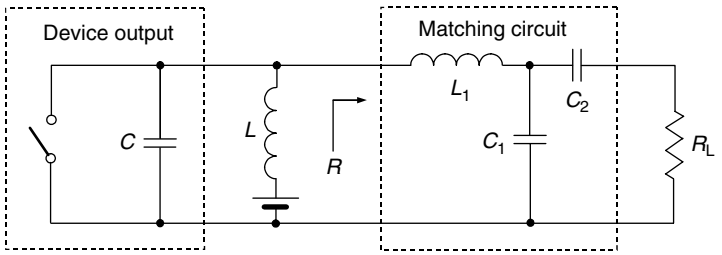



**Figure 6.12: Parallel-circuit Class-E power amplifier with lumped matching circuit.**

$$I_{\max} = 2.647 I_0 \tag{6.84}$$

$$V_{\max} = 3.647 V_{cc}. \tag{6.85}$$

When realizing the optimum Class-E operation mode, it is important to know the maximum frequency such an efficient operation mode can achieve. In this case, it is advisable to establish a relationship between the maximum frequency $f_{\max}$, device output capacitance $C_{out}$, and supply voltage $V_{cc}$. The device output capacitance $C_{out}$ gives the main limitation of the maximum operation frequency, as it is an intrinsic device parameter and cannot be reduced for a given active device. As a result, using Eqs. (6.79) and (6.81), when $C = C_{out}$ gives the value of maximum operation frequency of

$$f_{\max} = 0.0798 \frac{P_{out}}{C_{out} V_{cc}^2}, \tag{6.86}$$

which is 1.4 times higher than the maximum operation frequency for an optimum Class-E power amplifier with shunt capacitance [21].

## 6.5 Even-Harmonic Class E

The well-defined analytic solution was based on an assumption of the even-harmonic resonant conditions when the finite dc-feed inductance and parallel capacitance are tuned on any even-harmonic component [22]. The load network of an even-harmonic Class E is shown in Fig. 6.13 where, to compensate the required phase shift caused by the preliminary choice of particular load network parameters, the series capacitor $C_X$ is needed. The value of this capacitance can be found from the consideration of two fundamental voltage quadrature components across the switch given by Eqs. (6.56) and (6.57).

Since, for an even-harmonic Class E, the dc-feed inductance is restricted to values that satisfy an even-harmonic resonance condition and it is assumed the fundamental voltage across the switch and output voltage across the load have a phase difference of $\pi/2$, the two unknown parameters can be set in this particular case as

$$q = 2n \tag{6.87}$$

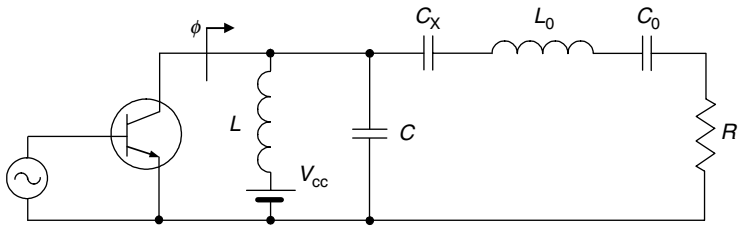



**Figure 6.13: Equivalent circuit of the even-harmonic Class-E power amplifier.**

$$\varphi = 90^\circ, \tag{6.88}$$

where $n = 1, 2, 3, \ldots$.

The third parameter $p$ can be found using an optimum condition given by Eq. (6.2) as

$$p = \frac{4n^2 - 1}{8n^2}\pi. \tag{6.89}$$

The dc supply current $I_0$ can be found from Eq. (6.50) when $L_b = 0$ by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\, d(\omega t) = \frac{1}{2(4n^2 - 1)} I_R. \tag{6.90}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \leq \omega t < 2\pi$ and current waveform for period of $0 \leq \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = 1 - \frac{\pi}{2}\sin\omega t + \frac{\pi}{4n}\sin(2n\omega t) - \cos(2n\omega t) \tag{6.91}$$

$$\frac{i(\omega t)}{I_0} = 2\left[\frac{8n^2}{\pi}\omega t - 4n^2 + 1 + (4n^2 - 1)\cos\omega t\right]. \tag{6.92}$$

Fig. 6.14 shows the normalized (*a*) load current and collector, (*b*) voltage, and (*c*) current waveforms for an idealized optimum even-harmonic Class-E mode. If the collector voltage waveform of an even-harmonic Class E is very similar to the collector voltage waveform of a Class E with shunt capacitance, then the behavior of the current waveform is substantially different. So, for even harmonic Class-E configuration, the collector current reaches its peak value, which is four times as high as the dc current, at the end of the conduction interval. Consequently, in the case of a sinusoidal driving signal it is impossible to provide close to the maximum collector current when the input base current is smoothly reducing to zero.

The optimum load-network parameters for the most practical case $n = 1$ can be calculated from

$$R = \frac{1}{18}\frac{V_{cc}^2}{P_{out}} = 0.056\frac{V_{cc}^2}{P_{out}} \tag{6.93}$$

$$L = \frac{9\pi}{8}\frac{R}{\omega} = 3.534\frac{R}{\omega} \tag{6.94}$$

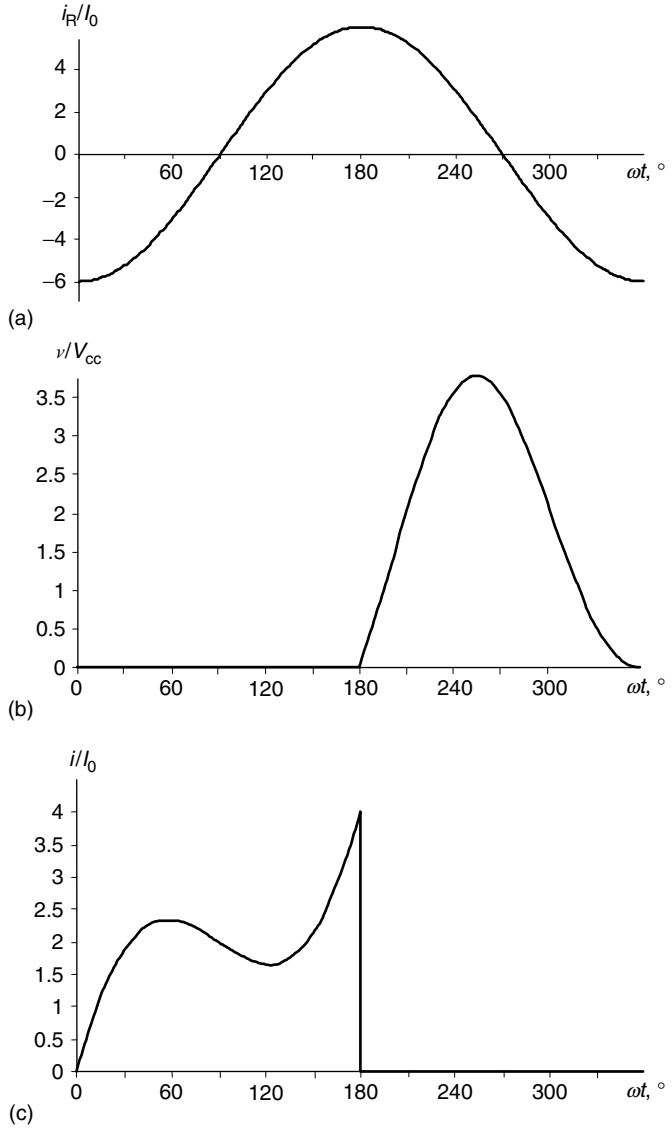



**Figure 6.14: Normalized (*a*) load current and collector, (*b*) voltage, and (*c*) current waveforms for idealized optimum even-harmonic Class E.**

$$C = \frac{2}{9\pi}\,\frac{1}{\omega R} = 0.071\,\frac{1}{\omega R} \tag{6.95}$$

$$C_X = \frac{4\pi}{32 + 3\pi^2}\,\frac{1}{\omega R} = 0.204\,\frac{1}{\omega R}. \tag{6.96}$$

The main problem of an even-harmonic Class-E mode is a substantially small value of the load resistance $R$, which is over an order of magnitude smaller than for a Class E with shunt capacitance and much smaller than for a parallel-circuit Class E.

The phase angle $\phi$ between the fundamental-frequency voltage and current components seen by switch is equal to

$$\phi = \frac{3}{4}\frac{R}{\omega L}\frac{1+(\omega C_X R)^2}{(\omega C_X R)^2} - \frac{1}{\omega C_X R} = 22.302^\circ, \tag{6.97}$$

while the maximum frequency $f_{max}$, up to which an optimum even-harmonic Class E can be realized, is calculated from

$$f_{max} = \frac{2}{\pi^2}\frac{P_{out}}{C_{out}V_{cc}^2} = 0.203\frac{P_{out}}{C_{out}V_{cc}^2}, \tag{6.98}$$

where $C_{out}$ is the device output capacitance.

## 6.6 Effect of Bond-wire Inductance

At higher frequencies when the discrete power transistors are used in hybrid power-amplifier integrated circuits, it is necessary to take into account the device output bond-wire and lead inductance. Its influence may be significant, especially in the practical cases of high output power level and low supply voltage. For instance, the effect of a bond-wire inductance for even-harmonic Class-E configuration gives unrealistically small values for the optimum load resistance and dc-feed inductance when, even at ultra-high frequencies, typical values for the

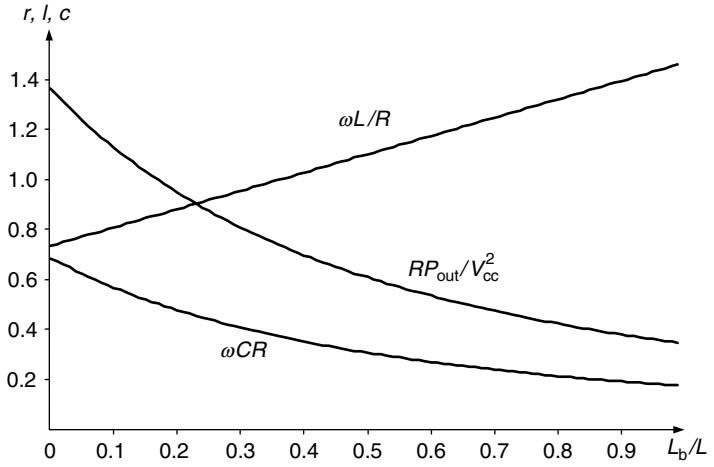



**Figure 6.15: Normalized optimum load network parameters versus normalized bondwire inductance $L_b/L$ for parallel-circuit Class E.**

bond-wire inductance of approximately. 1 nH constitute most, if not all, of the required dc-feed inductance [23].

The exact values for the optimum load network parameters can be easily obtained from Eqs. (6.52) to (6.55), which were derived analytically for a generalized Class-E load network. Fig. 6.15 shows the dependencies of the normalized parallel inductance $l = \omega L/R$, parallel capacitance $c = \omega CR$, and load resistance $r = RP_{\text{out}}/V_{\text{cc}}^2$ for a parallel-circuit Class-E mode as functions of the normalized bond-wire inductance $L_{\text{b}}/L$. From Fig. 6.15 it follows that an increasing effect of the bond-wire inductance $L_{\text{b}}$ leads to significantly reduced Class-E optimum values for the load resistance $R$ and shunt capacitance $C$ and increased optimum value for the finite dc-feed inductance $L$.

## 6.7 Load Network with Transmission Lines

At ultra-high and microwave frequencies, generally all inductances in the load-network circuits of the power amplifier are normally replaced by the transmission lines to minimize power losses and effects of the parasitic capacitances. The load-network circuit can be composed with any types of transmission lines including open-circuit or short-circuit stubs to provide the required matching and harmonic-suppression conditions. In some cases, for instance, for compact small-size power-amplifier modules developed for handset wireless transmitters, it is advisable to use series microstrip lines and shunt chip capacitors. Using a lumped-distributed Class-E load network structure with short-length transmission lines can be very effective and helpful to increase the efficiency of a microwave power amplifier [24]. Generally, the transmission-line modeling (TLM) technique in the time domain can be used to simulate the Class-E power amplifier. By means of the TLM technique, the load network elements can be modeled by the open-circuited and short-circuited stubs [25]. However, the TLM technique cannot be used to evaluate the required optimum parameter values directly to obtain the desired performance and the optimum conditions cannot be ensured. Idealized calculation of the collector voltage and current waveforms in the frequency domain, required for an optimum Class-E mode, implies the availability of an infinite number of harmonics with their optimum amplitudes and phases in the output spectrum.

First, consider a contribution of any harmonic in close approximation to a parallel-circuit Class-E mode similar to that for a Class E with shunt capacitance. The Fourier-series expansion of the collector voltage $v(\omega t)$ is defined as

$$v(\omega t) = V_{\text{cc}} + \sum_{\text{k}=1}^{\infty} [V_{\text{Rk}} \sin k(\omega t + \varphi) + V_{\text{Xk}} \cos k(\omega t + \varphi)], \tag{6.99}$$

where the dc supply voltage $V_{\text{cc}}$ and the real and imaginary harmonic components $V_{\text{Rk}}$ and $V_{\text{Xk}}$ are obtained respectively from

$$V_{cc} = \frac{1}{2\pi} \int_0^{2\pi} v(\omega t) d(\omega t) \tag{6.100}$$

$$V_{Rk} = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin k(\omega t + \varphi)\, d(\omega t) \tag{6.101}$$

$$V_{Xk} = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \cos k(\omega t + \varphi)\, d(\omega t). \tag{6.102}$$

The same Fourier analysis can be applied to the collector current $i(\omega t)$. Fig. 6.16 shows the normalized ideal collector (*a*) voltage and (*b*) current waveforms plotted by solid lines, where $I_0$ is the dc current. However, it is also clearly seen that a good approximation to a parallel-circuit Class-E mode can be obtained with only the fundamental-frequency and second harmonic components accounted for the collector voltage and current waveforms as

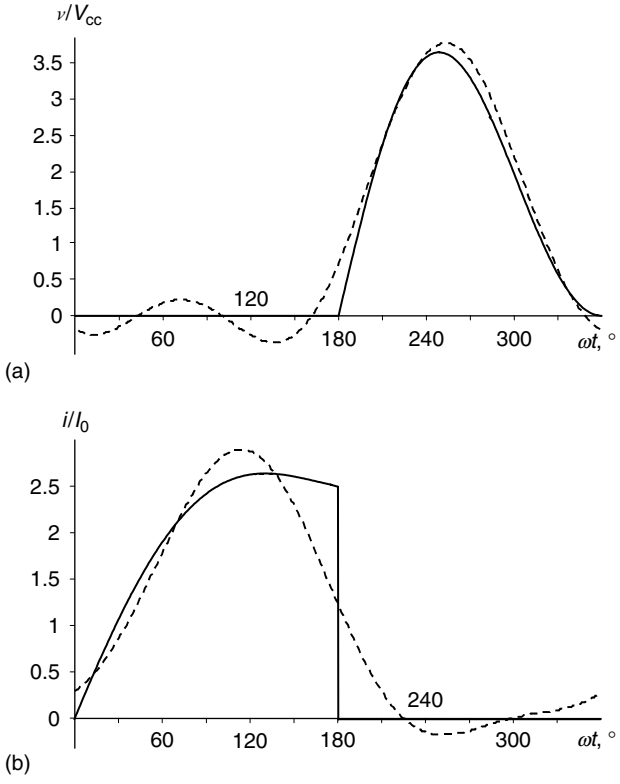



**Figure 6.16: Two-harmonic approximation to parallel-circuit Class E.**

indicated by the dashed lines. The same conclusion, being very important for practical design of microwave Class-E power amplifiers, was obtained for a Class-E mode with shunt capacitance [26]. Consequently, the high-efficiency parallel-circuit Class-E power-amplifier circuit can also be used effectively in monolithic microwave-integrated circuit (MMIC) design provided the optimum conditions for the fundamental frequency and second harmonic are fulfilled.

As a first step, the parallel inductance $L$ at microwaves should be replaced by a short-length short-circuited transmission line $TL$ as shown in Fig. 6.17($a$) according to

$$Z_0 \tan\theta = \omega L, \tag{6.103}$$

where $Z_0$ and $\theta$ are the characteristic impedance and electrical length of the transmission line $TL$, respectively [27]. To approximate the idealized parallel-circuit Class-E operation conditions for a microwave power amplifier, it is necessary to design the load network satisfying the required idealized optimum input impedance at fundamental frequency of

$$Z_{\text{net}}(\omega_0) = \frac{R}{1 - j\tan 34.244^\circ}, \tag{6.104}$$

which can be obtained from Eqs. (6.80), (6.81), and (6.83).

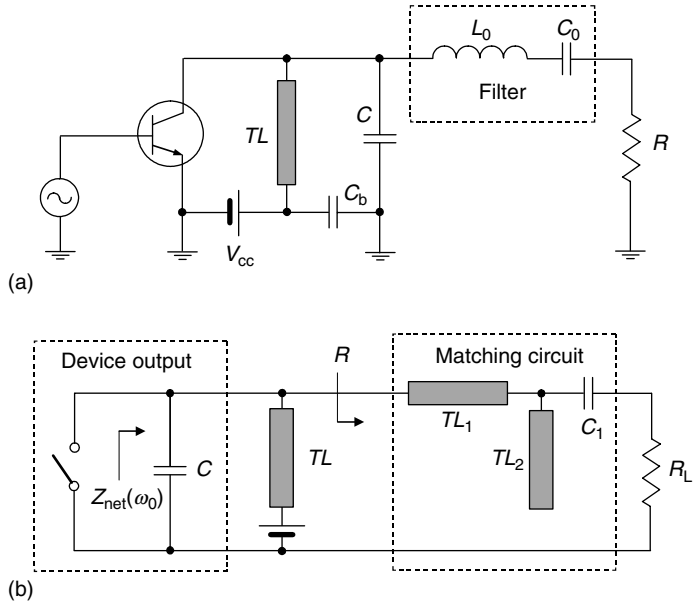



**Figure 6.17: Equivalent circuits of transmission-line parallel-circuit Class-E power amplifier.**

By using Eq. (6.80), defining the optimum parallel inductance $L$ for a parallel-circuit Class-E mode, Eq. (6.103) can be rewritten as

$$\tan\theta = 0.732\frac{R}{Z_0}. \tag{6.105}$$

In practical circuits, when the impedance transformation between the optimum load resistance $R$ and standard load resistance of $50\,\Omega$ is required, the series $L_0C_0$ filter should be replaced by the output-matching circuit, the input impedance of which needs to be sufficiently high at second and higher-order harmonics. For example, the series $L_0C_0$ filter can be replaced by a $T$-transformer containing two lumped capacitors and a lumped inductor. For a transmission-line realization, the output-matching circuit can be composed with any types of transmission lines including open-circuit or short-circuit stubs to provide the required matching and harmonic-suppression conditions. However, to maintain the optimum-switching conditions at the fundamental frequency, this output-matching circuit should contain the series transmission line as the first element, as shown in Fig. 6.17(*b*).

Fig. 6.18(*a*) shows an example of the transmission-line Class-E load network of a 1.75–1.91 GHz 2 W InGaP/GaAs HBT power amplifier, which was developed for a cellular handset transmitter-power amplifier, and includes the series microstrip line with two shunt chip capacitances [19, 28]. However, because of the finite electrical lengths of the transmission lines, it is impossible to realize simultaneously the required inductive impedance

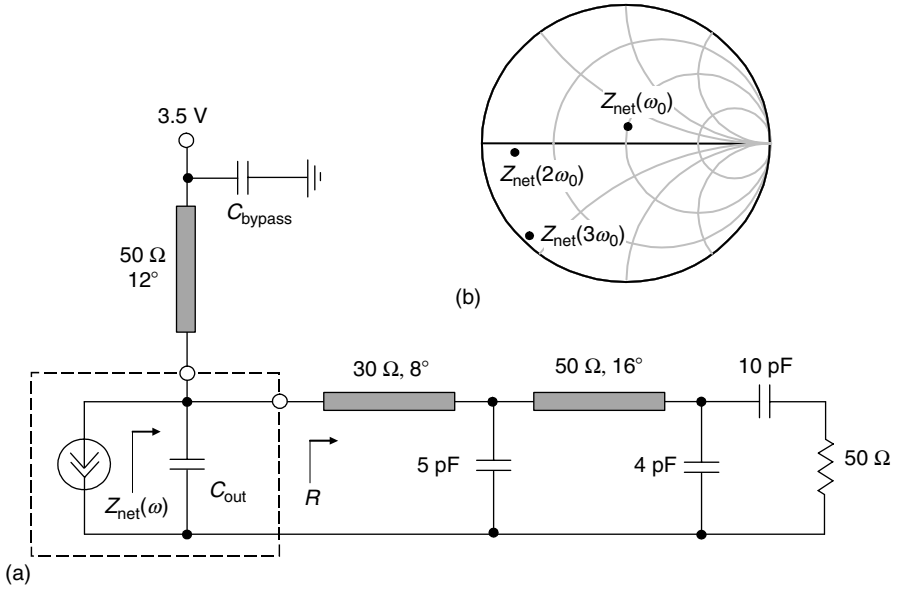



**Figure 6.18: Transmission-line load network of parallel-circuit Class-E power amplifier for handset application.**

at the fundamental frequency with the purely capacitive reactances at higher-order harmonics. For example, at the second harmonic, the real part of the load network impedance $Z_{net}(2\omega_0)$ is sufficiently high, as shown in Fig. 6.18(*b*). However, even this approximation is a good proximity to a parallel-circuit Class-E operation mode resulting in a high operating efficiency of the power amplifier. In this case, there is no need to use an additional RF choke for a dc supply current, whose function can be performed by a very short-length parallel microstrip line.

Comparison of the different Class-E load network topologies in terms of their parameters shows a clear preference of a parallel-circuit Class-E mode, especially for low supply voltage application with a high level of circuit integration. For such a load network, a dc-feed inductance $L$ is sufficiently short corresponding to a short-length transmission line and an optimum load resistance $R$ (for the same output power and supply voltage) is greater by approximately 2.4 times and 24 times compared to the Class E with shunt capacitance and even-harmonic Class E, respectively. In addition, the parallel-circuit Class-E configuration can be easily implemented in a high-efficiency broadband high-power and low-voltage power-amplifier design. In this case, it is just necessary to satisfy the required phase angle seen by the device collector at the fundamental frequency and to choose the proper low $Q_L$ factor of the series resonant $L_0C_0$ circuit [28, 29, 30].

Fig. 6.19(*a*) shows the circuit schematic of a single-stage 500 MHz parallel-circuit Class-E high-voltage LDMOSFET power amplifier with a supply voltage of 28 V, an output power of 22 W, a linear power gain of 15 dB and a power-added efficiency of 67%. The input and output matching circuits represent $T$-type transformers with the series 50 Ω microstrip lines fabricated by using a copper-clad laminate substrate with dielectric permittivity of 4.7 and thickness of 0.4 mm. The required fundamental-frequency load network phase angle is provided with the device output capacitance and parallel 50 Ω microstrip line with an electrical length of 25°. The overall size of a hybrid module is $45 \times 20\,\text{mm}^2$ shown in Fig. 6.19(*b*) with an eutectic-attached 1.25 μm LDMOSFET die with the total gate width of $28 \times 1.44$ mm having a small-signal transconductance $g_m = 0.6$ A/V and a transition frequency $f_T = 4.5$ GHz. The die is connected to the input microstrip line by four bond-wires and to the output microstrip line by five bond-wires each having 1.5 mm length. The measured output power and power-added efficiency of the power-amplifier module versus input power are shown in Fig. 6.19(*c*).

The two- and three-stage dual-band power amplifiers intended for handset cellular transmitter application in the DCS1800/PCS1900, CDMA2000, and WCDMA standards normally are built using InGaP/GaAs HBT technology. The MMIC of a three-stage power amplifier shown in Fig. 6.20 by the dotted box contains the RF devices, input matching circuit, two interstage matching circuits, and three bias circuits on a die of 1.1 $\text{mm}^2$ size. The emitter areas of the first, second, and third devices are 180 $\mu\text{m}^2$, 900 $\mu\text{m}^2$, and 5760 $\mu\text{m}^2$, respectively,

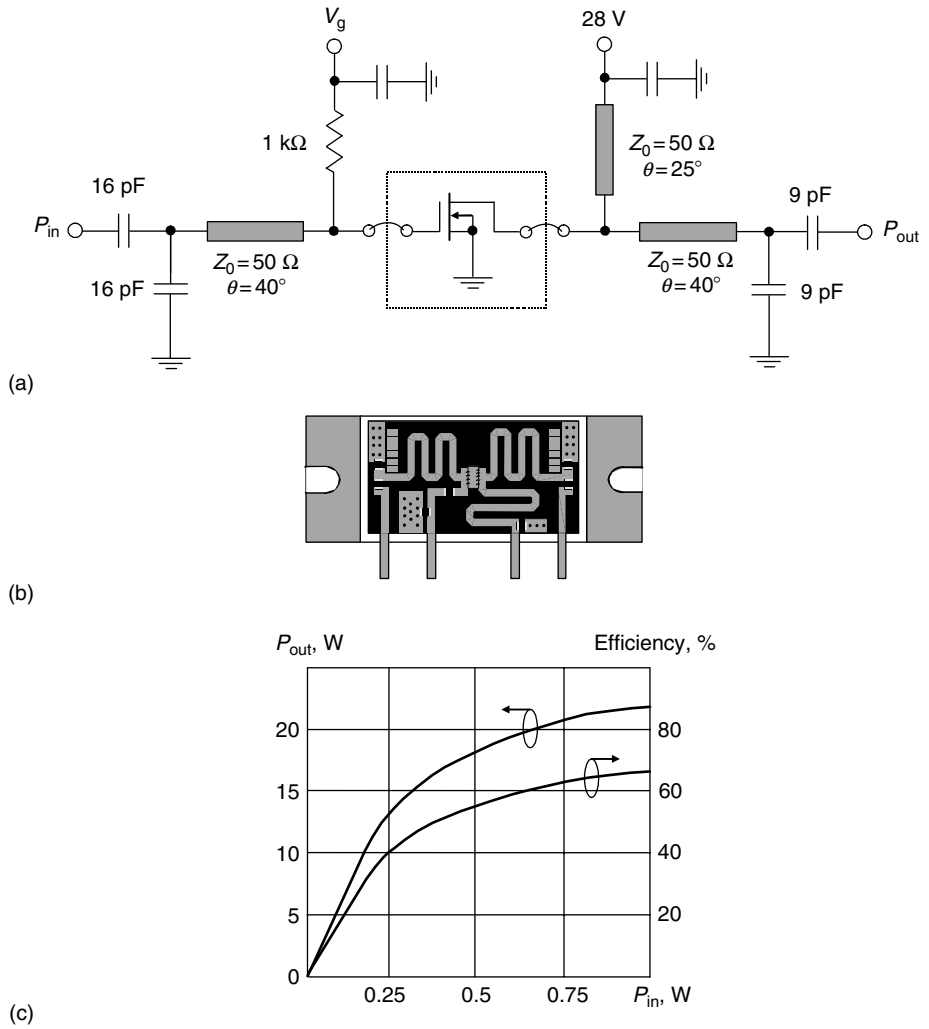



**Figure 6.19: Circuit schematic, module design, and performance of single-stage 500-MHz parallel-circuit Class-E high-voltage LDMOSFET power amplifier.**

corresponding to a median time to failure (MTTF) greater than $8 \cdot 10^5$ hours at the desired power level. The MMIC, packaged in a $3 \times 3\,\text{mm}^2$ package, was mounted on a FR4 substrate, which contains the output-matching circuit and microstrip transmission lines connected to the 3.5 V voltage supply from each device collector. The output-matching circuit was built up according to the optimum values from a detailed circuit simulation. Standard ceramic low $Q$-chip capacitors were used, and no more additional tuning was done. As a result, the minimum power gain of 33 dB, output power of 32.5 dBm, collector efficiency of 57%, and power-added efficiency of 47% were achieved in a frequency range of 1.71–1.91 GHz. It should be

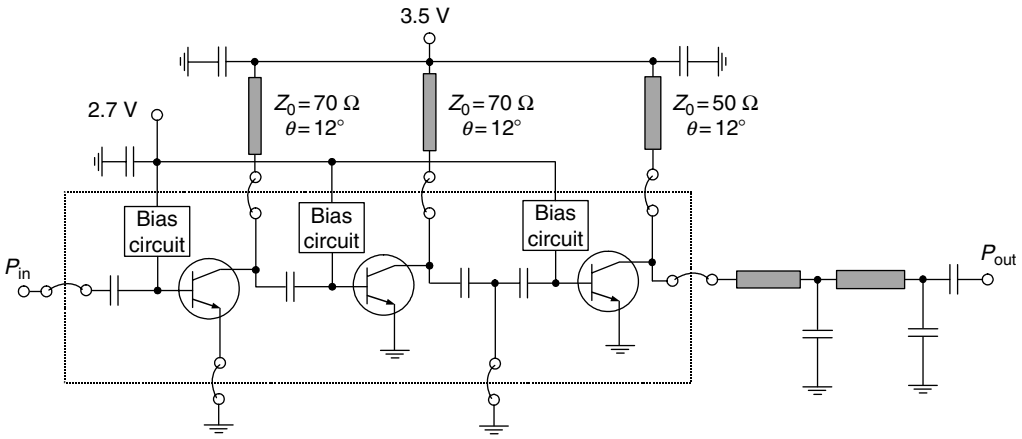



**Figure 6.20: Circuit schematic of high-efficiency low-voltage three-stage dual-band DCS1800/PCS1900 power amplifier.**

noted that the simulated results with accurate values of the high $Q$-capacitors in output-matching circuit had demonstrated collector efficiency of 68% and power-added efficiency of 57%, respectively. At the 3.5 dB backoff conditions when the output power decreases to 29 dBm required for a CDMA2000 standard, the adjacent channel power ratio (*ACPR*) becomes less than −47 dBc with power-added efficiency of 37% at 1.25 MHz offset.

The two-stage InGaP/GaAs HBT power amplifier intended to operate in WCDMA handset transmitters is shown in Fig. 6.21(*a*). The MMIC part of this power amplifier shown by the dotted box contains the RF devices with emitter areas of the first and second stage, which are 540 $\mu m^2$ and 3600 $\mu m^2$, input-matching circuit, interstage-matching circuit, and bias circuits on a die with dimensions of less than 1 $mm^2$. Without any tuning of the output-matching circuit, a saturated RF output power greater than 30 dBm and power-added efficiency greater than 50% were obtained. Using high $Q$-capacitors in the output-matching circuit can improve the power-added efficiency by about 8%. During all testing, the circuits exhibited stable and reliable performance, even at overrated power and voltage experiments. At the same time, a power amplifier without any tuning can provide the high-linearity performance for WCDMA band (1920–1980 MHz) at 3.5 dB backoff output power of about 27 dBm with sufficiently high efficiency. The measured power-added efficiency reached a value of 38.3% at the center bandwidth frequency of 1.95 GHz with the adjacent channel leakage power ratios (ACLR) of −37 dBc at 5 MHz offset and −56 dBc at 10 MHz offset. Fig. 6.21(*b*) shows all these parameters displayed versus output power.

As an example of a close proximity to the idealized switched-mode parallel-circuit Class-E mode, the appropriate simulated collector (*a*) voltage and (*b*) current waveforms at a supply

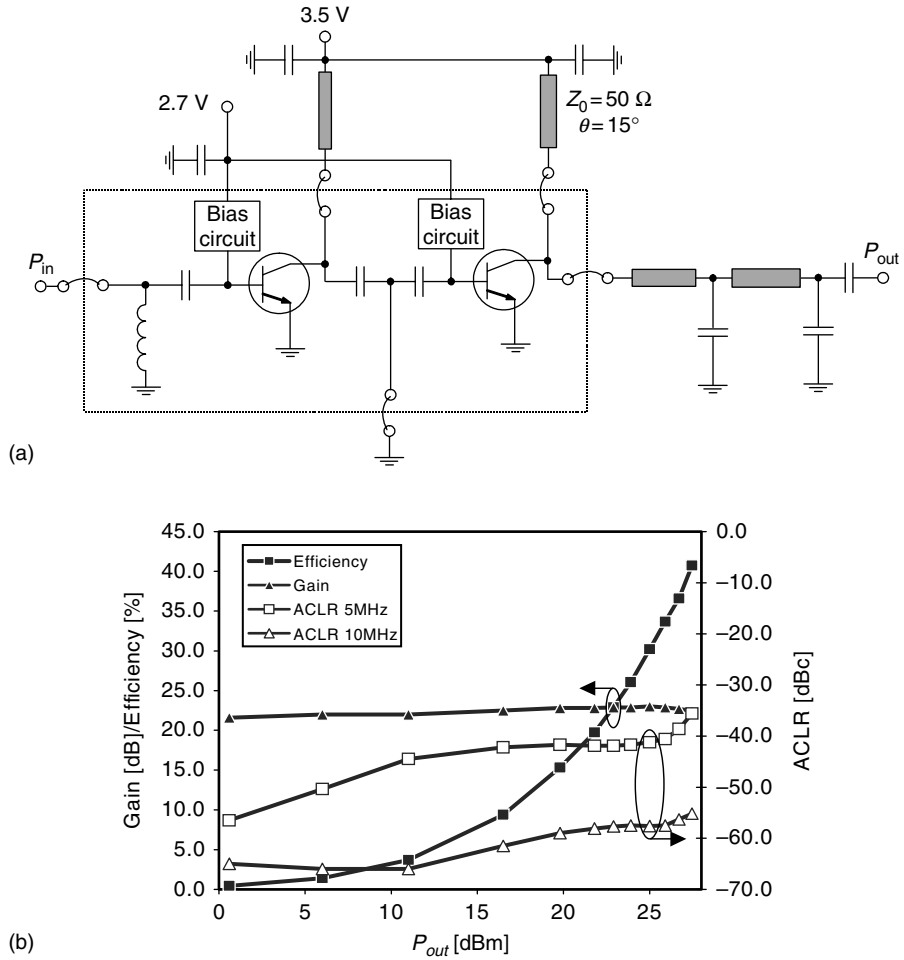



**Figure 6.21: Circuit schematic and performance of high-efficiency low-voltage two-stage WCDMA power amplifier.**

voltage of 5 V are shown in Fig. 6.22 [20]. During off-state operation mode, only the current flowing through the device collector capacitance defines the total collector current. The collector voltage waveform is very similar to the ideal one, with a peak factor of about three. The main reason for the significant efficiency degradation from an ideal 100% is the high value of saturation voltage of about 0.5–0.8 V compared to a supply voltage of 3.5 V, which resulted in 15–20% collector efficiency reduction. The further decrease in collector efficiency can be explained by a violation of the required optimum impedance conditions due to the transmission-line effect at the second and higher-order harmonics, device finite-switching time and parasitics, and power losses in the load network.

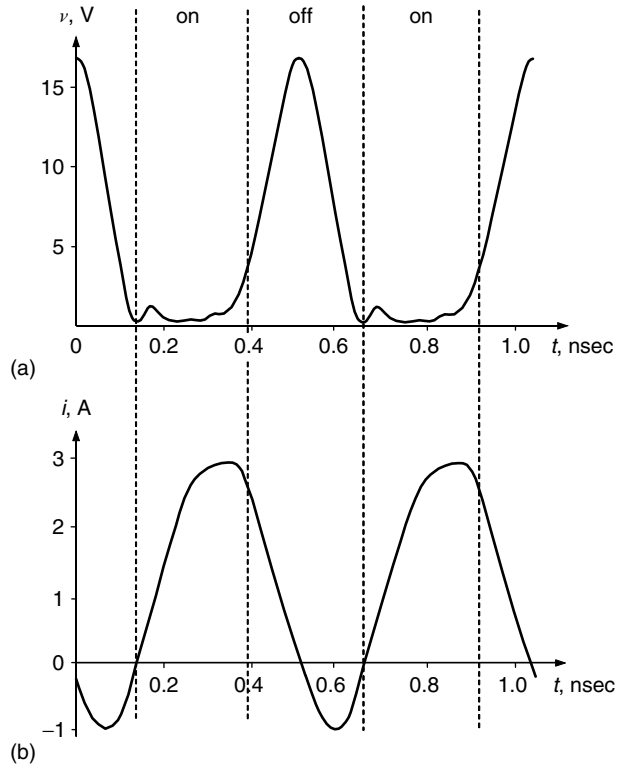



**Figure 6.22: Simulated (*a*) collector voltage and (*b*) current waveforms of transmission-line parallel-circuit Class-E low-voltage InGaP/GaAs HBT power amplifier.**

## 6.8 Broadband Class E

The conventional design of a high-efficiency switched-mode tuned Class-E power amplifier requires a high $Q_L$-factor to satisfy the necessary harmonic impedance conditions at the output device terminal. However, if a sufficiently small value of the loaded quality factor $Q_L$ is chosen, a high-efficiency broadband operation of the Class-E power amplifier can be realized. For example, a simple network consisting of a series resonant LC circuit tuned to the fundamental frequency and a parallel inductor provides a constant load phase angle of 50° in a frequency range of about 50% [31]. For the first time, such a reactance compensation technique using a single-resonant circuit had been applied to the varactor-tuned Gunn oscillator and parametric amplifier [32]. Moreover, it became possible to increase the tuning range of an oscillator by adding more stages of reactance compensation. For instance, for a resonant circuit having a 50 Ω load, an improvement of 4% in the tuning range can theoretically be achieved as a result of applying a double-resonant circuit reactance compensation, whereas, for a resonant circuit operating with 100 Ω load, an increase in the tuning range is 17% [33].

Computer-aided design of broadband microwave-transistor amplifiers normally requires considerable time and can be quite tedious. Therefore, an analytical approach, which is capable to define common regularities and express in explicit and simple form the ratios between load network elements, can be useful to substantially shorten and simplify the calculation procedure. Combined with an analytical approach, computer-optimization yields the fastest and most accurate results.

To describe reactance compensation circuit technique, let us consider the simplified equivalent load network with a series resonant $L_0C_0$ circuit tuned to the fundamental frequency and a shunt LC circuit providing a constant load phase angle seen by the device output, as shown in Fig. 6.23. The reactances of the series and shunt resonant circuits vary with frequency, increasing in the case of a series resonant circuit and reducing in the case of a loaded parallel resonant circuit near the radial resonant frequency $\omega_0$, as shown in Fig. 6.24 by curve 1 and curve 2, respectively. Near the resonant frequency $\omega_0$ of the series circuit with positive slope of its reactance, the slope of a shunt circuit reactance is negative. This reduces the overall reactance slope of the load network (dotted line). With a proper choice of the circuit elements, a constant load angle over a wide frequency bandwidth is established.

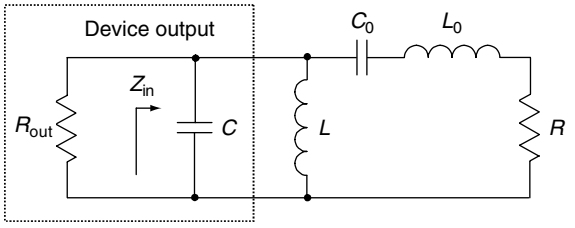



**Figure 6.23: Single reactance compensation circuit.**

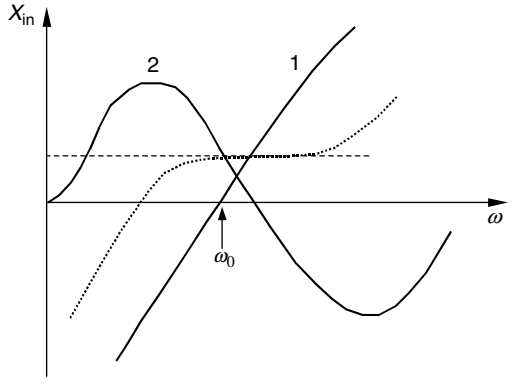



**Figure 6.24: Reactance compensation principle.**

This technique can be easily applied to the switched-mode parallel-circuit Class-E power amplifier because its load-network configuration has exactly the same structure [28, 29, 30]. The parallel-circuit configuration matches directly the broadband operation conditions, unlike the Class-E mode with shunt capacitance and series inductance. In this case, the optimum phase angle $\phi$ and load resistance $R$ of the load network can be obtained from Eqs. (6.83) and (6.79), respectively.

The load-network input admittance $Y_{\text{in}} = 1/Z_{\text{in}}$ can be written as

$$Y_{\text{in}}(\omega) = \left( j\omega C + \frac{1}{j\omega L} + \frac{1}{R + j\omega' L_0} \right), \tag{6.106}$$

where

$$\omega' = \omega \left( 1 - \frac{\omega_0^2}{\omega^2} \right) \tag{6.107}$$

and $\omega_0 = 1/\sqrt{L_0 C_0}$ is the resonant frequency.

At the resonant frequency, when $\omega' = 0$, the input admittance $Y_{\text{in}}(\omega)$ can be rewritten as

$$Y_{\text{in}}(\omega) = \left( j\omega C + \frac{1}{j\omega L} + \frac{1}{R} \right). \tag{6.108}$$

The parallel inductance $L$ and shunt capacitance $C$ required for an optimum switched-mode Class-E operation are calculated as functions of the load resistance $R$ and radian frequency $\omega$, from Eqs. (6.80) and (6.81), respectively. The parameters of the series-resonant $L_0C_0$ circuit must be chosen to provide a constant phase angle of the load network over a required wide frequency bandwidth.

The frequency bandwidth will be maximized if, at a resonant frequency $\omega_0$,

$$\left. \frac{dB_{\text{in}}(\omega)}{d\omega} \right|_{\omega=\omega_0} = 0, \tag{6.109}$$

where

$$B_{\text{in}}(\omega) = \text{Im} Y_{\text{in}}(\omega) = \omega C - \frac{1}{\omega L} - \frac{\omega' L_0}{R^2 + (\omega' L_0)^2} \tag{6.110}$$

is the load-network input susceptance. In this case, the concept of a susceptance compensation technique, which is similar to a reactance-compensation technique, is used to simplify the calculation procedure. An additional equation can be written as

$$C + \frac{1}{\omega_0^2 L} - \frac{2L_0}{R^2} = 0. \tag{6.111}$$

As a result, by substituting Eqs. (6.80) and (6.81) into Eq. (6.111), the series capacitance $C_0$ and inductance $L_0$ can be calculated at the resonant frequency $\omega_0$ by

$$L_0 = 1.026\frac{R}{\omega_0} \tag{6.112}$$

$$C_0 = 1/\omega_0^2 L_0. \tag{6.113}$$

Wider frequency bandwidth can be achieved using a double-resonant reactance-compensation circuit shown in Fig. 6.25, where $L_0C_0$ and $L_1C_1$ are the series and parallel resonant circuits, respectively. In this case, a system of two additional equations can be used and solved according to

$$\left.\frac{dB_{\text{in}}(\omega)}{d\omega}\right|_{\omega=\omega_0} = \left.\frac{d^3B_{\text{in}}(\omega)}{d\omega^3}\right|_{\omega=\omega_0} = 0 \tag{6.114}$$

as the second derivative cannot provide an appropriate analytical expression.

To determine the load-network parameters for a double-resonant circuit reactance compensation with the load-network input susceptance $B_{\text{in}} = \text{Im}Y_{\text{in}}$ given by

$$B_{\text{in}}(\omega) = \omega C - \frac{1}{\omega L} + \omega' \frac{C_1R^2\lfloor 1 - (\omega')^2 L_0C_1 \rfloor - L_0}{R^2[1 - (\omega')^2 L_0C_1]^2 + (\omega' L_0)^2}, \tag{6.115}$$

it is necessary to solve simultaneously the two following equations at the resonant frequency $\omega_0$:

$$C + \frac{1}{\omega_0^2 L} - 2\frac{C_1R^2 - L_0}{R^2} = 0 \tag{6.116}$$

$$\frac{1}{\omega_0^2 L} + \frac{C_1R^2 - L_0}{R^2} - 8\omega_0^2 L_0\left[C_1^2 + \frac{(C_1R^2 - L_0)\ (L_0 - 2C_1R^2)}{R^4}\right] = 0. \tag{6.117}$$

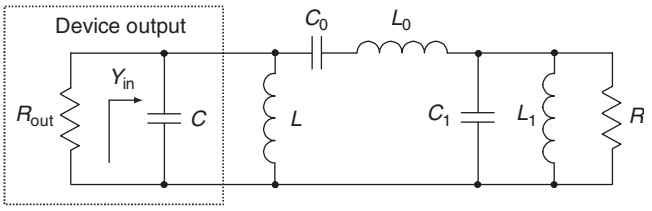



**Figure 6.25: Double reactance compensation circuit.**

As a result, the parameters of the series and shunt resonant circuits with the corresponding loaded quality factors $Q_0 = \omega_0 L_0/R$ and $Q_1 = \omega_0 C_1 R$ close to unity and greater—as a starting point for circuit optimization—can be calculated from

$$L_0 = \frac{R}{\omega_0}\frac{2}{\sqrt{5}-1} \quad C_0 = \frac{1}{\omega_0^2 L_0} \tag{6.118}$$

$$C_1 = \frac{L_0}{R^2}\frac{3-\sqrt{5}}{2} \quad L_1 = \frac{1}{\omega_0^2 C_1}. \tag{6.119}$$

The circuit simulations for these two types of reactance compensation load networks were performed at a resonant frequency $f_0 = 150\,\text{MHz}$ for a standard load resistance $R = 50\,\Omega$. Fig. 6.26 shows the frequency dependencies of the load network phase angle $\phi$ for the single-reactance (curve 1) and double-reactance (curve 2) compensation circuits. It is apparent that the reactance-compensation technique realizes very broadband operating conditions. Using just a single-reactance load network yields a significant widening of the operating frequency bandwidth with a minimum deviation of the magnitude and phase of the load-network input impedance. A double-reactance compensation load network yields a maximum deviation from the optimum value of about 34° by only 3° in the 1.5:1 frequency range of 120–180 MHz.

To achieve the high-efficiency broadband operating mode with high-power gain, it is best to design the power amplifier based on silicon LDMOSFET devices. It is easy to provide a very broadband input matching using a lossy-matching circuit, especially at operating frequencies about 10 times lower than the device transition frequency $f_T$. Fig. 6.27 shows the schematic of an LDMOSFET power amplifier designed for operation in a 2:1 frequency band of 100 to 200 MHz using a double-resonant load network. The lossy input-matching circuit includes a simple *L*-transformer connected in parallel with a series circuit consisting of an inductance of 20 nH and a resistance of 50 Ω. This provides a minimum input return loss at 200 MHz of

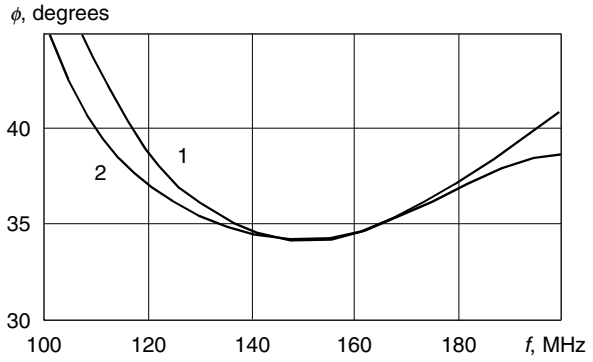



**Figure 6.26: Reactance-compensation load network broadband performance.**

about 15 dB and input *VSWR* less than 1.4 over the entire 2:1 band of 100 to 200 MHz. From Fig. 6.28 it follows that, for such an octave-band Class-E power amplifier with an input power of 1 W, a power gain of 10 dB with deviation of only $\pm$ 0.5 dB (curve 2) can be achieved with a drain efficiency of 69 to 75.6% and higher (curve 1).

An analysis of the drain-voltage and drain-current waveforms at the center-band frequency of 150 MHz, shown in Fig. 6.29, demonstrates that the broadband operating mode is very close to a nominal parallel-circuit Class-E operation mode, although the impedance conditions at higher harmonics are not controlled properly. As seen from the plots when the transistor is turned on, high values of drain current (up to 1.3 A) are achieved with small saturation voltages of 0 to 4 V. On the

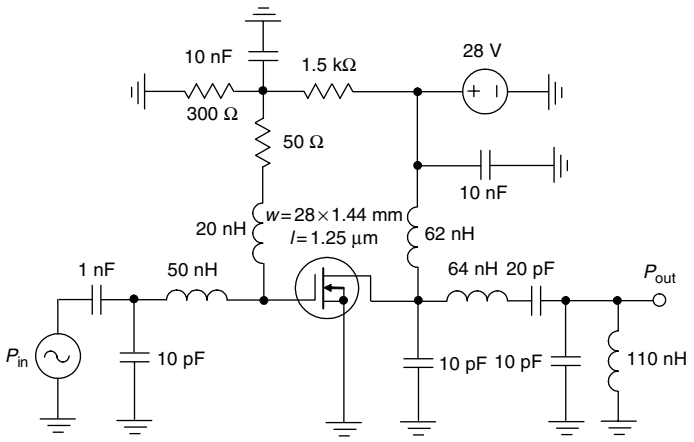



**Figure 6.27: Simulated broadband Class-E LDMOSFET power amplifier.**

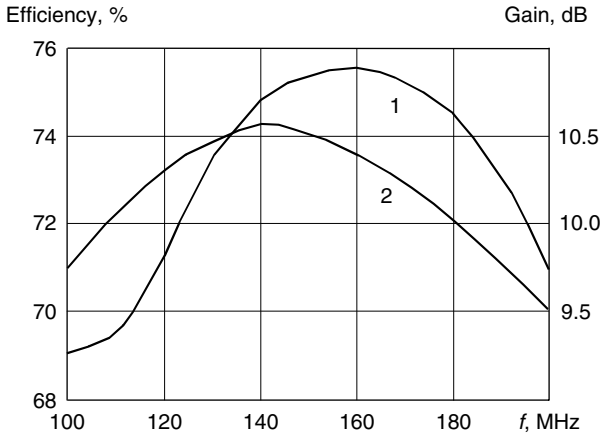



**Figure 6.28: Broadband switched-mode LDMOSFET power-amplifier performance.**

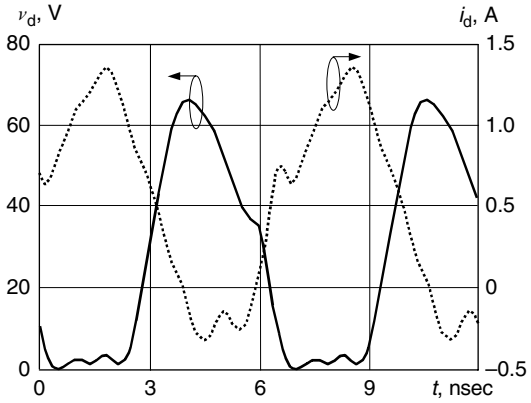



**Figure 6.29: Drain voltage and current waveforms.**

other hand, when the transistor is turned off, the drain current continues to flow, but now through the device gate-drain capacitance $C_{gd}$ and drain-source capacitance $C_{ds}$, not through the active channel.

This reactance-compensation circuit technique can also be applied to microwave-transistor amplifier design because the input and output transistor impedances generally can be represented by series or shunt *RLC* circuits. For compensating the reactive part and transforming the real part of the output transistor impedance to the conventional load impedance, quarter- or half-wavelength transmission lines can be used. With a quarter-wavelength transformer, the reactance compensation can also be realized using different topologies for shunt and series equivalent transistor circuits [34, 35].

Let us consider the characteristics of the transmission line as an element of the reactance-compensation circuit shown in Fig. 6.30. For a parallel equivalent circuit, which represents the device output, the load-network input susceptance $B_{in} = \mathrm{Im}Y_{in}$ can be defined as

$$B_{in}(\omega) = \omega LC\left(1 - \frac{\omega_0^2}{\omega^2}\right) + \frac{\tan\theta}{Z_0}\,\frac{R_L^2 - Z_0^2}{R_L^2 + Z_0^2\tan^2\theta}, \tag{6.120}$$

where

$$\theta = \frac{\pi}{2}\frac{f}{f_0}k \tag{6.121}$$

is the electrical length of the transmission line, $Z_0$ is the transmission-line characteristic impedance, $f_0 = \omega_0/2\pi$ is the transmission-line resonant frequency, and $k = 1, 2, \ldots, \infty$ [27, 28].

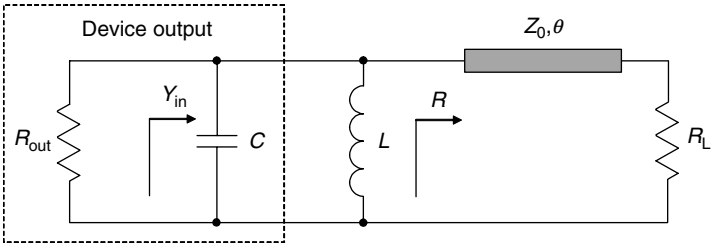



**Figure 6.30: Transmission-line reactance-compensation circuit.**

Applying the zero susceptance-derivative condition given by Eq. (6.109) to Eq. (6.120) allows us to obtain the reactance-compensation circuit parameters for different electrical lengths of a transmission line in accordance with

$$2C + \frac{\pi}{2Z_0\omega_0}\frac{R_L^2 - Z_0^2}{\cos^2\theta}\frac{R_L^2 - Z_0^2\tan^2\theta}{(R_L^2 + Z_0^2\tan^2\theta)^2} = 0. \tag{6.122}$$

For a quarter-wave transmission line, when $k = 1$ and $\theta = \pi/2$, the reactance compensation will be performed under the condition $Z_0 < R_L$ with the characteristic impedance $Z_0$ defined from the quadratic equation

$$Z_0^2 + 4\frac{Q_L R_L}{\pi}Z_0 - R_L^2 = 0, \tag{6.123}$$

where $Q_L = \omega_0\, CR$ and $R = Z_0^2/R_L$.

Consequently, the required value of the characteristic impedance $Z_0$ is obtained by

$$Z_0 = R_L\left(-\frac{2Q_L}{\pi} + \sqrt{\left(\frac{2Q_L}{\pi}\right)^2 + 1}\right) \tag{6.124}$$

or

$$Z_0 = R\Big/\left(-\frac{2Q_L}{\pi} + \sqrt{\left(\frac{2Q_L}{\pi}\right)^2 + 1}\right). \tag{6.125}$$

From Eq. (6.124), it follows that the maximum value of the characteristic impedance $Z_0$ is limited by the load resistance $R_L$, and usually is substantially smaller than $50\,\Omega$, which causes a problem in the practical implementation of a transmission line. Moreover, the characteristic impedance $Z_0$ becomes smaller for higher values of $Q_L$. In this case, it is best to apply a single frequency-equivalence technique when a quater-wave transmission line can be replaced by a

symmetrical π-type low-pass transmission-line section with two equal shunt capacitances at a single frequency $\omega_0$, as shown in Fig. 6.31.

The *ABCD* matrix for a quater-wave transmission line can be written as

$$ABCD_{90^\circ} = \begin{bmatrix} \cos 90^\circ & jZ_0 \sin 90^\circ \\ j\frac{\sin 90^\circ}{Z_0} & \cos 90^\circ \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix}, \tag{6.126}$$

whereas, for a π-type low-pass transmission-line section, we can write

$$\begin{aligned} ABCD_{\pi} &= \begin{bmatrix} 1 & 0 \\ j\omega C_T & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_T & jZ_T \sin\theta_T \\ j\frac{\sin\theta_T}{Z_T} & \cos\theta_T \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_T & 1 \end{bmatrix} \\ &= \begin{bmatrix} \cos\theta_T - \omega C_T Z_T \sin\theta_T & jZ_T \sin\theta_T \\ \frac{j}{Z_T}(2Z_T \omega C_T \cos\theta_T + \sin\theta_T - Z_T^2 \omega^2 C_T^2 \sin\theta_T) & \cos\theta_T - \omega C_T Z_T \sin\theta_T \end{bmatrix}. \end{aligned} \tag{6.127}$$

Hence, equalizing *A* and *B* elements from each matrix yields

$$Z_T = \frac{Z_0}{\sin\theta_T} \tag{6.128}$$

$$C_T = \frac{\cos\theta_T}{\omega Z_0}. \tag{6.129}$$

As a result, the electrical length of the transmission line can be reduced significantly with the increase of its characteristic impedance. Also, such a transformation is very important when the value of the device output capacitance exceeds the required optimum value for the nominal Class-E operation. In this case, the excess capacitance can be used as a part or the entire shunt capacitance in the π-type low-pass section and the nominal Class-E condition will be completely satisfied at the fundamental frequency.

As an example, let us consider the design of the transmission-line broadband Class-E load network for a 1.71–1.91 GHz 3.5 V power amplifier with an output power of 2 W at center-band frequency of $\omega_0 = \sqrt{1.71 \times 1.91} = 1.81\,MHz$ [30]. The large-signal simulations

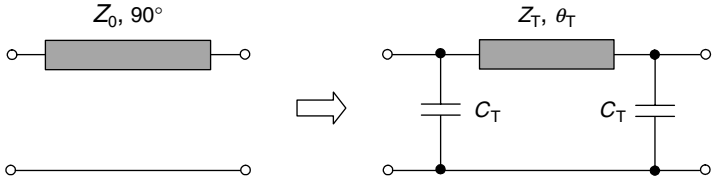



**Figure 6.31: Transmission-line single frequency equivalence technique.**

and measurements show that, for an InGaP/GaAs HBT device with overall emitter area of 5760 $\mu m^2$, the collector capacitance at maximum output power is 15 pF. By using Eqs. (6.79) to (6.81) and Eq. (6.105), the load-network parameters required for a parallel-circuit Class-E load network with a short-length transmission line, assuming zero device saturation resistance, can be found as

$$R = 8.4\,\Omega$$

$$C = 7.2\,\text{pF}$$

$$Q_L = \omega_0 CR = 0.685$$

$\theta = 7.0^\circ$ for a $50\,\Omega$ transmission line.

By applying a transmission-line reactance-compensation technique, the characteristic impedance of a quater-wave transmission line, is calculated from Eq. (6.125), is $Z_0 = 12.8\,\Omega$. This obtained value is too small for practical implementation of the transmission line. Therefore, it is necessary to use a $\pi$-type low-pass equivalent replacement using Eqs. (6.128) and (6.129) for the typical, and usually most convenient, characteristic impedance of the transmission line of $Z_T = 50\,\Omega$, resulting in

$$C_T = 6.6\,\text{pF}$$

$$\theta_T = 14.9^\circ.$$

As a result, the total shunt capacitance is $C_{tot} = 6.6 + 7.2 = 13.8\,\text{pF}$, which value is very close to the measured device collector capacitance. The equivalent transmission-line Class-E load-network representation of this example is shown in Fig. 6.32. Now the required optimum impedance conditions are almost satisfied but only at the fundamental frequency. Therefore, these calculated design parameters can only be a good starting point to speed up and conduct a considerably less time-consuming further computer optimization procedure, in order to maximize efficiency over a specified frequency bandwidth. To minimize the variation of the power delivered to the load over the entire frequency range and the effect of the variations of the load-network parameters in practical design, generally it is advisable to use either a two-stage or three-stage output-matching circuit.

Fig. 6.33(*a*) shows the circuit schematic of a broadband high-efficiency microstrip LDMOSFET power amplifier with an output power of 15 W and a power gain of more than 10 dB in a frequency range of 225–400 MHz, at a supply voltage of 28 V. Here, to approximate the parallel-circuit Class-E mode in a wide frequency range, the load network was designed to realize a single-reactance compensation technique using a parallel short-length transmission line in conjunction with a single T-type transmission-line transformer, since a ratio between

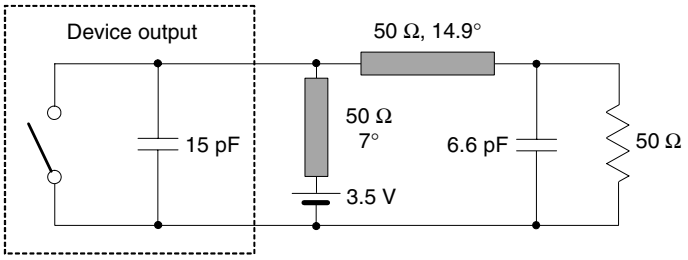
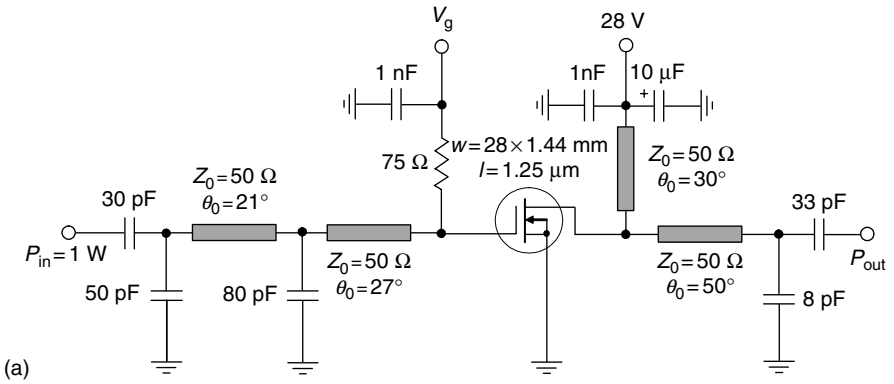



**Figure 6.32: Transmission-line Class-E load network with reactance compensation.**



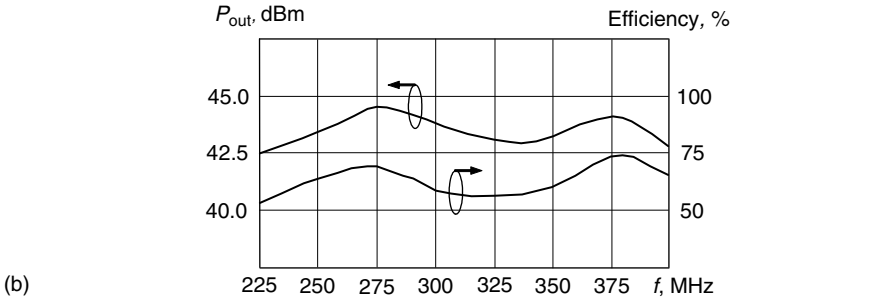




**Figure 6.33: Broadband high-efficiency microstrip LDMOSFET power amplifier.**

the device output resistance required for an optimum Class-E operation and standard load resistance of 50 Ω is not significant. The input-matching circuit includes two low-pass matching sections to compensate for the device input capacitance over the entire frequency range. A lossy parallel resistance of 75 Ω is necessary to simplify the matching procedure and improve the input return loss. As a first step, each matching network structure is calculated at the center-band frequency based on the technical requirements and device equivalent-circuit parameters. Then, to optimize the power-amplifier performance over the entire frequency band, the simplest and fastest way is to apply an optimization procedure using computer simulation

to satisfy certain criteria. For such a broadband power amplifier, these criteria can be a minimum-output power ripple and an input return loss with the maximum power gain and efficiency. Generally, applying a nonlinear broadband optimization technique and setting the ranges of electrical length of the transmission lines between 0 and 90° and parallel capacitances from 0–100 pF, we can obtain the parameters of the input-matching and output-load network.

However, to speed up this procedure, it is best to optimize circuit parameters separately for the input and output circuits. In this case, the input-matching circuit is loaded by a device equivalent input series *RC* circuit, consisting of its gate-resistance and gate-source capacitance. The load network must include at its input the device equivalent output shunt *RC* circuit consisting of an optimum Class-E load resistance required for a specified output power and supply-voltage and drain-source capacitance. In this case, it is sufficient to use a fast linear optimization process, which will take only a few minutes to complete the circuit design procedure. Finally, the resulting optimized values are incorporated into the overall power-amplifier circuit for each element and final optimization is performed using a large-signal-active device model. The optimization process is finalized by choosing the nominal level of input power with optimizing elements in narrower ranges of their values of about 10–20% for most critical elements. For practical convenience, it is advisable to choose the characteristic impedances of all transmission lines of 50 Ω. Fig. 6.33(*b*) illustrates the simulated broadband high-efficiency power-amplifier performance achieving an output power in limits of 42.5–44.5 dBm, a power gain of 13.5 ± 1 dB, and drain efficiency of 64 ± 10% in a frequency bandwidth of 225–400 MHz.

## 6.9 Power Gain

The load network corresponding to any type of Class-E mode, in order to realize the idealized switching conditions, is tuned to provide inductive or capacitive impedance at the fundamental frequency, thus violating the conjugate matching conditions required for conventional Class-B operation to provide maximum power delivery to the load. This means that generally the output voltage and current waves consist of both incident and reflected components. Besides, the power gain in a switching mode is normally lower than in a conventional mode because it requires higher driving voltage to realize a device voltage-saturation mode. In this case, the ratio of the power gain in a Class-E power amplifier to that in a Class-B power amplifier, for the same output power, is inversely proportional to a squared ratio of their voltage peak factors [36]. For a Class E with one inductor and one capacitor, a maximum operating power gain $G_{P(E)max}$ of a single-stage bipolar power amplifier can be estimated by

$$G_{P(E)max} \approx \frac{\pi}{2} \frac{f_T}{f} \frac{V_{cc}}{V_{th}}, \tag{6.130}$$

where $f$ is the operating frequency, $V_{th}$ is the threshold voltage, and it is assumed that the effect of a non-zero fall time is negligible [37].

However, it is very important to qualitatively compare the power gains of the Class-B and Class-E power amplifiers as functions of the device and load-network parameters. In this case, a parallel-circuit Class-E mode looks very attractive since it provides the highest value of load resistance compared with other Class-E alternatives. The operating power gain $G_P$, expressed through the active-device $Y$-parameters and load, can be obtained as

$$G_P = \frac{|Y_{21}|^2}{\mathrm{Re}Y_{in}} \frac{G}{|Y_{22} + Y_L|^2}, \tag{6.131}$$

where $Y_{21}$ and $Y_{22}$ are the device transfer and driving-point output admittances, $Y_{in}$ is the input admittance of the loaded device, and $Y_L = G + jB$ is the load admittance [38]. Since the power amplifier is operated in a nonlinear mode, the admittance $Y$-parameters of the active device are considered as linearized at the fundamental frequency. For example, for a power amplifier operating at the same conduction angle over various bias and drive conditions, these $Y$-parameters remain constant and the operating power gain becomes a function of only the load admittance.

Eq. (6.131) can be rewritten as

$$G_P = \frac{|Y_{21}|^2}{\mathrm{Re}Y_{in}} \frac{R}{\left(1 + \frac{G_{22}}{G}\right)^2 + \left(\frac{B_{22}+B}{G}\right)^2}, \tag{6.132}$$

where $G_{22} = \mathrm{Re}Y_{22}$, $B_{22} = \mathrm{Im}Y_{22}$, and $R = 1/G$ is the load resistance. Without significant loss of accuracy, the output conjugate-matching condition between the imaginary parts of the device output admittance and the load admittance can be replaced by a simple condition of $B_{22} + B = 0$, which means a resonance tuning of the load network including the device output susceptance $B_{22}$. Also, normally the device output conductance $G_{22}$ is significantly smaller than the load conductance $G$ for both MOSFET and bipolar transistors, especially at frequencies well below the device transition frequency $f_T$.

Consequently, the simplified ratio between the operating power gain of a parallel-circuit Class-E power amplifier $G_{P(E)}$ and the operating power gain of a conventional Class-B power amplifier $G_{P(B)}$ with conjugate-matched load can be written as

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{1}{1 + (B_{22} + B)^2 R_{(E)}^2} \frac{R_{(E)}}{R_{(B)}}, \tag{6.133}$$

where $R_{(E)}$ is the load resistance of a Class-E power amplifier and $R_{(B)}$ is the load resistance of a Class-B power amplifier.

For an ideal nominal Class-E operating mode with 100% collector efficiency, from Eq. (6.53) it follows that

$$V_{R(E)} = 1.652\,V_{cc}. \tag{6.134}$$

For the same output power $P_{out}$ and taking into account that $V_{R(B)} = V_{cc}$ in a conventional Class B with zero saturation voltage, we can write

$$\frac{R_{(E)}}{R_{(B)}} = \frac{V_{R(E)}^2}{V_{R(B)}^2} = 2.729 \tag{6.135}$$

that shows the significantly higher value for the load resistance in an optimum parallel-circuit Class-E operation mode.

As a result, the power gain ratio given by Eq. (6.133) can be rewritten in the form of

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{2.729}{1 + \tan^2\phi} = 1.865, \tag{6.136}$$

where $\phi = 34.244^\circ$ is the phase angle between the fundamental-frequency voltage and current components at the device output required for the nominal parallel-circuit Class-E mode.

The result given by Eq. (6.136) means that, ideally, the operating power gain for a switched-mode parallel-circuit Class-E mode, compared to a conventional Class-B mode, is almost the same, and even slightly greater, despite the mistuning of the load network. This can be explained by the larger value of the load resistance required for the optimum parallel-circuit Class-E load network. For example, for a Class E with shunt capacitance, the operating power gain is smaller compared to a Class-B power amplifier because its optimum Class-E load resistance is about 2.4 times smaller than that of a parallel-circuit Class-E mode [39]. The idealized conditions for a switched-mode operation can be achieved with instant on/off active device switching, which requires the rectangular input-driving signal compared with sinusoidal-driving signal for a conventional Class-B mode. However, the power losses due to the switching time are sufficiently small and, for example, for switching time of $\tau_s = 0.35$ or $20^\circ$ they are only about 1% [20]. Consequently, a slight overdrive of the active device is needed when the input power should be increased by 1–2 dB to minimize the switching time and maximize the collector efficiency of a switched-mode parallel-circuit Class-E power amplifier. As a result, its resulting operating power gain becomes approximately equal to the operating power gain of a conventional Class-B power amplifier.

## 6.10 CMOS Class-E Power Amplifiers

Recent progress in CMOS technology has shown their promising future for RF power application. Much progress has been achieved at the research level, and the obvious possibility to minimize the cost and size of the integrated circuits for RF handset transmitters, especially power-amplifier MMICs, makes CMOS technology very feasible and brings considerable economic benefits. However, realizing high-efficiency operation of power amplifiers is limited by some technology issues, such as the high value of the device saturation resistance, low value of the breakdown voltage, and lossy silicon substrate. Therefore, it is vital to apply high-efficiency technique in the design of the CMOS power amplifiers.

For example, a 900-MHz cascode power amplifier based on a 0.25-$\mu$m CMOS technology with active die area of $2 \times 2\,\text{mm}^2$ can provide an output power of 0.9 W and a power-added efficiency of 41% using a Class-E load network with shunt capacitance and finite dc-feed inductance, the circuit schematic of which is shown in Fig. 6.34 [40]. Minimizing the value of the dc-feed inductance is necessary to minimize the die size, resulting also in higher values of the load resistance and shunt capacitance required for a nominal Class E with finite dc-feed inductance. For the same value of saturation resistance, this contributes to lower power loss on the active device and can absorb a larger value of the device output capacitance. Cascode configuration and thick-oxide transistors are used to eliminate the effects of oxide breakdown voltage and hot-carrier degradation effect, allowing the supply voltage $V_{dd}$ to be as high as 1.8 V. Since a cascode switch has higher on-resistance per unit channel width than a single common-source switch during the on state, wider devices of 15 mm gate widths are used. The inter-stage bond-wire inductor of 2 nH and external variable capacitor are used to resonate out-the-gate capacitance of the cascode device. Since the quality factor of on-chip

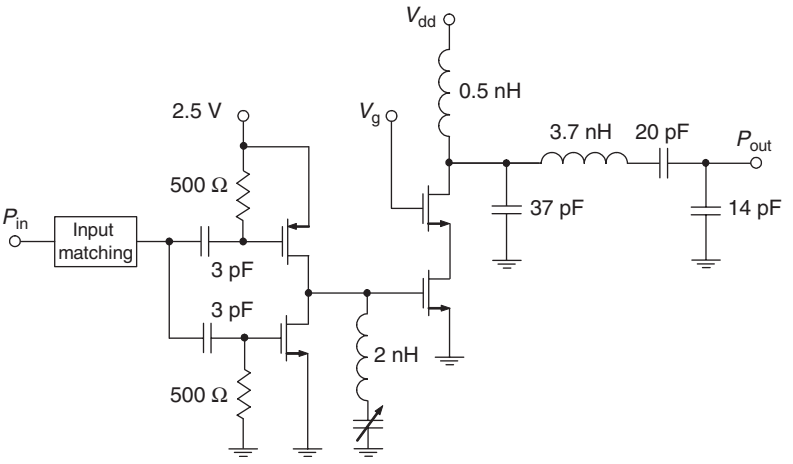



**Figure 6.34: Cascode Class-E power amplifier with finite dc-feed inductance [40].**

spiral inductors provided by a typical CMOS technology is low because of a large loss in the silicon substrate and metal layers, bonding-wire inductors can be successfully used instead of spiral inductors. This provides less than 5% of inductance variation and less than 6% of $Q$-factor variation as a result of the wire-bonding process. As a result, the complete power-amplifier load network consists of two aluminum bond-wire inductors and one on-chip (37 pF) and two off-chip (20 pF and 14 pF) capacitors. The implemented power amplifier is differential, and baluns were used at both input and output to combine the two single-ended paths. By using an injection-locked oscillator technique and differential circuit topology implemented in a 0.35-$\mu$m CMOS technology, the Class-E power amplifier provided a power-added efficiency of 41% and an output power of 1 W at the operating frequency of 1.98 GHz [41].

Optimizing the cascode topology requires setting the bias voltage $V_g$ of the common-gate transistor shown in Fig. 6.35($a$) in order to minimize the voltage drop across the oxide of each transistor $M_1$ and $M_2$ when these voltage drops become equal, allowing the use of approximately twice the supply voltage [42]. However, there is an additional power-loss mechanism as a specific property of a cascode configuration in a switching Class-E mode, when the common source device $M_1$ is turned off, that is associated with charging and discharging processes of the shunt parasitic capacitor $C_p$ consisting of the drain-bulk capacitance of the device $M_1$ and gate-source and source-bulk capacitances of the device $M_2$. This results in a non-zero switching time of the common-gate device $M_2$ when it cannot be instantly switched from the saturation mode to the pinch-off mode and operates in the active region, when output current and output voltage are simultaneously positive, causing power dissipation within the device. The parasitic capacitance $C_p$ can be three to four times larger than the drain-bulk capacitance of device $M_2$, resulting in a power loss as large as 20% of the output power, being five times that due to the saturation resistance of device $M_1$. A simple and effective way to minimize this power-loss contribution is to use a parallel inductor $L_p$ resonating the parasitic capacitor $C_p$ at the operating frequency, as shown in Fig. 6.35($b$), where $C_b$ is a dc-blocking capacitor. The series-resonant circuit required to provide a sinusoidal current flowing to the load is replaced by the series inductor $L_m$ and shunt capacitor $C_m$ forming an L-type lumped transformer to transform the standard load resistance of 50 $\Omega$ to the nominal Class-E load resistance. As a result, the two-stage cascode Class-E power amplifier with a compensating inductor implemented in a 0.13-$\mu$m CMOS technology achieved a drain efficiency of 71% and a power-added efficiency of 67% when delivering an output power of 23 dBm (200 mW) at an operating frequency of 1.7 GHz with a dcsupply voltage of 2.5 V. The driving stage with a supply voltage of 1.2 V is biased in Class C. The value of the dc-feed inductor $L_d$ is chosen to compensate for the gate-source capacitance of device $M_1$. The measured power-added efficiency was higher than 60% over the frequency band of 1.4–2.0 GHz.

In a cascode configuration, the voltage across each transistor reduces by two times with the same current, thus resulting in a higher overall saturation resistance and power loss.

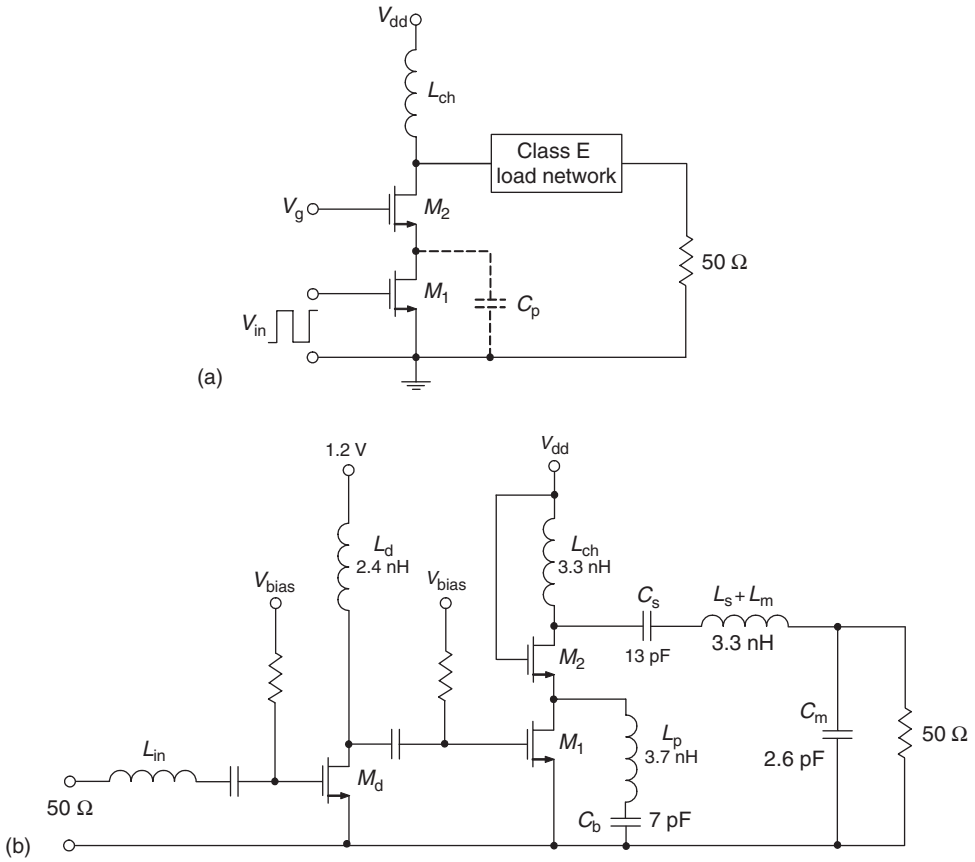



**Figure 6.35: Cascode Class-E power amplifier with compensating inductor [42].**

To overcome this problem, a common-gate Class-E power amplifier, the equivalent circuit of which is shown in Fig. 6.36, can be used [43]. Here, the input signal is applied directly to the device source, and power losses can be reduced for the same voltage across the device by choosing an inductor with a high $Q$-factor. Since CMOS monolithic inductors are known for their low-quality factors due to high-substrate losses and high parasitics, a bond-wire inductor can be used instead of a monolithic inductor to maximize the inductor quality factor. However, these bond-wire inductors must be modeled very accurately for a particular design since their geometry is difficult to predetermine. For a two-stage power amplifier, it is very important to minimize the power consumption of the driving stage to minimize its effect of reducing the overall efficiency. In this case, the driver stage can include a positive feedback, working as an injection-locked oscillator to maximize the power gain. When using a differential structure of a CMOS Class-E power amplifier, a driver stage can be designed by utilizing a cross-coupled differential pair to form a positive feedback. As a result, such a two-stage differential 2.45-GHz Class-E power amplifier, implemented in a 0.25-$\mu$m standard CMOS process with chip area of $0.8 \times 0.9\,\text{mm}^2$, achieved a power-added

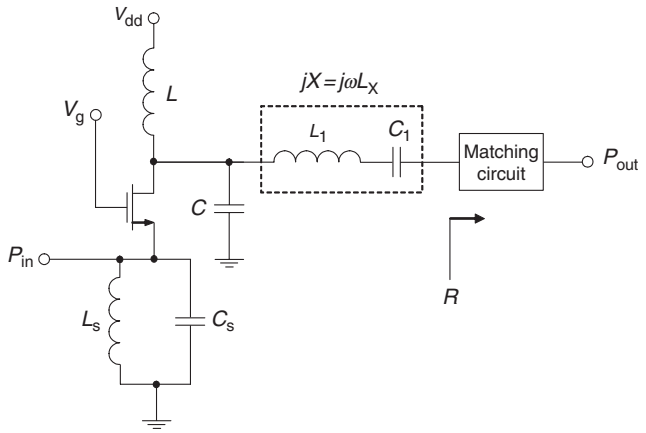



**Figure 6.36: Common-gate Class-E power amplifier [43].**

efficiency of 34.5% and an output power of 18 dBm (63 mW) at a supply voltage of 1 V. The power-added efficiency was at least 33% over the frequency range of 2.4–2.48 GHz.

For a given geometry of a CMOS device, there is an optimum output power that provides the maximum power-added efficiency. Maximizing the output power by lowering an optimum load resistance will result in a higher current flowing through the saturation resistance, increasing the power dissipation. On the other hand, lowering the output power by increasing the optimum load resistance will decrease the power-added efficiency because of a reduced power gain. Also, there is an optimum device size that provides the maximum power-added efficiency. A larger transistor size will lower the saturation resistance, but will require more power from the driver stage and consumes more silicon area. In this case, it is more difficult to provide the input matching due to increasing gate-source capacitance and lower gate resistance, with a sufficiently small dc-feed inductance resulting in implementation difficulties [44]. For example, for a simulated 1 GHz CMOS power amplifier fabricated using a 0.35-$\mu$m standard CMOS technology, a maximum power-added efficiency of about 62% is achieved for device gate widths of 6000–8000 $\mu$m with output power of about 900 mW, dc-feed inductance of 2 nH, and load resistance of 2 $\Omega$ [45].

Fig. 6.37 shows the circuit schematic of a two-stage fully differential Class-E power amplifier designed in a 0.18-$\mu$m standard CMOS technology [46]. The driver stage is used to convert the sinusoidal input signal into its square-wave approximation to drive the output stage. In some cases, the interstage circuit can contain parallel tank circuits tuned to the fundamental and third-harmonic frequencies, realizing a Class-F mode of the driving stage and making the driving voltage waveform closer to a square-wave, thus minimizing the power loss due to the finite switching time [47, 48]. To obtain high-operating efficiency, bond-wires are used to implement the inductors $L_1$ and $L_2$, while the

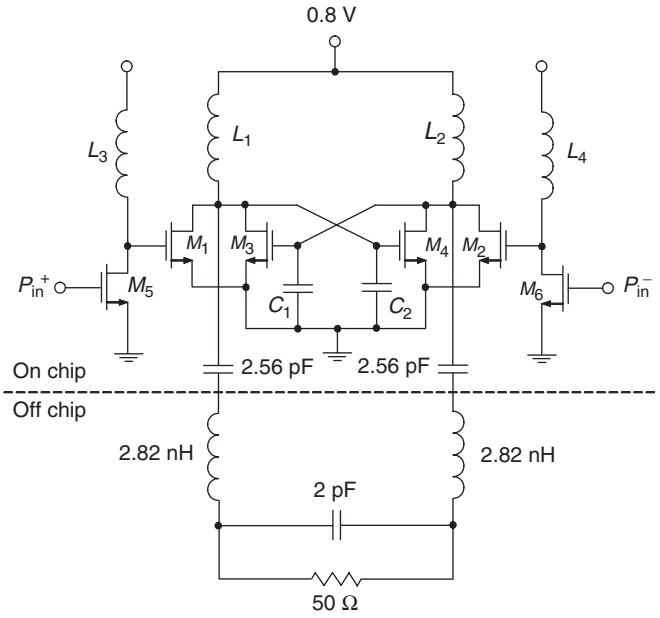



**Figure 6.37: Two-stage injection-locked Class-E power amplifier [46].**

on-chip spiral inductors $L_3$ and $L_4$ are used in the driver stage for better matching. The NMOS transistors $M_3$ and $M_4$ in the output stage are cross-coupled to assist the operation of the NMOS transistors $M_1$ and $M_2$, respectively, thus resulting in a significant reduction of the input-driving requirement due to injection-locking operating mode. The sizes of the NMOS devices were optimized to compromise the efficiency and output power. The shunt capacitors $C_1$ and $C_2$ can be used if the values of the gate-source capacitances are not enough to get the self-oscillations at the operating frequency to realize an injection-locking mode. As a result of an accurate simulation and optimization design procedure, such a two-stage Class-E power amplifier is able to deliver an output power of 84.8 mW with a drain efficiency of 69.1% at an operating frequency of 2.4 GHz. The results of practical implementation of a two-stage injection-locked differential CMOS power amplifier in a 0.25 $\mu$m standard CMOS technology demonstrate the possibility to achieve an output power of 26 dBm (398 mW) with a power-added efficiency of 62% at a carrier frequency of 1 GHz, using a dc power supply of 1 V [49].

## References

[1] N. O. Sokal, ''Class E High-Efficiency Switching-Mode Tuned Power Amplifier with Only One Inductor and One Capacitor in Load Network—Approximate Analysis,'' *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 380–384, August 1981.

[2] M. Kazimierczuk, ''Exact Analysis of Class E Tuned Power Amplifier with Only One Inductor and One Capacitor in Load Network,'' *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 214–221, April 1983.

[3] I. A. Popov (Ed.), *Transistor Generators of Harmonic Oscillations in Switching Mode* (in Russian), Moskva: Radio i Svyaz, 1985.

[4] V. I. Degtev, ''Switching-Mode Tuned Power Amplifier with Forming Circuit (in Russian),'' *Radiotekhnika*, vol. 40, pp. 77–80, August 1985.

[5] V. V. Gruzdev, ''Calculation of Circuit Parameters of Single-Ended Switching-Mode Tuned Power Amplifier (in Russian),'' Trudy MEIS, vol. 2, pp. 124–128, 1969.

[6] M. Kazimierczuk, ''Class E Tuned Power Amplifier with Nonsinusoidal Output Voltage,'' *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 575–581, August 1986.

[7] P. M. Gaudio, C. Bernal, and A. Mediano, ''Exact Analysis of a Simple Class E Circuit Version for Device Characterization,'' *2003 IEEE MTT-S Int. Microwave Sym. Dig.*, vol. 3, pp. 1737–1740.

[8] R. E. Zulinski and J. W. Steadman, ''Class E Power Amplifiers and Frequency Multipliers with Finite DC-Feed Inductance,'' *IEEE Trans. Circuits and Systems*, vol. CAS-34, pp. 1074–1087, September 1987.

[9] C. P. Avratoglou, N. C. Voulgaris, and F. I. Ioannidou, ''Analysis and Design of a Generalized Class E Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-36, pp. 1068–1079, August 1989.

[10] G. H. Smith and R. E. Zulinski, ''An Exact Analysis of Class E Power Amplifiers with Finite DC-Feed Inductance at Any Output *Q*,'' *IEEE Trans. Circuits and Systems*, vol. CAS-37, pp. 530–534, April 1990.

[11] H. Sekiya, I. Sasase, and S. Mori, ''Computation of Design Values for Class E Amplifiers without Using Waveform Equations,'' *IEEE Trans. Circuits and Systems–I: Fundamental Theory Appl.*, vol. CAS-I-49, pp. 966–978, July 2002.

[12] C.-H. Li and Y.-O. Yam, ''Maximum Frequency and Optimum Performance of Class E Power Amplifiers,'' *IEE Proc. Circuits Devices Syst.*, vol. 141, pp. 174–184, June 1994.

[13] C. K. Ho, H. Wong, and S. W. Ma, ''Approximation of Non-Zero Transistor ON Resistance in Class-E Amplifiers,'' *Proc. 5th IEEE Int. Caracas Conf. Devices Circuits Syst.*, pp. 90–93, 2004.

[14] D. Milosevic, J. van der Tang, and A. van Roermund, ''Explicit Design Equations for Class-E Power Amplifiers with Small DC-Feed Inductance,'' *Proc. 2005 Europ. Conf. Circuit Theory and Design*, vol. 3, pp. 101–104.

[15] A. Grebennikov, ''Load Network Design Techniques for Class E RF and Microwave Amplifiers,'' *High Frequency Electronics*, vol. 3, pp. 18–32, July 2004.

[16] M. Acar, A. J. Annema, and B. Nauta, ''Generalized Design Eqs. for Class-E Power Amplifiers with Finite DC Feed Inductance,'' *Proc. 36th Europ. Microwave Conf.*, 2006, pp. 1308–1311.

[17] V. B. Kozyrev, ''Single-Ended Switching-Mode Tuned Power Amplifier with Filtering Circuit (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Svyazi*, vol. 6, pp. 152–166, 1971.

[18] A. Grebennikov, ''Class E High-Efficiency Power Amplifiers: Historical Aspect and Future Prospect,'' *Applied Microwave & Wireless*, vol. 14, pp. 64–71, July 2002, pp. 64–72, August 2002.

[19] A. V. Grebennikov and H. Jaeger, ''Class E with Parallel Circuit—A New Challenge for High-Efficiency RF and Microwave Power Amplifiers,'' *2002 IEEE MTT-S Int. Microwave Sym. Dig.*, vol. 3, pp. 1627–1630.

[20] A. Grebennikov, ''Switched-Mode RF and Microwave Parallel-Circuit Class E Power Amplifiers,'' *Int. J. RF and Microwave Computer-Aided Eng.*, vol. 14, pp. 21–35, January/February 2004.

[21] M. K. Kazimierczuk and W. A. Tabisz, ''Class C-E High-Efficiency Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-36, pp. 421–428, March 1989.

[22] M. Iwadare, S. Mori, and K. Ikeda, ''Even Harmonic Resonant Class E Tuned Power Amplifier without RF Choke,'' *Electronics and Communications in Japan*, vol. 79, pp. 23–30, January 1996.

[23] D. K. Choi and S. I. Long, ''Finite DC Feed Inductor in Class E Power Amplifiers—A Simplified Approach,'' *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1643–1646.

[24] N. Zhang, Y.-O. Yam, B. Gao, and C.-W. Cheung, ''A New Type High Frequency Class E Power Amplifier,'' *Proc. 1997 Asia Pacific Microwave Conf.*, vol. 3, pp. 1117–1120.

[25] Y.-O. Yam, C.-W. Cheung, and C.-H. Li, ''Transmission-Line Modelling of the Class E Amplifier with an Analytical Method,'' *Int. J. Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 8, pp. 357–366, November 1995.

[26] T. B. Mader, E. W. Bryerton, M. Marcovic, M. Forman, and Z. Popovic, ''Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 1391–1398, October 1998.

[27] A. V. Grebennikov and H. Jaeger, ''High Efficiency Transmission Line Tuned Power Amplifier,'' U.S. Patent 6,552,610, April 2003.

[28] A. V. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[29] H. Jaeger, A. V. Grebennikov, E. P. Heaney, and R. Weigel, ''Broadband High-Efficiency Monolithic InGaP/GaAs HBT Power Amplifiers for 3G Handset Applications,'' *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 1035–1038.

[30] H. Jaeger, A. Grebennikov, E. Heaney, and R. Weigel, ''Broadband High-Efficiency Monolithic InGaP/GaAs HBT Power Amplifiers for Wireless Applications,'' *Int. J. RF and Microwave Computer-Aided Eng.*, vol. 13, pp. 496–510, November/December 2003.

[31] J. K. A. Everard and A. J. King, ''Broadband Power Efficient Class E Amplifiers with a Non-Linear CAD Model of the Active MOS Device,'' *J. IERE*, vol. 57, pp. 52–58, March 1987.

[32] C. S. Aitchison and R. V. Gelsthorpe, ''A Circuit Technique for Broadbanding the Electronic Tuning Range of Gunn Oscillators,'' *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 21–28, February 1977.

[33] R. V. Gelsthorpe and C. S. Aitchison, ''Analytical Evaluation of the Components Necessary for Double Reactance Compensation of an Oscillator,'' *Electronics Lett.*, vol. 12, pp. 485–486, September 1976.

[34] E. Camargo and D. Consoni, ''Reactance Compensation Matches FET Circuits,'' *Microwaves*, vol. 24, pp. 93–95, June 1985.

[35] R. Soares, *GaAs MESFET Circuit Design*, Boston: Artech House, 1988.

[36] I. A. Popov, ''Switching Mode of Single-Ended Transistor Power Amplifier (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Svyazi*, vol. 5, pp. 15–35, 1970.

[37] M. Kazimierczuk, ''Charge-Control Analysis of Class E Tuned Power Amplifier with Only One Inductor and One Capacitor in Load Network,'' *IEEE Trans. Electron Devices*, vol. ED-31, pp. 366–373, March 1984.

[38] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, New York: John Wiley & Sons, 1980.

[39] J. Modzelewski, ''Power Gain of Class E and Class B VHF Tuned Power Amplifiers,'' *Proc. 15th Int. Conf. Microwaves Radar Wireless Commun.*, vol. 1, pp. 41–44, 2004.

[40] C. Yoo and Q. Huang, ''A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25-$\mu$m CMOS,'' *IEEE J. Solid-State Circuits*, vol. SC-36, pp. 823–830, May 2001.

[41] K.-C. Tsai and P. R. Gray, ''A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications,'' *IEEE J. Solid-State Circuits*, vol. SC-34, pp. 962–970, July 1999.

[42] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, ''Analysis of Reliability and Power Efficiency in Cascode Class-E PAs,'' *IEEE J. Solid-State Circuits*, vol. SC-41, pp. 1222–1229, May 2006.

[43] K.-W. Ho and H. C. Luong, ''A 1-V CMOS Power Amplifier for Bluetooth Applications,'' *IEEE Trans. Circuits and Systems–II: Analog and Digital Signal Process.*, vol. CAS-II-50, pp. 445–449, August 2003.

[44] C. Wang, L. E. Larson, and P. M. Asbeck, ''Improved Design Technique of a Microwave Class-E Power Amplifier with Finite Switching-on Resistance,'' *Proc. 2002 IEEE Radio and Wireless Conf.*, pp. 241–244.

[45] P. Reynaert, K. L. R. Mertens, and M. S. J. Steyaert, ''A State-Space Behavioral Model for CMOS Class E Power Amplifiers,'' *IEEE Trans. Computer-Aided Design Integrated Circuits Syst.*, vol. CAD-22, pp. 132–138, February 2003.

[46] Z. Xu and E. I. El-Masry, ''Design and Optimization of CMOS Class-E Power Amplifier,'' *2003 IEEE Int. Symp. Circuits and Systems Dig.*, vol. 1, pp. 325–328.

[47] T. Sowlati, C. Andre, T. Salama, J. Sitch, G. Rabjohn, and D. Smith, ''Low Voltage, High Efficiency GaAs Class E Power Amplifiers for Wireless Transmitters,'' *IEEE Trans. Solid-State Circuits*, vol. SC-30, pp. 1074–1080, October 1995.

[48] T. Sowlati, Y. Greshishchev, C. Andre, and T. Salama, ''1.8 GHz Class E Power Amplifier for Wireless Communications,'' *Electronics Lett*., vol. 32, pp. 1846–1848, September 1996.

[49] T. T. Hung and M. N. El-Gamal, ''Class-E CMOS Power Amplifiers for RF Applications,'' *2003 IEEE Int. Symp. Circuits and Systems Dig*., vol. 1, pp. 449–452.

CHAPTER 7

# Class E with Quarter-wave Transmission Line

This chapter presents the results of exact time-domain analysis of the switched-mode tuned Class-E power amplifiers with a quarter-wave transmission line. The load-network parameters are derived analytically. The ideal collector voltage and current waveforms demonstrate a possibility of 100% efficiency without overlapping each other. The load network implementation including output-matching circuit at RF and microwave frequencies using lumped and transmission-line elements is considered with accurate derivation of the matching-circuit parameters. The switched-mode Class-E power amplifiers with a quarter-wave transmission line offer a new challenge for RF and microwave power amplification providing the high-efficiency and harmonic-suppression operation conditions.

## 7.1 Load Network with Parallel Quarter-wave Line

The ideal Class-F load network with a quarter-wave transmission line and a series $L_0C_0$ filter tuned to the fundamental frequency can provide a collector efficiency of 100% when the open-circuit conditions for odd-harmonic components and short-circuit conditions for even-harmonic components are realized. However, in practice, the idealized collector rectangular voltage and half-sinusoidal current waveforms corresponding to a Class-F operation mode provided by using a quarter-wave transmission line in the load network can be realized at sufficiently low frequencies when an effect of the device output capacitance shown in Fig. 7.1 is negligibly small. Generally, the effect of the device output capacitance contributes to a finite switching time resulting in time periods when the collector voltage and collector current exist at the same time. As a result, such a load network with the quarter-wave transmission line and shunt capacitance cannot provide the switched-mode operation with an instantaneous transition from the device pinch-off mode to saturation mode. Hence, during a finite time interval, the device operates in the active region as a current source with reverse-biased collector-base junction, and the collector current is provided by this current source. In this case, the required optimum conditions can be provided only for the fundamental frequency and several higher-order harmonic components. Moreover, at high frequencies, it is necessary to take into account the effects of the bond-wire inductor connecting physically the

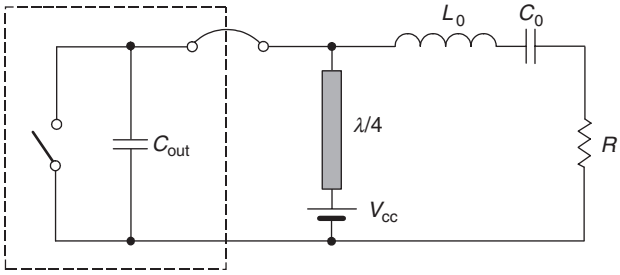



**Figure 7.1: Class-F load network with parasitic shunt capacitance and bondwire inductance.**

device die with the off-chip board. In a packaged device, it adds to the lead inductance and its effects must be assessed. Therefore, a special case is a load network with a quarter-wave transmission line when the lossless transformation of a dc power to a fundamental-frequency output power can be provided. Fortunately, as it will be further demonstrated, the collector efficiency can be increased and the effect of the collector capacitance can be compensated with an inclusion of a series inductance between a shunt capacitance and a quarter-wave transmission line realizing the switching Class-E operation conditions. The obvious advantage of such a load network is a combination of the high-operating efficiency corresponding to a Class-E mode and an even-harmonic suppression due to a quarter-wave transmission line used in the Class-F mode.

The possibility to include a quarter-wave transmission line into the Class-E load network with a shunt capacitance instead of an RF choke was first considered in 1975 [1]. However, such a location for a quarter-wave transmission line with a straight connection to the device collector violates the required capacitive-reactance conditions at even harmonics by providing simply their short circuiting. As a result, an optimum Class-E operation mode cannot be realized when the shapes of the collector current and voltage waveforms provide a condition at which the high current and high voltage do not overlap simultaneously. Moreover, the larger the value of the shunt capacitance, the smaller the collector efficiency achieved.

Fig. 7.2 shows a Class-E load network consisting of a shunt capacitor $C$, a series inductor $L$, a quarter-wave transmission line, a series-reactance $X$, a series-resonant $L_0C_0$ circuit tuned to the fundamental frequency, and a load resistor $R$. The bottom end of the quarter-wave transmission line is connected between the series inductor $L$ and the series reactance $X$, while its top end is connected to a dc power supply being RF grounded through the bypass capacitor. In a common case, a shunt capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The series reactance $X$ generally can be positive (inductance), negative (capacitance), or zero depending on the values of the shunt capacitance $C$ and series inductance $L$. The active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the switch

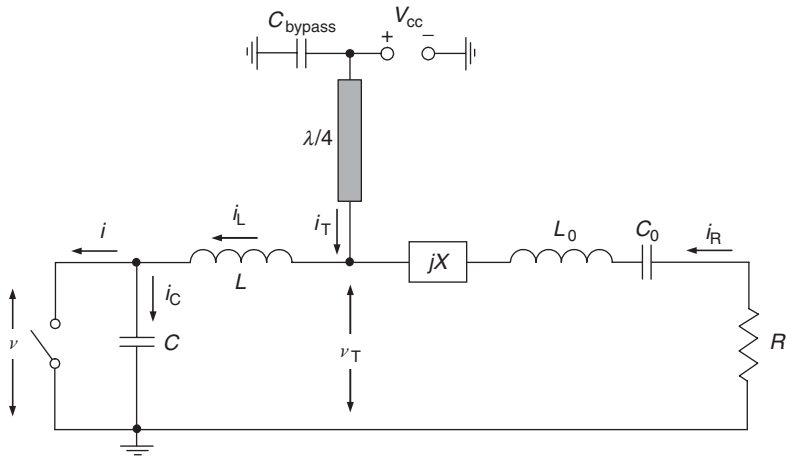



**Figure 7.2: Equivalent circuit of Class-E power amplifier with quarter-wave transmission line.**

when it is turned on and by the transient response of the load network when the switch is turned off.

To simplify an analysis of a Class-E power amplifier with a quarter-wave transmission line, the following assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The total shunt capacitance is independent of the collector and is assumed linear.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series-resonant $L_0C_0$ circuit tuned to the fundamental frequency is high enough that the output current is sinusoidal at the switching frequency.
- There are no losses in the circuit except in the load $R$.
- For an optimum switching operation mode, a 50% duty ratio is used.

Let the output current flowing into the load be sinusoidal as

$$i_R(\omega t) = I_R \sin(\omega t + \varphi), \tag{7.1}$$

where $\varphi$ is the initial phase shift due to the shunt capacitance and series inductance.

For lossless operation, it is necessary to provide the following optimum conditions for voltage across the switch at the turn-on instant of $\omega t = 2\pi$, when the transistor is voltage saturated:

$$v(\omega t)\big|_{\omega t=2\pi} = 0 \tag{7.2}$$

$$\left.\frac{dv(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0, \tag{7.3}$$

where $v$ is the voltage across the switch.

When the switch is turned on for $0 \leq \omega t < \pi$, the current flowing through the shunt capacitance $i_C(\omega t) = 0$ and, consequently,

$$i(\omega t) = i_L(\omega t) = i_T(\omega t) + i_R(\omega t). \tag{7.4}$$

When the switch is turned off for $\pi \leq \omega t < 2\pi$, there is no current flowing through the switch when $i(\omega t + \pi) = 0$, and the current flowing through the shunt capacitance $C$ is

$$i_C(\omega t + \pi) = i_L(\omega t + \pi) = i_T(\omega t + \pi) + i_R(\omega t + \pi). \tag{7.5}$$

To link both Eqs. (7.4) and (7.5), each corresponding to one-half period, it is necessary to use a basic equation for the current flowing into the quarter-wave transmission line given by Eq. (3.71) as

$$i_T(\omega t) = i_T(\omega t + \pi), \tag{7.6}$$

which means that the period of a signal flowing into the quarter-wave transmission line is equal to $\pi$ because it contains only even harmonics.

Then,

$$i_L(\omega t) = i_T(\omega t + \pi) + i_R(\omega t) = i_L(\omega t + \pi) + i_R(\omega t) - i_R(\omega t + \pi), \tag{7.7}$$

resulting in

$$i_L(\omega t) - i_L(\omega t + \pi) = 2i_R(\omega t). \tag{7.8}$$

The current $i_L(\omega t + \pi) = i_C(\omega t + \pi)$ can be expressed through the voltages $v_T(\omega t + \pi)$ and

$$v_L(\omega t + \pi) = \omega L \frac{di_L(\omega t + \pi)}{d(\omega t)} \tag{7.9}$$

as

$$\begin{aligned} i_{\mathrm{L}}(\omega t+\pi) &= \omega C \frac{dv(\omega t+\pi)}{d(\omega t)} \\ &= \omega C \frac{d}{d(\omega t)}\left[v_{\mathrm{T}}(\omega t+\pi) - \omega L \frac{di_{\mathrm{L}}(\omega t+\pi)}{d(\omega t)}\right]. \end{aligned} \tag{7.10}$$

Now we can use the equation for a voltage at the input of the quarter-wave transmission line corresponding to each of a period given by Eq. (3.70) as

$$v_{\mathrm{T}}(\omega t) = 2V_{\mathrm{cc}} - v_{\mathrm{T}}(\omega t+\pi). \tag{7.11}$$

Hence, when the switch is turned on resulting in $v_{\mathrm{T}}(\omega t) = v_{\mathrm{L}}(\omega t)$,

$$v_{\mathrm{T}}(\omega t+\pi) = 2V_{\mathrm{cc}} - \omega L \frac{di_{\mathrm{L}}(\omega t)}{d(\omega t)}. \tag{7.12}$$

Substituting Eq. (7.12) in Eq. (7.10) and using Eqs. (7.1) and (7.8) yields a second-order non-homogeneous differential equation corresponding to half a period of $\pi \leq \omega t < 2\pi$ when $i_{\mathrm{L}}(\omega t+\pi) = i_{\mathrm{C}}(\omega t+\pi)$ in the form of

$$\frac{d^2 i_{\mathrm{C}}(\omega t+\pi)}{d(\omega t)^2} + \frac{q^2}{2} i_{\mathrm{C}}(\omega t+\pi) - I_{\mathrm{R}} \sin(\omega t+\varphi) = 0 \tag{7.13}$$

or

$$\frac{d^2 i_{\mathrm{C}}(\omega t)}{d(\omega t)^2} + \frac{q^2}{2} i_{\mathrm{C}}(\omega t) + I_{\mathrm{R}} \sin(\omega t+\varphi) = 0, \tag{7.14}$$

where

$$q = \frac{1}{\omega\sqrt{LC}}. \tag{7.15}$$

The general solution of Eq. (7.14) in the normalized form can be written as

$$\frac{i_{\mathrm{C}}(\omega t)}{I_{\mathrm{R}}} = C_1 \cos\left(\frac{q\omega t}{\sqrt{2}}\right) + C_2 \sin\left(\frac{q\omega t}{\sqrt{2}}\right) + \frac{2}{2-q^2}\sin(\omega t+\varphi), \tag{7.16}$$

where the coefficients $C_1$ and $C_2$ are determined from the initial off-state conditions.

The first initial condition is obtained from Eq. (7.8) as

$$i_{\mathrm{C}}(\omega t)\big|_{\omega t=\pi} = 2i_{\mathrm{R}}(\pi) \tag{7.17}$$

taking into account that $i_{\mathrm{L}}(\pi) = i_{\mathrm{C}}(\pi)$ and $i_{\mathrm{L}}(2\pi) = i_{\mathrm{C}}(2\pi) = 0$.

To obtain a second initial condition, let us substitute Eq. (7.9) in Eq. (7.11) and use Eq. (7.8). As a result,

$$\begin{aligned}\omega L\frac{di_{\mathrm{L}}(\omega t+\pi)}{d(\omega t)} &= 2V_{\mathrm{cc}}-\omega L\frac{di_{\mathrm{L}}(\omega t)}{d(\omega t)}\\ &= 2V_{\mathrm{cc}}-\omega L\frac{di_{\mathrm{L}}(\omega t+\pi)}{d(\omega t)}-2\omega L\frac{di_{\mathrm{R}}(\omega t)}{d(\omega t)}.\end{aligned} \tag{7.18}$$

Then, by taking into account that $i_{\mathrm{L}}(\pi)=i_{\mathrm{C}}(\pi)$, we can write

$$\left.\frac{di_{\mathrm{C}}(\omega t)}{d(\omega t)}\right|_{\omega t=\pi}=\frac{V_{\mathrm{cc}}}{\omega L}-I_{\mathrm{R}}\cos\varphi. \tag{7.19}$$

As a result, applying the initial conditions given by Eqs. (7.17) and (7.19) to Eq. (7.16) yields

$$\begin{aligned}C_1=&-\frac{\sqrt{2}}{qp}\sin\left(\frac{q\pi}{\sqrt{2}}\right)-\frac{q\sqrt{2}}{2-q^2}\sin\left(\frac{q\pi}{\sqrt{2}}\right)\cos\varphi\\ &-2\frac{1-q^2}{2-q^2}\cos\left(\frac{q\pi}{\sqrt{2}}\right)\sin\varphi\end{aligned} \tag{7.20}$$

$$\begin{aligned}C_2=&\frac{\sqrt{2}}{qp}\cos\left(\frac{q\pi}{\sqrt{2}}\right)+\frac{q\sqrt{2}}{2-q^2}\cos\left(\frac{q\pi}{\sqrt{2}}\right)\cos\varphi\\ &-2\frac{1-q^2}{2-q^2}\sin\left(\frac{q\pi}{\sqrt{2}}\right)\sin\varphi,\end{aligned} \tag{7.21}$$

where

$$p=\frac{\omega LI_{\mathrm{R}}}{V_{\mathrm{cc}}}. \tag{7.22}$$

The dc supply current $I_0$ can be written using the Fourier formula and Eqs. (7.5) and (7.6) by

$$\begin{aligned}I_0=\frac{1}{2\pi}\int_0^{2\pi}i_{\mathrm{T}}(\omega t)d(\omega t)&=\frac{1}{\pi}\int_0^{\pi}i_{\mathrm{T}}(\omega t+\pi)\,d(\omega t)\\ &=\frac{1}{\pi}\int_0^{\pi}[i_{\mathrm{C}}(\omega t+\pi)-i_{\mathrm{R}}(\omega t+\pi)]\,d(\omega t).\end{aligned} \tag{7.23}$$

Then, substituting Eqs. (7.1) and (7.16) in Eq. (7.23) results in

$$I_0 = \frac{I_R}{\pi}\left\{C_1\frac{\sqrt{2}}{q}\left[\sin(q\pi\sqrt{2}) - \sin\left(\frac{q\pi}{\sqrt{2}}\right)\right]\right.$$

$$\left. -C_2\frac{\sqrt{2}}{q}\left[\cos(q\pi\sqrt{2}) - \cos\left(\frac{q\pi}{\sqrt{2}}\right)\right] - \frac{2q^2}{2-q^2}\cos\varphi\right\}. \tag{7.24}$$

The voltage $v(\omega t)$ across the switch is produced by the charging of the shunt capacitor $C$ by the current given by Eq. (7.16) according to

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_C(\omega t)\,d\omega t = -\frac{I_R\sqrt{2}}{q\omega C}\left\{C_1\left[\sin\left(\frac{q\omega t}{\sqrt{2}}\right) - \sin\left(\frac{q\pi}{\sqrt{2}}\right)\right]\right.$$

$$\left. -C_2\left[\cos\left(\frac{q\omega t}{\sqrt{2}}\right) - \cos\left(\frac{q\pi}{\sqrt{2}}\right)\right] - \frac{q\sqrt{2}}{2-q^2}[\cos(\omega t+\varphi) + \cos\varphi]\right\}. \tag{7.25}$$

Generally, Eq. (7.25) for the collector voltage contains the three unknown parameters $q$, $p$, and $\varphi$, which must be determined. In a common case, the parameter $q$ can be considered a variable, and the other two parameters $p$ and $\varphi$ are determined from a system of the two equations resulting from applying the two optimum zero-voltage and zero voltage-derivative conditions given by Eqs. (7.2) and (7.3) to Eq. (7.25). Fig. 7.3 shows the dependences of the optimum parameters $p$ and $\varphi$ versus $q$ for a Class E with a parallel quarter-wave transmission line.

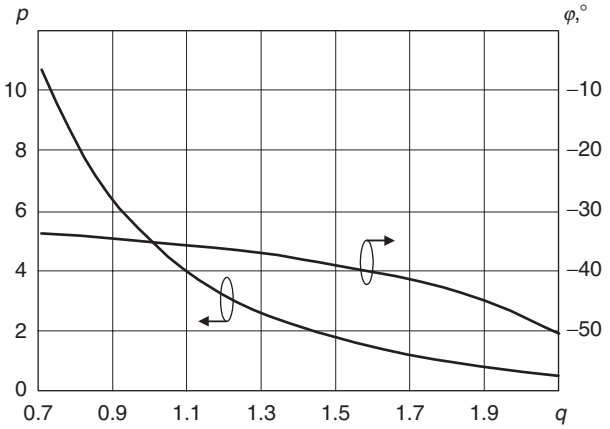



**Figure 7.3: Optimum quarter-wave-line Class-E parameters $p$ and $\varphi$ versus $q$.**

For the boundary cases when $q = 1/\sqrt{2}$ and $q = 3/\sqrt{2}$, the optimum parameters $p$ and $\varphi$ can easily be defined analytically, the exact values of which are for

$$q = \frac{1}{\sqrt{2}} = 0.707 \tag{7.26}$$

$$\varphi = \tan^{-1}\left(-\frac{2}{3}\right) = -33.69^\circ \tag{7.27}$$

$$p = -\frac{6}{\sin\varphi} = 10.82 \tag{7.28}$$

and for

$$q = \frac{3}{\sqrt{2}} = 2.12 \tag{7.29}$$

$$\varphi = \tan^{-1}\left(-\frac{6}{5}\right) = -50.2^\circ \tag{7.30}$$

$$p = -\frac{10}{27\sin\varphi} = 0.482. \tag{7.31}$$

The current $i(\omega t) = i_L(\omega t)$ flowing through the inductor $L$ and the switch when the switch is turned on $0 \leq \omega t < \pi$ can be written using Eqs. (7.4) to (7.6) and (7.16) in a normalized form as

$$\frac{i(\omega t)}{I_R} = C_1 \cos\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + C_2 \sin\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + 2\,\frac{1-q^2}{2-q^2}\sin(\omega t + \varphi). \tag{7.32}$$

Then, the normalized voltage $v_T(\omega t)$ during this period can be obtained by

$$\frac{v_T(\omega t)}{V_{cc}} = \frac{\omega L I_R}{V_{cc}}\,\frac{di_L(\omega t)}{d(\omega t)} = p\left\{-C_1\frac{q}{\sqrt{2}}\sin\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right]\right.$$
$$\left. + C_2\frac{q}{\sqrt{2}}\cos\left[\frac{q}{\sqrt{2}}(\omega t + \pi)\right] + 2\,\frac{1-q^2}{2-q^2}\cos(\omega t + \varphi)\right\}. \tag{7.33}$$

However, when the switch is turned off for $\pi \leq \omega t < 2\pi$, it can be calculated from Eq. (7.11).

## 7.2 Optimum Load Network Parameters

To calculate the optimum load network parameters for a Class E with a parallel quarter-wave transmission line, first it is necessary to define the reactive quadrature fundamental-frequency Fourier component of the voltage $v_T(\omega t)$ according to

$$\begin{aligned} V_X = &-\frac{1}{\pi}\int_0^{\pi} v_T(\omega t)\cos(\omega t+\varphi)\,d(\omega t) \\ &-\frac{1}{\pi}\int_{\pi}^{2\pi}[2V_{cc}-v_T(\omega t-\pi)]\cos(\omega t+\varphi)\,d(\omega t). \end{aligned} \tag{7.34}$$

Then, the two active and reactive quadrature fundamental-frequency Fourier components of the collector voltage $v(\omega t)$ are defined from

$$V_R = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t+\varphi)\,d(\omega t) \tag{7.35}$$

$$V_{L+X} = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t+\varphi)\,d(\omega t). \tag{7.36}$$

Finally, as it follows from Fig. 7.4, the optimum normalized series reactance $X$, series inductance $L$, and shunt capacitance $C$ can be calculated from

$$\frac{X}{R} = \frac{V_X}{V_R} \tag{7.37}$$

$$\frac{\omega L}{R} = \frac{V_{L+X}}{V_R} - \frac{X}{R} \tag{7.38}$$

$$\omega CR = \frac{1}{q^2\frac{\omega L}{R}}. \tag{7.39}$$

By taking into account that $R = V_R^2/2P_{out}$, the optimum load resistance $R$ for the specified values of a supply voltage $V_{cc}$ and an output power $P_{out}$ delivered to the load can be obtained by

$$R = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2\frac{V_{cc}^2}{P_{out}}, \tag{7.40}$$

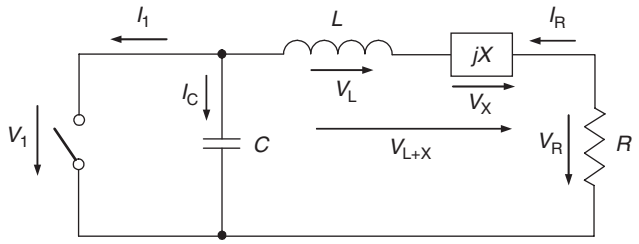



**Figure 7.4: Equivalent quarter-wave-line Class-E load network at fundamental frequency.**

or, using Eq. (7.22), by

$$R = \frac{1}{2}\left(\frac{p}{l}\right)^2 \frac{V_{cc}^2}{P_{out}}, \tag{7.41}$$

where $l = \omega L/R$.

The dependences of the normalized optimum series inductance $\omega L/R$ and series reactance $X/R$ are shown in Fig. 7.5($a$), while the dependences of the normalized optimum shunt capacitance $\omega CR$ and load resistance $RP_{out}/V_{cc}^2$ are plotted in Fig. 7.5($b$). Here, we can see that the lower value is $q$ and the greater value is the normalized series inductance $\omega L/R$. To compensate for such an increased inductive value, the reactance $X$ should have a negative capacitive value. Generally, the value of the series reactance $X$ changes its sign from negative to positive, which means that the capacitive reactance is followed by the inductive reactance, and it is required to add an additional inductance at higher values of $q$. As a result, there is a special case of a load network with $X = 0$ when there is no need for additional phase compensation. The variations of normalized values of $\omega CR$ and $RP_{out}/V_{cc}^2$ versus $q$ are not so significant.

Fig. 7.6 shows the circuit schematics of the Class-E power amplifiers with a parallel quarter-wave transmission line corresponding to different values of the optimum parameter $q$. The inclusion of a series capacitance $C_x$ is necessary to compensate for the excess inductive reactance at the fundamental frequency when the series reactance $X$ is negative, as shown in Fig. 7.6($a$). However, when the series reactance $X$ is positive, an additional series inductance $L_X$ shown in Fig. 7.6($c$) is necessary to increase the total series inductance at the fundamental frequency. The special case is a zero series reactance $X$ corresponding to a circuit schematic shown in Fig. 7.6($b$), which we will consider later in more detail.

## 7.3 Load Network with Zero Series Reactance

In this case, the Class-E load network consists of a shunt capacitor $C$, a series inductor $L$, a parallel quarter-wave transmission line connected to a voltage supply, a series $L_0C_0$-resonant circuit tuned to the fundamental frequency, and a load resistor $R$. Because the parameter

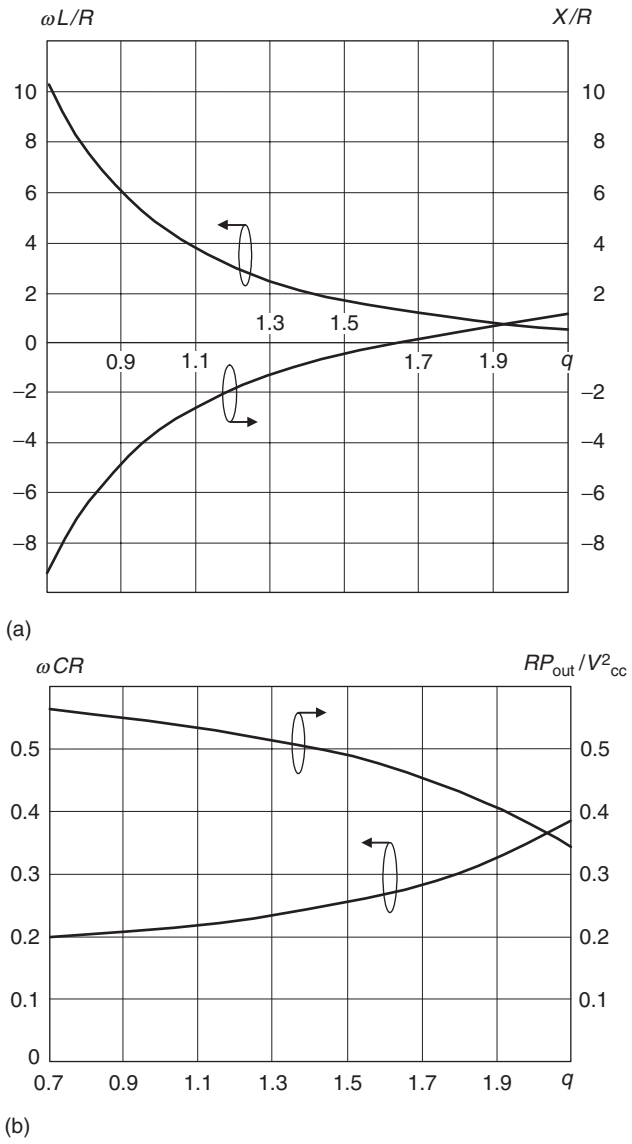



**Figure 7.5: Normalized optimum quarter-wave-line Class-E load network parameters.**

$q$ corresponding to a zero reactance $X$ is unknown a priori, generally it is necessary to solve a system of three equations to define the three unknown parameters $q$, $p$, and $\varphi$. Two equations are the result of applying the two optimum zero-voltage and zero-voltage derivative conditions given by Eqs. (7.2) and (7.3) to Eq. (7.25). Since the fundamental component of the voltage $v_T(\omega t)$ is fully applied to the load, this means that its reactive part must have zero value, resulting in an additional equation

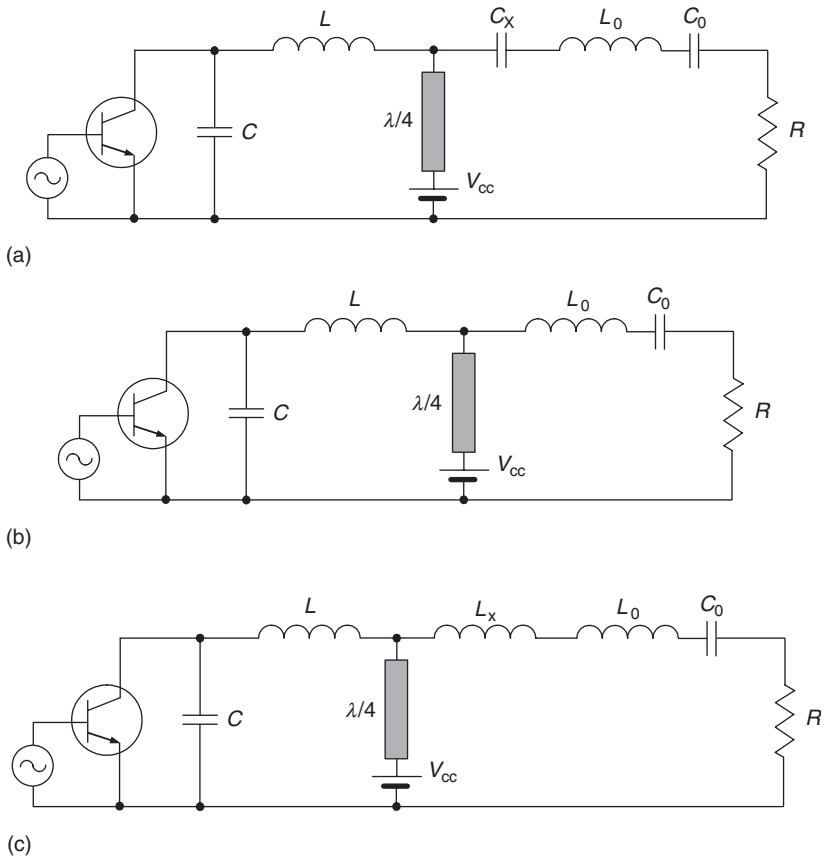



**Figure 7.6: Schematic of Class-E power amplifiers with quarter-wave line.**

$$V_X = -\frac{1}{\pi}\int_0^{\pi} v_T(\omega t)\cos(\omega t + \varphi)\, d(\omega t)$$
$$-\frac{1}{\pi}\int_{\pi}^{2\pi} [2V_{cc} - v_T(\omega t - \pi)]\cos(\omega t + \varphi)\, d(\omega t) = 0. \tag{7.42}$$

As a result, the following exact values can be obtained numerically for the unknown parameters [2, 3]:

$$q = 1.649 \tag{7.43}$$

$$p = 1.302 \tag{7.44}$$

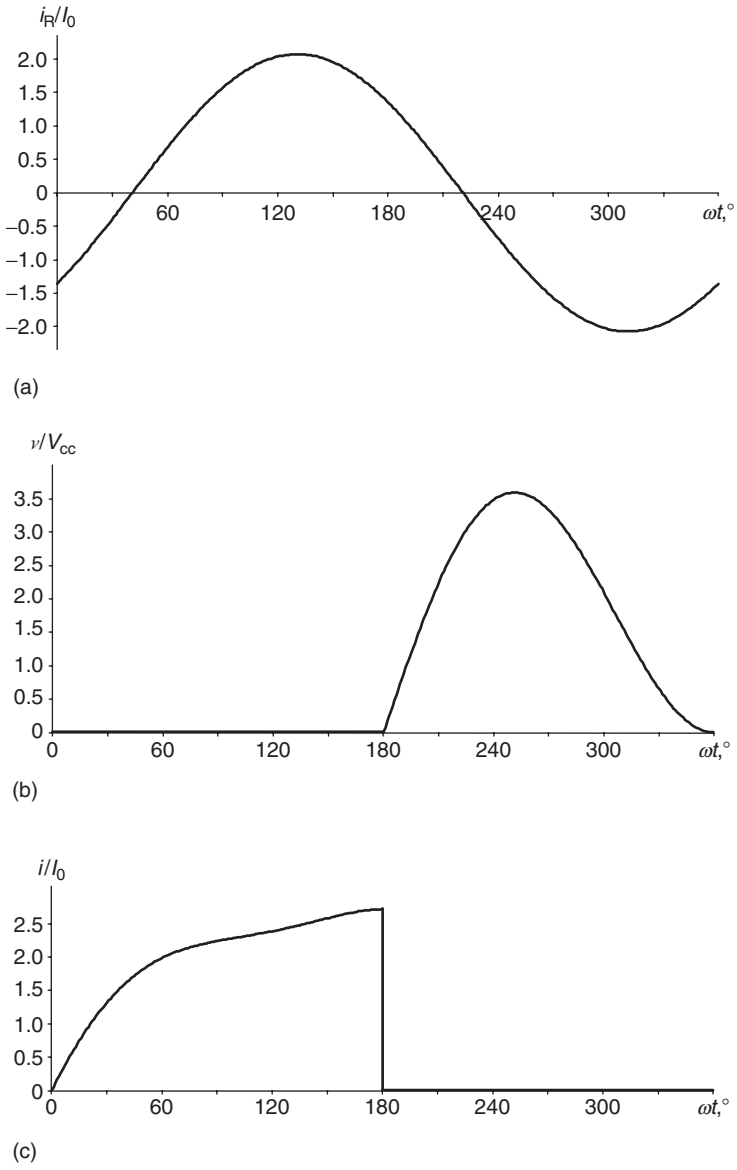



**Figure 7.7: Voltage and current waveforms of quarter-wave-line Class-E power amplifier.**

$$\varphi = -40.8^\circ. \tag{7.45}$$

Fig. 7.7 shows the normalized (*a*) load current, (*b*) collector voltage, and (*c*) current waveforms for idealized optimum Class-E mode with a parallel quarter-wave transmission line. From the collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch, and the collector current consisting of the load

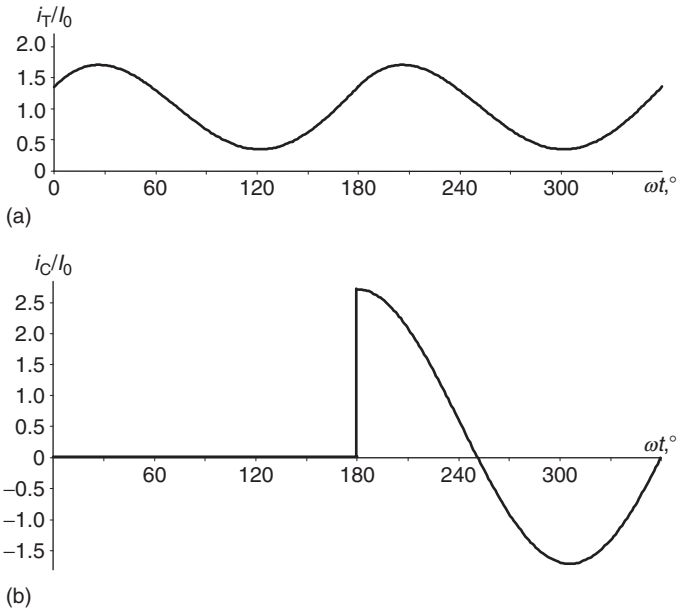



**Figure 7.8: Current waveforms of quarter-wave-line Class-E power amplifier.**

sinusoidal current shown in Fig. 7.7(*a*) and transmission-line current shown in Fig. 7.8(*a*) flows through the switch. However, when the transistor is turned off, this current with the waveform shown in Fig. 7.8(*b*) now flows through the shunt capacitance, the charging process of which produces the collector voltage.

In an idealized Class-E operation mode, there is no nonzero voltage and current simultaneously; that means a lack of power losses and gives an idealized collector efficiency of 100%. This implies that the dc power and the fundamental output power are equal,

$$I_0 V_{cc} = \frac{I_R V_R}{2}, \tag{7.46}$$

where $V_R = I_R R$ is the fundamental voltage amplitude across the load resistance $R$.

By using Eqs. (7.22) and (7.46), the normalized inductance can be defined as

$$\frac{\omega L}{R} = \frac{p}{2}\left(\frac{I_0}{I_R}\right)^{-1}. \tag{7.47}$$

As a result, the exact values of the optimum series inductance $L$, shunt capacitance $C$, and load resistance $R$ can be calculated by using Eqs. (7.24), (7.39), and (7.41) from

$$L = 1.349\frac{R}{\omega} \tag{7.48}$$

$$C = \frac{0.2725}{\omega R} \tag{7.49}$$

$$R = 0.465\frac{V_{cc}^2}{P_{out}}. \tag{7.50}$$

The peak collector current $I_{max}$ and peak collector voltage $V_{max}$ can be determined directly from Eqs. (7.25) and (7.32) using Eq. (7.24) from numerical calculations that gives

$$I_{max} = 2.714\ I_0 \tag{7.51}$$

$$V_{max} = 3.589\ V_{cc}. \tag{7.52}$$

Using Eqs. (7.49) and (7.50) when $C = C_{out}$, where $C_{out}$ is the device output capacitance, gives the value of a maximum operation frequency $f_{max}$ of

$$f_{max} = 0.093\frac{P_{out}}{C_{out}V_{cc}^2}, \tag{7.53}$$

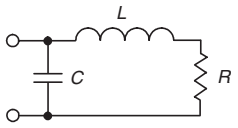
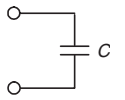
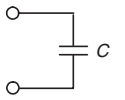
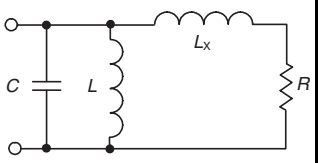
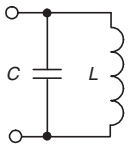
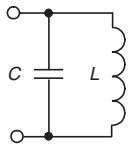
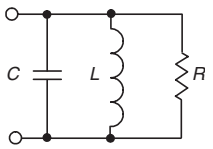
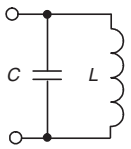
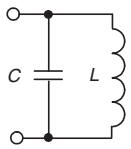
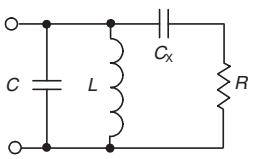
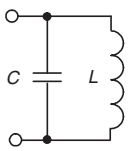
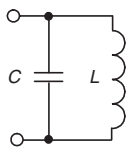
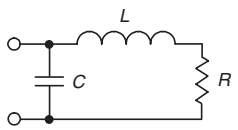
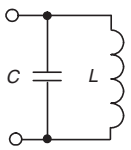
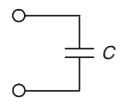
which is 1.63 times as high as the maximum operation frequency for an optimum Class-E mode with shunt capacitance [4].

In Table 7.1, the optimum impedances seen by the device collector at the fundamental-frequency and higher-order harmonic components are illustrated by the appropriate circuit configurations. It can be seen that Class-E mode with a quarter-wave transmission line shows different impedance properties at even and odd harmonics. At odd harmonics, the optimum impedances can be established by the shunt capacitance that is required for all harmonic components in Class E with a shunt capacitance. At even harmonics, the optimum impedances are realized by using a parallel LC circuit that is required for all harmonic components in Class E with a finite dc-feed inductance. Thus, the frequency properties of a grounded parallel quarter-wave transmission line with its open-circuit conditions at odd harmonics and short-circuit conditions at even harmonics enable Class E with a quarter-wave transmission line to combine simultaneously the harmonic impedance conditions typical for both Class E with a shunt capacitance and Class E with a finite dc-feed inductance.

## 7.4 Matching Circuit with Lumped Elements

The theoretical results obtained for the Class-E power amplifier with a quarter-wave transmission line show that it is enough to use a very simple load network to realize the optimum impedance conditions even for four harmonics. As follows from Fig. 7.8(*a*), the

**Table 7.1: Optimum Impedances at Fundamental and Harmonics for Different Class-E Load Networks**

| Class-E Load Network | $f_0$ (fundamental) | $2nf_0$ (even harmonics) | $(2n+1)f_0$ (odd harmonics) |
|---|---|---|---|
| Class E with shunt capacitance |  |  |  |
| Subharmonic Class E |  |  |  |
| Parallel-circuit Class E |  |  |  |
| Even-harmonic Class E |  |  |  |
| Class E with quarter-wave transmission line |  |  |  |

current flowing into the quarter-wave transmission line is very close to the sinusoidal second harmonic current, which means that the level of fourth and higher-order harmonic components is negligible because of the significant shunting effect of the capacitance $C$. In this case, as the shunt capacitor $C$ and series inductor $L$ provide optimum inductive impedance at the fundamental frequency and the quarter-wave transmission line realizes the shorting of even harmonics, it is only required to provide an open-circuit condition at the third harmonic component. Consequently, when the ideal series $L_0C_0$ circuit is replaced by the output matching circuit, the optimum impedance conditions for Class-E load network with a quarter-wave transmission line can be practically fully realized by simply providing an open-circuit condition at the third-harmonic component.

Fig. 7.9 shows the circuit schematic of a lumped Class-E power amplifier with a parallel quarter-wave transmission line, where the parallel resonant $L_1C_1$ circuit tuned to the third harmonic component is used and $C_b$ represents the blocking or bypass capacitor. Since the reactance of the parallel third harmonic tank circuit is inductive at the fundamental frequency, it is enough to use the shunt capacitance $C_2$ composing the L-type low-pass matching circuit to provide the required impedance matching of the optimum Class-E load resistance $R$ with the standard load impedance of $R_L = 50\,\Omega$. In this case, it is assumed that $R < R_L$, which is normally the case for high-power or low-voltage power amplifiers.

To calculate the parameters of the matching-circuit elements, consider the loaded quality factor $Q_L = \omega C_2 R_L$, which also can be expressed through the resistances $R$ and $R_L$ as [3, 5]

$$Q_L = \sqrt{\left(\frac{R_L}{R}\right) - 1}. \tag{7.54}$$

As a result, the matching circuit parameters can be calculated at the fundamental frequency $\omega_0$ from

$$C_2 = \frac{Q_L}{\omega_0 R_L} \tag{7.55}$$

$$L_1 = \frac{8}{9}\frac{Q_L R}{\omega_0} \tag{7.56}$$

$$C_1 = \frac{1}{9\omega_0^2 L_1}. \tag{7.57}$$

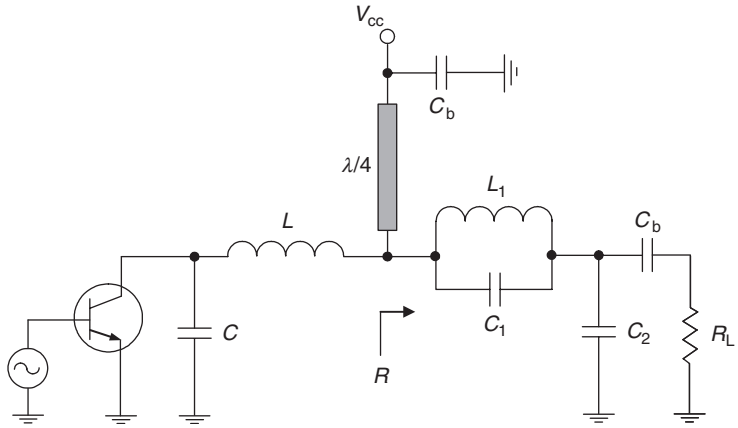



**Figure 7.9: Schematic of quarter-wave-line Class-E power amplifier with lumped matching circuit.**

## 7.5 Matching Circuit with Transmission Lines

At ultra-high frequencies and microwaves, the series lumped inductor $L$ should be replaced by a short-length series transmission line. In this case, when the shunt capacitance $C$ represents a fully internal active-device output capacitance, the bond-wire and lead inductances can also be taken into account because they provide an inductive reactance and make the series transmission line shorter. Fig. 7.10 shows the circuit schematic of a transmission-line Class-E power amplifier with a parallel quarter-wave transmission line. The output-matching circuit represents the L-type low-pass matching circuit consisting of a series transmission line with a short electrical length $\theta_1$, which provides an inductive reactance, and a shunt open-circuit stub with an electrical length $\theta_2$ of less than $90^\circ$, which provides a capacitive reactance.

Usually, the characteristic impedance $Z_0$ of a transmission line (in most practical cases equal to $50\,\Omega$) is much higher than the required optimum Class-E load network resistance $R$. Consequently, the input impedance $Z_{\text{in}}$ of the loaded series transmission line with the characteristic impedance $Z_0$ and electrical length $\theta_0$ under the condition of

$$\frac{R\tan\theta_0}{Z_0} << 1$$

when the electrical length of a sufficiently short transmission line is less than $45^\circ$, is determined by

$$\begin{aligned} Z_{\text{in}} &= Z_0\frac{R + jZ_0\tan\theta_0}{Z_0 + jR\tan\theta_0} \\ &= Z_0\frac{\frac{R}{Z_0} + j\tan\theta_0}{1 + j\frac{R}{Z_0}\tan\theta_0} \cong R + jZ_0\tan\theta_0. \end{aligned} \tag{7.58}$$

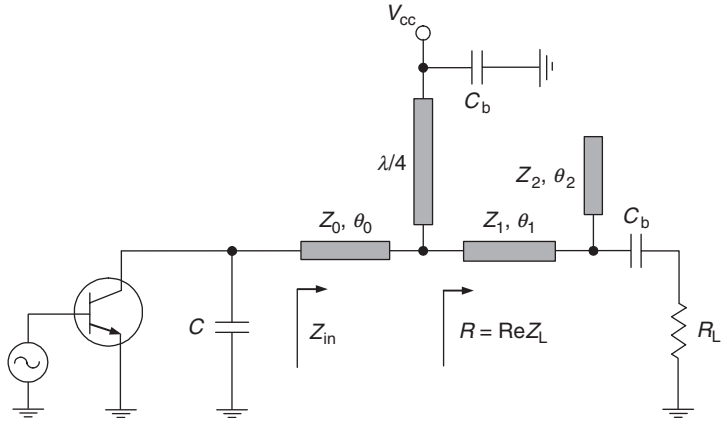



**Figure 7.10: Schematic of transmission-line Class-E power amplifier.**

As a result, the required optimum value of $\theta_0$ for Class-E mode with a quarter-wave transmission line using Eqs. (7.48) and (7.58) can be obtained from

$$\theta_0 = \tan^{-1}\left(1.349\frac{R}{Z_0}\right). \tag{7.59}$$

The output-matching circuit is necessary to match the required optimum Class-E resistance $R$ calculated in accordance with Eq. (7.50) to a standard load resistance of $50\,\Omega$. In addition, it is required to provide an open-circuit condition at the third-harmonic component. This can be easily done using the output-matching topology in the form of an L-type transformer with the series transmission line and open-circuit stub [3, 6]. In this case, the electrical lengths of the series transmission line and open-circuit stub should be chosen to be $30^\circ$ each. The load impedance $Z_L$ seen by a quarter-wave transmission line can be written by

$$Z_L = Z_1\frac{R_L(Z_2 - Z_1\tan^2\theta) + jZ_1Z_2\tan\theta}{Z_1Z_2 + j(Z_1 + Z_2)R_L\tan\theta}, \tag{7.60}$$

where $\theta = \theta_1 = \theta_2 = 30^\circ$, $Z_1$ and $\theta_1$ are the characteristic impedance and electrical length of the series transmission line, and $Z_2$ and $\theta_2$ are the characteristic impedance and electrical length of the open-circuit stub.

Hence, the complex-conjugate matching with the load can be provided by proper choice of the characteristic impedances $Z_1$ and $Z_2$. Separating Eq. (7.60) into real and imaginary parts and taking into account that $\mathrm{Re}Z_L = R$ and $\mathrm{Im}Z_L = 0$, the following system of two equations with two unknown parameters is obtained:

$$Z_1^2Z_2^2 - R_L^2(Z_1 + Z_2)(Z_2 - Z_1\tan^2\theta) = 0 \tag{7.61}$$

$$(Z_1 + Z_2)^2R_L^2R\tan^2\theta - Z_1^2Z_2^2[R_L(1 + \tan^2\theta) - R] = 0, \tag{7.62}$$

which enables the characteristic impedances $Z_1$ and $Z_2$ to be properly calculated.

This system of two equations can be solved explicitly as a function of the parameter $r = R_L/R$ resulting in

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r - 3}}{r} \tag{7.63}$$

$$\frac{Z_1}{Z_2} = 3\left(\frac{r - 1}{r}\right). \tag{7.64}$$

Consequently, for the specified value of the parameter $r$ with the required Class-E optimum load resistance $R$ and standard load $R_L = 50\,\Omega$, the characteristic impedance

$Z_1$ is calculated from Eq. (7.63) and, then, the characteristic impedance $Z_2$ is calculated from Eq. (7.64). For example, if the required Class-E optimum load resistance $R$ is equal to 12.5 Ω resulting in $r = 4$, the characteristic impedance of the series transmission line $Z_1$ is equal to 45 Ω and the characteristic impedance of the open-circuit stub $Z_2$ is equal to 20 Ω.

Unlike the transmission-line Class-E load network approximations with two-harmonic control [7] and with three-harmonic control [8], the Class-E load network with a quarter-wave transmission line, which can provide the optimum-impedance conditions for at least four harmonic components, is very simple in circuit implementation and does not require an additional lumped RF choke element. In addition, there is no need to use the special computer simulation tools required to calculate the parameters of the existing Class-E transmission-line load-network topologies [8–10], since all parameters of the Class-E load network with a quarter-wave transmission line, and the output-matching circuit parameters, are easily calculated explicitly from simple analytical equations. Besides, such a Class-E load network with a quarter-wave transmission line is very useful in practical design providing simultaneously significant higher-order harmonic suppression.

## 7.6 Load Network with Series Quarter-wave Line and Shunt Filter

Fig. 7.11 shows an alternative configuration for the Class-E power amplifier with a parallel quarter-wave transmission line consisting of a shunt capacitor $C$, a series inductor $L$, a series quarter-wave transmission line, a parallel-resonant $L_0C_0$ circuit tuned to the fundamental frequency, a shunt susceptance $B$, and a load resistor $R$. In a common case, the shunt capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The shunt susceptance $B$ generally can be positive (capacitance), negative (inductance), or zero, depending on the value of the optimum-load network parameter $q$. The RF choke is necessary to isolate the dc power supply from the RF circuit, while the blocking capacitor $C_b$ is necessary to separate the dc supply circuit from the load. The operation principle of such a Class-E load network with a series quarter-wave line is similar to

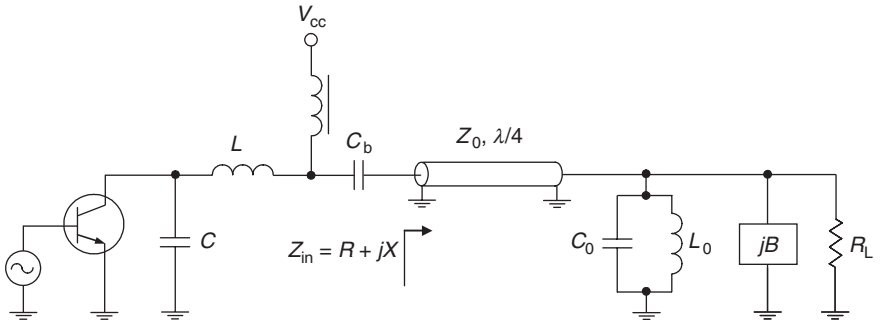



**Figure 7.11: Class-E power amplifier with series quarter-wave transmission line and shunt filter.**

that of the amplifier with a parallel quarter-wave line, assuming that the parallel $L_0C_0$ filter is ideal, having infinite impedance at the fundamental frequency and zero impedances at the second and higher-order harmonic components. In this case, the short circuit on the load side of the quarter-wave transmission line produces a short circuit at its input for even harmonics and open circuit at its input for odd harmonics with resistive load at the fundamental frequency.

However, unlike the parallel quarter-wave transmission line, a series quarter-wave transmission line can serve as an impedance transformer at the fundamental frequency, as well. In this case, there is no need for an additional output-matching circuit as required for a Class-E power amplifier with a parallel quarter-wave transmission line. The impedance $Z_{\text{in}}$ at the input of the loaded quarter-wave transmission line with the characteristic impedance $Z_0$ and electrical length $\theta_0$ at the fundamental frequency can be written as

$$Z_{\text{in}} = Z_0 \frac{Z_{\text{L}} + jZ_0 \tan\theta_0}{Z_0 + jZ_{\text{L}} \tan\theta_0}\bigg|_{\theta_0=90^\circ} = \frac{Z_0^2}{Z_{\text{L}}}, \tag{7.65}$$

where

$$Z_{\text{L}} = \frac{R_{\text{L}}}{1 + jBR_{\text{L}}}. \tag{7.66}$$

Substituting Eq. (7.66) to Eq. (7.65) yields

$$R + jX = Z_0^2 \frac{1 + jBR_{\text{L}}}{R_{\text{L}}}. \tag{7.67}$$

Then, separating Eq. (7.67) into real and imaginary parts enables the standard load resistance $R_{\text{L}}$ and shunt susceptance $B$ to be expressed through the optimum load resistance $R$ and series reactance $X$ corresponding to the Class E with a parallel quarter-wave line as

$$R_{\text{L}} = \frac{Z_0^2}{R} \tag{7.68}$$

$$B = \frac{X}{Z_0^2}. \tag{7.69}$$

To calculate the optimum parameters of a Class-E load network with series quarter-wave transmission line and shunt filter, it is necessary to use Eqs. (7.37) to (7.41) for a Class-E load network with parallel quarter-wave transmission line defining the optimum shunt capacitance $C$, series inductance $L$, series reactance $X$, and a load resistance $R$ in a common case or Eqs. (7.48) to (7.50) in a particular case when $X = 0$.

## References

[1] N. O. Sokal and A. D. Sokal, ''High-Efficiency Tuned Switching Power Amplifier,'' US Patent 3,919,656, November 1975.

[2] A. Grebennikov, ''Load Network Design Techniques for Class E RF and Microwave Amplifiers,'' *High Frequency Electronics*, vol. 3, pp. 18–32, July 2004.

[3] A. V. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[4] M. K. Kazimierczuk and W. A. Tabisz, ''Class C-E High-Efficiency Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-36, pp. 421–428, March 1989.

[5] A. V. Grebennikov, ''A Simplified CAD Approach to Analyzing Lumped Elements,'' *RF Design*, vol. 23, pp. 22–38, July 2000.

[6] A. V. Grebennikov, ''Create Transmission-Line Matching Circuits for Power Amplifiers,'' *Microwaves & RF*, vol. 39, pp. 113–122, 172, October 2000.

[7] T. B. Mader, E. W. Bryerton, M. Marcovic, M. Forman, and Z. Popovic, ''Switched-Mode High-Efficiency Microwave Power Amplifiers in a Free-Space Power-Combiner Array,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-46, pp. 1391–1398, October 1998.

[8] F. J. Ortega-Gonzalez, J. L. Jimenez-Martin, A. Asensio-Lopez, and G. Torregrosa-Penalva, ''High-Efficiency Load-Pull Harmonic Controlled Class-E Power Amplifier,'' *IEEE Microwave and Guided Wave Lett.*, vol. 8, pp. 348–350, October 1998.

[9] T. B. Mader and Z. B. Popovic, ''The Transmission-Line High-Efficiency Class-E Amplifier,'' *IEEE Microwave and Guided Wave Lett.*, vol. 5, pp. 290–292, September 1995.

[10] A. J. Wilkinson and J. K. A. Everard, ''Transmission-Line Load-Network Topology for Class-E Power Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-49, pp. 1202–1210, June 2001.

CHAPTER 8

# Alternative and Mixed-Mode High-Efficiency Power Amplifiers

In this chapter, the different alternative and mixed-mode configurations of high-efficiency power amplifiers are presented. A Class-DE power amplifier is based on the combination of a voltage-switching Class-D mode with Class-E switching conditions, thus extending the switching Class-D operation to higher frequencies. Effects of the saturation resistance and nonlinear capacitance, driving waveforms, and some practical examples of Class-DE power amplifiers are discussed. The switched-mode Class-E/F power amplifier can provide lower voltage peak factors when zero voltage and zero voltage-derivative conditions corresponding to Class-E mode, required to eliminate discharge loss of the shunt capacitance, are accompanied by harmonic tuning using the resonant circuits tuned to selected harmonic components realizing Class-F mode. Also, the biharmonic Class-$E_M$ mode is described, which can eliminate the efficiency degradation of a Class-E operation mode at higher frequencies due to the increased switching power losses with increasing values of the turn-off switching time. The requirements of both jumpless voltage and current waveforms and sinusoidal load waveform with nonzero output power delivered to the load can be provided by using nonlinear reactive elements in the load network to convert fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source. An inverse Class-E power amplifier represents an inverse version of a classical Class-E power amplifier with a shunt capacitor where the load network inductor and capacitor replace each other. Generally, it is limited to low operating frequencies or low output powers since it is based on zero current and zero current-derivative switching conditions. However, to compensate for the device output capacitor finite discharging process, it is necessary to provide zero voltage-derivative conditions at the same time, and collector efficiency will drop drastically if this capacitance is significant. Finally, harmonic-control techniques for designing microwave power amplifiers are given with a description of a systematic procedure of multiharmonic load-pull simulation using the harmonic-balance method and active load-pull measurement system.

## 8.1 Class-DE Power Amplifier

The complementary voltage-switching Class-D power amplifier with a series filter, which equivalent circuit is shown in Fig. 8.1, has the advantage of a lower transistor peak-voltage factor = Vpeak/Vdc, compared with the current-switching Class D amplifier. That factor is 1 for the voltage-switching Class D and is $\pi = 3.14$ for the current-switching Class D. Those two circuits are exact duals. What is V in one circuit becomes I in the other circuit, and vice versa. Another advantage of the voltage-switching circuit is that the transistors are switched on and off at near-zero current, while the current-switching circuit is switched on and off at full current. That results in less switching power dissipation on the transistors in the voltage-switching circuit. Yet another advantage of the voltage-switching Class D is that it can be operated as a voltage-switching Class DE circuit, in which the charging and discharging of the shunt capacitance at the switching node [$C_{c1}$ and $C_{c2}$ in Fig. 8.1(b)] can be done without the transistors needing to participate in those actions, and without the transistor power dissipation that would occur if the transistors would charge and discharge that capacitance.

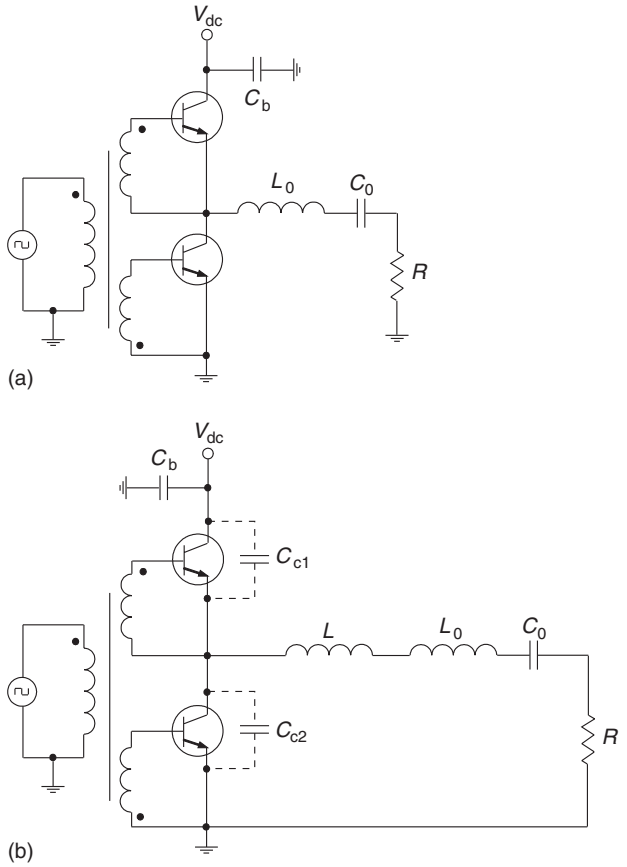



**Figure 8.1: Complementary voltage-switching Class-D power amplifier with series filter.**

However, the frequency limitations of such a voltage-switching Class-D power amplifier are provided by the device parasitic collector shunt capacitances, as shown in Fig. 8.1(*b*), resulting in increased switching transition times due to the capacitor charging and discharging processes, and the fact that the transistor switches charge and discharge the shunt capacitance, dissipating power in the charging and discharging processes.

A possible way to eliminate these power losses and to extend the voltage-switching Class-D mode to higher frequencies is to introduce a dead time during the period when one device has already turned off but the other has not turned on yet, and the inductive load network is used to charge and discharge the shunt capacitances. This can be done by introducing the Class-E switching conditions when the switching loss during off-to-on transition is reduced to zero by the operating requirements of zero voltage at zero voltage slope at the end of the period. Since the shunt capacitor must be discharged at that exact time, an additional series inductor $L$ with optimum value should be included into the load network, as shown in Fig. 8.1(*b*). As a result, the switching current and voltage waveforms have the characteristics of both Class-D and Class-E operation modes. The series $L_0C_0$ filter is still necessary to suppress the harmonic components to allow only the sinusoidal signal to flow into the load $R$.

Such a Class-DE power amplifier was first described by Zhukov and Kozyrev in [1] and has found some particular applications due to its high operation efficiency at higher operating frequencies [2, 3]. The optimum parameters of a voltage-switching Class-DE power amplifier can be determined based on its steady-state collector voltage and current waveforms. Fig. 8.2 shows the three different Class-DE switching circuits that occur during a switching cycle, the load network of which consists of the shunt collector capacitances $C_{c1}$ and $C_{c2}$, a series inductor $L$, a series fundamentally tuned $L_0C_0$ circuit, and a load resistor $R$. Both active devices $Q_1$ and $Q_2$ are considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions. The collector of the top device $Q_1$ is connected to the dc supply voltage, and the emitter of the bottom device $Q_2$ is connected to the ground. To simplify the analysis of a Class-DE power amplifier, the following assumptions are introduced:

- The transistors have zero saturation voltage, zero saturation resistance, infinite off-resistance, and their switching is instantaneous and lossless.
- The shunt capacitances are independent of the collector and are assumed linear.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant $L_0C_0$ circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except into the load $R$.

The Class-E switching conditions for each device can be written as

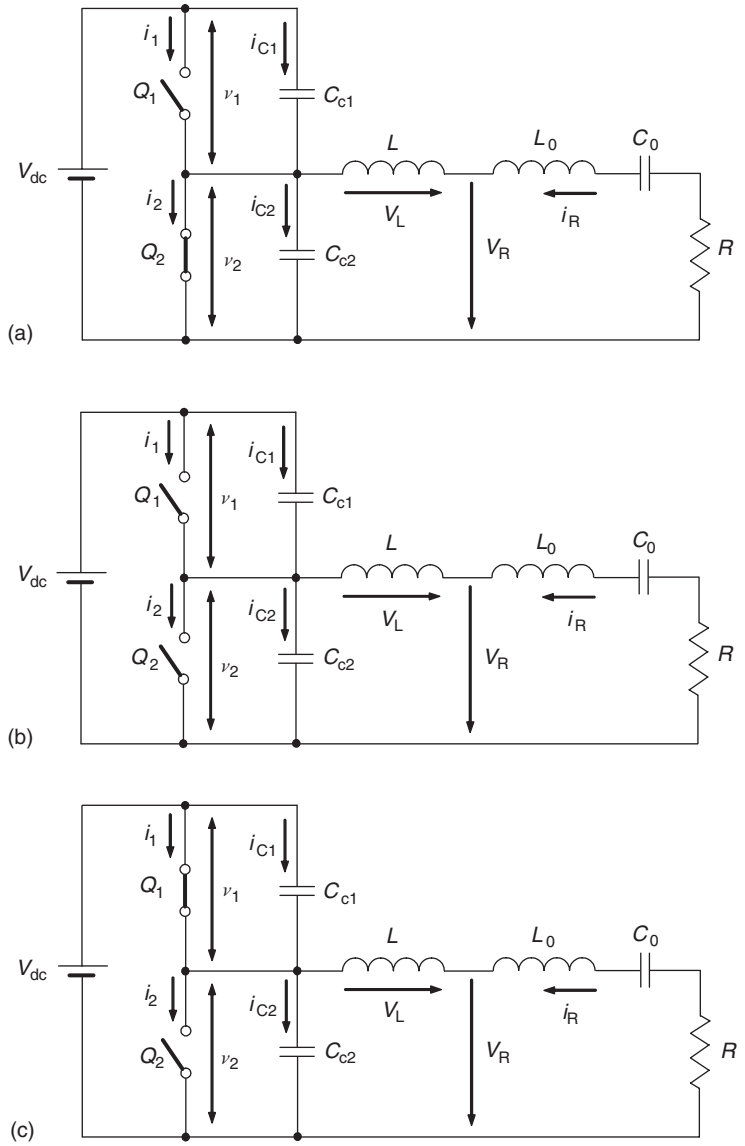



**Figure 8.2: Equivalent circuits of voltage-switching Class-DE power amplifier.**

$$v_1(\omega t)|_{\omega t=\pi} = 0 \quad \left.\frac{dv_1(\omega t)}{d\omega t}\right|_{\omega t = \pi} = 0 \tag{8.1}$$

$$v_2(\omega t)|_{\omega t=2\pi} = 0 \quad \left.\frac{dv_2(\omega t)}{d\omega t}\right|_{\omega t = 2\pi} = 0, \tag{8.2}$$

where $v_1$ and $v_2$ are the voltages across the two switches $Q_1$ and $Q_2$, respectively.

The detailed theoretical analysis of a Class-DE power amplifier in a general form is given in [1], where the output current is assumed sinusoidal,

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi), \tag{8.3}$$

where $I_{\mathrm{R}}$ is the current amplitude and $\varphi$ is the initial phase shift.

The analysis is performed in the interval $0 \leq \omega t \leq 2\pi$ with dead time $\tau_{\mathrm{d}}$ during which both of the switches $Q_1$ and $Q_2$ are turned off. The basic Kirchhoff equations characterizing the electrical behavior of the equivalent circuits of a voltage-switching Class-DE power amplifier are

$$i_2(\omega t) + i_{\mathrm{C2}}(\omega t) = i_1(\omega t) + i_{\mathrm{C1}}(\omega t) + i_{\mathrm{R}}(\omega t) \tag{8.4}$$

$$v_1(\omega t) = V_{\mathrm{dc}} - v_2(\omega t) \tag{8.5}$$

$$i_{\mathrm{C1}}(\omega t) = \omega C_{\mathrm{c1}} \frac{dv_1(\omega t)}{d(\omega t)} \tag{8.6}$$

$$i_{\mathrm{C2}}(\omega t) = \omega C_{\mathrm{c2}} \frac{dv_2(\omega t)}{d(\omega t)}. \tag{8.7}$$

During the interval of $0 \leq \omega t \leq \pi - \tau_{\mathrm{d}}$ before the switching instant, the switch $Q_1$ is turned off and switch $Q_2$ is turned on, conducting the load current, as shown in Fig. 8.2(*a*), resulting in the current and voltage conditions of

$$i_1(\omega t) = 0 \tag{8.8}$$

$$i_2(\omega t) = i_{\mathrm{R}}(\omega t) \tag{8.9}$$

$$i_{\mathrm{C1}}(\omega t) = i_{\mathrm{C2}}(\omega t) = 0 \tag{8.10}$$

$$v_1(\omega t) = V_{\mathrm{dc}} \tag{8.11}$$

$$v_2(\omega t) = 0, \tag{8.12}$$

where $V_{\mathrm{dc}} = 2V_{\mathrm{cc}}$ is the dc supply voltage.

During the interval of $\pi - \tau_{\mathrm{d}} \leq \omega t \leq \pi$ or dead time, the switch $Q_1$ is still turned off while the switch $Q_2$ is then turned off, as shown in Fig. 8.2(*b*), and currents continue to flow through the device shunt capacitances. The current discharges the capacitor of one device, while it charges the capacitor of the other device. If it is assumed that these capacitors are identical, then the

load current is equally divided between them. Using Eqs. (8.5) to (8.7) and an initial condition of $v_2(\pi - \tau_d) = 0$ yields

$$i_1(\omega t) = i_2(\omega t) = 0 \tag{8.13}$$

$$i_{C2}(\omega t) - i_{C1}(\omega t) = i_R(\omega t) \tag{8.14}$$

$$\begin{aligned} v_2(\omega t) &= \frac{1}{\omega C} \int_{\pi-\tau_d}^{\omega t} i_{C2}(\omega t) d(\omega t) + v_2(\pi - \tau_d) \\ &= -\frac{I_R}{\omega C}[\cos(\tau_d + \varphi) + \cos(\omega t + \varphi)], \end{aligned} \tag{8.15}$$

where $C = C_{c1} + C_{c2}$.

Eq. (8.14) can also be written in a differential form using Eqs. (8.3), (8.6), and (8.7) as

$$\frac{dv_2(\omega t)}{d(\omega t)} = \frac{I_R}{\omega C} \sin(\omega t + \varphi). \tag{8.16}$$

Applying the switching conditions given in Eq. (8.2) to Eq. (8.16) results in

$$\sin(2\pi + \varphi) = 0, \tag{8.17}$$

from which it follows that the initial phase $\varphi$ can be set to zero.

During the interval of $\pi \leq \omega t \leq 2\pi - \tau_d$ before the switching instant, the switch $Q_1$ is then turned on and switch $Q_2$ is still turned off, as shown in Fig. 8.2($c$), resulting in

$$i_1(\omega t) = -i_R(\omega t) \tag{8.18}$$

$$i_2(\omega t) = 0 \tag{8.19}$$

$$i_{C1}(\omega t) = i_{C2}(\omega t) = 0 \tag{8.20}$$

$$v_1(\omega t) = 0 \tag{8.21}$$

$$v_2(\omega t) = V_{dc}. \tag{8.22}$$

During the interval of $2\pi - \tau_d \leq \omega t \leq 2\pi$ or dead time, switches $Q_1$ and $Q_2$ are turned off, as shown in Fig. 8.2($b$), and currents flow through the device shunt capacitances, charging the upper one and discharging the lower one. Using Eqs. (8.5) to (8.7) and an initial condition of $v_2(2\pi - \tau_d) = V_{ds}$ yields

$$i_1(\omega t) = i_2(\omega t) = 0 \tag{8.23}$$

$$i_{C2}(\omega t) - i_{C1}(\omega t) = i_R(\omega t) \tag{8.24}$$

$$\begin{aligned} v_2(\omega t) &= \frac{1}{\omega C} \int_{2\pi-\tau_d}^{\omega t} i_{C2}(\omega t) d(\omega t) + v_2(2\pi - \tau_d) \\ &= \frac{I_R}{\omega C} (\cos \tau_d - \cos \omega t) + V_{dc}. \end{aligned} \tag{8.25}$$

Fig. 8.3 shows the current and voltage waveforms of a voltage-switching Class-DE power amplifier in an optimum operation mode during the whole interval $0 \leq \omega t \leq 2\pi$ corresponding to its equivalent circuits shown in Fig. 8.2.

From the boundary condition $v_2(\pi) = V_{dc}$ or $v_2(2\pi) = 0$ by using the corresponding Eq. (8.15) or Eq. (8.25), we can write

$$\omega C V_{dc} = \frac{1 - \cos \tau_d}{I_R}. \tag{8.26}$$

The fundamental-frequency component of the voltage $v_2(\omega t)$ across the switch $Q_2$ can be represented by the two quadrature components shown in Fig. 8.2, whose amplitudes can be found using Fourier formulas by

$$V_R = -\frac{1}{\pi} \int_{\pi-\tau_d}^{2\pi} v_2(\omega t) \sin \omega t \, d(\omega t) = \frac{1 + \cos \tau_d}{\pi} V_{dc} = I_R R \tag{8.27}$$

$$V_L = -\frac{1}{\pi} \int_{\pi-\tau_d}^{2\pi} v_2(\omega t) \cos \omega t \, d(\omega t) = \frac{\tau_d - \sin \tau_d \cos \tau_d}{\pi} \frac{I_R}{\omega C}. \tag{8.28}$$

As a result, the optimum normalized total shunt capacitance $C$ and series inductance $L$ as the functions of a dead time $\tau_d$ can be calculated using Eq. (8.26) from

$$\omega C R = \frac{\sin^2 \tau_d}{\pi} \tag{8.29}$$

$$\frac{\omega L}{R} = \frac{V_L}{V_R} = \frac{\tau_d - \sin \tau_d \cos \tau_d}{\sin^2 \tau_d}. \tag{8.30}$$

The optimum load resistance $R$ can be obtained using Eq. (8.27) for the supply voltage $V_{dc}$ and fundamental-frequency output power $P_{out}$ delivered to the load as

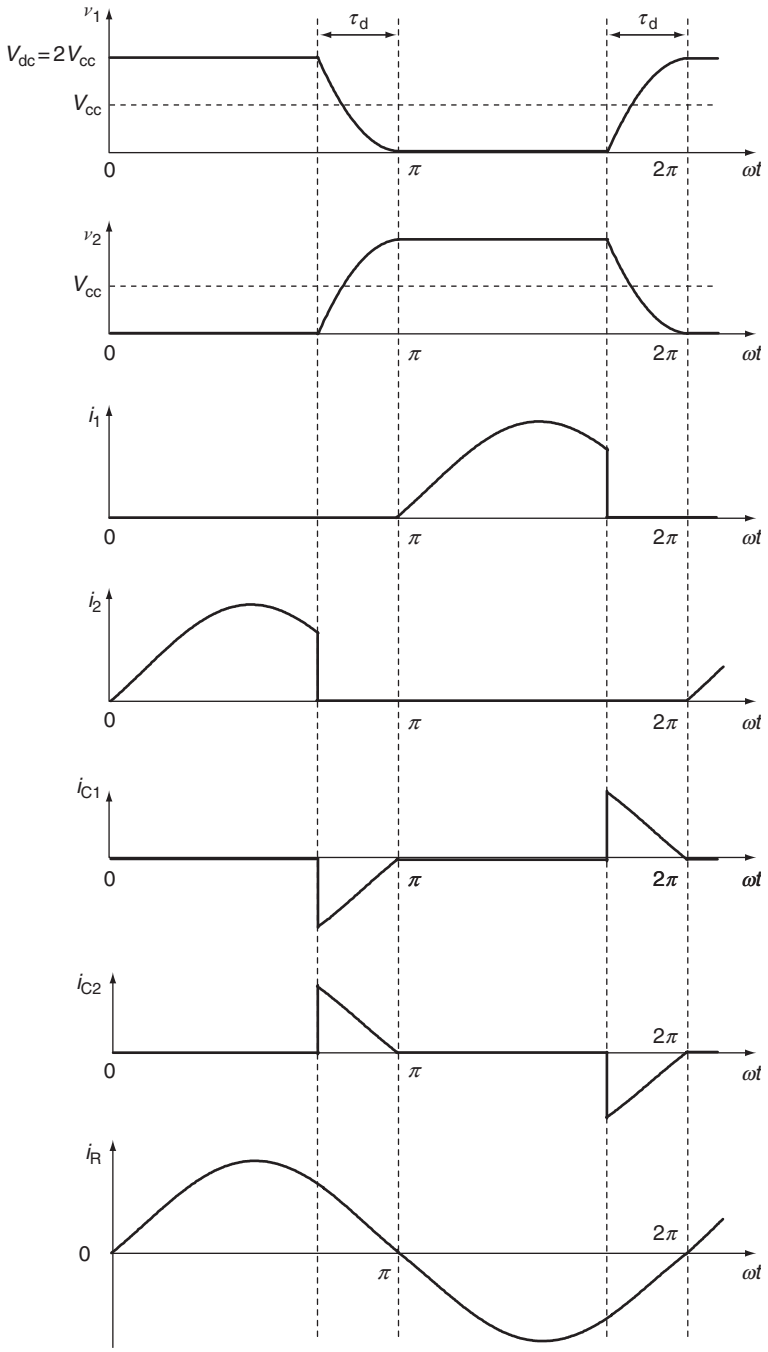



**Figure 8.3: Waveforms for optimum Class-DE operation mode.**

$$R = \frac{1}{2}\frac{V_R^2}{P_{out}} = \frac{(1+\cos\tau_d)^2}{2\pi^2}\frac{V_{dc}^2}{P_{out}}. \tag{8.31}$$

The maximum fundamental-frequency output power $P_{out}$ delivered to the load as functions of the dead time $\tau_d$ and capacitance $C$ can be obtained using Eqs. (8.29) and (8.31) for the supply voltage $V_{dc}$ as

$$P_{out} = \frac{1}{2\pi}\left(\frac{1+\cos\tau_d}{\sin\tau_d}\right)^2 \omega C V_{dc}^2. \tag{8.32}$$

For practical design procedure, it is important to know the dependence of

$$\tau_d = \cos^{-1}\frac{2\pi\frac{P_{out}}{\omega C V_{dc}^2} - 1}{2\pi\frac{P_{out}}{\omega C V_{dc}^2} + 1}. \tag{8.33}$$

It should be mentioned that the parasitic device lead inductors $L_{c1}$ and $L_{c2}$ shown in Fig. 8.4, which are located between the output shunt capacitance of each device ($C_{c1}$ and $C_{c2}$) and load network inductor $L$, do not cause power losses if their quality factors are high enough. However, their presence results in an increased peak collector voltage, which will become more than $V_{dc}$ due to the parasitic oscillations with the oscillation frequency of

$$\omega_1 = \frac{1}{\sqrt{(L_{c1}+L_{c2})\frac{C_{c1}C_{c2}}{C_{c1}+C_{c2}}}} \tag{8.34}$$

when both switches, $Q_1$ and $Q_2$, are turned off, and with the oscillation frequency of

$$\omega_2{}' = \frac{1}{\sqrt{(L_{c1}+L_{c2})C_{c1}}} \tag{8.35}$$

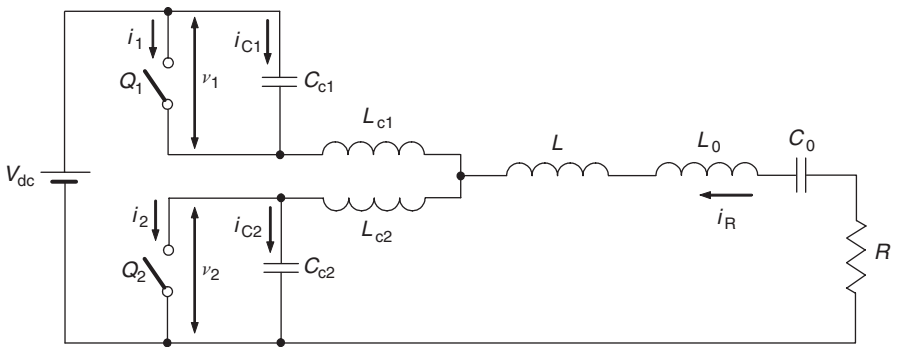



**Figure 8.4: Equivalent circuit of voltage-switching Class-DE power amplifier with parasitic inductors.**

or

$$\omega_2'' = \frac{1}{\sqrt{(L_{c1} + L_{c2})C_{c2}}} \tag{8.36}$$

when either switch $Q_1$ or switch $Q_2$ is turned on.

To minimize such an increase in the collector voltage peak factor to only 10%, their values must be sufficiently small at the switching frequency defined by

$$L_{c1} < \frac{0.01}{\omega^2 C_{c1}} \tag{8.37}$$

$$L_{c2} < \frac{0.01}{\omega^2 C_{c2}}. \tag{8.38}$$

Fig. 8.5(*a*) shows the equivalent circuit of a voltage-switching Class-DE power amplifier using switching devices with nonzero saturation resistances, $r_{sat1}$ and $r_{sat2}$. In this case, during the interval of $0 \le \omega t \le \pi - \tau_d$ when the device $Q_2$ is saturated, the collector voltage $v_2(\omega t)$ shown in Fig. 8.5(*b*) can be defined as $v_{2sat}(\omega t) = r_{sat2} i_2(\omega t) > 0$. The similar changes of the collector voltage shape occur during the interval of $\pi \le \omega t \le 2\pi - \tau_d$ when the device $Q_2$ is pinched off that is a result of a nonzero saturation voltage across the device $Q_1$ equal to $v_{2sat}(\omega t) = r_{sat2} i_2(\omega t) > 0$. Hence, assuming identical devices when $r_{sat} = r_{sat1} = r_{sat2}$, the collector efficiency of the device $Q_2$ as the function of a dead time $\tau_d$ can be written by

$$\eta = 0.5 + 0.5\sqrt{1 - 16\xi^2(\tau_d)\frac{r_{sat} P_{out2}}{V_{dc}^2}}, \tag{8.39}$$

where

$$\xi(\tau_d) = \frac{\pi}{\sqrt{(1 + \cos\tau_d)^2 + \left(\frac{\tau_d - \sin\tau_d \cos\tau_d}{1 - \cos\tau_d}\right)^2}} \tag{8.40}$$

is the ratio between the dc supply voltage $V_{dc}$ and the fundamental-frequency component of the collector voltage $v_2$ when $r_{sat} = 0$, and $P_{out2}$ is the output power from the device $Q_2$ [1].

The maximum operating frequency $f_{max}$ in an optimum mode is limited by the device collector capacitances $C_{c1}$ and $C_{c2}$. To correctly compare the collector efficiencies corresponding to the push-pull Class-DE and single-ended Class-E operation modes, it is better to determine $f_{max}$ for a Class-DE power amplifier through the parameters of a single transistor. Then, by taking into account that $V_{cc} = V_{dc}/2$, $C_{c2} = C/2$ and $P_{out2} = P_{out}/2$, from Eq. (8.32) we can derive that

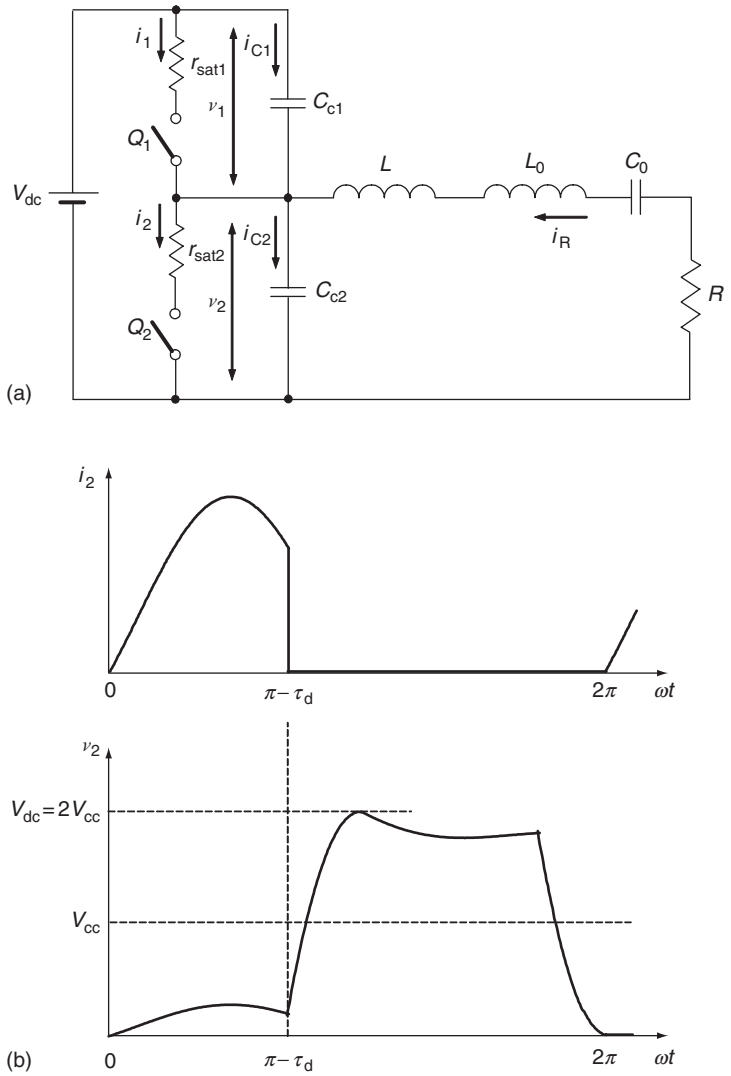



**Figure 8.5: Equivalent circuit of voltage-switching Class-DE power amplifier with saturation resistances.**

$$f_{max} = 0.25\left(\frac{\sin\tau_d}{1+\cos\tau_d}\right)^2 \frac{P_{out2}}{C_{c2}V_{cc}^2}. \tag{8.41}$$

The comparison of both Class-DE and Class-E modes as functions of the saturation time period $\tau_{sat} = \pi - \tau_d$ shows that a complementary voltage-switching Class-DE power amplifier provides a substantially lower maximum operating frequency in an optimum mode. For example, for $\tau_d = 60^\circ$ and $\tau_{sat} = 120^\circ$, the maximum operating frequency of a

Class-E power amplifier is greater by a factor of more than three [1, 4]. However, when using a Class-DE mode, the operating frequency range with collector (or drain) efficiencies of about 90% can be two to three times higher when compared to a Class-D mode [5].

Fig. 8.6 shows the equivalent circuit of a voltage-switching Class-DE power amplifier with nonlinear shunt capacitances, since generally the output device capacitance is nonlinear. For example, the drain-source capacitance of a power MOSFET can be represented as a junction capacitance with linearly graded or abrupt junction, while the collector capacitance of a bipolar transistor is normally modeled as a junction capacitance with abrupt junction having a reverse square-root dependence on the voltage between the collector and the emitter [4, 6]. The large-signal behavior of the drain-source capacitance $C_{ds}$ of a MOSFET device can be approximately described by $C_{ds} \approx C_V\sqrt{V_{dc}/2V_{ds}}$, where $C_V$ is the large-signal capacitance with the drain-source voltage amplitude $V_{ds} = V_{dc}/2$. The results of numerical calculations show that an abrupt junction nonlinearity of the output capacitances does not affect the value of a normalized inductance $\omega L/R$; however, the normalized total shunt capacitance $\omega CR$ is $\sqrt{2}$ times smaller compared to the case with the constant capacitances [5]. It should be mentioned that, for loaded quality factors of the series resonant $L_0C_0$ circuit $Q_L > 3$, the current flowing into the load is nearly sinusoidal. However, if $Q_L < 3$, the design and performance values of a Class-DE power amplifier are strongly affected by $Q_L$ especially for values of $\tau_{sat}$ close to 0.5, resulting in significant harmonic content as well [4].

Practically, it is difficult to drive a Class-DE power amplifier operating at high frequencies using a rectangular driving signal, since the dead time must be controlled with high accuracy (of the order of 1 nsec) that also requires a very wide-band input transformer. In this case, it is better and easier to apply a sinusoidal drive because it reduces the driving power requirements, and control of the dead time can be provided by the drive amplitude. Besides, the transition from a pinch-off mode to a saturation mode for the power switching MOSFETs occurs very fast once the device gate threshold or pinch-off voltage is crossed. Consider the

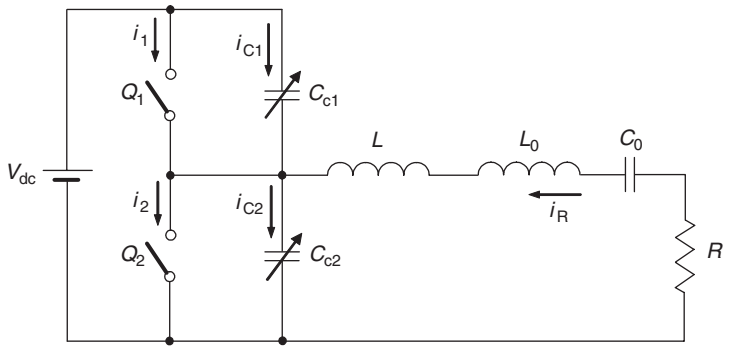



**Figure 8.6: Equivalent circuit of voltage-switching Class-DE power amplifier with nonlinear shunt capacitances.**

out-of-phase sinusoidal signals driving each device, as shown in Fig. 8.7 [2]. When the gate voltage of one device will cross its pinch-off voltage to turn that device off at angular time $\pi - 0.5\tau_d$, the gate voltage across the other device is still below threshold. Thus, during this crossover period from $\pi - 0.5\tau_d$ to $\pi + 0.5\tau_d$ the two devices are turned off simultaneously.

For a sinusoidal gate voltage across the gate-source capacitance,

$$v_g(\omega t) = V_g \sin \omega t, \tag{8.42}$$

where $V_g$ is the voltage amplitude, this voltage is equal to a device pinch-off voltage $V_p$ at angular times $\tau_d$, $\pi - 0.5\tau_d$ and $\pi + 0.5\tau_d$, respectively, that gives

$$V_p = V_g \sin\frac{\tau_d}{2} = V_g \sin\left(\pi - \frac{\tau_d}{2}\right) = -V_g \sin\left(\pi + \frac{\tau_d}{2}\right). \tag{8.43}$$

Eq. (8.43) can be rewritten as

$$V_g = \frac{V_p}{\sin\frac{\tau_d}{2}} \tag{8.44}$$

representing dependence of the required gate-voltage amplitude $V_g$ for a given device dead time $\tau_d$.

On the other hand, it is important first to examine the range of dead times versus gate-voltage amplitude of a sinusoidal drive. By rearranging Eq. (8.44), we can write

$$\tau_d = 2\sin^{-1}\left(\frac{V_p}{V_g}\right). \tag{8.45}$$

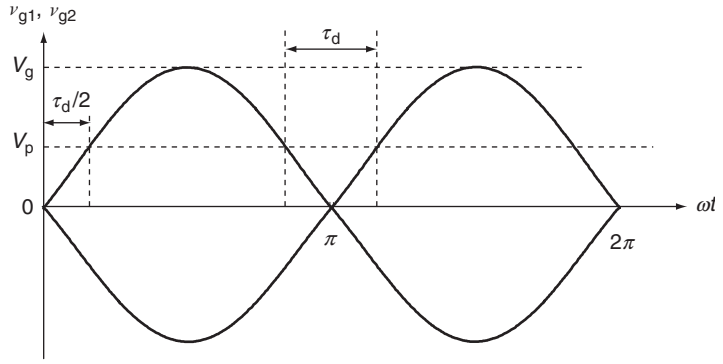



**Figure 8.7: Sinusoidal out-of-phase driving waveforms.**

For example, if the peak gate voltage of the devices is limited to 20 V, then, assuming $V_p = 3.5\,V$, the minimum dead time is approximately 20°. The other limit occurs when the gate voltage becomes too low to turn on the device properly. Usually, this means that the gate-voltage amplitude must not be lower than about 6.5 V in practice. Hence, the maximum dead time that can be achieved is about 65°.

Fig. 8.8 shows an experimental circuit of the Class-DE power amplifier operating at 1 MHz with rectangular drive [3]. To get the output power of 1 W at a supply voltage of 10 V, the two MOSFET devices 2SK982 were used as the switching active devices. Assuming that the device dead time $\tau_d = 90°$ and load network quality factor $Q = 10$, the load resistance $R$ can be found from Eq. (8.31) equal to 5.07 Ω, the shunt capacitances $C_1$ and $C_2 (C_1 = C_2 = C/2)$ can be determined from Eq. (8.29) as equal to 5 nF each, while the series inductance $L_s$ can be calculated from $L_s = QR/\omega$ equal to 8.07 $\mu$H combining the additional compensating inductance $L$ and series filter inductance $L_0$ too. In this case, the inductance $L_0$ can be found using Eq. (8.30) as

$$L_0 = L_s - L = \left(Q - \frac{\pi}{2}\right)\frac{R}{\omega} = 6.8\,\mu\text{H}. \tag{8.46}$$

Then, the series capacitance $C_0$ can be obtained by

$$C_0 = \frac{1}{\omega^2 L_0} = 1/\omega R\left(Q - \frac{\pi}{2}\right) = 3.73\,\text{nF}. \tag{8.47}$$

As a result, the measured drain efficiency was 96.2% with an output power of 0.51 W at an operating frequency of 1.04 MHz. The output power was reduced by increasing the operating frequency to 1.04 MHz. The smoothest switching voltage waveforms were observed in this

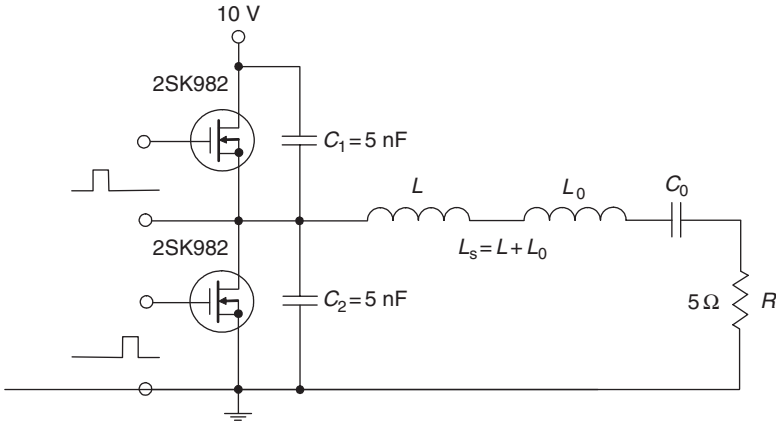



**Figure 8.8: Circuit diagram of experimental Class-DE power amplifier with rectangular drive.**

case. Generally, the output power could be changed from 30–136% by controlling the operating frequency within 10%.

Fig. 8.9 shows an experimental circuit of a high-power Class-DE power amplifier operating at 1 MHz with sinusoidal drive [2]. The two gates of the two switching MOSFET devices IRF540 are driven from the two transformers with series-connected primary windings and secondary windings connected with opposite polarities to give the phase shift of 180° between the gate voltages. The two gates could be driven with a single transformer with one primary winding; however, using the separate primary windings has an advantage to eliminate a positive feedback mechanism due to the device feedback gate-source capacitances. The output power $P_{\text{out}} = 300\,\text{W}$ was achieved at the operating frequency of 13.56 MHz and supply voltage $V_{\text{dc}} = 72.5\,\text{V}$. The dc supply is bypassed by several 0.1 $\mu$F ceramic capacitances, which have a self-resonance at close to 13.56 MHz. Assuming the load current amplitude $I_{\text{R}} = 15.3\,\text{A}$, the load resistance can be obtained by

$$R = \frac{2P_{\text{out}}}{I_{\text{R}}^2} = 2.56\,\Omega. \tag{8.48}$$

For a load network quality factor $Q = 10$, the series inductance $L_{\text{s}}$ can be calculated from

$$L_{\text{s}} = \frac{QR}{\omega} = 0.3\,\mu\text{H}. \tag{8.49}$$

The dead time $\tau_{\text{d}}$ can be found from Eq. (8.27) equal to approximately 45°. By using Eq. (8.30), the series inductance $L$ required to compensate for the device output capacitance of 500 pF (at $V_{\text{ds}} = 25\,\text{V}$) is equal to 17.2 nH. Then, the series capacitance $C_0$ can be obtained by

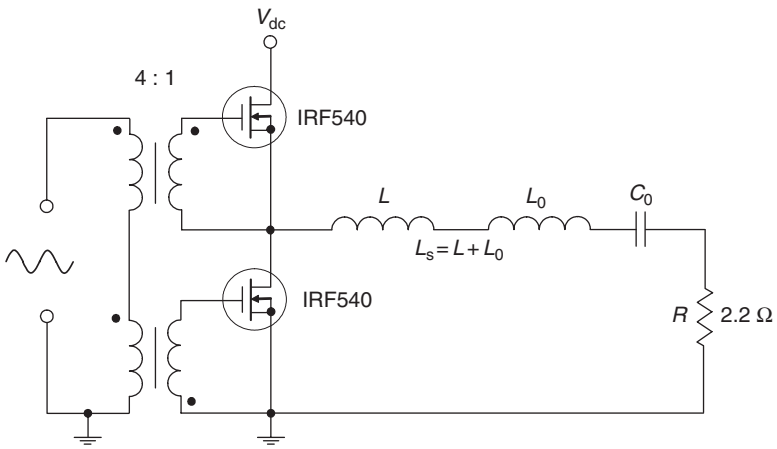



**Figure 8.9: Circuit diagram of experimental Class-DE power amplifier with sinusoidal drive.**

$$C_0 = \frac{1}{\omega^2(L_s - L)} = 487\,\text{pF}. \tag{8.50}$$

As a result, the measured output power of 298.2 W with a drain efficiency of 94.2% was achieved at a supply voltage of 73.1 V. The total power dissipated in the gate circuit was only 9.6 W with a gate-voltage amplitude of 7 V.

By using two IRFP450 MOSFETs fed by supply voltages of +150 V and −150 V (300 V with the center-point at ground, allowing a direct connection from the switching node to a grounded load), an output power of 1 kW can be achieved in a frequency range of 50 kHz to 5 MHz with efficiency of more than 91% [7].

## 8.2 Class-E/F Power Amplifiers

When comparing Class E to its two counterparts, conventional Class F and inverse Class F, both advantages and disadvantages can be found with respect to each class. For example, using a switched-mode Class E can result in high efficiency with a simple load network, whereas an efficiency improvement by using Class F is achieved at the expense of circuit complexity. Even with tuning up to the seventh-harmonic component, the collector (or drain) voltage and current waveforms exhibit significant overlapping, and the maximum theoretical collector efficiency cannot exceed 90%. The switching speed of the Class-E power amplifier is limited only by the active device, provided the optimum parameters of the load network are properly set. Then the switching speed of the Class F is defined by both the active device and a limited number of the controlled harmonic components composing the collector voltage and current waveforms. In addition, Class E can incorporate the device output capacitance into the load-network topology, but a large capacitance becomes a limiting factor at high frequencies. In the presence of large output capacitance, it is possible to realize a simple Class-F topology with control of only a few harmonics. However, the collector-voltage peak factor in Class-F mode cannot exceed a maximum value of 2, while the maximum collector-voltage peak factor in Class-E mode can be greater than 3.5.

Fig. 8.10 shows a generalized switched-mode Class-E/F power amplifier where zero voltage and zero voltage-derivative conditions corresponding to Class-E mode can be used to eliminate discharge loss of the shunt capacitance, and harmonic tuning can be provided by using resonant circuits tuned to selected harmonic components realizing Class-F mode with improved collector waveforms [8]. Each resonant circuit or filter presents a desired impedance at the corresponding harmonic component that it tunes, while leaving other harmonics unaffected. Consequently, the load network describes a family of switching power amplifiers for which the impedance seen by the switch is capacitive at all harmonics, except for a selected number of tuned harmonics.

To achieve Class-E optimum conditions, the choice of an inverse Class F is natural to provide mixed Class-E/F mode since it provides a zero-voltage condition for a half-sinusoidal collector

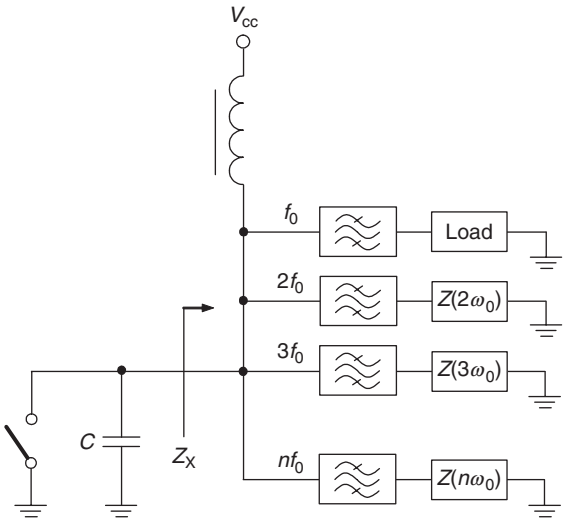
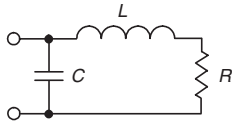
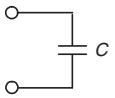
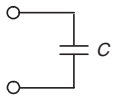
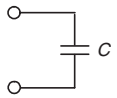
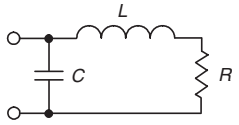
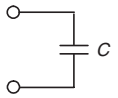
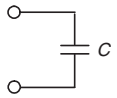
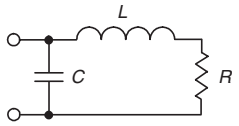
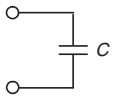
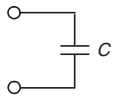
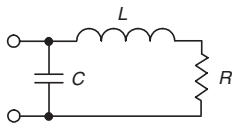
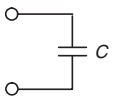
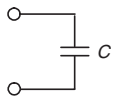



**Figure 8.10: Generalized harmonic-tuned Class-E/F power amplifier.**

voltage waveform, unlike the conventional Class F, which presents voltage discontinuity at the switching instant in the ideal case of infinite-harmonics tuning. The Class-E/F name indicates that this mixed mode is based on Class E and inverse Class F (or Class 1/F) rather than the conventional Class F. Generally, some selection of even harmonics may be open-circuited, some selection of odd harmonics may be short-circuited, and the remaining harmonics are presented with a fixed capacitance. According to a Class-E mode, the load resistance $R$, shunt capacitance $C$, and series inductance $L$ shown in Table 8.1 are adjusted at the fundamental frequency to achieve the required inductive impedance to obtain the overall zero voltage and zero voltage-derivative conditions in an ideal case with different tuning at the harmonics. To differentiate these harmonic tunings among each other, different names can be used of the form Class $E/F_{n1, n2, n3, \ldots}$, where the numerical subscripts indicate the harmonic orders of the tuned harmonics in an inverse Class-F mode. Table 8.1 shows the load-network harmonic-impedance specifications of several Class-E/F power amplifiers. Even-harmonic tuning tends to primarily affect the current waveform, whereas odd-harmonic tuning tends to have the most effect on the voltage waveform. As a result, tuning of several harmonics can minimize the peak voltage amplitude with a current waveform approximating a square wave. The minimum peak factor of 3.08 is realized for Class $E/F_{2, 3, 4}$, which is lower than in an inverse Class F of 3.12 and much lower than in a Class E with shunt capacitance of 3.56.

In practice, it is difficult to eliminate the effects of the resonant circuits tuned to different harmonics, on each other or on the fundamental-frequency impedance. For example, if a series resonator is tuned to create a short circuit for the third-harmonic component in a Class-E/$F_3$ mode, it will present a capacitance at the second harmonic, reducing the second-harmonic impedance and

**Table 8.1: Optimum Class-E/F Impedances at Fundamental and Harmonics**

| Class E/F type | $f_0$ (fundamental) | $2f_0$ | $3f_0$ | $4f_0$ | $nf_0, n = 5, 6, \ldots$ |
|---|---|---|---|---|---|
| Class $E/F_3$ |  |  | short |  |  |
| Class $E/F_{2,3}$ |  | open | short |  |  |
| Class $E/F_{2,4}$ |  | open |  | open |  |
| Class $E/F_{3,4}$ |  |  | short | open |  |

degrading the voltage waveform. In this case, either a very high loaded quality factor of this resonator is required, or additional resonances must be introduced into the circuit. The easiest and most convenient way to separate the effects of even and odd harmonics is to use a symmetrical push-pull switching power amplifier configuration. By using the effects of a virtual ground for odd harmonics and a virtual open for even harmonics, a push-pull Class-$E/F_3$ power amplifier can be constructed by placing the third-harmonic short circuit as a differential load. In this case, the shorting of the third harmonic can be provided by a low-$Q_L$ resonator without reducing the impedances at any even harmonics. A similar strategy can be used to selectively tune the impedances at even harmonics. Fig. 8.11(*a*) shows the Class-$E/F_{odd}$ circuit implementation with short-circuiting of all odd harmonics by placing a differential short circuit between the two switches [8]. To avoid short-circuiting of a fundamental-frequency component, a bandstop filter such as a parallel LC-tank can be used to provide a differential short circuit at all odd harmonics other than the fundamental.

The bandstop filter between two switches forces the differential voltage $v_2 - v_1$ to be sinusoidal,

$$v_2(\omega t) - v_1(\omega t) = V \sin(\omega t + \varphi), \tag{8.51}$$

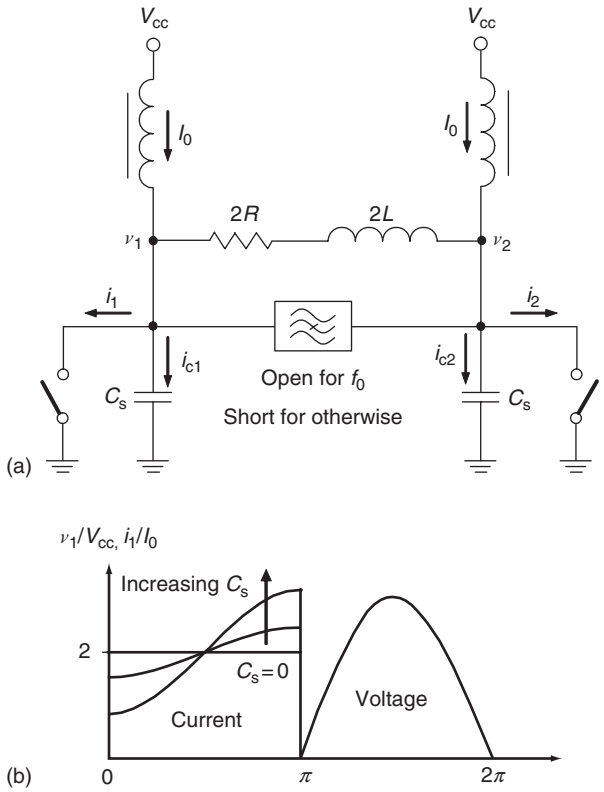



**Figure 8.11: Class-E/F$_{odd}$ circuit implementation and collector waveforms.**

where $V$ is the differential voltage amplitude and $\varphi$ is the arbitrary initial phase shift.

Since one of the switches is always turned on during half a period and has zero voltage across it for an idealized case, the voltages $v_1$ and $v_2$ can be written respectively as

$$v_1(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ -V\sin(\omega t + \varphi) & \pi \le \omega t \le 2\pi \end{cases} \tag{8.52}$$

and

$$v_2(\omega t) = \begin{cases} V\sin(\omega t + \varphi) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi, \end{cases} \tag{8.53}$$

where $V$ is the drain voltage amplitude and $V_{cc}$ is the supply voltage.

According to Class-E zero voltage switching conditions, both voltages must be equal to zero at turn-on, resulting in the only trivial solution for $\varphi$ to be zero. This means that the properly

tuned switch voltages $v_1$ and $v_2$ are purely half-sinusoidal. Since each switch is connected to the supply voltage through the RF choke, the dc voltage of each switch voltage waveform is the supply voltage $V_{cc}$. Then, the peak voltage for a half-sine waveform can be written as $V = \pi V_{cc}$.

Then, the currents $i_{c1}$ and $i_{c2}$ flowing through linear shunt capacitors can be found respectively from

$$i_{c1}(\omega t) = C_s \frac{dv_1(\omega t)}{d(\omega t)} = \begin{cases} 0 & 0 \le \omega t \le \pi \\ -\pi V_{cc} C_s \cos \omega t & \pi \le \omega t \le 2\pi \end{cases} \tag{8.54}$$

and

$$i_{c2}(\omega t) = C_s \frac{dv_2(\omega t)}{d(\omega t)} = \begin{cases} \pi V_{cc} C_s \cos \omega t & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi. \end{cases} \tag{8.55}$$

During each one-half period, one of the transistors is open-circuited, while the other transistor is short-circuited. Hence, the switch currents $i_1$ and $i_2$ can be written respectively as

$$i_1(\omega t) = \begin{cases} 2I_0 - i_{c2}(\omega t) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{8.56}$$

and

$$i_2(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ 2I_0 - i_{c1}(\omega t) & \pi \le \omega t \le 2\pi. \end{cases} \tag{8.57}$$

The switch voltage and current waveforms for various values of the shunt capacitance $C_s$ corresponding to a Class-E/$F_{odd}$ mode are shown in Fig. 8.11(*b*). If the shunt capacitance is zero, the switch current $i_1$ (or $i_2$) represents a rectangular waveform corresponding to a well-known current-switching Class-D mode. However, according to Eqs. (8.49) and (8.50), the increasing shunt capacitance $C_s$ results in higher current peak values, also changing the shape of a current waveform.

The Class-E/$F_{odd}$ topology shown in Fig. 8.11(*a*) can be transformed to a similar circuit schematic with only one RF choke connected between the dc power supply and the center tap of the tank inductor $L_1$, where $C_b$ is the bypass capacitor, and the resonator composed of the tank inductor $L_1$ and capacitor $C$ is detuned to have the required inductance at the fundamental frequency to achieve Class-E switching conditions [9]. In some special cases, the RF choke can be replaced by an inductor $L_2$, as shown in Fig. 8.12(*a*), which can be tuned to resonate with the shunt capacitors at the second harmonic, providing an open-circuit to each switch at that frequency, similar to a single-ended even-harmonic Class-E mode [10].

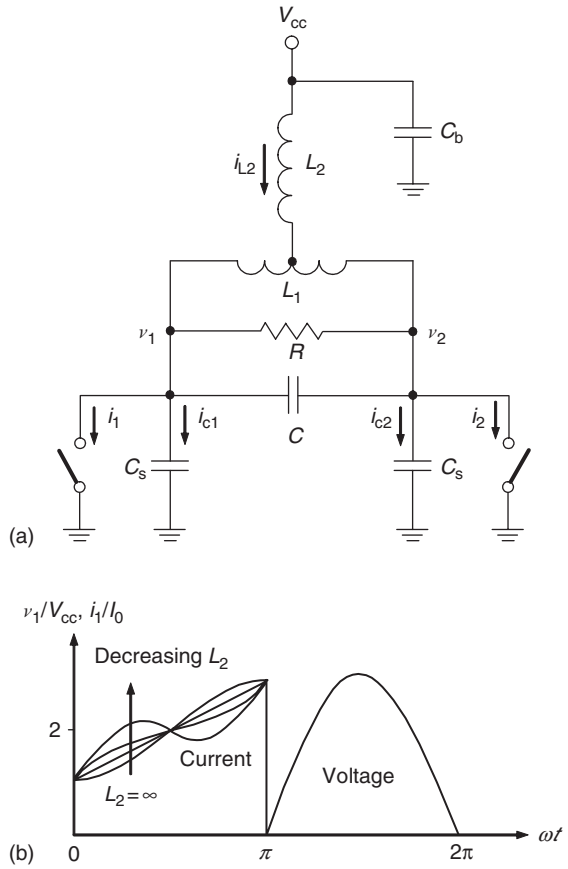



**Figure 8.12: Class-E/$F_{2,odd}$ power amplifier and collector waveforms.**

The voltage $v_{L2}$ across the inductor $L_2$ can be written as

$$v_{L2}(\omega t) = \frac{v_1(\omega t) + v_2(\omega t)}{2} = \begin{cases} \frac{\pi}{2} V_{cc} \sin \omega t & 0 \le \omega t \le \pi \\ -\frac{\pi}{2} V_{cc} \sin \omega t & \pi \le \omega t \le 2\pi. \end{cases} \tag{8.58}$$

The current $i_{L2}$ flowing through the inductor $L_2$ during each one-half period can be obtained by

$$\begin{aligned} i_{L2}(\omega t) &= \frac{1}{\omega L_2} \int [V_{cc} - v_{L2}(\omega t)] d(\omega t) \\ &= \begin{cases} \frac{\pi}{2} \frac{V_{cc}}{\omega L_2} \left( \frac{2\omega t}{\pi} - 1 + \cos \omega t \right) & 0 \le \omega t \le \pi \\ \frac{\pi}{2} \frac{V_{cc}}{\omega L_2} \left( 2 \frac{\omega t - \pi}{\pi} - 1 - \cos \omega t \right) & \pi \le \omega t \le 2\pi. \end{cases} \end{aligned} \tag{8.59}$$

Then, the switch currents $i_1$ and $i_2$ can be found respectively from

$$i_1(\omega t) = \begin{cases} i_{L2}(\omega t) - i_{c2}(\omega t) & 0 \le \omega t \le \pi \\ 0 & \pi \le \omega t \le 2\pi \end{cases} \tag{8.60}$$

and

$$i_2(\omega t) = \begin{cases} 0 & 0 \le \omega t \le \pi \\ i_{L2}(\omega t) - i_{c1}(\omega t) & \pi \le \omega t \le 2\pi, \end{cases} \tag{8.61}$$

where the capacitor currents $i_{c1}$ and $i_{c2}$ are defined by Eqs. (8.52) and (8.53).

The switch voltage and current waveforms for various values of inductance $L_2$, corresponding to a Class-E/$F_{2,odd}$ mode, are shown in Fig. 8.12(*b*). For each inductance tuning, the voltage waveform remains half-sinusoidal. The current waveforms depend on the even harmonics tuned and the switch shunt capacitance. For high values of $L_2$, corresponding to a basic Class-E/$F_{2,odd}$ mode, the switch current represents a nearly trapezoidal waveform. However, for low values of $L_2$ with open-circuit even-harmonic tuning, the switch current approximates more closely the rectangular waveform with peak value at the turn-off switching instant, even for very large values of the shunt capacitance [8]. Classes E/$F_{odd}$ and E/$F_{2,odd}$ can tolerate twice the shunt capacitance of a Class E for the same operating frequency, supply voltage, and output power, without having negative switch current. As a result, the maximum operating frequency can be doubled compared to a single-ended Class-E mode using the same transistor size.

The tuning of several even harmonics realizing Class-E/$F_x$ operation mode, where x is a set of tuned even harmonics, can be accomplished with the generalized circuit implementation shown in Fig. 8.13, where the additional resonators are connected in parallel to each switch [8]. Each additional resonator

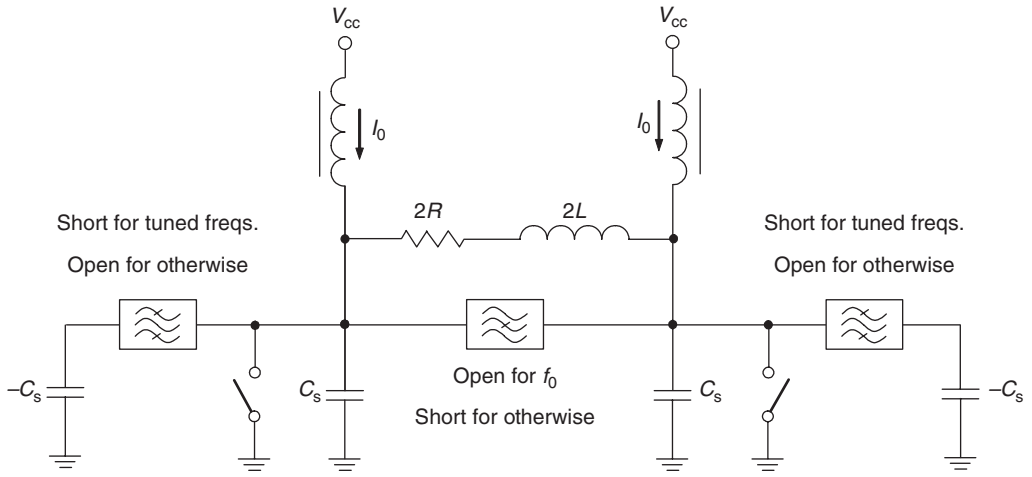



**Figure 8.13: Generalized Class-E/$F_{x,odd}$ circuit implementation.**

can be treated as a bandpass filter placed in-series with negative capacitance $-C_c$. The filter connects this negative capacitance in parallel with the switch a shunt capacitance at the tuned even harmonics, thus canceling the capacitance at those frequencies.

Fig. 8.14 shows the schematic of a high-power Class-E/$F_{2,odd}$ MOSFET power amplifier designed to provide an output power of 1 kW at 7 MHz [9]. The magnetizing inductance of an output air-core transformer was used as the tank inductance of 240 nH. To reduce a ringing transient superimposed on the drain voltage and current waveforms due to parasitic device package inductances resonating with the tank capacitor and the drain-source capacitances, the loaded quality factor of the parallel *LC* resonator was lowered to 3.6. The second-harmonic tuning helps to keep the drain current positive, providing an additional peaking in the early part of the current waveform where the ringing has the highest amplitude. The transistors are mounted directly to an aluminum heatsink through holes cut in the FR4 circuit board. To suppress the third-harmonic component to an acceptable level, a third-harmonic trap was added in series with the load. As a result, the second and third harmonic components in the output spectrum were 33 dB and 35 dB below the fundamental-frequency component respectively, and all other higher-order harmonic components were at least 40 dB below the fundamental. The Class-E/$F_{2,odd}$ power amplifier exhibited an output power over 1.1 kW with a drain efficiency of 85% and a power gain of 17 dB.

Fig. 8.15 shows the high-power dual-band Class-E/$F_{odd}$ MOSFET power amplifier designed to operate in the 7 MHz and 10 MHz frequency bands [11]. The input network consisting of the parallel capacitor $C_{in}$, parallel inductor $L_{in}$, balanced-to-unbalanced impedance transformer

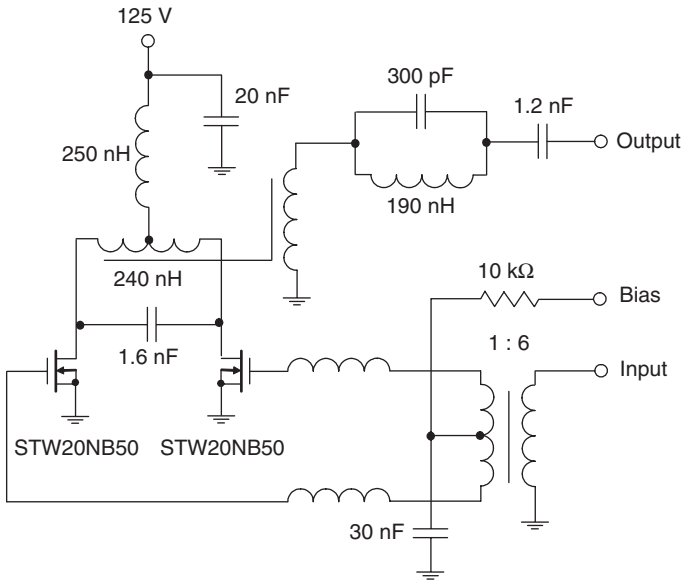



**Figure 8.14: Schematic of Class-E/$F_{2,odd}$ power amplifier with third harmonic trap [9].**

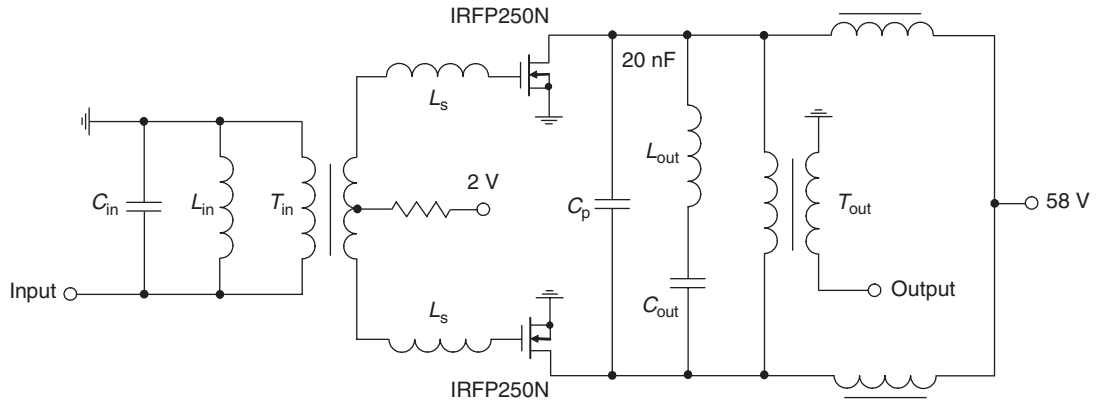



**Figure 8.15: Schematic of dual-band Class-E/$F_{odd}$ power amplifier [11].**

$T_{in}$, and two series inductors $L_s$ converts a source impedance of 50 Ω to balanced impedance conjugately matched to each transistor input. The load network consists of the parallel capacitor $C_p$, series tank with $L_{out}$ and $C_{out}$, output air-core transformer $T_{out}$ representing a 1:1 balun, the magnetizing inductance of which is used in the load-network tuning. Such a load network provides inductive, capacitive, and again inductive admittances, as frequency is increased for Class-E switching conditions at each mid-band frequency. At all odd harmonics of each mid-band frequency, the load network, including the device drain-source capacitances, provides a capacitive susceptance with a low-impedance path to ground, compared to the load resistance. As a result, output power of 250 W with a drain efficiency of 94% and a power gain of 16 dB was achieved at 7.15 MHz, and output power of 225 W with a drain efficiency of 90% and a power gain of 15 dB was measured at 10.1 MHz. The bandwidth in both bands was sufficient to allow high-efficiency operation from 7.0–7.3 MHz and from 10.0–10.18 MHz bands.

## 8.3 Biharmonic Class-$E_M$ Power Amplifier

A basic limitation of a Class-E operation mode at higher frequencies is significant efficiency degradation due to the increased switching power losses with increasing values of the turn-off switching time. To minimize this undesirable effect, it is necessary to find a solution without an instant jump in the ideal collector current waveform at turn-off to allow efficient operation at frequencies high enough that the switch turn-off transition would occupy a substantial fraction of the waveform period, of 30% or more. However, the Class-E power amplifier can deliver nonzero output power only if at least one of the switch waveforms, either voltage or current, has a jump under assumption that the circuit comprises an ideal switch and linear passive components [12]. To satisfy the requirements of both jumpless voltage and current waveforms and sinusoidal load waveform with nonzero output power delivered to the load, it

is necessary to allow power flow in the system at two or more harmonically related frequencies. This can be done by using nonlinear reactive elements in the load network to convert the fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source.

The simplest low-order implementation approach having jumpless switch voltage and current waveforms, called the *biharmonic Class-$E_M$ mode* [13], comprises the two-part output stage including

- Main amplifier that consumes dc power equal to approximately 75% of the load power, and converts this power and the power generated by the auxiliary amplifier to power at the output frequency *f*.
- Smaller auxiliary amplifier (or varactor frequency multiplier), phase-locked to the main amplifier, which generates approximately 25% of the load power at the frequency 2*f*.

The main amplifier has jumpless switch voltage and current waveforms, while the auxiliary amplifier can be a conventional Class-E power amplifier. If the frequency multiplier is fed from the output of the main amplifier, the load power is reduced by the amount of power converted by the frequency multiplier from frequency *f* to frequency 2*f* to change the waveform shapes to continuous ones. The higher-order implementations can use harmonic components of order higher than two, or multiple harmonics. For operation at higher frequencies, the biharmonic Class-$E_M$ power amplifier can be energetically superior to a conventional Class-E power amplifier using the same power device and supplying the same output power at the same operating frequency. That is because it can tolerate slow transistor turn-off with much less efficiency loss. In addition, less input drive is needed for the biharmonic Class-$E_M$ power amplifier because slower switching times are tolerable, taking into account that switching times are inversely proportional to the square root of the input driving power.

Fig. 8.16 shows the circuit schematic of a biharmonic Class-$E_M$ MOSFET power amplifier designed to operate at a 3.5 MHz with second-harmonic power injection from an auxiliary amplifier operating at 7 MHz. The derivation of the ideal drain waveforms of the main amplifier is based on the assumption that the resultant current of the active device operating as a switch, and its shunt capacitor, contains only dc, fundamental, and second-harmonic components, written as

$$i(\omega t) = I_0 + I_{1A}\cos\omega t + I_{1B}\sin\omega t + I_{2A}\cos 2\omega t + I_{2B}\sin 2\omega t, \tag{8.62}$$

where $\omega$ is the angular fundamental frequency, $I_{1A}$ and $I_{1B}$ are the quadrature fundamental current components, and $I_{2A}$ and $I_{2B}$ are the quadrature second-harmonic current components,

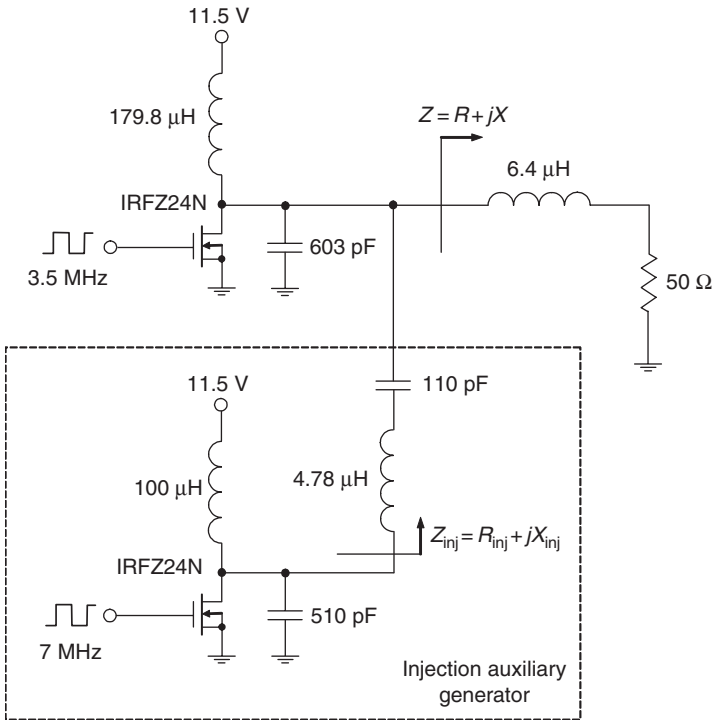



**Figure 8.16: Biharmonic Class-$E_M$ power-amplifier schematic [13].**

respectively. The shunt capacitors at the transistor drains can be composed of the device output capacitances and external capacitors.

For a 50% duty ratio when the switch is off during $0 < \omega t \leq \pi$, the current through the switch $i(\omega t) = 0$, and the current $i_C(\omega t)$ flowing through the shunt capacitor $C$ fully represents the current $i(\omega t)$ given in Eq. (8.60), reproducing the voltage across the switch by the charging of this capacitor according to

$$v(\omega t) = \frac{1}{\omega C} \int_0^{\omega t} i(\omega t) d(\omega t). \tag{8.63}$$

The conditions for a biharmonic Class-$E_M$ optimum operation with jumpless voltage and current waveforms, $v(\omega t)$ and $i(\omega t)$, and unipolar switch current are

$$i(\omega t)\big|_{\omega t = 0} = 0 \tag{8.64}$$

$$i(\omega t)\big|_{\omega t = \pi} = 0 \tag{8.65}$$

$$v(\omega t)|_{\omega t=\pi} = 0 \tag{8.66}$$

$$\left.\frac{v(\omega t)}{d(\omega t)}\right|\omega t = 0 = 0. \tag{8.67}$$

Substituting Eq. (8.59) into Eq. (8.60) and applying the boundary conditions given by Eqs. (8.61) to (8.64) yields

$$I_{1A} = 0 \tag{8.68}$$

$$I_{1B} = -\frac{\pi}{2} I_0 \tag{8.69}$$

$$I_{2A} = -I_0 \tag{8.70}$$

$$I_{2B} = \frac{\pi}{4} I_0. \tag{8.71}$$

As a result, the normalized steady-state ideal switch voltage waveform for a period of $0 \leq \omega t < \pi$ and current waveform for a period of $\pi \leq \omega t < 2\pi$ are

$$\frac{i(\omega t)}{I_0} = 1 - \frac{\pi}{2}\sin\omega t + \frac{\pi}{4}\sin 2\omega t - \cos 2\omega t \tag{8.72}$$

$$\frac{v(\omega t)}{V_{dd}} = \frac{2}{\pi}(8\omega t + 4\pi\cos\omega t - \pi\cos 2\omega t - 4\sin 2\omega t - 3\pi), \tag{8.73}$$

where $V_{dd}$ is the dc supply voltage.

Fig. 8.17(*b*) shows the normalized switch voltage and current waveforms for an idealized optimum biharmonic Class $E_M$ with second-harmonic power injection. From switch voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch, and the current $i(\omega t)$ consisting of the dc, fundamental, and injected second harmonic components flows through the device. However, when the transistor is turned off, this current flows through the shunt capacitance $C$. There is no jump in the switch current waveform at the instant of switching off compared to the switch current corresponding to a Class E with shunt capacitance, the voltage and current waveforms of which are shown in Fig. 8.17(*a*). However, the voltage peak factor is higher in a biharmonic Class-$E_M$ mode exceeding a value of 4. It should be mentioned that injecting a higher-order harmonic component will generally increase the voltage peak factor even more. Also, there is no solution for a biharmonic Class-$E_M$ mode with third-harmonic injection and duty cycle of 50%. The voltage peak factor can exceed a value of 7 for a third-harmonic injection with a duty

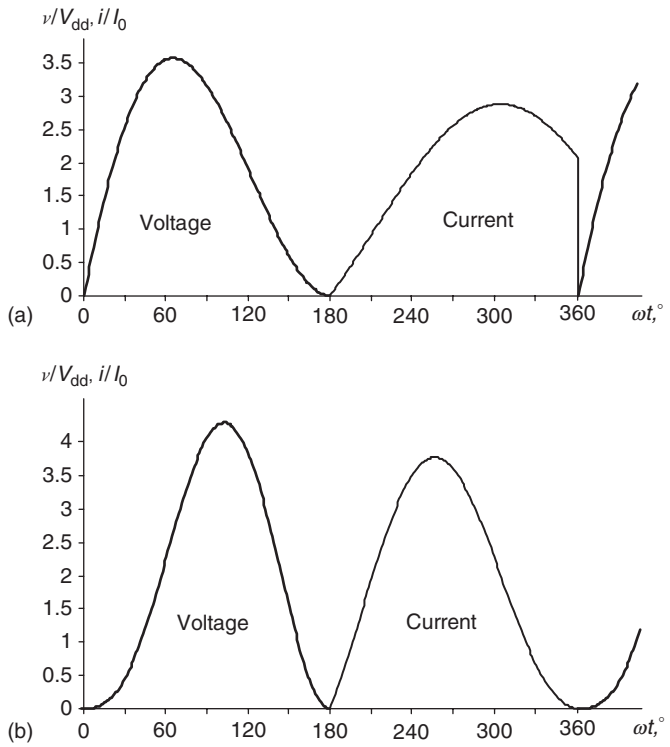



**Figure 8.17: Normalized ideal switch waveforms of (*a*) Class E with shunt capacitance and (*b*) biharmonic Class $E_M$ with second harmonic power injection.**

cycle of 33%. The voltage and current waveforms of the auxiliary amplifier are the usual waveforms corresponding to a switched-mode Class E with shunt capacitance.

In a biharmonic Class-$E_M$ mode, it is assumed that the dc power $P_0 = I_0 V_{dd}$ is equal to approximately 75% of the output load power $P_{out}$ delivered to the load that results in

$$I_0 V_{cc} = \frac{3}{4} \frac{P_{out}}{V_{dd}}. \tag{8.74}$$

The fundamental-frequency load network impedance of the main amplifier and the second-harmonic injection-port impedance of the auxiliary amplifier can be determined by a Fourier-series analysis of the voltage and current waveforms. As a result, the optimum shunt capacitance and load network impedance $Z = R + jX$ for the main amplifier as a function of the dc supply voltage $V_{dd}$ and the output power $P_{out}$ are written as

$$C = \frac{3\pi}{64} \frac{P_{out}}{\omega V_{dd}^2} \tag{8.75}$$

$$R = \frac{128}{9\pi^2}\frac{V_{dd}^2}{P_{out}}, \tag{8.76}$$

$$X = \frac{32(3\pi^2 - 32)}{9\pi^3}\frac{V_{dd}^2}{P_{out}} \tag{8.77}$$

while the optimum injection-port impedance $Z_{inj} = R_{inj} + jX_{inj}$ for an auxiliary amplifier can be calculated from

$$R_{inj} = \frac{128}{9(\pi^2 + 16)}\frac{V_{dd}^2}{P_{out}} \tag{8.78}$$

$$X_{inj} = -\frac{16(3\pi^2 + 16)}{9\pi(\pi^2 + 16)}\frac{V_{dd}^2}{P_{out}}. \tag{8.79}$$

The measured output power of a second-harmonic Class-$E_M$ power amplifier was 13.2 W with overall power-added efficiency of 85.2% at an operating frequency of 3.5 MHz. The injected power at $2f$ necessary to achieve jumpless drain waveforms was measured as 29.8% of the total dc power of the main amplifier instead of the theoretical value of 25% due to the resistive power losses in reactive components, finite loaded quality factors of the series filters, and harmonic power conversions in the nonlinear device capacitances.

Fig. 8.18 shows the comparison between power-added efficiencies of the second-harmonic Class-$E_M$ and classical Class-E power amplifiers as functions of the normalized transistor switching time $\tau_s$. It is assumed that the switching time is inversely proportional to the input-drive power. The plots were simulated for power amplifiers delivering 3.2 W output power at operating frequency 870 MHz using a pHEMT device with a gate periphery of $0.5\,\mu\text{m} \times 50\,\text{mm}$ in the main amplifier. The peak value of power-added efficiency for the

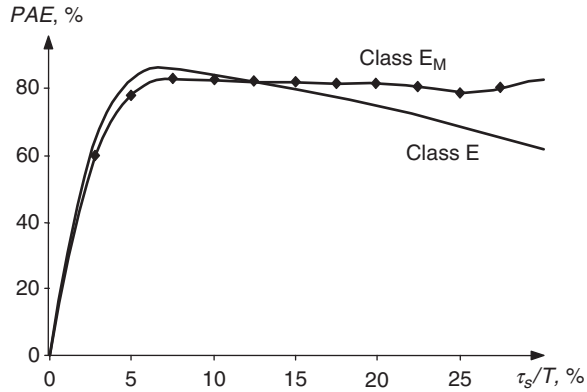



**Figure 8.18: Efficiency versus switching time for Class-$E_M$ and Class-E power amplifiers.**

biharmonic Class-$E_M$ power amplifier is 3.3% lower than that for the classic Class-E power amplifier. However, the Class-$E_M$ power-added efficiency varies by just ± 2% for all switching times from 6–30% of the period, whereas the Class-E efficiency drops monotonically from its peak to 73.5% of its peak value for switching times of 30% of the period.

## 8.4 Inverse Class-E Power Amplifiers

Another approach to the design of the Class-E power amplifier with efficiency of 100% under idealized operation conditions is to use its configuration with a shunt inductance [14]. Such a Class-E power amplifier represents an inverse version of a classic Class-E power amplifier with a shunt capacitor, where the load-network inductor and capacitor replace each other. In this case, the storage element is a shunt inductor instead of a shunt capacitor, resulting in the inverse collector voltage and current waveforms. The basic circuit of the Class-E power amplifier with a shunt inductance as a simplest version of an inverse Class-E mode is shown in Fig. 8.19(*a*) where the load network consists of an inductor $L$ shunting the transistor, a series capacitor $C$, a series fundamentally tuned $L_0C_0$ circuit, and a load resistor $R$. Fig. 8.19(*b*) shows the equivalent circuit of such a switched-mode power amplifier where the active device is considered an ideal switch that is driven in such a way as to provide the device switching between its on-state and off-state operation conditions.

To simplify an analysis of a Class-E power amplifier, the following assumptions are introduced:

- The transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless.
- The loaded quality factor $Q_L = \omega L_0/R = 1/\omega C_0 R$ of the series resonant $L_0C_0$ circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency.
- There are no losses in the circuit except in the load $R$.
- For an optimum operation mode, a 50% duty ratio is used.

In the Class-E mode with a shunt inductance similar to the other Class-E modes, it is possible to eliminate power losses during on-to-off transition by providing the following collector-current conditions:

$$i(\omega t)\big|_{\omega t=2\pi} = 0 \tag{8.80}$$

$$\left.\frac{di(\omega t)}{d(\omega t)}\right|_{\omega t = 2\pi} = 0, \tag{8.81}$$

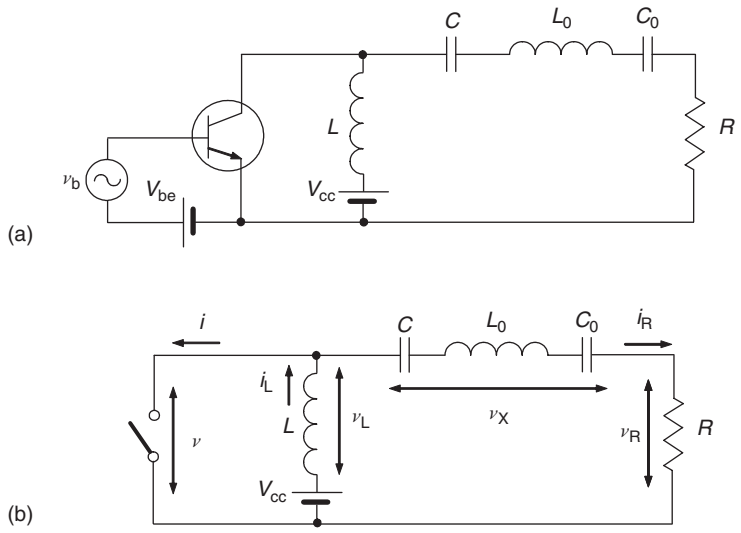



**Figure 8.19: Basic circuits of Class-E power amplifier with shunt inductance.**

when $i(\omega t)$ is the current flowing through the switch. These conditions are important to provide zero on-to-off switching time without any power dissipation and can be performed by proper choice of the load-network parameters.

For the simplified power-amplifier circuit shown in Fig. 8.19(b), the relationships between the voltages and currents can be written as

$$i(\omega t) = i_{\mathrm{L}}(\omega t) - i_{\mathrm{R}}(\omega t) \tag{8.82}$$

$$v(\omega t) = V_{\mathrm{cc}} - v_{\mathrm{L}}(\omega t), \tag{8.83}$$

where the load current is assumed sinusoidal as

$$i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi) \tag{8.84}$$

with the amplitude $I_{\mathrm{R}}$ and initial phase $\varphi$.

When switch is off during $0 \leq \omega t \leq \pi$,

$$i(\omega t) = 0 \tag{8.85}$$

then from Eqs. (8.82) and (8.84) it follows that

$$i_{\mathrm{L}}(\omega t) = i_{\mathrm{R}}(\omega t) = I_{\mathrm{R}} \sin(\omega t + \varphi). \tag{8.86}$$

At the same time, the voltage across the inductance $L$ can be written as

$$v_{\mathrm{L}}(\omega t) = \omega L \frac{di_{\mathrm{L}}(\omega t)}{d(\omega t)} = \omega L I_{\mathrm{R}} \cos(\omega t + \varphi), \tag{8.87}$$

from which it follows that the voltage $v(\omega t)$ according to Eq. (8.83) is

$$v(\omega t) = V_{\mathrm{cc}} - \omega L I_{\mathrm{R}} \cos(\omega t + \varphi). \tag{8.88}$$

When the switch is on during $\pi \leq \omega t \leq 2\pi$,

$$v(\omega t) = 0 \tag{8.89}$$

then, substituting Eq. (8.89) into Eq. (8.83) yields

$$v_{\mathrm{L}}(\omega t) = V_{\mathrm{cc}}. \tag{8.90}$$

By using Eqs. (8.86), (8.87), and (8.90), the current flowing through the inductance $L$ can be obtained as

$$i_{\mathrm{L}}(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}(\omega t - \pi) - I_{\mathrm{R}} \sin \varphi. \tag{8.91}$$

Then, from Eqs. (8.82), (8.84), and (8.91) it follows that

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}(\omega t - \pi) - I_{\mathrm{R}}[\sin(\omega t + \varphi) + \sin \varphi]. \tag{8.92}$$

Applying the zero-current condition given by Eq. (8.80) gives

$$I_{\mathrm{R}}(\omega t) = \frac{\pi V_{\mathrm{cc}}}{2\omega L \sin \varphi}, \tag{8.93}$$

where $0 < \varphi < \pi$ because $I_{\mathrm{R}} > 0$.

Hence, by using Eqs. (8.85), (8.92), and (8.93), the steady-state current waveform in the switch can be obtained by

$$i(\omega t) = \frac{V_{\mathrm{cc}}}{\omega L}\left[\omega t - \frac{3\pi}{2} - \frac{\pi}{2 \sin \varphi} \sin(\omega t + \varphi)\right]. \tag{8.94}$$

Applying the zero current-derivative condition given by Eq. (8.81) to Eq. (8.94) gives

$$\tan \varphi = \frac{\pi}{2}, \tag{8.95}$$

resulting in the phase angle equal to

$$\varphi = \tan^{-1}\left(\frac{\pi}{2}\right) = 57.518^{\circ}. \tag{8.96}$$

From Eq. (8.95) it follows that

$$\sin\varphi = \frac{\pi}{\sqrt{\pi^2+4}} \tag{8.97}$$

$$\cos\varphi = \frac{2}{\sqrt{\pi^2+4}}, \tag{8.98}$$

which allows us to rewrite Eq. (8.94) as

$$i(\omega t) = \frac{V_{cc}}{\omega L}\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right). \tag{8.99}$$

By using a Fourier-series expansion, the dc-supply current is

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)d(\omega t) = \frac{V_{cc}}{\pi\omega L}, \tag{8.100}$$

while the fundamental-current amplitude can be determined using Eqs. (8.93), (8.97), and (8.100) as

$$I_R = \frac{\pi\sqrt{\pi^2+4}}{2} I_0 = 5.8499 I_0. \tag{8.101}$$

As a result, the normalized steady-state collector-current waveform for $\pi \le \omega t \le 2\pi$ and the collector-voltage waveform for $0 \le \omega t \le \pi$ are

$$\frac{i(\omega t)}{I_0} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{8.102}$$

$$\frac{v(\omega t)}{V_{cc}} = \frac{\pi}{2}\sin\omega t - \cos\omega t + 1. \tag{8.103}$$

From the voltage and current waveforms shown in Fig. 8.20 (*a*) and (*b*), it follows that when the switch is turned off, the switch current $i(\omega t)$ is zero, and the inductor current $i_L$ is determined by the sinusoidal load current $i_R$. However, when the switch is turned on, the switch voltage $v(\omega t)$ is zero and dc-supply voltage $V_{cc}$ produces the linearly increasing current $i_L$. The difference between the inductor current $i_L$ and the load current $i_R$ flows through the switch.

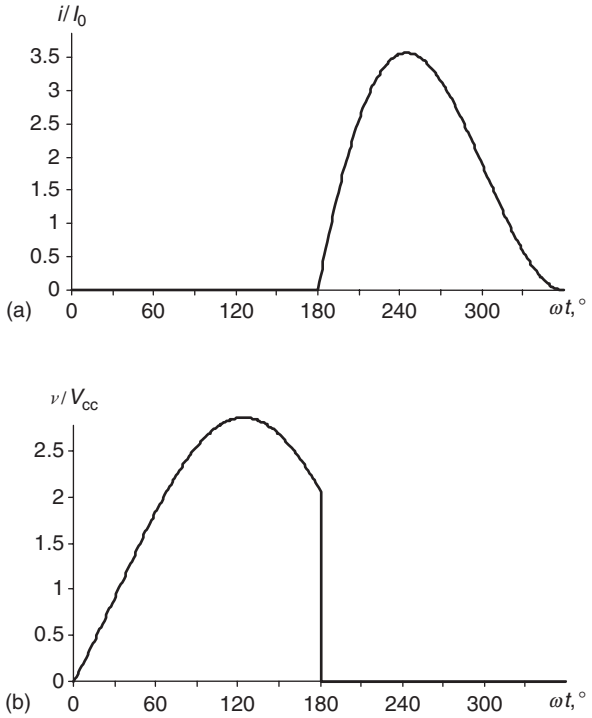



**Figure 8.20: Normalized switch voltage and current waveforms for inverse Class-E mode.**

The peak collector current $I_{\max}$ and peak collector voltage $V_{\max}$ can be determined by differentiating the corresponding waveforms given by Eqs. (8.102) and (8.103) and setting the results equal to zero, thus resulting in

$$I_{\max} = \pi(\pi - 2\varphi)I_0 = 3.562I_0 \tag{8.104}$$

$$V_{\max} = \left(\frac{\sqrt{\pi^2 + 4}}{2} + 1\right)V_{\rm cc} = 2.8621V_{\rm cc}. \tag{8.105}$$

Under the assumption of a sinusoidal load current, the load voltage is sinusoidal also,

$$v_{\rm R}(\omega t) = V_{\rm R}\sin(\omega t + \varphi), \tag{8.106}$$

where $V_{\rm R} = I_{\rm R}R$ is the load-resistor voltage amplitude.

The voltage $v_{\rm X}$ across the elements of the series-resonant circuit is not sinusoidal. Consequently, its fundamental component across the capacitance $C$ is determined due to an assumed high $Q_{\rm L}$ factor by

$$v_C(\omega t) = -V_C \cos(\omega t + \varphi), \tag{8.107}$$

where $V_C = I_R/\omega C$ is the capacitor voltage amplitude.

As a result, the phase shift between the fundamental components of the capacitor and load-resistor voltages can be defined by

$$\tan\psi = -\frac{V_C}{V_R} = -\frac{1}{\omega RC}. \tag{8.108}$$

Using Eq. (8.103) for the idealized collector-voltage waveform and applying a Fourier-series expansion yields

$$V_R = \frac{1}{\pi}\int_0^{2\pi} v(\omega t)\sin(\omega t + \varphi)d(\omega t) = \frac{4V_{cc}}{\pi\sqrt{\pi^2+4}} = 0.3419V_{cc} \tag{8.109}$$

$$V_C = -\frac{1}{\pi}\int_0^{2\pi} v(\omega t)\cos(\omega t + \varphi)d(\omega t) = \frac{(\pi^2+12)V_{cc}}{4\sqrt{\pi^2+4}} = 1.4681V_{cc}. \tag{8.110}$$

Substituting Eqs. (8.100) and (8.101) into Eqs. (8.109) and (8.110) results in

$$V_R = \frac{8}{\pi(\pi^2+4)}\omega L I_R \tag{8.111}$$

$$V_C = \frac{\pi^2+12}{2(\pi^2+4)}\omega L I_R \tag{8.112}$$

Hence, by using Eq. (8.108), the optimum series inductance $L$ and shunt capacitance $C$ can be calculated from

$$\frac{\omega L}{R} = \frac{\pi(\pi^2+4)}{8} = 5.4466 \tag{8.113}$$

$$\omega CR = \frac{16}{\pi(\pi^2+12)} = 0.2329 \tag{8.114}$$

with an optimum phase angle $\psi$ equal to

$$\psi = -\tan^{-1}\left[\frac{\pi(\pi^2+12)}{16}\right] = -76.891^\circ. \tag{8.115}$$

The optimum phase angle $\phi$ of the entire load network with the shunt inductance and the series capacitance is calculated by using Eqs. (8.113) and (8.114) as equal to

$$\phi = -35.945^\circ, \tag{8.116}$$

which indicates that the input impedance of such a load network is capacitive.

The optimum load resistance $R$ can be found using Eq. (8.109) by

$$R = \frac{V_{cc}^2}{P_{out}} \frac{8}{\pi^2(\pi^2+4)} = 0.05844 \frac{V_{cc}^2}{P_{out}}. \tag{8.117}$$

The high-$Q_L$ assumption for the series-resonant $L_0C_0$ circuit can lead to considerable errors if its value is actually small in real circuits [15]. For example, for a 50% duty ratio, the values of the optimum shunt inductance $L$ and the collector-current peak factor and the second-harmonic component increase rapidly for $Q_L$ less than 5.

Fig. 8.21 shows an alternative inverse Class-E load-network configuration with a series inductor $L$, a shunt capacitor $C$, and a parallel-resonant $L_0C_0$ circuit tuned to the fundamental frequency [16]. Here, the RF choke is necessary to supply the dc current $I_0$, and the blocking capacitor $C_b$ is required to decouple the parallel-resonant circuit from the dc path. Such an inverse Class E with a series inductance and a shunt capacitance is dual to a classic Class E with a shunt capacitance and a series inductance. In this case, the series-resonant $L_0C_0$ circuit is replaced by its parallel-equivalent configuration. However, it is characterized by the same switch-voltage and current waveforms, as shown in Fig. 8.20 for an inverse Class-E configuration with a shunt inductance and a series capacitance.

The optimum series inductance $L$, shunt capacitance $C$, and load resistance $R$ of the inverse Class-E load network with a series inductance and a shunt capacitance can be calculated from

$$\frac{\omega L}{R} = \frac{8}{\pi(\pi^2+4)} = 1.1525 \tag{8.118}$$

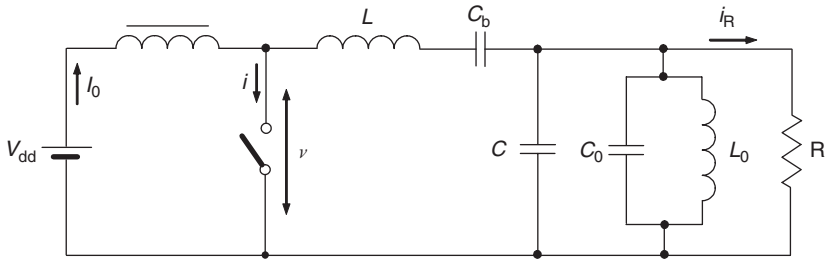



**Figure 8.21: Equivalent circuit of inverse Class-E power amplifier with series inductance.**

$$\omega CR = \frac{\pi(\pi^2 - 4)}{16} = 0.1836 \tag{8.119}$$

$$R = \frac{\pi^2 + 4}{8} \frac{V_{dd}^2}{P_{out}} = 1.7337 \frac{V_{dd}^2}{P_{out}}, \tag{8.120}$$

where $V_{dd}$ is the drain-supply voltage and $P_{out}$ is the fundamental-frequency output power delivered to the load [17].

The previous analysis was based on the assumption of zero device output capacitance. However, at high frequencies, especially for high-power applications, this capacitance cannot be considered negligible and should be taken into account. In this case, the power amplifier is operated in a switching mode with both shunt and series capacitances, and the required idealized operating conditions must be realized with zero current and zero current-derivative-switching conditions. However, to compensate for the capacitor non-zero discharging process, it is necessary to provide zero voltage-derivative condition at the same time. Therefore, the theoretical analysis illustrates the infeasibility of a zero-current-switching Class-E mode to approach 100% collector efficiency with non-zero device output capacitance [18]. Moreover, the collector efficiency will drop drastically if the output device capacitance is significant. This means that, in the frequency domain, the harmonic impedance conditions should be different, being inductive at the fundamental frequency and capacitive for higher-order harmonics, which can be achieved only with zero-voltage-switching conditions.

However, there is a class of pHEMT devices, the output capacitance of which is sufficiently small and can be used for low-power high-frequency Class-E power-amplifier applications. The typical value of the drain-source capacitance for a 0.15 $\mu$m or 0.5 $\mu$m pHEMT device with a total gate width of $8 \times 75\,\mu$m is about 0.25 pF, and, as a first approximation, it increases linearly with total gate width [17]. The simulation results at an operating frequency of 2.5 GHz show that, for the same device parameters when using output capacitance as a variable, the drain efficiency is just slightly affected when its value is less than 0.7 pF; however, the drain efficiency reduces drastically as the drain-source capacitance increases above 0.7 pF. Consequently, there is a limitation in the device size, above which it is not possible to achieve high drain efficiency. To estimate the maximum achievable output power, it is necessary to take into account the typical pHEMT dc current density of 300 mA/mm for reliable operation. The measurement results of a hybrid single-stage power amplifier using an OMMIC pHEMT device with a gate width of $6 \times 50\,\mu$m and standard surface-mounted components in an inverse Class-E mode with series inductance exhibited an output power of 18 dBm (63 mV) with a power gain of 18 dB and a drain efficiency of 95% at an operating frequency of 870 MHz and a dc-supply voltage of 2 V [16].

## 8.5 Harmonic Tuning Using Load-Pull Techniques

Generally, the transistor is operated as a nonlinear active device under large-signal conditions, resulting in a significant amount of harmonic components. Since the second harmonic is the largest harmonic component, it was found experimentally that just providing the proper source and load second harmonic-terminating impedances at the input and output ports of the transistor can significantly improve the power-amplifier efficiency. At microwave frequencies, the special network based on three coupled bars positioned between two ground planes can be used to realize a wide range of impedance matching at the fundamental frequency, while simultaneously presenting reactive impedance at the second-harmonic component, thus decoupling the second-harmonic signal from the 50-Ω load [19].

To maximize the amplifier efficiency, the proper harmonic impedances must be provided at the transistor output port. At microwave frequencies, those impedances must be measured or simulated accurately, taking account of the transistor's parasitic elements and defining accurately the values of the equivalent-circuit parameters under large-signal operation. Since it is neccessary to realize zero or infinite-harmonic impedance conditions seen by the internal device current source required for ideal conventional Class-F or inverse Class-F modes, the corresponding optimum reactances at the harmonics must be presented at the device external output port which can then be translated to those internal reactance required for switched-mode operation. Once the optimum impedances at the device output for the second and third harmonics are established by accurate measurements or simulations, the next step is to properly design the load network using lumped or transmission-line elements to achieve those impedances.

Fig. 8.22 shows the circuit configuration of a high-efficiency MESFET power amplifier using a harmonic-reaction technique based on the effect of second-harmonic injection [20].

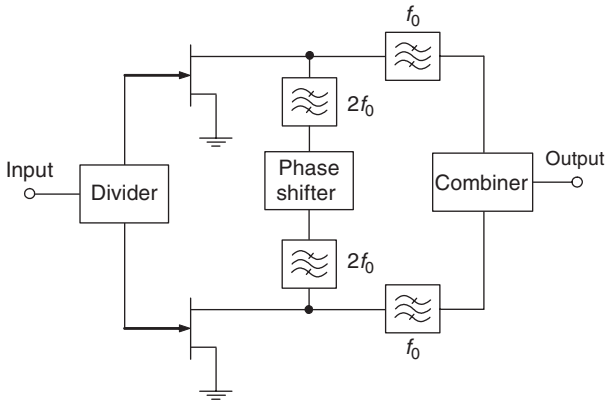



**Figure 8.22: Circuit configuration of harmonic-reaction amplifier [20].**

Unlike the balanced power amplifier, this configuration includes a second-harmonic path between the output ports of the devices. The fundamental-frequency output paths and the second-harmonic path are designed to provide independent matching of the device output impedances, conjugate impedance matching with 50 Ω load at the fundamental frequency, and optimum reactance matching at the second harmonic for maximum drain efficiency. Since the second-harmonic path has well-matched impedance characteristics, each MESFET device mutually injects without reflection a second-harmonic component into the other MESFET device through the second-harmonic path. However, it should be noted that high-efficiency operation is possible only if both devices are driven with phase-coherent and equal-amplitude input signals. As a result, output power of 5 W with a power-added efficiency of 70% and a drain efficiency of 75% was obtained at the operating frequency of 2 GHz and dc-supply voltage of 7 V.

Fig. 8.23(*a*) shows the circuit diagram of a single-ended *X*-band MESFET power amplifier designed to provide simultaneously the optimum load impedance at the fundamental frequency and zero impedance at the second harmonic at the device output [21]. The load network includes the series parasitic drain lead inductance, which was optimized to provide the proper reactance to the device. A quarter-wave open stub was used for the second-harmonic short circuit. It becomes capacitive at the fundamental frequency and its capacitance is a part of the output-matching circuit. An output power of 450 mW and maximum power-added efficiency of 61% with drain efficiency of 76% were obtained at the operating frequency of 10 GHz, using a MESFET device with a gate geometry of 0.5 $\mu$m $\times$ 1200 $\mu$m. The same power amplifier without the second-harmonic tuning circuit had demonstrated a power-added efficiency of only 50%. Fig. 8.23(*b*) shows an *X*-band 0.5-W MESFET power amplifier with

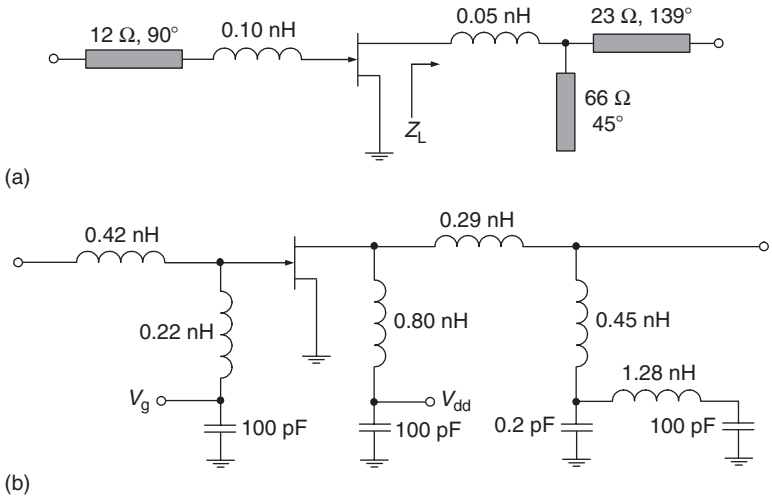



**Figure 8.23: Circuit diagrams of Class-B X-band power amplifiers with harmonic tuning [21, 22].**

the same device geometry having a load network with lumped elements tuned to optimally terminate the second and third harmonics [22]. As a result, the measured efficiency of the power amplifier with optimal harmonic tuning was 49.3%, while the maximum efficiency measured for a device tuned to only the fundamental was 44.5%.

One popular and effective way to measure the fundamental optimum device output impedances is to use passive or active load-pull measurement system [23, 24]. The objective of the active load-pull measurement technique is to find the best output load in terms of the optimum value of the load reflection coefficient $\Gamma_L(f_0)$ presented to the transistor output at the fundamental frequency, such that the power gain and power-added efficiency are optimized. Although cumbersome and labor intensive, such an experimental technique can provide accurate information regarding the nonlinear operation of the active device. It should be mentioned that the transistor large-signal *S*-parameters measured at a certain bias condition and output power provide insufficient information for the design of strongly driven power amplifiers with strongly nonlinear behavior of the active device. Therefore, when the transistor is operated in a nonlinear mode, measurement techniques are required that reproduce large-signal operation as input and output impedances or a nonlinear active-device model, that are valid for all used bias conditions and frequency ranges.

Fig. 8.24 shows the basic components of an active load-pull measurement system based on two six-port reflectometers [25]. At the input of the device under test (DUT), the six-port reflectometer SP1 provides a measurement of the large-signal reflection coefficient $\Gamma_{in}(f_0)$ and the input power $P_{in}(f_0)$ absorbed by the DUT. At the output of the DUT, the measurements of the large-signal reflection coefficient $\Gamma_L(nf_0)$ and the output power $P_L(nf_0)$ for $n = 1, 2$ are achieved by the six-port reflectometer SP2. The evaluation of $\Gamma_L(nf_0)$ and $P_L(nf_0)$ at a particular frequency requires that the power at that frequency be extracted from the output spectrum by means of splitting and filtering circuits inserted between all detection ports and the power sensors. Performing a fundamental load-pulling consists of varying the load $\Gamma_L(f_0)$ over the entire Smith chart with RF and dc measurements for each load, while the load $\Gamma_L(2f_0)$ is maintained constant and near $50\,\Omega$. However, the fundamental load-pull technique does not include the effects of harmonic loading. The second harmonic load-pull characterization consists in varying the load $\Gamma_L(2f_0)$, while maintaining the load $\Gamma_L(f_0)$ at a desired value. As a result, it was found that the best performance in terms of power gain and power-added efficiency is obtained for purely reactive second-harmonic loads, since this allows the elimination of the resistive power losses. For a specific case of the MESFET power amplifier designed to operate at 3.5 GHz, an improvement of power-added efficiency by about 8% was achieved by using a second harmonic active load-pull characterization technique. The active load-pull system based on a six-port reflectometer can also be used to optimize both linearity and output power or power-added efficiency for modulated signal [26].

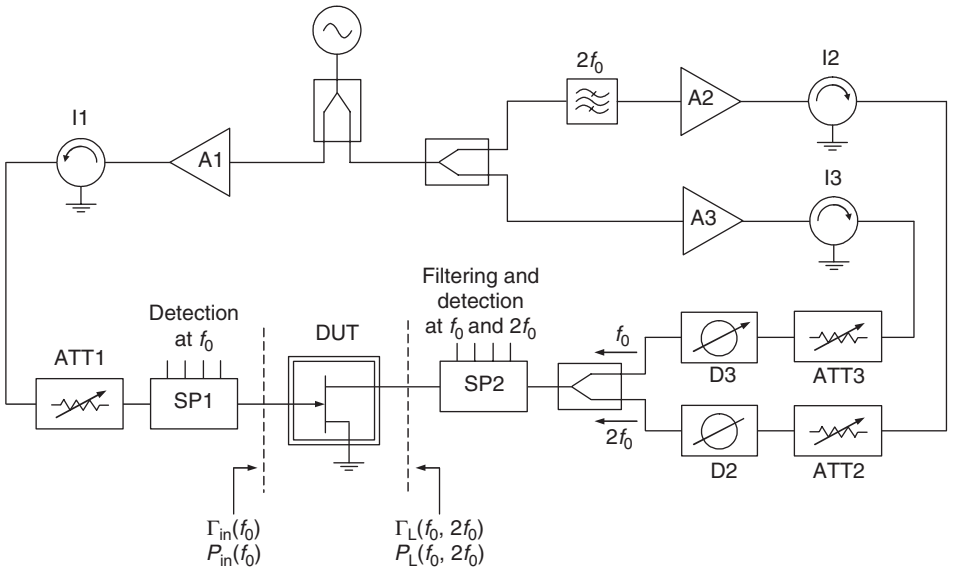



**Figure 8.24: Harmonic active load-pull measurement system schematic [25].**

In addition to harmonic loading at the device output, harmonic tuning at the device input can be effective. For Class-AB power amplifiers, both the linearity and overall efficiency can be improved by the suppression of even-order harmonic components at the device input. Fig. 8.25 shows an example of the circuit schematic of a microwave MESFET power amplifier with source second-harmonic tuning designed to operate in a Class-AB mode [27]. To terminate even harmonics at the device input, a quarter wavelength transmission line at the fundamental frequency, was short-circuited at its far end using a large-value capacitance $C_2$. The series transmission line with varying electrical length $\theta$ is necessary to provide a symmetrical gate-voltage waveform by compensating for the phase of the second-harmonic termination, taking into account the device input-shunt capacitance and parasitic series-gate inductance. The results of nonlinear circuit simulations show a linear (at 1 dB gain compression point) output power of 37.4 dBm at an operating frequency of 6 GHz with an

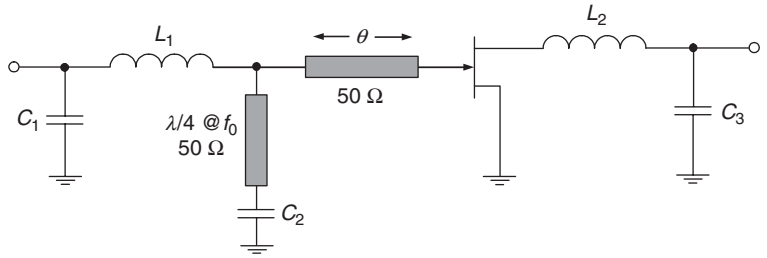



**Figure 8.25: Circuit schematic of Class-AB power amplifier with source harmonic tuning [27].**

power-added efficiency improved by 7% by using source harmonic tuning. It should be noted that changes in the source second harmonic impedance can vary power-added efficiency significantly, from 30–80% for a 5-GHz 28.4-dBm (692 mW) MESFET power amplifier [28].

A systematic procedure of multi-harmonic load-pull simulation using the harmonic-balance method includes two basic steps: finding the optimal loading at each harmonic component, and checking the power levels of higher harmonics [29]. An impedance-sampling method can be used to find the optimal harmonic loading. Generally, only one impedance component $Z_i(k\omega_0)$ at $k$th harmonic and $i$th external port is sampled at the defined impedance plane, while the others are kept constant at each step. For a specific case of a MESFET power amplifier with input and output tuners, as shown in Fig. 8.26(*a*), the design procedure steps are as follows:

1. Start load-pull simulation by sampling the impedance at the fundamental frequency $Z_i(\omega_0)$ and find the optimal load $Z_{iopt}(\omega_0)$.

2. Fix $Z_i(\omega_0)$ at $Z_{iopt}(\omega_0)$ and check the output spectrum to observe the effects of higher harmonic loads on the power-amplifier response.

3. Perform load-pull simulation by sampling the $k$th harmonic impedance $Z_i(k\omega_0)$ and find the optimal load $Z_{iopt}(k\omega_0)$.

4. Fix $Z_i(k\omega_0)$ at $Z_{iopt}(k\omega_0)$ and check the output spectrum to observe the effects of higher harmonic loads on the power-amplifier response.

It should be noted that, if checking the output power spectrum shows that the power at higher harmonics is sufficiently small, the design procedure is stopped.

For a 900-MHz power amplifier using a GaAs MESFET device with a gate periphery of $0.7\,\mu\text{m} \times 600\,\mu\text{m}$ biased at 3 V with a quiescent current of approximately 10% of total dc drain current, it was shown that, with sinusoidal driving signal, the best power-added efficiencies are achieved at load phase angles close to $\pm 180^\circ$ for the second harmonic, corresponding to short-circuit condition, and at load phase angles close to zero at the third harmonic, corresponding to open-circuit condition, approximating a conventional Class-F mode [30]. The simulation results demonstrated a strong dependence of efficiency on the second-harmonic termination, while the effect of the third harmonic was much weaker. The effect of the fourth- and fifth-harmonic terminations, stronger in the former case and weaker in the latter case, results in efficiency variation of approximately 2.5%. It is necessary to minimize the resistive losses in the harmonic terminations, intended to be purely reactive, that could be changed from reactive to resistive if the harmonic terminations are excessively lossy.

The properly phased input and output voltage harmonic components using a multi-harmonic terminating scheme shown in Fig. 8.26(*b*) can be achieved by choosing the optimum impedances for each harmonic component [31, 32]. For example, in a Class-F mode these output impedances can be purely resistive (low at even harmonics and high at odd harmonics), since the drain (collector) current second harmonic is always in-phase and the drain (collector) current third harmonic is always out-of-phase with respect to the fundamental component for conduction angles ranging from 180° (Class-B biasing) to 0° (Class-C biasing). Under slightly overdriven device operation when the drain-current waveform represents a truncated half-sinusoid, the third harmonic becomes out-of-phase also for Class-AB biasing with conduction angles greater than 180°. The same result can be obtained by using a driver stage in a Class-F mode. However, in an inverse Class-F mode, the drain current second harmonic must be out-of-phase with respect to the fundamental-frequency component, which can only be realized by reactive input termination of the second harmonic providing the required phase shift. Fortunately, the main contribution to the harmonic-generating mechanism at the device input is given by its nonlinear input gate-source capacitor acting in a required reverse direction by generating the second and third harmonic components with proper phasing. As a result, optimum half-sinusoidal drain-voltage waveform corresponding to an inverse Class-F mode is achieved by optimizing the input and output impedances at the second and third harmonics simultaneously.

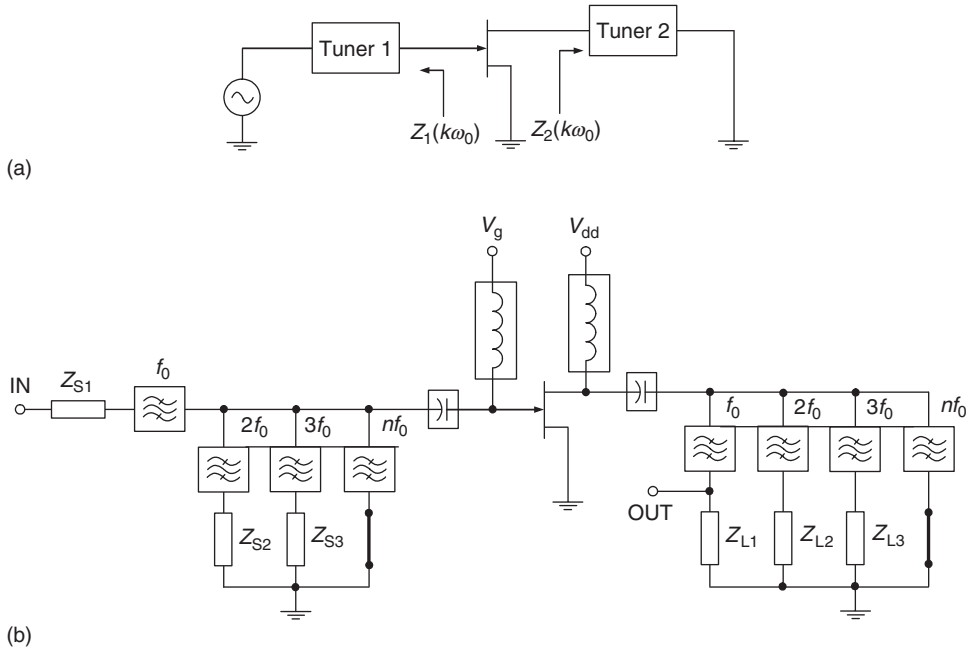



**Figure 8.26: Circuit topologies for multi-harmonic load-pull design procedure [31, 32].**

Generally, it is very difficult to provide accurate source- and load-pull measurements at very high microwave frequencies where de-embedding of waveguide transitions and parasitic discontinuities leads to significant measurement errors. It can be done accurately enough by using on-wafer measurements for an active device with limited output-power capability at the fundamental frequency. At the same time, the *S*-parameters of tuner structures can be accurately predicted using both linear and electromagnetic circuit simulators. The determination of the optimum impedances at the second harmonic can be done by computer source- and load-pull analysis. In this case, it is no problem to isolate the fundamental and second-harmonic paths to determine their optimum impedances. Fig. 8.27 shows the schematic of the source- and load-pull simulation setup for a *V*-band InP HEMT power amplifier, where the ideal output duplexer separates the fundamental from the second-harmonic-components [33]. By changing the ideal transformer turns ratio and the reactive component values, the output power, power-added efficiency, power gain, and stability circle contours can be simulated for various bias voltages and operating frequencies around a center-band frequency of 60 GHz. The optimum second-harmonic termination resulted in a theoretical 6% improvement in power-added efficiency at the 3-dB gain-compression point under Class-AB bias. However, in practice, a smaller improvement is expected because low-loss reactive harmonic loading at 120 GHz is difficult to physically implement without degrading the fundamental load match at 60 GHz.

Au: dc?

Three basic methods of harmonic tuning have been offered commercially for a load-pull system with passive automated tuners [34]. The *triplexer tuning method* uses filters to separate the fundamental and harmonic signals so they can be tuned separately. The block diagram corresponding to this method is shown in Fig. 8.28(*a*) where a triplexer includes a low-pass filter for the fundamental frequency $f_0$, a band-pass filter for the second harmonic $2f_0$, and a band-pass or high-pass filter for the third harmonic $3f_0$. The *stub resonator method* is based on using open stubs with quarter-wave lengths at the second and third harmonic components,

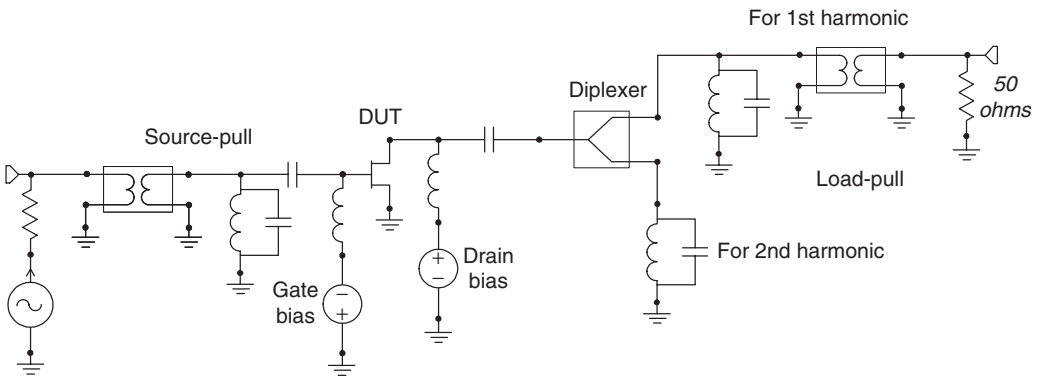



**Figure 8.27: Schematic of source- and load-pull simulation setup.**

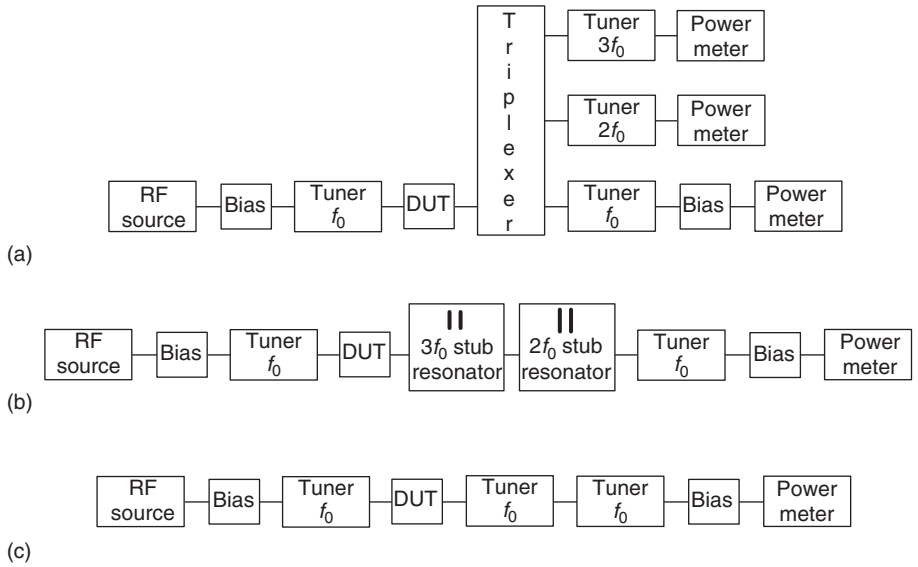



**Figure 8.28: Circuit topologies for multi-harmonic load-pull design procedure [34].**

respectively, connected to the center conductor with a sliding contact according to the block diagram shown in Fig. 8.28(*b*). The *cascaded tuner method* uses the two cascaded tuners shown in Fig. 8.28(*c*) with 625 states each, producing nearly 400,000 available impedance states at the fundamental frequency with a variety of the impedances at the second harmonic. This allows the possibility to optimize the impedance at $2f_0$ with approximately constant impedance at $f_0$. Each method has its own advantages and disadvantages. For example, the triplexer method is the only approach with high tuning isolations, however with slightly more power loss at harmonic frequency, especially at the third harmonic, compared to the stub-resonator method. At the same time, the stub-resonator method with dual stubs is operated over a very narrow bandwidth. The cascaded-tuner method has an advantage here, because no hardware needs to be changed; however, its tuning isolation is very poor. Thus, the triplexer method looks the best because of the major advantages over the other methods, with typical return-loss isolation over 100 dB and insertion loss of 0.2 to 0.3 dB.

## References

[1] S. A. Zhukov and V. B. Kozyrev, ''Push-Pull Switching-Mode Tuned Power Amplifier without Commutation Losses (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Elektrosvyazi*, vol. 15, pp. 95–106, 1975.

[2] S.-A. El-Hamamsy, ''Design of High-Efficiency RF Class-D Power Amplifier,'' *IEEE Trans. Power Electronics*, vol. PE-9, pp. 297–308, May 1994.

[3] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Ikeda, ''Class DE High-Efficiency Tuned Power Amplifier,'' *IEEE Trans. Circuits and Systems—I: Fundamental Theory Appl.*, vol. CAS-I-43, pp. 51–60, January 1996.

[4] M. Albulet, ''An Exact Analysis of Class DE Amplifier at Any Output *Q*,'' *IEEE Trans. Circuits and Systems—I: Fundamental Theory Appl.*, vol. CAS-I-46, pp. 1228–1239, October 1999.

[5] A. Alipov and V. Kozyrev, ''Push/Pull Class-DE Switching Power Amplifier,'' *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1635–1638.

[6] A. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

[7] I. de Vries, ''High Power and High Frequency Class-DE Inverters,'' PhD thesis, Department of Electrical Engineering, University of Cape Town, South Africa, August 1999.

[8] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, ''The Class-E/F Family of ZVS Switching Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-51, pp. 1677–1690, June 2003.

[9] S. D. Kee, I. Aoki, and D. Rutledge, ''7-MHz, 1.1-kW Demonstration of the New $E/F_{2,odd}$ Switching Amplifier Class,'' *2001 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1505–1508.

[10] M. Iwadare, S. Mori, and K. Ikeda, ''Even Harmonic Resonant Class E Tuned Power Amplifier without RF Choke,'' *Electronics and Communications in Japan*, vol. 79, pp. 23–30, January 1996.

[11] F. Bohn, S. Kee, and A. Hajimiri, ''Demonstration of the New $E/F_{odd}$ Dual-Band Power Amplifier,'' *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1631–1634.

[12] B. Molnar, ''Basic Limitations on Waveforms Achievable in Single-Ended Switching-Mode Tuned (Class E) Power Amplifiers,'' *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 144–146, February 1984.

[13] A. Telegdy, B. Molnar, and N. O. Sokal, ''Class-$E_M$ Switching-Mode Tuned Power Amplifier—High Efficiency with Slow-Switching Transistor,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-51, pp. 1662–1676, June 2003.

[14] M. Kazimierczuk, ''Class E Tuned Power Amplifier with Shunt Inductor,'' *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 2–7, February 1981.

[15] C. P. Avratoglou and N. C. Voulgaris, ''A Class E Tuned Amplifier Configuration with Finite DC-Feed Inductance and No Capacitance in Parallel with Switch,'' *IEEE Trans. Circuits and Systems*, vol. CAS-35, pp. 416–422, April 1988.

[16] T. Brabetz and V. F. Fusco, ''Voltage-Driven Class E Amplifier and Applications,'' *IEE Proc. Microwaves Antennas Propag.*, vol. 152, pp. 373–377, October 2005.

[17] T. Mury and V. F. Fusco, ''Series-L/Parallel-Tuned Versus Shunt-C/Series-Tuned Class-E Power Amplifier Comparison,'' *IEE Proc. Circuits Devices Syst.*, vol. 152, pp. 709–717, December 2005.

[18] K. J. Herman and R. E. Zulinski, ''The Infeasibility of a Zero-Current Switching Class E Amplifier,'' *IEEE Trans. Circuits and Systems*, vol. CAS-37, pp. 152–154, January 1990.

[19] S. R. Mazumder, A. Azizi, and F. E. Gardiol, ''Improvement of a Class-C Transistor Power Amplifier by Second-Harmonic Tuning,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 430–433, May 1979.

[20] T. Nojima and S. Nishiki, ''High Efficiency Microwave Harmonic Reaction Amplifier,'' *1988 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1007–1010.

[21] M. A. Khatibzadeh and H. Q. Tserng, ''Harmonic Tuning of Power FETs at X-Band,'' *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 989–992.

[22] B. Kopp and D. D. Heston, ''High-Efficiency 5-Watt Power Amplifier with Harmonic Tuning,'' *1988 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 839–842.

[23] J. M. Cusak, S. M. Perlow, and B. S. Perlman, ''Automatic Load Contour Mapping for Microwave Power Transistors,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, pp. 1146–1152, December 1974.

[24] Y. Takayama, ''A New Load-Pull Characterization Method for Microwave Power Transistors,'' *1976 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 218–220.

[25] P. Berini, M. Desgagne, F. M. Ghannouchi, and R. G. Bosisio, ''An Experimental Study of the Effects of Harmonic Loading on Microwave MESFET Oscillators and Amplifiers,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-42, pp. 943–950, June 1994.

[26] S. Bensmida, E. Bergeault, G. I. Abib, and B. Huyart, ''Power Amplifier Characterization: An Active Load-Pull System Based on Six-Port Reflectometer

Using Complex Modulated Carrier,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-54, pp. 2707–2712, June 2006.

[27] S. Watanabe, S. Takatsuka, K. Takagi, H. Kuroda, and Y. Oda, ''Effect of Source Harmonic Tuning on Linearity of Power GaAs FET under Class AB Operation,'' *IEICE Trans. Electron.*, vol. E79-C, pp. 611–616, May 1996.

[28] L. C. Hall and R. J. Trew, ''Maximum Efficiency Tuning of Microwave Amplifiers,'' *1991 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 123–126.

[29] Q. Cai, J. Herber, and S. Peng, ''A Systematic Scheme for Power Amplifier Design Using a Multi-Harmonic Loadpull Simulation Technique,'' *1998 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 161–165.

[30] J. Staudinger, ''Multiharmonic Load Termination Effects on GaAs MESFET Power Amplifiers,'' *Microwave J.*, vol. 39, pp. 60–77, April 1996.

[31] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, ''Multiharmonic Manipulation for Highly Efficient Microwave Power Amplifiers,'' *Int. J. RF & Microwave Computer-Aided Eng.*, vol. 11, pp. 366–384, November 2001.

[32] P. Colantonio, F. Giannini, E. Limiti, and V. Teppati, ''An Approach to Harmonic Load- and Source-Pull Measurements for High-Efficiency PA Design,'' *IEEE Trans. Microwave Theory Tech.*, vol. MTT-52, pp. 191–198, January 2005.

[33] O. S. A. Tang, S. M. J. Liu, P. C. Chao, W. M. T. Kong, K. C. Hwang, K. Nichols, and J. Heaton, ''Design and Fabrication of a Wideband 56- to 63-GHz Monolithic Power Amplifier with Very High Power-Added Efficiency,'' *IEEE J. Solid-State Circuits*, vol. SC-35, pp. 1298–1306, September 2000.

[34] G. Simpson, ''A Comparison of Harmonic Tuning Methods for Load Pull Systems,'' *Maury Microwave Corp.,* 2004.

CHAPTER 9

# Computer-Aided Design of Switched-Mode Power Amplifiers

Nonlinear circuit simulation in the frequency and time domains is a very important tool for analysis, design, and optimization of high-efficiency switched-mode power amplifiers of Classes D, DE, and E. The advantages are significantly reduced development time and final product cost, better understanding of the circuit behavior, and faster obtaining of the optimum design. It is especially important at very high frequencies, including microwaves, and for MMIC development, where the transistor and circuit parasitics can significantly affect the overall power-amplifier performance. Therefore, it is very important to incorporate into the simulator as accurate a transistor model as possible, to approximate correctly the device behavior, not only at the fundamental frequency, but also at the second and higher harmonics of the operating frequency. In this chapter, the different CAD programs are described to analyze the time-domain and frequency-domain behavior of the switched-mode high-efficiency power amplifiers in different frequency ranges from high frequencies to microwaves, including HB-PLUS and SPICE CAD tools for Class-D and Class-DE circuits and HEPA-PLUS, SPICE, and ADS CAD tools for Class-E circuits. We present and discuss a detailed simulation example of a high-efficiency two-stage 1.75-GHz HBT MMIC power amplifier that uses microstrip transmission lines in the supply and load networks.

## 9.1 HB-PLUS Program for Half-Bridge and Full-Bridge Direct-Coupled Voltage-Switching Class-D and Class-DE Circuits

*Program capabilities*. The HB-PLUS CAD program can simulate and automatically optimize resonant and non-resonant half-bridge or full-bridge circuits with a load that receives the output power, driven through a load network [1]. Several versions of the circuit are described in Chapter 2; the simplest tuned version is shown in Fig. 2.6. The switching power transistors can be operated in the hard-switching mode (Class D; both switches operating at 50% duty ratio, and the transistor switch is turned on with the full dc supply voltage across the transistor), or the soft-switching mode (Class DE; each transistor is turned on with nearly zero voltage across the transistor, achieved by using smaller than 50% duty ratio of each transistor).

The circuit can be used as an RF or microwave power amplifier, as a dc-dc converter, as a dc-ac inverter, or as an ac (including RF and microwave) power generator. The HB-PLUS program performs the following functions:

- Simulates very rapidly the steady-state periodic response of the circuit, 100 to 1000 times as fast as with SPICE and about 10 times as fast as with Agilent ADS. The outputs are time-domain graphical plots and frequency-domain spectra of all important circuit voltage and current waveforms, and a tabulation of input power from the dc supply, RF output power, efficiency, inefficiency, and power dissipation in each circuit element (including the parasitic power losses in each inductor and capacitor). The spectrum is computed for frequencies from dc through the 31st harmonic of the operating frequency.

- Simulates the cycle-by-cycle transient response, from any computed or user-specified starting condition, to any combination of time-varying circuit parameters, such as switching frequency, switch duty ratio, dc supply voltage, and load impedance. The available outputs are the same as for the steady-state periodic response.

- Sweeps up to 28 circuit parameters and plots one or two output variables versus the swept parameter.

- Optimizes the design automatically, according to tradeoffs that can be specified among input dc power, output RF power, efficiency, inefficiency, and each component of power loss.

- Computes transfer functions: any output variable versus any circuit parameter.

The steady-state periodic response of the circuit to the periodic input drive is the circuit operation after the start-up transient has died away, which is the operation usually observed in experimental results. HB-PLUS simulates the voltage-switching Class-D or Class-DE circuit very quickly and the simulation requires about 8 ms second on a Pentium III/667-MHz computer.

Using the cycle-by-cycle transient response, it is possible to evaluate transient stresses:

- Occurring during equipment turn-on and turn-off

- Resulting from transient changes of load (including load faults of shorted or open load, or any arbitrary impedance magnitude and angle)

- Resulting from application or removal of input drive with the dc supply voltage present

- Resulting from transient changes of dc supply voltage
- Resulting from failure of any circuit element

or to simulate the transient response to modulation of any combination of time-varying circuit parameters. This text refers to the half-bridge circuit; the *HB-PLUS User Manual* also explains how to simulate and optimize the full-bridge circuit.

*Circuit topologies*. Fig. 9.1(*a*) shows the general model of a half-bridge voltage-switching Class-D or Class-DE circuit used in HB-PLUS, including a dc power supply $V_{cc}$, a load network and load, and two switches. The switch-enhanced macro-model, which can accurately represent any type of input-controlled solid-state switches based on different types of bipolar junction transistors (BJTs), MOSFETs, or MESFETs, is shown in Fig. 9.1(*b*), where $V_o$ is the saturation offset voltage, $V_t$ is the turn-on threshold voltage of internal or external anti-parallel diode (the parasitic substrate diode of a silicon MOSFET or an external diode intentionally connected from emitter to collector of a BJT), $R_d$ is the ohmic resistance of the anti-parallel diode, $R_{on}$ is the on-resistance ($R_{ds(on)}$ for a MOSFET or $R_{ce(sat)}$ for a BJT), and $C_{out}$ is the equivalent transistor output capacitance characterized by its parasitic resistance $R_{Cout}$ [2].

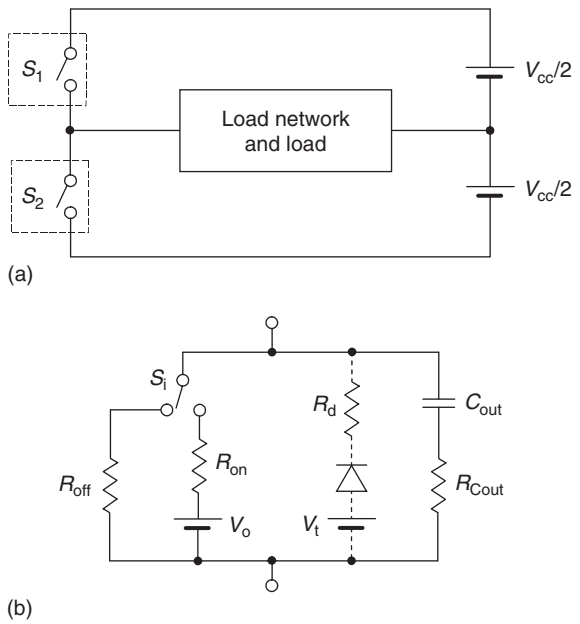



**Figure 9.1: General model of half-bridge voltage-switching Class-D power amplifier: *a*) basic circuit, *b*) equivalent switch model.**

The load-network configuration shown in Fig. 9.2 includes a general-purpose multiple-inductor/multiple-capacitor network. It can be used to represent a non-resonant network or a resonant network that is series-loaded, parallel-loaded, or split-reactor-loaded, where either loss resistances or quality factors for all inductors and capacitors can be specified. The extended configuration of the load network provides considerable flexibility for representing a particular circuit arrangement. $R_{\text{load}}$ is a resistance to which the RF output power is delivered. The inductor and capacitor that are adjacent to $R_{\text{load}}$ allow representing the load as generic *RLC* impedance. Alternatively, $R_{\text{load}}$ and its adjacent $L$ and $C$ can represent the input-port impedance of an external two-port network that performs the functions of coupling, tuning, and impedance-transformation of a load located at the output port. Which $L$ and $C$ components will be adjacent to $R_{\text{load}}$ depends on which reactive components the user includes in the load network; the user can remove unwanted components. The two-port network's input/output transmission function can include attenuation, by using the *ESR* and *EPR* components that are associated with the $L$ and $C$ that are adjacent to $R_{\text{load}}$. For example, the two-port network's input/output transmission function has an attenuation $(1/EPR_{\text{C5}} + 1/EPR_{\text{L6}})/(1/EPR_{\text{C5}} + 1/EPR_{\text{L6}} + 1/R_{\text{load}})$. The full high-frequency $T$-model of a transformer includes mutual inductance and core loss ($L_4$ and $EPR_{\text{L4}}$), primary and secondary leakage inductances ($L_3$ and $L_5$), winding resistances ($ESR_{\text{L3}}$ and $ESR_{\text{L5}}$), and winding capacitances ($C_3$ and $C_5$). The capacitor $C_4$ represents a distributed model of winding capacitance. The inductor $L_2$ can be the inductor of a resonant load network or the commuting inductor of a non-resonant soft-switching (zero-voltage turn-on) load network. The capacitor $C_2$ can be the resonance capacitor of a resonant load network or the dc-blocking capacitor of a non-resonant network. If the user is not using the two-port macro-modeling technique discussed previously, $R_{\text{load}}$, $L_6$, and the remainder of $C_5$, and the parasitic loss resistances

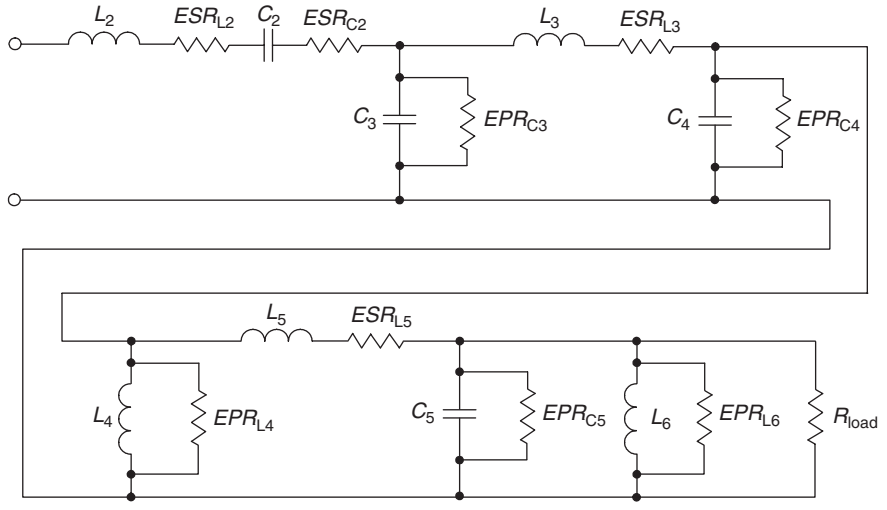



**Figure 9.2: Load network and load in HB-PLUS.**

$EPR_{L6}$ and $EPR_{C5}$, can represent a general-purpose *RLC* network that models any chosen four parameters of any arbitrary load impedance; e.g., magnitude and phase at the operating frequency, magnitude or phase at the third-harmonic frequency (the even-harmonic voltages and currents are usually negligibly small in bridge-type power converters), and fractional power loss (attenuation) at all frequencies, as discussed earlier. Alternatively, $C_4L_4$ can represent a parallel resonator, $C_2C_3$ can represent a split resonance capacitor, $L_3L_4$ (or $L_5L_6$) can represent a split resonance inductor, etc. Using a two-port macro-model for the external two-port network yields accurate results with faster computation than would be obtained by computing separately the voltages and currents of all of the individual components that collectively provide the functions modeled by the two-port macro-model.

*Class D versus Class DE*. P. J. Baxandall published the first description of a Class-D circuit in a paper discussing voltage-switching and current-switching self-excited oscillators [3]. Later publications by other authors discussed the use of the circuit in tuned and untuned amplifiers. In those early publications, the transistor switches were operated with ''on'' duty ratio of 50%, resulting in ''hard turn-on switching'' of the transistors: a turning-on upper transistor ($S_1$ in Fig. 9.1(*a*)) would charge the switching-node capacitance from ground up to the positive-supply rail; a turning-on lower transistor ($S_2$ in Fig. 9.1(*a*)) would discharge that capacitance from the positive-rail voltage down to ground. The switching-node capacitance is the output capacitances of the two transistors, plus circuit wiring capacitance. The charging and discharging power dissipations resulting from hard-switching were $(CV^2f)/2$ at each turn-on transition (twice per cycle of the switching frequency), where $C$ is the node capacitance, $f$ is the switching frequency, and $V$ is the dc supply voltage (labeled ''$2V_{cc}$'' in Figs. 2.6 and 2.7, and ''$V_{cc}$'' in Fig. 9.1(*a*)). When the circuit was being used at audio frequencies, that power dissipation was not a problem, but as users applied the technique at frequencies higher than a few hundred kHz, the capacitor-discharge power dissipation became objectionable.

S. A. Zhukov and V. B. Kozyrev published a technique for eliminating the power dissipation associated with charging and discharging the node capacitance [4]. The duty ratio of each transistor switch is reduced from 50% to a lower value, leaving a ''conduction gap'' during which both switches are ''off,'' as shown in Fig. 9.3. During that conduction gap, the current in the inductor of the load network can charge the node capacitance up to the positive rail, and discharge that capacitance down to ground. They suggested choosing the circuit parameters to yield a switch-voltage waveform that has zero voltage and zero-voltage slope, at the time the switch will be turned ''on.'' Those conditions are the same as in the nominal waveform of a Class-E amplifier described in Chapter 5. Because the circuit operates like Class D, modified to have turn-on transitions like Class E, later authors referred to that variant of Class D as ''Class DE.'' D. C. Hamill updated [4] and made it easily available to the English-speaking part of the world [5].

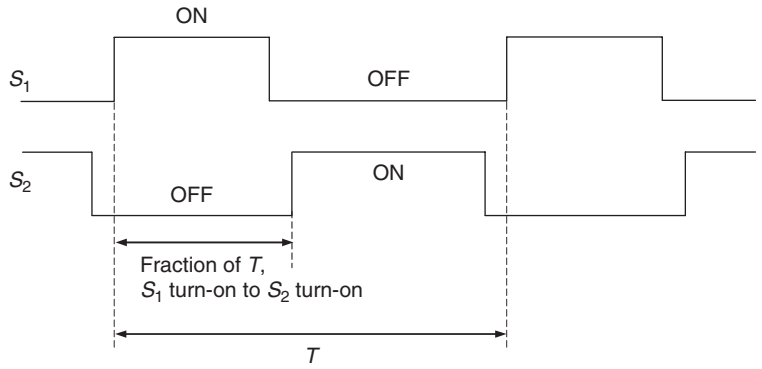



**Figure 9.3: Switch timing for Class DE.**

If the load-network inductance value is intentionally made larger than the value needed for resonance with the network capacitance at the switching frequency, zero-voltage turn-on switching can be achieved with a larger switch duty ratio (narrower conduction gap) than would be needed if the inductance resonated with the capacitance at the switching frequency. That increases the output power available at a given level of peak current in the transistor, or decreases the peak current needed for a specified output power. A unique feature of HB-PLUS program is the ability to adjust automatically the values of the circuit elements (capacitors, inductors, and resistors) and circuit parameters (switching frequency and switch conduction duty cycle) to achieve optimum performance. The meaning of ''optimum'' is defined by an *objective function* that comprises a series of terms, each of which pertains to one aspect of circuit performance. For each performance parameter of interest, a *target* value and a *handicap* (tradeoff) value are entered. The target value is the value that is required to achieve representing, for example, the number of watts of output power. The handicap value represents the relative number of units of that performance parameter that corresponds in importance to the specified handicap values of each of the other performance parameters. For example, if the handicap for efficiency is 2.0 and the handicap for output power is 5.0, the program will understand that an increase of efficiency of 2.0 percent points has the same importance as an increase of output power of 5.0 W. A handicap value of zero instructs the program to ignore that parameter in computing the objective function.

## 9.2 HEPA-PLUS CAD Program for Class E

*Program capabilities*. The HEPA-PLUS CAD program can be used to simulate a variety of topologies of tuned and untuned single-ended and push-pull power amplifiers operating in Classes AB, B, and C in output-power saturation and in Class E and some types of Class F [6]. The program performs the following design functions:

- Evaluates a priori the performance achievable with a candidate transistor in a nominal-waveform Class-E circuit using inductors and capacitors with specified

quality factors. The output is plots of efficiency versus frequency at four values of output power, for specified ranges of frequency and output power.

- Automatically makes a preliminary circuit design to meet the specified design goals using inductors and capacitors with specified quality factors. The output is a complete set of circuit-element values, which can be a starting point for a circuit optimization.

- Simulates very rapidly the steady-state periodic response of the circuit 100 to 1000 times as fast as with SPICE and about 10 times as fast as with ADS. The outputs are time-domain graphical plots and frequency-domain spectra of all circuit voltage and current waveforms and a tabulation of input power from the dc supply, output power, efficiency, inefficiency, power dissipation in each element (including the parasitic power losses in each inductor and capacitor), and transistor peak voltage and current in the normal and inverse directions.

- Simulates the cycle-by-cycle transient response, from any starting condition, to a transient change of any combination of input drive, dc supply voltage, and circuit-parameter values. The available outputs are the same as for the steady-state periodic response.

- Sweeps any of the 25 circuit parameters and plots any one or two output variables versus the swept parameter.

- Optimizes the design automatically according to the specified trade-offs, among seven evaluation factors that include output power, efficiency, and transistor stresses.

- Computes required control functions: value of any circuit parameter versus any other circuit parameter to maintain a specified output voltage, current, or power, e.g., transistor conduction angle (duty cycle or duty ratio) versus required output-voltage amplitude, in a linear-amplifier or high-level modulator application.

*Steady-state periodic response*. The steady-state periodic response of the circuit to the periodic input drive is the circuit operation after the start-up transient has died away, which is the operation usually observed in experimental measurements. HEPA-PLUS simulates the switched-mode Class-E circuit very quickly. For example, the simulation requires about 8 milliseconds on a 667-MHz computer making a 256-point frequency sweep from 13.5–14 MHz of the built-in default circuit.

*Transient response*. Using the cycle-by-cycle transient response, it is possible to evaluate transient stresses

- occurring during equipment turn-on and turn-off

- resulting from transient changes of load (including load faults of shorted or open load, or any arbitrary impedance magnitude and angle)
- resulting from application or removal of input drive with the dc supply voltage present
- resulting from transient changes of dc supply voltage
- resulting from failure of any circuit component

or to simulate the transient response to modulation of any combination of time-varying circuit parameters such as dc supply voltage, input-drive frequency, transistor duty ratio (conduction angle), or any circuit-element value.

*Circuit topology*. Fig. 9.4 shows the generic single-ended topology used in HEPA-PLUS including both a switch and a load network. The switch model comprises a saturation offset voltage $V_o$, a turn-on threshold voltage $V_t$ of internal or external anti-parallel diode (the parasitic substrate diode of a silicon MOSFET or an external diode intentionally connected from emitter to collector of a BJT), an ohmic resistance of the anti-parallel diode $R_d$, an on-resistance $R_{on}$ ($R_{ds(on)}$ for a MOSFET or $R_{ce(sat)}$ for a BJT), an equivalent nonlinear transistor output capacitance $C_{out}$ characterized by its parasitic resistance $R_{Cout}$, and a series parasitic inductance $L_q$ modeling the inductance of the emitter or source bondwires. The load network includes five resonators (main series resonator $L_2C_2$ with parasitic loss resistances $ESR_{L2}$ and $ESR_{C2}$, main parallel resonator $L_3C_3$ with parasitic loss resistances $EPR_{L3}$ and $EPR_{C3}$, two auxiliary series resonators, $L_QC_{out}$ and $L_{C1}C_1$, and auxiliary parallel resonator $C_{out}L_{C1}$, an arbitrary *RLC* load impedance that can be placed at the $R_2$ location in series with the resonator $L_2C_2$ or at the $R_3$ location in parallel with resonator $C_3L_3$, and parasitic loss resistances for all circuit components. The resonators can each be made resonant at any chosen frequency, not necessarily at the operating frequency and not necessarily all at the same frequency. Components not used in a particular circuit can be deleted from the generic circuit topology by giving them negligibly small or large values, or removing them.

*Optimization*. The HEPA-PLUS CAD program optimizes all components of the load network shown in Fig. 9.4, including simultaneous optimization of the load-network resistance and the impedance transformation (''matching'') network that transforms the external load impedance (connected at the matching-network's output port) to the optimum value of load-network resistance (presented at the matching-network's input port). That is, the external load $R_3$ is shunted by $C_3$, and the equivalent series $C$ and lower-resistance $R$ are tuned to purely resistive by adding an inductance in series with the equivalent $C$ and $R$. The optimum values of $C_3$ and the added inductance are found automatically by the optimizer. That needed inductance is automatically added to the value of $L_2$ that would have been used as a resonator with $C_2$ and a purely resistive load. The external load impedance can be any arbitrary parallel *RLC* circuit

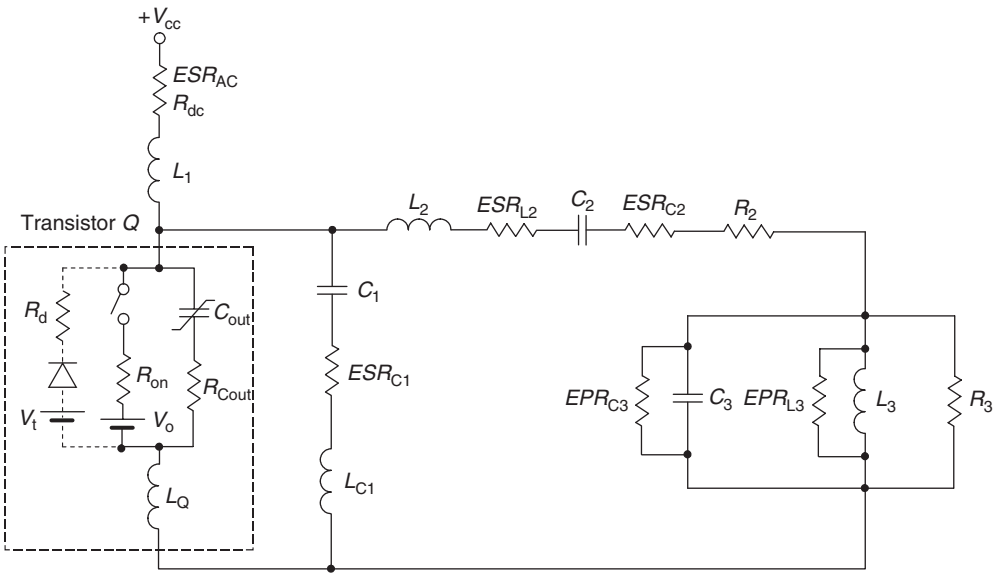



**Figure 9.4: Generic single-ended circuit topology (two such circuits are used for push-pull amplifiers; three types of combiners are available for combining the "push" and "pull" halves of the push-pull circuit).**

(e.g., $R_3$, $L_3$, and $C_3$), not necessarily the commonly used purely resistive 50 ohms. The *HEPA-PLUS User Manual* gives full information on this useful feature.

## 9.3 Effect of Class-E Load-Network Parameter Variations

Mistuning of the Class-E load network parameters can have a significant effect on the output power and efficiency. In this case, it is convenient to define this effect visually based on the collector current and voltage waveforms to faster tune the load network parameters to their optimum values. The effect of a change in the load angle $\psi = \tan^{-1}(\omega L/R)$ or normalized series inductance $L$ on collector voltage and current waveforms of a Class-E power amplifier with shunt capacitance is shown in Fig. 9.5 [7]. For values of $\psi$ slightly less inductive than optimum of 49.05°, the collector voltage at the turn-on instant attains a certain positive value, as shown in Fig. 9.5($a$). However, for values of $\psi$ slightly more inductive than optimum, a small negative voltage swing appears, as shown in Fig. 9.5($b$). For capacitive loading and larger inductive loading, the collector voltage becomes large at the turn-on time, causing low efficiency. For extremely reactive loads, the collector voltage tends toward the ramp shape, which it would have with no load at all. The negative current capability is needed whenever the load is more inductive than the ideal 49.05°. It should be mentioned that the efficiency remains close to 100 percent for load angles between about 40° and 70°.

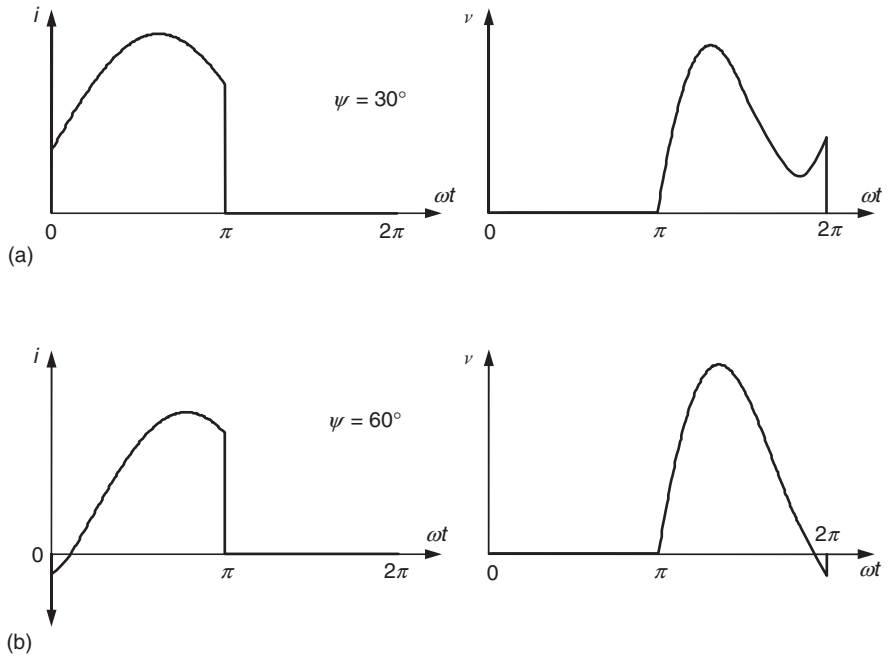



**Figure 9.5: Collector waveforms as functions of load angle.**

Fig. 9.6 illustrates the effect in the collector current and voltage waveforms of a change in the normalized shunt susceptance $\xi = \omega CR$ in a Class-E power amplifier with shunt capacitance of otherwise nominal design [7]. In this case, low values of shunt susceptance produce a collector voltage that swings to both large positive and large negative values, as shown in Fig. 9.6(*a*). While the voltage at turn-on time is never negative, the negative current is required for some values of $\xi$, as shown in Fig. 9.6(*b*). As the shunt susceptance becomes very large for the same load resistance, it tends to dominate, producing a ramp voltage waveform and drawing such current as is necessary to charge the capacitor. Under these conditions, the output power becomes constant but is small. It should be noted that the power amplifier is quite tolerant of variations of shunt susceptance and maintains high efficiency for values $\xi$ between 0.06 and 0.3. The effect caused by deviation of the load resistance $R$ from its optimum value shows that efficiency varies gradually, remaining at 95% or more for variations in the load resistance of $+55\%$ to $-37\%$.

Fig. 9.7 shows the low-order Class-E load network with shunt capacitance and the typical mistuned collector voltage waveform demonstrating the transistor turn-on, turn-off, and waveform ''trough.'' The inductor $L_1$ is considered an RF choke with high reactance to isolate dc and RF paths between each other. The reactance of the series circuit composing of $L_2$ and $C_2$ is inductive. At the turn-on time of the transistor, the collector voltage waveform has zero slope and zero voltage. An actual load network can approximate the idealized optimum

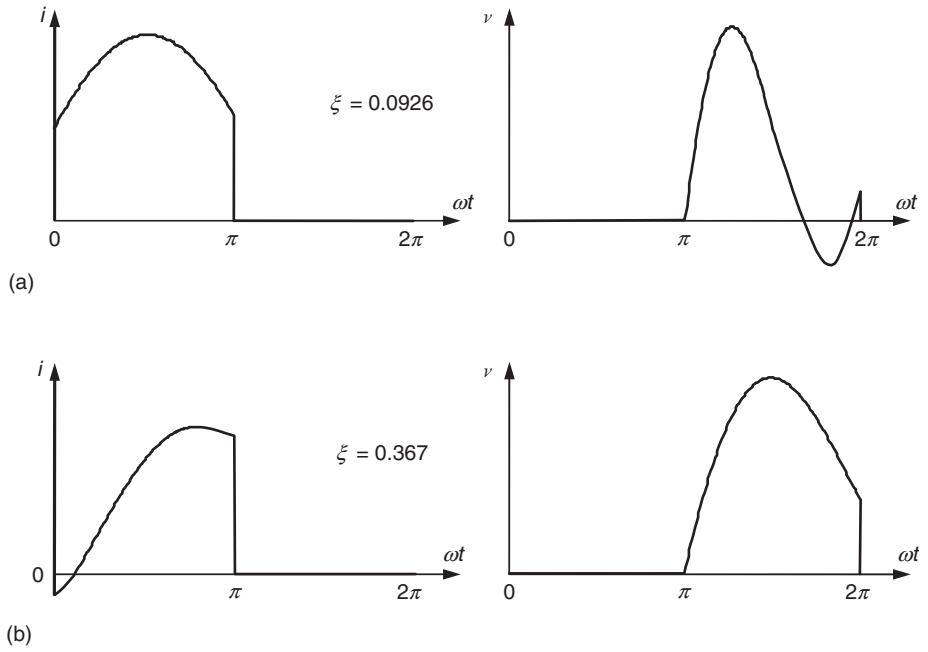



**Figure 9.6: Collector waveforms as functions of normalized shunt capacitance.**

(or nominal) conditions by adjusting its parameters $C_1$, $C_2$, and/or $L_2$. If $R$ is not already the desired value for the desired output power, it may need adjustment as well. The circuit will operate with the nominal Class-E waveform, while delivering the specified output power at the specified frequency, if the chosen parameter values are installed in the actual hardware. The possible need for tuning results from tolerances on the component values (normally not a problem, because Class E has low sensitivity to component tolerances) and the possibility of unknown-value reactances in series with $R$ (therefore, in series with $L_2$ and $C_2$) after the load resistance has been transformed to the chosen value of $R$. Those series reactances require that the reactances of $L_2$ and $C_2$ be reduced by the amounts of the unknown inserted inductive and capacitive series reactances, but how can we do that when those inserted reactances are unknown?

If we know how changes of $L_2$ and $C_2$ will affect the collector-voltage waveform, we can adjust $L_2$ and $C_2$ to meet two criteria at the operating frequency: achieve close to the nominal collector-voltage waveform and deliver the specified value of output power [8]. Fig. 9.7(*b*) shows how $L_2$ and $C_2$ affect the collector-voltage waveform. We know also that increasing $L_2$ reduces the output power and vice versa. In practice, with an oscilloscope displaying the voltage waveform and a directional power meter indicating the power delivered to the load, we can adjust $L_2$ and $C_2$ to simultaneously fulfill the two desired conditions (nominal waveform and desired output power) even if the reactances in a series with $R$ are unknown.

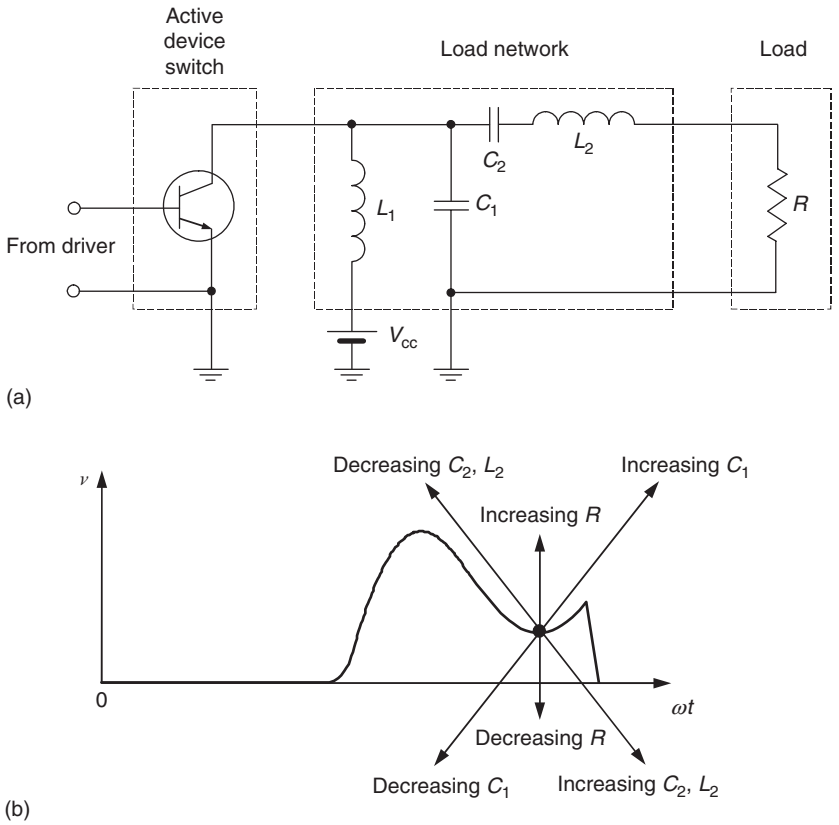



**Figure 9.7: Load network and effect of adjusting its components.**

If $C_1$ (comprised of the transistor output capacitance and the external capacitor connected in parallel with it) is within about 10% of the intended value, $C_1$ will normally not need adjustment. When there is a large deviation from the design value, $C_1$ can be adjusted to achieve the nominal collector-voltage waveform, using the information in Fig. 9.7(*b*) about the effects of $C_1$ on this waveform. In that case, the three components $C_1$, $C_2$, and $L_2$ can be adjusted to achieve three conditions simultaneously at the operating frequency: desired output power, transistor saturation voltage just before transistor turn-on, and zero slope of the voltage waveform just before turn-on.

Changes in the values of the load network components affect the collector voltage waveform as follows:

- Increasing $C_1$ moves the trough of the waveform upward and to the right.
- Increasing $C_2$ moves the trough of the waveform downward and to the right.
- Increasing $L_2$ moves the trough of the waveform downward and to the right.

- Increasing $R$ moves the trough of the waveform upward ($R$ is not normally an adjustable circuit element).

Knowing these effects, it is easy to adjust the load network for nominal Class-E operation by observing the collector voltage waveform. The adjustment procedure is:

- Set $R$ to the desired value or accept what exists.
- Set $L_2$ for the desired $Q_L = 2\pi f L_2/R$ or accept what exists.
- Set the frequency as desired.
- Adjust $C_1$ and/or $C_2$ as shown in Fig. 9.7($b$).

## 9.4 HB-PLUS CAD Examples for Class D and Class DE

Section 9.1 introduced you to the basic features of the HB-PLUS program. Now, we shall demonstrate the use of HB-PLUS to simulate and analyze a 3-kW 3-MHz half-bridge (voltage-switching Class D) tuned dc-ac power inverter, ac power amplifier, or RF power generator (different specialists use those different terms for what is basically the same thing). The circuit uses a pair of International Rectifier IRFP460 TO-247 MOSFETs, operating from a 450-volt dc supply.

After that, we reduce the duty ratio of both switches to generate a Class-DE version of the circuit in the simplest possible way, using the same transistors, inductors, and capacitors as in the Class-D circuit. For this simplest possible demonstration of the advantages of Class-DE operation, we omit the full optimization that could be achieved by having the optimizer adjust the values of all of the important parameters, avoiding the need for a more-arcane explanation of subtle details. In this example, we demonstrate the benefit of using soft switching (i.e., having the switch turn on at nearly zero switch voltage, and therefore not discharging, through the turning-on switch, a node capacitance that is charged to the full supply voltage). To obtain soft switching, a conduction gap (''dead time'') is provided between the turn-off of one switch and the turn-on of the other switch (shown in Fig. 9.3), and the load network can also be made slightly inductive at the switching frequency. The inductive characteristic can shift the phase of the sinusoidal current, so that the current at switch turn-off can be larger (higher up on the falling part of the sine-wave). That higher current will discharge the node capacitance more quickly. During the switch-conduction gap, the inductive load current charges the node capacitance from the former voltage level to the new voltage level, or to nearly that level. Consequently, the turning-on transistor turns on at near-zero voltage, rather than with the node capacitance charged to the full power-supply voltage, thus avoiding the power dissipation that would occur if the turning-on transistor would charge or discharge the node capacitance.

This example shows the general case, illustrating both waveform features: (*a*) the node capacitance is charged by the inductive load current to nearly the new voltage level, and (*b*) the turning-on switch charges the capacitance the rest of the way. In a full optimization, that combination might result in the smallest total power dissipation at the specified output power and frequency, depending on the set of numerical values of all of the circuit parameters.

*Class D with hard-switching*. As noted previously, the example Class-D circuit is a 3-kW, 3-MHz power amplifier with a duty ratio of 50% for each of the two switches. Hence, this circuit does not yet have the conduction gap (dead time, as shown in Fig. 9.3) that provides soft switching; we shall add that later, after we compute the efficiency of the amplifier output stage and the power losses at different places in the circuit, without yet providing the soft-switching operation. The ''Enter Circuit Parameters'' screens of Figs. 9.8 and 9.9 show the numerical values of all of the circuit parameters. The ''Efficiency and Powers'' screen of Fig. 9.10 shows the drain efficiency and inefficiency, and each of the components of power dissipation. Summarizing the results for Class-D operation: 3213.4 W output at 82.733% drain efficiency, with 612.94 W power dissipation in the two transistors (19.1% of the output power). That amount of power dissipation is higher than desired, and can be reduced significantly by reducing the duty ratio of the two switches to provide soft-switching in the Class-DE mode of operation. A major portion of the power loss in each transistor occurs during turn-on switching; that portion will be essentially eliminated by providing soft-switching operation.

Fig. 9.11 shows graph plots of the waveforms $V_{sw1}$ (the voltage across switch $S_1$) and $I_{sw1(actv)}$ (the current in the active portion of switch 1, i.e., not including the current in the output capacitance of the switch). Note the large spike of switch current at transistor turn-on, while

```
═ Half-Bridge power amplifier/converter (HB) DEMO ═══  Jan. 27, 2007 22:32 ═
Example for HB-Tutorial: 3 kW at 3 MHz

                ENTER CIRCUIT PARAMETERS and TITLE  SCREEN-1

        Switching frequency (f).................[Hz]:       3E+06
        DC supply voltage (Vcc or Vdd).......[volts]:       450
        Fraction of period, turn-on of Sw1 to Sw2...:       0.5
        Switch 1 parameters
          Duty ratio of switch 1.....................       0.5
          Ron1...............................[ohms]:       0.4
          Roff1..............................[ohms]:       1E+06
          Cout1..............................[farads]:       4E-10
          Cout1 series resistance (Rcout1)....[ohms]:       1.2
          Saturation offset voltage (Vo1)....[volts]:       0.8
        Switch 2 parameters
          Duty ratio of switch 2.....................       0.5
          Ron2...............................[ohms]:       0.4
          Roff2..............................[ohms]:       1E+06
          Cout2..............................[farads]:       4E-10
          Cout2 series resistance (Rcout2)....[ohms]:       1.2
          Saturation offset voltage (Vo2)....[volts]:       0.8
SELECTION: <↑,↓>       ENTRY: ALPHANUM.      EXECUTE: <PgDn>      ABORT: <ESC>
SELECTING PARAMETER...
```

**Figure 9.8: "Enter Circuit Parameters—Screen 1" for Class D.**

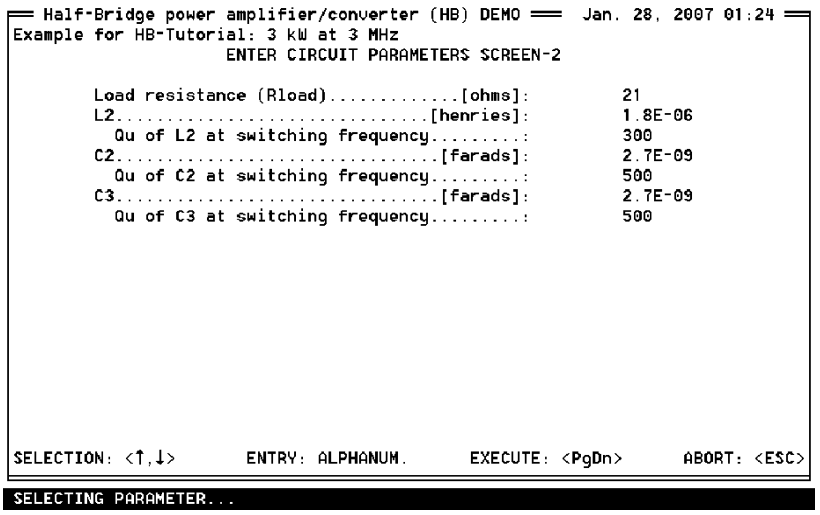



**Figure 9.9: "Enter Circuit Parameters—Screen 2" for Class D.**

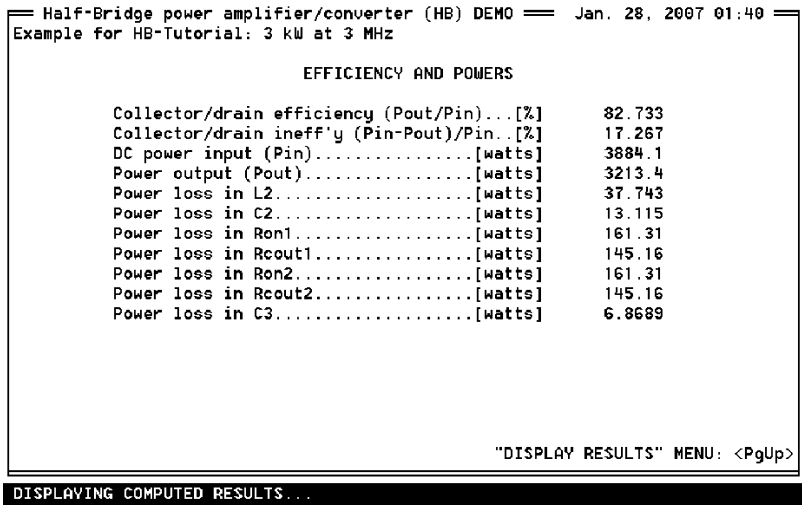



**Figure 9.10: "Efficiency and Powers" screen for Class D.**

the node capacitance is being discharged from +450 V down to the ground; that current spike is the source of much of the transistors' power dissipation, in the ''on'' resistance ($R_{on}$) of the turning-on transistor and in the series resistances ($R_{Cout}$) of the output capacitances of both transistors.

*Class DE with soft-switching*. To obtain soft-switching operation in a simple way, as explained in Section 9.1, we change only the duty ratio of the two transistors, from the original 50% in Class-D operation, down to 40%. Repeating the simulation with only that one change,

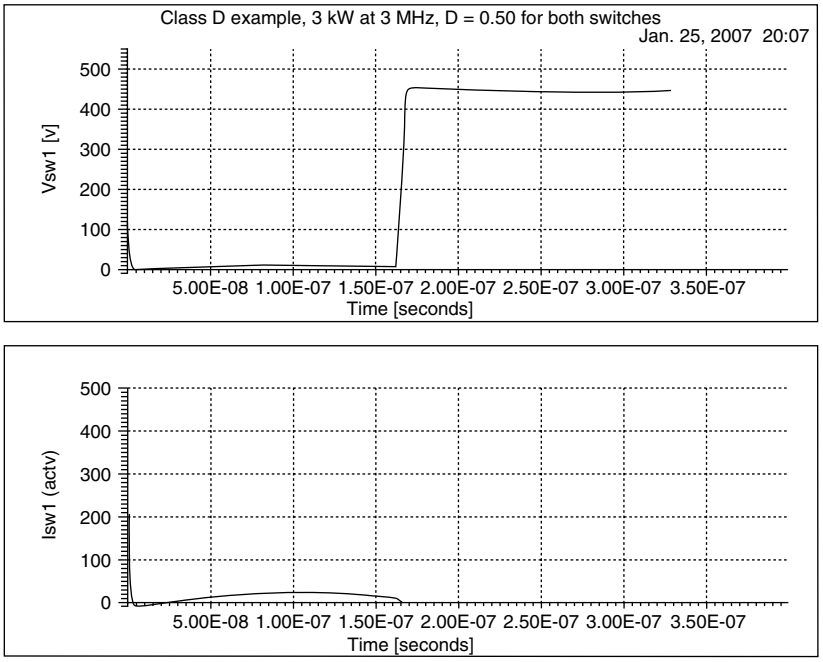



**Figure 9.11: Voltage and current waveforms for Class D.**

we obtain the following results: Fig. 9.12 shows the voltage and current waveforms for $S_1$. Note that the current spike previously existing during the Class-D turn-on switching (see Fig. 9.11) has almost completely disappeared because the conduction gap allows the inductive load current to pull almost all of the stored energy from the node capacitance before the turning-on switch is commanded to turn on (i.e., the node voltage swings most of the way toward the new voltage level before the switch turns on). When the switch turns on, it pulls the node voltage the rest of the way to the new voltage level, in approximately a step change of voltage. Fig. 9.13 shows the ''Efficiency and Powers'' screen for Class-DE operation that can be compared with Fig. 9.10 for the Class-D circuit. Now the drain efficiency is 93.56%, 10.8 percentage points higher than the 82.733% obtained with switch duty ratios of 0.5. The output power is 3073.9 W, 95.7% of the 3213.4 W output of the Class-D circuit. But the transistors' power dissipation has been reduced from 612.9 W in the two transistors in Class-D operation to only 156.5 W in Class-DE operation, a reduction by a factor of 3.92. This reduction of power dissipation and increase of drain efficiency are the result of the soft-switching circuit operation. (In this simple example, about 95% of the voltage swing is achieved by lossless charging of the node capacitance by the inductive load-network current; the remaining approximately 5% of the voltage swing is accomplished by the turning-on transistor charging the capacitance. The combination of load-network parameter values determines what fraction of the voltage swing is accomplished by lossless charging of the capacitance; under some conditions, it can be the full voltage swing.)

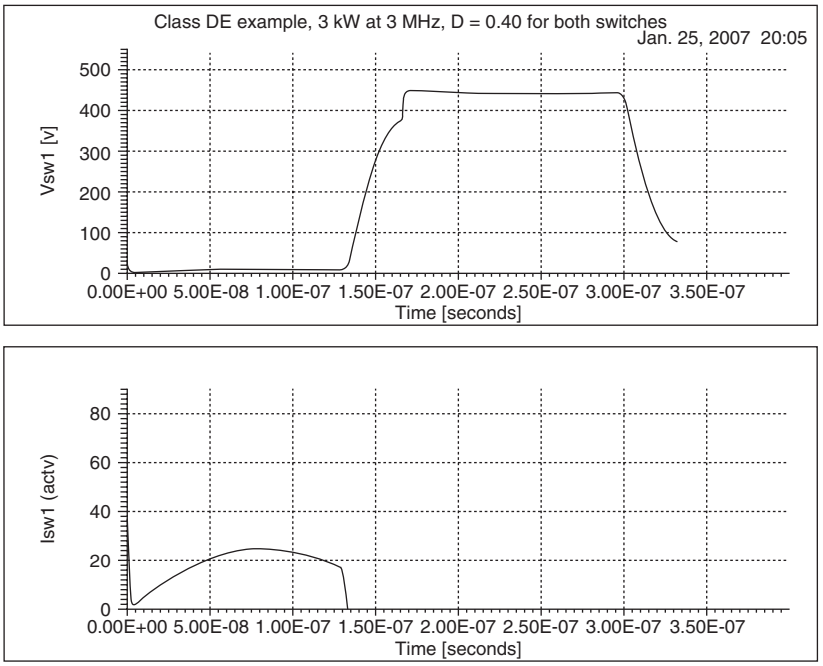



**Figure 9.12: Voltage and current waveforms for Class DE.**

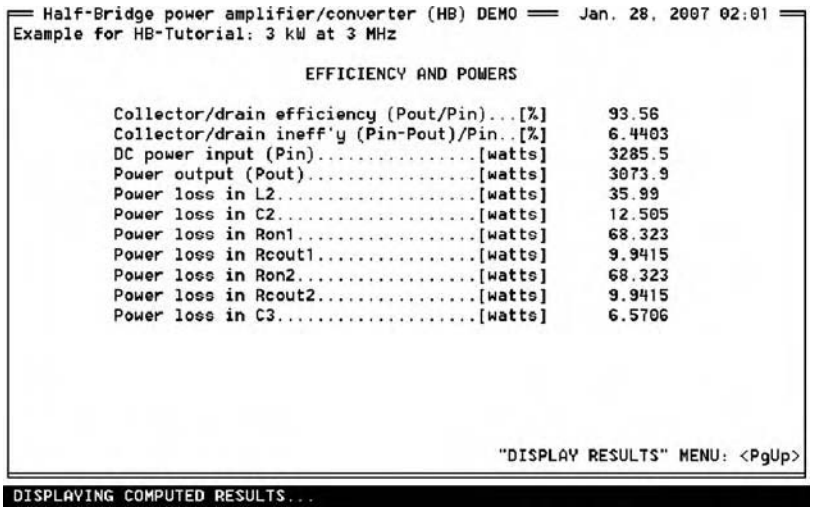



**Figure 9.13: "Efficiency and Powers" for Class DE.**

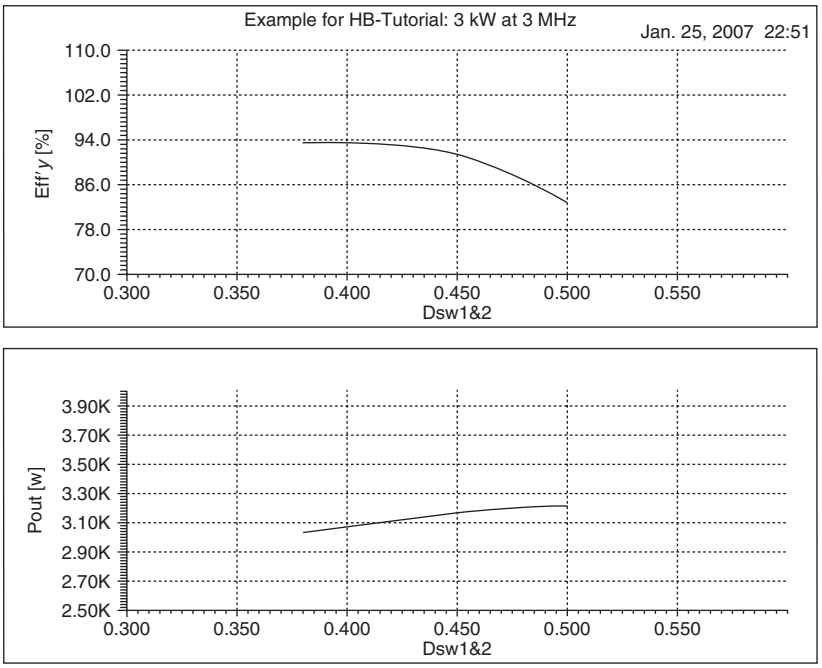



**Figure 9.14: Efficiency and output power versus duty ratio for Class DE.**

We can sweep the duty ratio of both switches from 0.38–0.50 to see continuous functions of the efficiency and output power vs. duty ratio, to verify that the chosen duty cycle is a good choice. The drop of efficiency between the almost-zero-voltage-switching operation at $D = 0.4$ and the hard-switching operation at $D = 0.5$ should be approximately a quadratic function of the increase of duty ratio beyond the value at the borderline of soft switching. This is because (*a*) the power dissipation when the transistors charge the node capacitance is proportional to the square of the voltage change through which the transistors charge the capacitance, and (*b*) the voltage change is approximately proportional to the shortage of conduction gap below the value that just provides soft switching. We can confirm this prediction by sweeping the duty ratio of both switches from 0.40 to 0.50; the result is shown in Fig. 9.14. Sweeping the duty ratio and observing the change of efficiency with duty ratio also demonstrate that the sensitivity of efficiency to changes of duty ratio is quite small in the vicinity of the chosen operating point of $D = 0.4$.

The program displays the numerical results for each point in the sweep as that point is computed. In about a second, the program completes the sweep and plots the two requested variables (Efficiency and Output Power) versus the swept variable (Duty ratio of switches 1 and 2). Note that the shape of the curve of Efficiency versus Duty ratio confirms the predictions in the preceding paragraph.

## 9.5 HEPA-PLUS CAD Example for Class E

Section 9.2 introduced you to the basic features of HEPA-PLUS program. Now, we shall demonstrate a typical design procedure using HEPA-PLUS to design a 13.56-MHz, 100-W Class-E RF power amplifier with a bandwidth of about 5 MHz.

*Evaluate a candidate transistor.* As a first step, it is necessary to evaluate a candidate transistor. In this case, the user examines the amplifier efficiency that can be achieved with one or more candidate transistors, at the desired output power of 100 W at 13.56 MHz. For this example, we use the transistor parameters for the International Rectifier IRF540N silicon MOSFET, and quality factors of 150 for inductors and 1000 for capacitors. We assume that the transistor internal temperature is 95°C, obtained as a 60°C rise above an ambient air temperature of 35°C. We use the vendor-specified maximum $R_{ds(on)}$ of 0.044 ohms at 25°C, and increase that value by a factor of 1.72 to obtain the increased value at 95°C. $R_{Cout}$ is never specified by the vendors of silicon-gate transistors; it is typically five times as large as $R_{ds(on)}$ [2]; we used that factor.

To begin, the user goes from the ''Main Menu'' (Fig. 9.15) to ''Transistor Evaluation'' (Fig. 9.16). The user enters the transistor parameters, the desired frequency range, the amplifier relative bandwidth (the ratio of the frequencies at the upper and lower edges of the desired operating frequency band), and the desired range of output power to be assessed. The desired output power is 100 W; the user brackets that value by specifying the power range to be evaluated as 50–200 W, to be able to see quantitatively the trade-off between efficiency and output power (lower output power yields higher efficiency). The user presses **<Page Down>** to

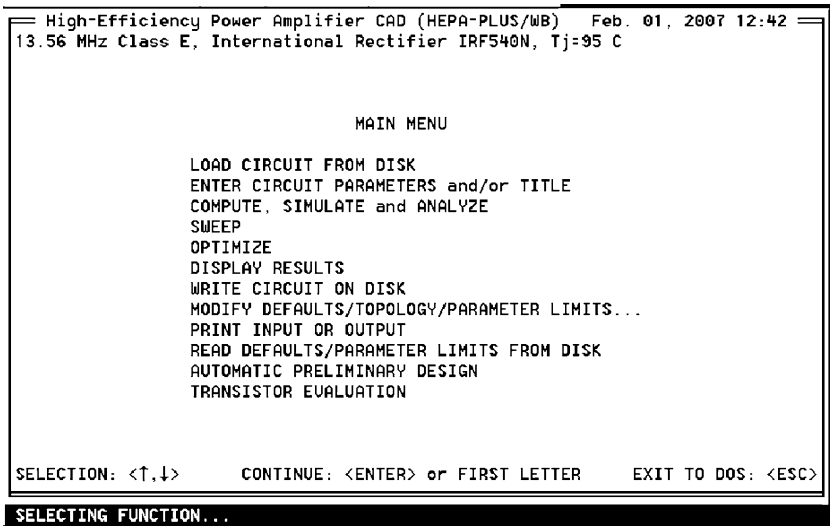



**Figure 9.15: "Main Menu."**

execute the transistor evaluation. After a few seconds, a family of curves is displayed with frequency on the *X*-axis, efficiency on the *Y*-axis, and output power as a parameter, as shown in Fig. 9.17. Observe that for a 13.56-MHz Class-E circuit with an output power of 100 W, the

```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 12:45
13.56 MHz Class E, International Rectifier IRF540N, Tj=95 C
                          TRANSISTOR EVALUATION
                            Single transistor
     Transistor application
        Frequency range.......[Hz]:   Min.:  6.7802E+06 Max.:  2.7121E+07
        Power range.........[watts]:  Min.:  50         Max.:  200
        Amplifier relative bandwidth [f(upper)/f(lower)]:      1.5
     Transistor characteristics
        Peak voltage at nominal tuning...........[volts]:      66
        Turn-off and turn-on times, each.........[sec]:        7.37E-09
        "On" resistance (Ron)....................[ohms]:       0.07568
        Output capacitance (Cout)................[farads]:     2.7376E-10
        Series resistance of output capacitance...[ohms]:      0.3784
        Transistor saturation offset voltage (Vo)[volts]:      0
     Passive components characteristics
        Unloaded Q of L1 at operating frequency.....           150
        Unloaded Q of L2 at operating frequency.....           150
        Unloaded Q of L3 at operating frequency.....           150
        Unloaded Q of C1 at operating frequency.....           1000
        Unloaded Q of C2 at operating frequency.....           1000
        Unloaded Q of C3 at operating frequency.....           1000
SELECTION: <↑,↓,←,→>   ENTRY: ALPHANUM.      EXECUTE: <PgDn>      ABORT: <ESC>
SELECTING PARAMETER...
```

**Figure 9.16: "Transistor Evaluation."**

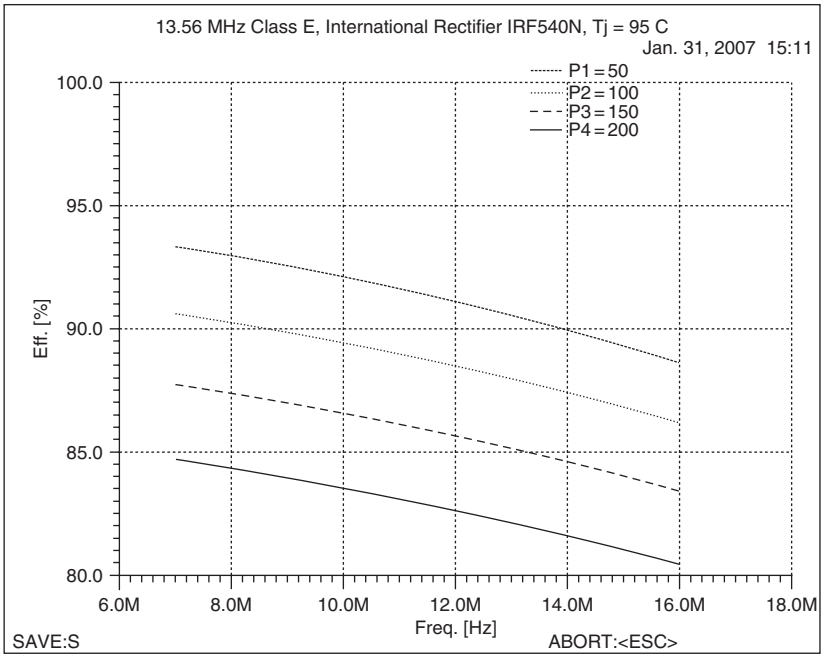



**Figure 9.17: Transistor evaluation: efficiency versus frequency and output power.**

expected efficiency of a nominal-waveforms Class-E circuit is about 87.5%. For the present design example, we shall assume that this efficiency is satisfactory. In an actual design, if there were other candidate transistors, the user would check the expected efficiency of each, in turn, by modifying the transistor characteristics entered on the ''Transistor Evaluation'' screen.

*Use the Automatic Preliminary Design module to obtain a nominal-waveforms Class-E design.* The user goes to the ''Automatic Preliminary Design'' screen by pressing **A** at the Main Menu. The Automatic Preliminary Design module designs a nominal-waveforms Class-E circuit (transistor voltage and voltage-slope both zero at transistor turn-on time [8]), and calculates the expected amplifier efficiency, using the parameters:

- Desired frequency band
- Two of the following: output power, DC supply voltage, and AC load resistance
- Transistor parameters (saved from ''Transistor Evaluation'')
- Quality factors of inductors and capacitors (saved from ''Transistor Evaluation'')

To begin, the user specifies a 1.5:1 frequency band with a geometric mean of about 13.56 MHz: 11.296 MHz to 16.296 MHz (a bandwidth of 5 MHz centered at 13.56 MHz). The user specifies a desired output power of 100 W and a dc drain-supply voltage $V_{dd}$ of 22 V to have the nominal $V_{ds(pk)}$ (estimated as approximately $3.4\,V_{dd}$ after optimization) be about 75% of the maximum rated $V_{dd}$ of 100 V, to provide a 30% safety factor to allow for off-nominal loads and component tolerances. The user enters ''Transistor turn-off and turn-on times'' as (in this example) 10% of the RF period, hence 7.37 ns (5% to 10% of the RF period is usually quite satisfactory). The user presses **<Page Down>** to execute the Automatic Preliminary Design. Almost immediately, the program displays (without making a simulation) a predicted drain efficiency, for this nominal-waveforms design, of 87.8%, and displays the load resistance to be provided at the $R_3$ location as 1.923 ohms. The impedance-transformation (''matching'') network (not yet designed) will transform the external load resistance (e.g., 50 ohms) to this computed value. The results so far are deemed acceptable, so there is no need to evaluate other candidate transistors. The user transfers the computed circuit design to the ''Enter Circuit Parameters'' screen by pressing **<Page Up>**, after which the user will simulate the circuit to verify its correctness. If it is deemed correct, it will be the starting point for an optimization. The result is shown on the screen ''Enter Circuit Parameters and/or Title,'' as in Fig. 9.18.

*Simulate the nominal-waveforms circuit.* Pressing **<Page Down>** at the ''Enter Circuit Parameters'' screen simulates the circuit in about 8 ms on a Pentium III/667 MHz, and faster on faster computers. The result is shown in the screen ''Efficiency, Powers, and Stresses,'' as in Fig. 9.19. The drain efficiency ($P_{out}/P_{in,dc}$) is 87.686% and the output power is 96.848 W.

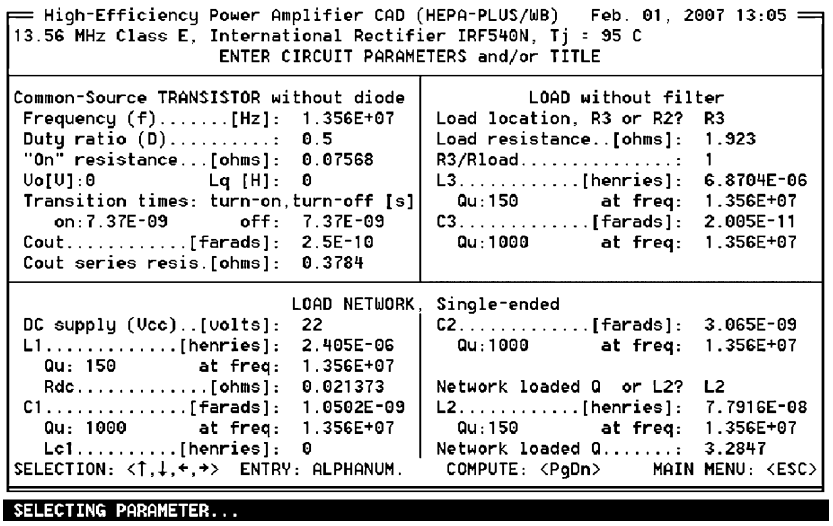



**Figure 9.18: "Enter Circuit Parameters and/or Title."**

The peak transistor voltage and current are 75.346 V and 13.827 A, well within the transistor's maximum ratings of 100 V and 110 A. The Automatic Preliminary Design module, using explicit design equations and no simulation, was designed for 100 W output and achieved within 3.2% of that target value, and had predicted 87.8% efficiency, within 0.11 percentage points of the results of the accurate simulation. Fig. 9.20 shows the transistor voltage and current waveforms of this nominal-waveforms Class-E power amplifier. They are seen to be the same as the theoretical waveforms in Figs. 5.5 and 6.8 except that the simulation

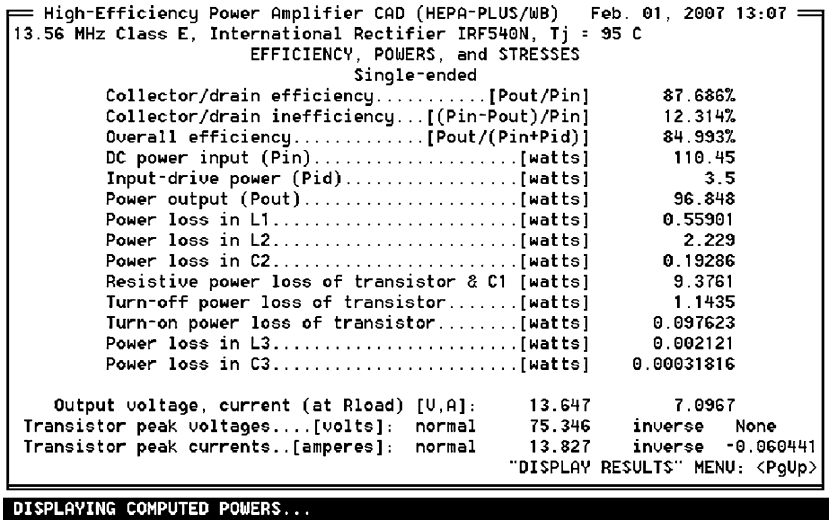



**Figure 9.19: "Efficiency, Powers, and Stresses."**

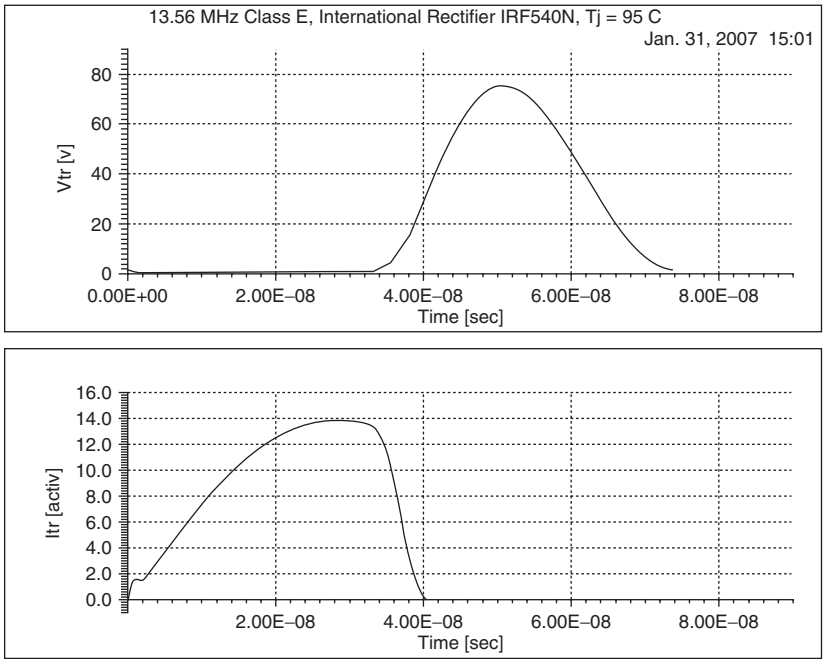
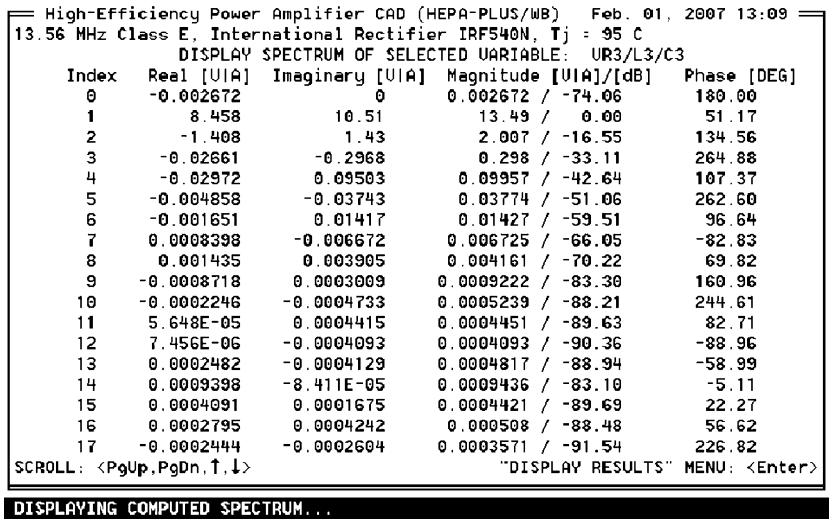



**Figure 9.20: Transistor voltage and current waveforms of nominal-waveforms Class-E power amplifier.**

includes the non-zero switching times, not included in those theoretical waveforms. Note that *high voltage and high current do not exist simultaneously*, even if the transistor turn-on and turn-off transition times are appreciable fractions of the RF cycle. That is the fundamental characteristic of a high-efficiency power amplifier. In this 13.56-MHz design, the transistor turns ''on'' at the left edge of the plot ($t = 0$), and begins to turn ''off'' near the middle of the plot (at $t = 33.2$ ns).

*RF output spectrum*. A spectrum of the RF output power delivered to $R_3$ is available at the screen ''Display Spectrum of Plot Variable $VR_3/L_3/C_3$,'' shown for the optimized circuit as Fig. 9.21. (Other voltages and currents can be chosen also, as the variable to be displayed. For example, the harmonic content of $I_{L1}$, the dc current drawn from the dc power supply, gives an indication of how much bypass-capacitance filtering is needed on the $V_{dd}$ line to maintain the conducted EMI current below a desired maximum allowed value.) The first spectrum screen shown in Fig. 9.21 lists the dBc values from dc (actually zero output, listed as $-74.06$ dBc, an approximation to $-\infty$ dBc) through the 17th harmonic. A similar second screen (not shown here) lists the values for the 18th through 31st harmonics. At each harmonic, the difference between the listed value and the maximum allowed harmonic output is the number of dB of suppression needed in the post-amplifier harmonic-suppression filter. For example, if all harmonics must be below $-65$ dBc, the 7th and higher harmonics need no suppression,



```
═══ High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 13:09 ═══
13.56 MHz Class E, International Rectifier IRF540N, Tj = 95 C
            DISPLAY SPECTRUM OF SELECTED VARIABLE:  VR3/L3/C3
    Index   Real [V|A]  Imaginary [V|A]  Magnitude [V|A]/[dB]   Phase [DEG]
      0     -0.002672            0      0.002672 / -74.06       180.00
      1         8.458        10.51         13.49 /   0.00        51.17
      2        -1.408         1.43          2.007 / -16.55       134.56
      3       -0.02661       -0.2968         0.298 / -33.11       264.88
      4       -0.02972       0.09503        0.09957 / -42.64      107.37
      5      -0.004858      -0.03743        0.03774 / -51.06      262.60
      6      -0.001651       0.01417        0.01427 / -59.51       96.64
      7      0.0008398     -0.006672       0.006725 / -66.05      -82.83
      8       0.001435       0.003905       0.004161 / -70.22       69.82
      9     -0.0008718      0.0003009      0.0009222 / -83.30      160.96
     10     -0.0002246     -0.0004733      0.0005239 / -88.21      244.61
     11      5.648E-05      0.0004415      0.0004451 / -89.63       82.71
     12      7.456E-06     -0.0004093      0.0004093 / -90.36      -88.96
     13      0.0002482     -0.0004129      0.0004817 / -88.94      -58.99
     14      0.0009398     -8.411E-05      0.0009436 / -83.10       -5.11
     15      0.0004091      0.0001675      0.0004421 / -89.69       22.27
     16      0.0002795      0.0004242       0.000508 / -88.48       56.62
     17     -0.0002444     -0.0002604      0.0003571 / -91.54      226.82
SCROLL: <PgUp,PgDn,↑,↓>                    "DISPLAY RESULTS" MENU: <Enter>
DISPLAYING COMPUTED SPECTRUM...
```

**Figure 9.21: "Display Spectrum of Plot Variable $VR_3/L_3/C_3$."**

$2f$ (−16.55 dBc) needs 65 − 16.55 = 48.45 dB of suppression, $3f$ (−33.11 dBc) needs 65 − 33.11 = 31.89 dB of suppression, etc.

*Optimize the design, using the nominal-waveforms design as a starting-point*. The Optimizer module is entered by pressing **O** at the Main Menu or by highlighting that line and pressing the **<Enter>** key. That takes the user to the screen ''Inputs to Optimizer, Screen 1—Objectives of Optimization,'' shown as the upper screen in Fig. 9.22. That upper screen shows the first four of the seven performance characteristics that can be used to define the meaning of ''optimum'' for this application; the next three characteristics are on the continuation Screen 2, shown below Screen 1 in Fig. 9.22. For this example, we shall give the weighting factors $w_1$ (deviation from the target value of output power) and $w_2$ (inefficiency) equal weights of 1, and leave the remaining five weighting factors at their default values of zero. [Note: all mathematicians except the Russians optimize by *minimizing* the ''badness'' of the design (here, $w_1$ is for the *deviation* from the target value of output power, and $w_2$ is for the *in*efficiency); the Russians optimize by *maximizing* the ''goodness'' of the design. Both methods work well, and are basically equivalent.]

The optimization can be done at one frequency or up to 16 frequencies simultaneously, useful for wideband designs. For simplicity, we shall illustrate the optimization at one frequency: 13.56 MHz. The user proceeds to the screen ''Inputs to Optimizer, Screen 3—Circuit Parameters to Be Varied by the Optimizer,'' shown in Fig. 9.23. Here, the user can choose which parameters the Optimizer is allowed to vary, and the minimum and maximum allowed values of those parameters, as constraints on the Optimizer. We shall choose

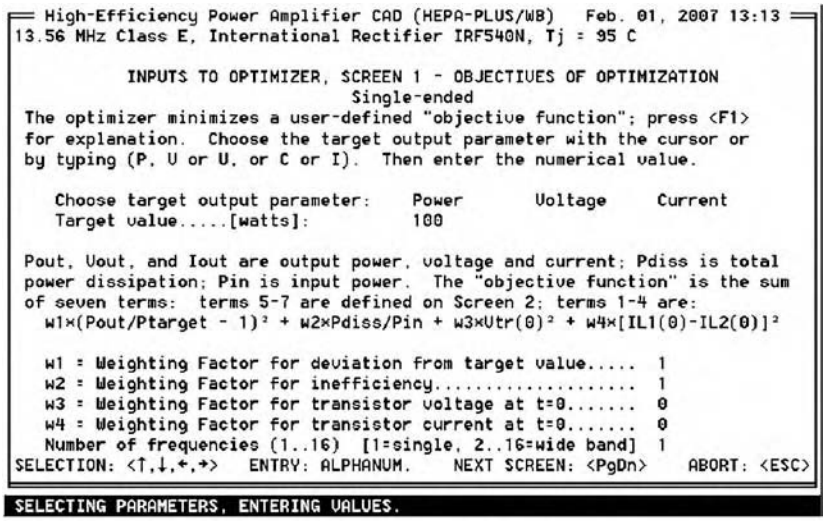



**Figure 9.22: "Inputs to Optimizer—Objectives of Optimization."**

$C_1$, $C_2$, $L_2$, and Load Resistance as the parameters to be varied in the search for the optimum combination. Parameters not chosen to be varied:

1. The duty ratio is set to 50%, already known to be a reasonable compromise among conflicting trade-off factors.

2. $L_1$ is effectively ''infinite''; higher inductance will have essentially no effect, and lower inductance is not needed.

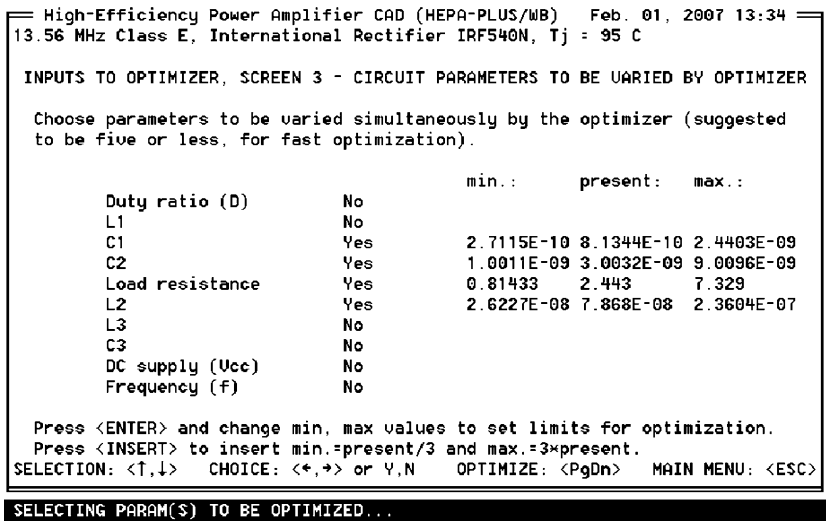



**Figure 9.23: "Inputs to Optimizer, Screen 3—Circuit Parameters to Be Varied by the Optimizer."**

3. $L_3$ and $C_3$ are tuned to the operating frequency, but are given high enough reactance values that they are essentially removed from the circuit. They are available if a tuned load is desired, but that is not needed in this case. For harmonic suppression, a better way to use an inductor and a capacitor (such as $L_3$ and $C_3$) would be to place them in a *LC* low-pass filter (−6 dB per octave above the operating frequency), rather than as a parallel resonator at the load (−3 dB per octave above the operating frequency).

4. The DC supply voltage was already chosen as 22 V to provide sufficient margin against excessive peak transistor voltage.

5. The operating frequency was already chosen as 13.56 MHz, according to the requirements placed on the design.

The user presses the **<Page Down>** key to begin the optimization. In a few seconds, the result is shown at the screen ''Results of Optimization, Completed at Power Evaluation No. nnn,'' where *nnn* is the number of evaluations made on the way to finding the optimum (156 in this example). Fig. 9.24 shows that screen for the case computed here. The initial value of efficiency of the starting circuit (87.686% for the nominal-waveforms design shown in Fig. 9.19, already quite high) was improved by 0.563 percentage points to the listed value of 88.249% on Fig. 9.24. (The optimizer usually reduces the power dissipation by about 30% of its value for the starting circuit, usually increasing the drain efficiency by about 5 percentage points. But if the starting circuit already has high efficiency, the increase of efficiency from optimizing can be small.) To illustrate the larger improvement that can be obtained when the nominal-waveforms circuit does not *already* have high efficiency, the authors increased the

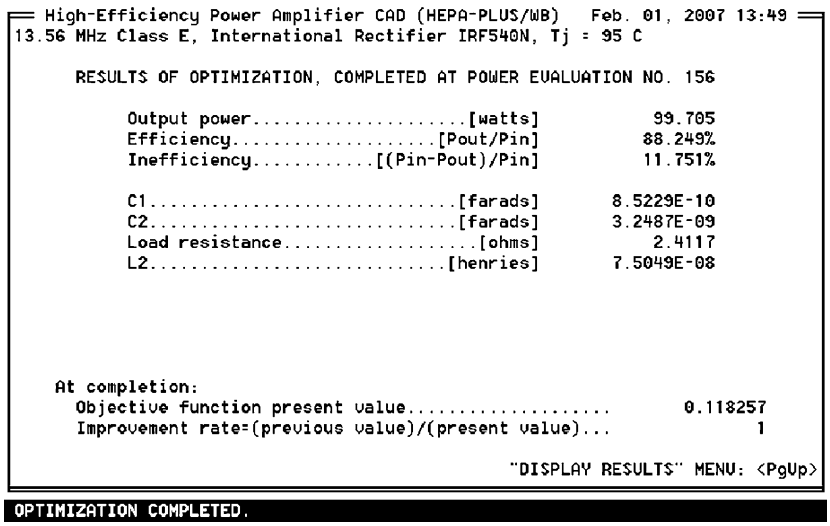



**Figure 9.24: "Results of Optimization, Completed at Power Evaluation No. 156."**

required output power from 100 W to 300 W, and reduced the $Q$ values of $L$ and $C$ from 150 and 1000 to 50 and 200; both changes increase the resistive power losses. Results: for the nominal-waveforms circuit: 300 W at 75.207% efficiency, waveforms similar to Fig. 9.20; for the optimized circuit: 302 W at 80.585% efficiency, efficiency increased by 5.378 percentage points, waveforms similar to Fig. 9.25.

The transistor voltage and current waveforms in the first optimized circuit are shown in Fig. 9.25; they are off-nominal as compared with the non-ideal nominal waveforms in Fig. 9.20 or the idealized nominal waveforms in Figs. 5.5 and 6.8. The user can read out $X$ and $Y$ numerical values from the plot by pressing the left/right cursor keys to move a vertical read-out cursor to the point of interest. The numerical values are displayed at the upper-left and lower-left corners of the plots. The read-out cursor is positioned at the peak of the transistor-voltage waveform; the peak voltage is seen to be 74.79 V, the same as the value that would be listed at the bottom of the screen ''Efficiency, Powers, and Stresses,'' for the optimized circuit.

*Use the SWEEP function.* The program can sweep any of 25 circuit parameters and display graph-plots of one or two of 18 available output variables. At the Main Menu, the user presses **S** for SWEEP. The program presents the screen ''Sweep Menu,'' shown as Fig. 9.26. For this demonstration, we shall sweep Frequency, chosen from a menu of 20 available parameters. The user enters values to compute the results at 13 points from 11 MHz to 17 MHz in an algebraic sweep (equal steps of the swept variable between adjacent points). Also available is Geometric sweep, that has a given multiplication factor on the swept variable between adjacent points. The program determines the step value, given the user-specified range, number of points, and type of sweep.

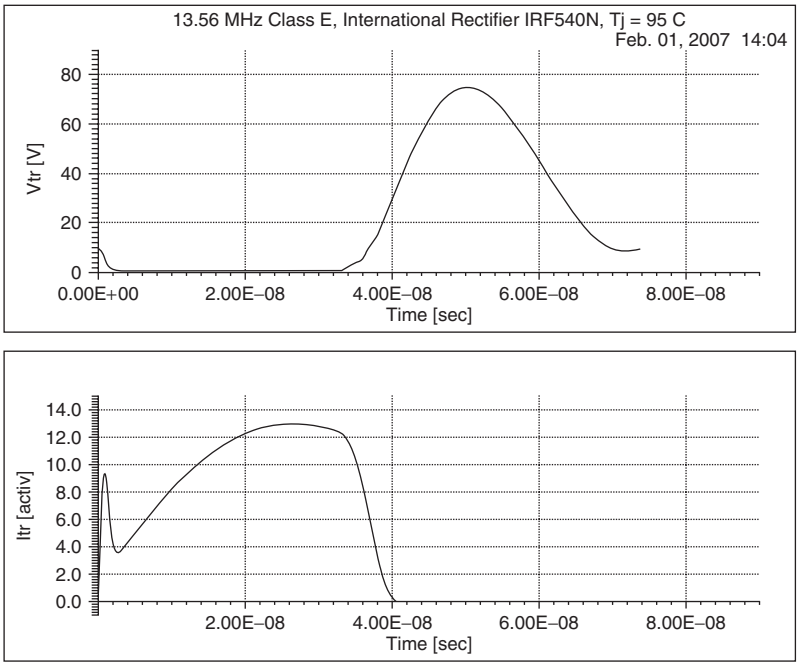



**Figure 9.25: Transistor optimized off-nominal voltage and current waveforms in first optimized circuit.**

```
High-Efficiency Power Amplifier CAD (HEPA-PLUS/WB)   Feb. 01, 2007 20:08
13.56 MHz Class E, International Rectifier IRF540N, Tj=95 C

                              SWEEP MENU

          Parameter to be swept....:      Freq.[Hz]
          Step mode (Alg./Geom.)...:      Algebraic
          Number of points in sweep:      13
          Start value..............:      1.1E+07
          Stop value...............:      1.7E+07
          Step value...............:      5E+05
          First output plot........:      Pout [W]
          Second output plot.......:      Eff'y [%]

SELECTION: <↑,↓,←,→>    ENTRY: ALPHANUM.      EXECUTE: <PgDn>     ABORT: <ESC>
SELECTING PARAMETER...
```

**Figure 9.26: "Sweep Menu."**

The user chooses to plot the default output variables: Output Power and Efficiency. The user presses **<Page Down>** to execute the sweep. During the sweep calculations, the latest values of the swept parameter and the variables to be plotted are displayed in a table at the right side of the screen; the user can watch that table change during the sweep. At the completion of the computation, the program displays graphs of Output Power and Efficiency versus frequency, as shown in Fig. 9.27. Note the variation of output power with frequency. A proprietary design of Design Automation, Inc. (DAI) gives very flat output power and efficiency versus frequency; that is the subject of a patent application by Nathan O. Sokal, one of the authors of this book.

Two more interesting waveforms to display are the currents in the power transistor. We can examine both $I_{tr(activ)}$ (the current in *the active part* of the transistor) and $I_{tr(total)}$ (*the terminal current*, which is the sum of the currents in the active part and in the transistor's output capacitance), and we can compare the two current waveforms. (If we wish, we can also display separately the current in the transistor's output capacitance.) In order to begin, return to the screen ''Variable(s) to Be Plotted'' by pressing **<Enter>**, **<Page Up>**, and **P**. Then press **<6>** to open a window showing a list of variables that can be plotted. Move the cursor to $I_{tr(activ)}$ and press **<Enter>**. Then press **<6>** to place the cursor on $I_{tr(total)}$ and press **<Enter>**. Press **<Page Down>** to display the two waveforms, as shown in Fig. 9.28.

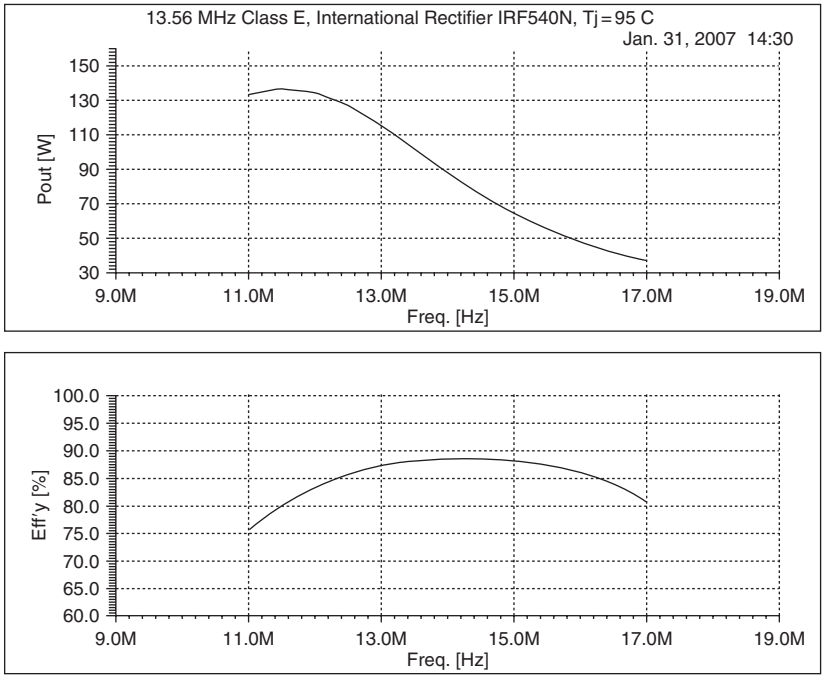



**Figure 9.27: Output power and efficiency versus swept frequency.**

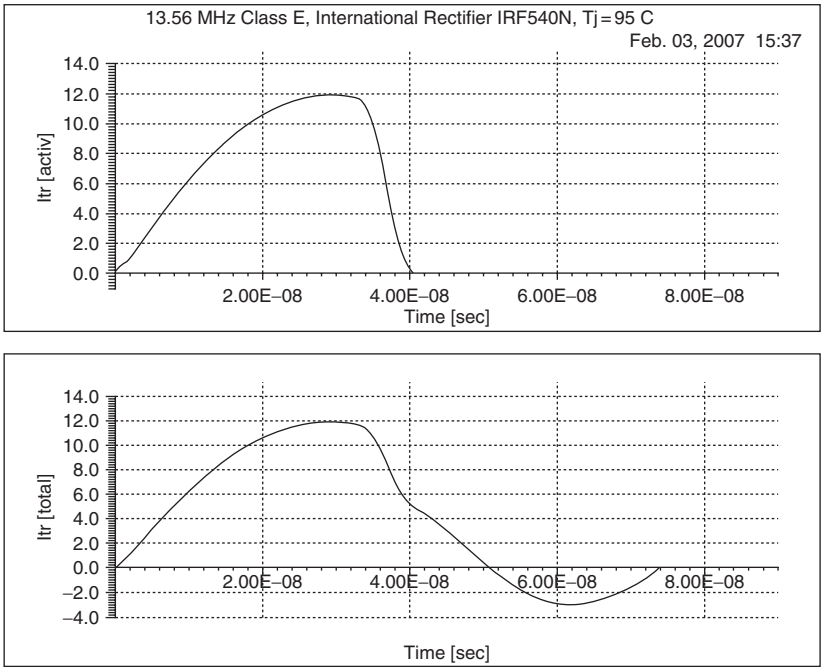



**Figure 9.28: Waveforms of current in active part of transistor and total transistor current.**

In the laboratory, using an oscilloscope, you can observe only $I_{\mathrm{tr(total)}}$, and that only up to about 50 MHz. Unfortunately, this does not give you a clear picture of the details of circuit operation. With the program, however, you can observe clearly the circuit operation with $I_{\mathrm{tr(activ)}}$, and you can see $I_{\mathrm{tr(total)}}$ at the same time. By means of the latter, you can compare experimental observations with the computer simulation, or you can *predict* what you can *expect* to see in a laboratory test.

Similarly, you can observe two versions of the transistor voltage waveform when the transistor internal wiring inductance ($L_{\mathrm{Q}}$ in Fig. 9.4) is non-zero: the transistor *internal* voltage at the transistor die, termed $V_{\mathrm{tr(inter)}}$, and the transistor *terminal* voltage $V_{\mathrm{tr(term)}}$, which includes also the voltage across $L_{\mathrm{Q}}$. Experimentally, you can observe only $V_{\mathrm{tr(term)}}$, but $V_{\mathrm{tr(inter)}}$, which you cannot observe experimentally, gives you much more information about the circuit operation. You can easily observe both voltages with the program if you have set $L_{\mathrm{Q}}$ to a nonzero value at the screen ''Enter Circuit Parameters.'' If $L_{\mathrm{Q}}$ is zero, the internal and external voltages are identical, so the transistor voltage is called simply $V_{\mathrm{tr}}$.

## 9.6 Class-E Power-Amplifier Design Using SPICE

The high-voltage MOSFET devices are preferable to provide a very high output power at high frequencies operating in the switched-mode Class E. Fig. 9.29 shows the simulated circuit

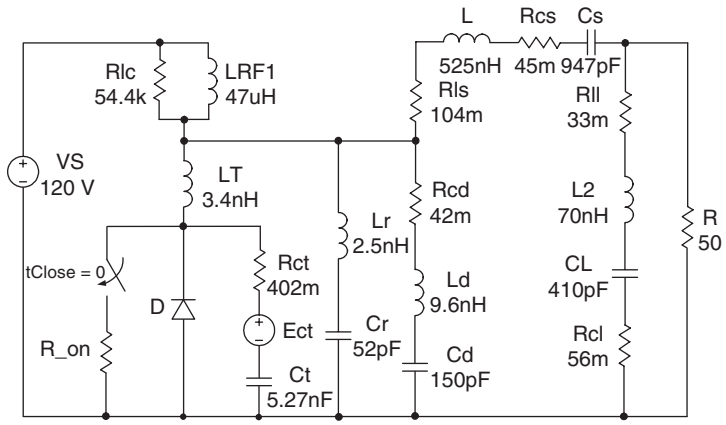



**Figure 9.29: 13.56 MHz Class-E power amplifier SPICE Model [9].**

schematic of a 13.56-MHz 400-W MOSFET Class-E power amplifier implemented in SPICE [9]. The MOSFET device IRFP450LC is modeled as a switch with a linear capacitor $C_t$ and a nonlinear voltage source $E_{ct}$ to model the square-root behavior of the drain-source capacitance. To simulate an accurate frequency-domain behavior, it is important to include the parasitic inductance $L_{cd}$ of the drain-source capacitor $C_d$ and the parasitic capacitor $C_r$ due to the heat sink, insulating pad, and MOSFET assembly. The sum of the inductances $L_T$ and $L_r$ along with capacitance $C_r$ predicts the resonant frequency at the 22nd harmonic component or 298 MHz. The final SPICE simulation involved the calculation of component losses using the measured values of the resistances for the inductors and capacitors. The accuracy of the drain efficiency and output power simulations was of about 1% compared to the experiment. The practical circuit schematic of this high power Class-E MOSFET power amplifier is shown in Fig. 5.24 in Chapter 5.

High-voltage MOSFETs are now available from Microsemi (formerly named Advanced Power Technology) in mirror-image pairs and the heat spreader of the plastic TO-247 package is connected to the source. They operate up to supply voltage of 300 V and at frequencies up to 100 MHz. The device, which can be used for this amplifier, is ARF448A (or its more rugged version ARF460A) having a breakdown voltage of 450 V and drain junction thermal resistance of 0.55°C/W. The power gain in Class C is more than 25 dB at 27 MHz. The drain-source capacitance $C_{oss}$ is 125 pF at a supply voltage $V_{dd}$ of 125 V and the saturation resistance $R_{ds(on)}$ is 0.4 Ω. These data-sheet parameters were entered in the HEPA-PLUS Class-E design program and it generated starting design values for the Class-E load network. The circuit schematic of the 27.12-MHz 500-W MOSFET power amplifier common to most Class-E amplifiers is shown in Fig. 9.30 [10]. In Class-E amplifiers there is a capacitor shunted across the drain to source. There is none used here because the output capacitance of the device is slightly larger than the optimum value for that component required for Class E. This defines the upper frequency limit for efficient class E operation of

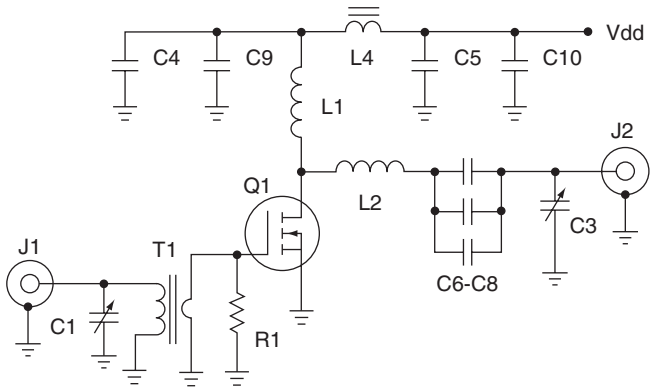



**Figure 9.30: Circuit schematic of 27.12-MHz MOSFET Class-E power amplifier [10].**

a particular device. The parasitic series resistance of 3 Ω of the lossy drain-source capacitance $C_{oss}$ is one of the primary loss mechanisms in the circuit. However, $C_{oss}$ exhibits little of the parasitic inductance. The output circuit values were adjusted slightly for maximum efficiency at an output power of 490 W.

While the designing of the output circuit is straightforward enough, it was not reduced to practice very easily. The main problem was providing enough RF voltage to the gate to drive the drain into voltage saturation. The input impedance of the gate at 27 MHz is $(0.1 - j2.7)$ Ω and the gate-source capacitance $C_{iss}$ is 1400 pF. If 10 V of peak gate drive is needed, a reasonable match between the drive source and gate is required. There is approximately 9 nH of parasitic gate inductance. This is enough inductance to make it impossible to observe with an oscilloscope the actual voltage applied to the gate. SPICE was used to model the gate-drive circuit. A SPICE macro-model for the device is shown in Fig. 9.31 [10]. The goal was to design a network to match the gate impedance sufficiently to permit sine-wave drive.

The input circuit using a 4:1 transformer and a low-pass $L$-network was designed using a Smith chart software program. To stabilize the power amplifier operation, a 25-Ω 5-W padding resistance was placed across the gate-source port representing the parallel equivalent of the capacitance 2200 pF in parallel with resistance 210 Ω. This raises the effective input impedance to $(0.38 - j2.6)$ Ω, lowers the network quality factor, and makes it much easier to match and drive properly. The input transformer is made from a two-hole ferrite ''binocular'' bead balun. The secondary winding consists of two 7/8-inch pieces of 3/16-inch diameter brass tubing connected with copper shim stock. The four-turn primary is wound inside the tubes for maximum coupling and minimum leakage which measured 19 nH referenced to the secondary side. High-quality passive components are required in the output network. Most important of these is the series inductor $L_2$. It had a quality factor of 375 and the calculated dissipation is 4.2 W, and was wound from bare copper wire, as described in Table 9.1. This coil is not

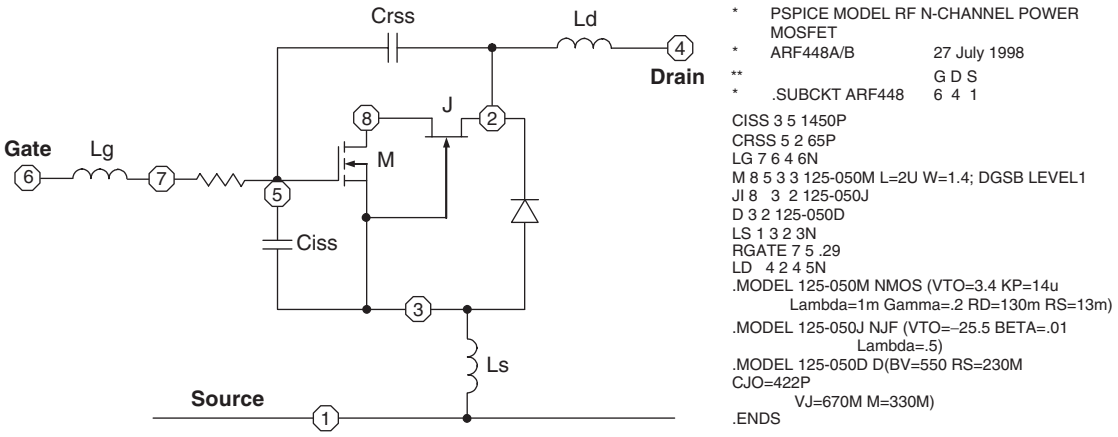



**Figure 9.31: SPICE model for ARF448 MOSFET [10].**

capable of continuous duty operation unless it is attached with high-temperature solder and/or a separate mechanical termination support is used. It was necessary to parallel three 10-nF ceramic coupling capacitors (type BX or Y5V) to carry the RF current. Table 9.1 shows the component values of a 27.12-MHz 500-W Class-E power amplifier.

A simple SPICE model of the power amplifier was compared with HEPA simulation and measured results. Overall, the agreement was good, especially between HEPA and the ideal circuit SPICE model. Attempts to insert the SPICE macro-model of the transistor into the amplifier were not successful. A much more sophisticated model is needed to adequately simulate the effects of the nonlinear capacitances of the MOSFET. However, the SPICE model was very useful for understanding the gate-drive problem mentioned earlier. HEPA assumes that the device is being driven into voltage saturation; the only input parameter it considers is input drive power used for the overall efficiency calculation. The gate drive was the biggest problem in the design because a large RF-capable power MOSFET has very small

**Table 9.1: 27.12 MHz Class-E Power Amplifier Component Values [10]**

| | |
|---|---|
| C1, C3 | 75–380 pF mica trimmer, ARCO 465 |
| C4–C8 | .01 uF 1 kV disc ceramic |
| C9, C10 | .01 uF 500 V disc ceramic |
| L1 | 6 uH. 25t #24 ga.enam. 0.5″ dia. |
| L2 | 210 nH. 4t #8 ga. .75″ id, 1″ long |
| L4 | 2t #20 PTFE on .5″ ferrite bead $\mu = 850$ |
| Q1 | APT ARF448A |
| R1 | 25 Ω 5 W non-inductive |
| T1 | Pri: 4t #20 PTFE, Sec: 1t brass tube on 2 hole balun bead Fair-Rite #2843010302 $\mu = 850$ |

input impedance. One of the best tests for reliability of an amplifier is mismatch load testing. The ARF448 has about 175 watts of available dissipation in the test amplifier with its air-cooled heat sink. The performance at eight points around a 2:1 *VSWR* mismatch circle was calculated using HEPA. It was found that there is a region with the high inductive impedance that should be avoided. Without protection, the output power soared to 750 W and the drain current was almost twice normal. The efficiency stayed quite constant, never losing more than 11% at any load angle. The measured gate and drain voltage waveforms are shown in Fig. 9.32. The peak drain voltage measures 430 V. The highest efficiency of 83% was measured at 490 W, which is 5.5% below the simulated due to the lossy nonlinear drain-source capacitance and longer switching time.

Fig. 9.33 shows the PSPICE model describing the transistor switched-mode operation with the output voltage-dependent capacitance [11]. The five basic elements are included in this model: ideal switch SW, transistor on-resistance $R_{on}$ which normally can be found from data sheet, saturation offset voltage $V_o$ which is equal to zero for FET devices, nonlinear equivalent for the output capacitance ($C_X$ in series to $E_X$), and equivalent series resistance $R_{Co}$ due to lossy output capacitance.

To implement the nonlinear voltage dependence of the output capacitance (the SPICE standard capacitor supports only linear capacitance), its nonlinear behavior can be represented by the junction-voltage dependence in the form of

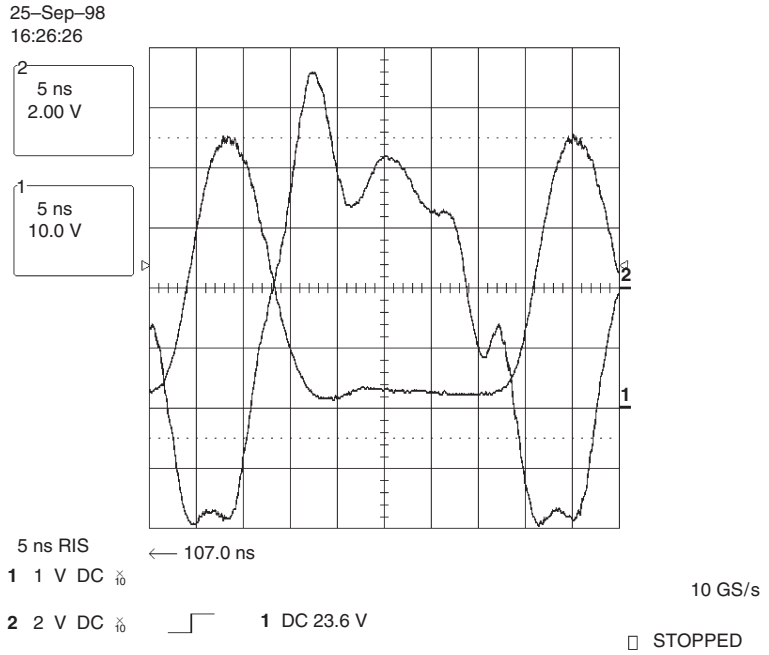
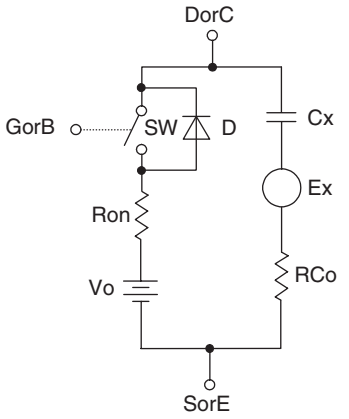



**Figure 9.32: Measured gate and drain voltage waveforms [10].**




```
.SUBCKT T_MODEL  DorC  GorB  SorE
       + PARAMS: Co=1pF  phi=0.6V  n=0.5  Ron=0.5
       + RCo=3  Vo=0
.MODEL  ONOFF  VSWITCH  (RON=0.01)
       + ROFF=1e8  VON=4  VOFF=0)
.MODEL        Dmode  D( )
Sw     DorC  E  GorB  SorE  ONOFF
Dsw    E              DorC     Dmodel
Ron    E              K        {Ron}
Vo     K              SorE     {Vo}
Cx     DorC           H        {phi*Co/(1-n)}
Ex     H      J       VALUE={V(DorC,SorE)-
       +PWRS((1+V(DorC,SorE)/phi),(1-n))}
RCo    J      SorE                {RCo}
.ENDS
```

**Figure 9.33: PSPICE model of switching-mode transistor [11].**

$$C(v) = \frac{C_0}{\left(1 + \frac{v}{\phi}\right)^n} \tag{9.1}$$

where $C_0$ is the capacitance for $v = 0$ and $n$ is the junction profile coefficient. During optimization procedure, the parameters $C_0$, $n$ and $\phi$ are considered as the fitting parameters that can be extracted from the data-sheet curve for the MOSFET output capacitance $C_{\text{oss}}$.

The nonlinear voltage dependence can be modeled with a fixed capacitor $C_{\text{X}}$ and a series voltage-controlled voltage source $E_{\text{X}}$, which can be found from the expression for the total voltage $v$ given by

$$v = v_{\text{C}} + E_{\text{X}}(v) \tag{9.2}$$

where $v_{\text{C}}$ is the voltage across the capacitor $C_{\text{X}}$ and $E_{\text{X}}$ is defined as

$$E_{\text{X}}(v) = v - \left(1 + \frac{v}{\phi}\right)^{(1-n)}. \tag{9.3}$$

By differentiating both parts of Eq. (9.2) and taking into account that $i/\text{C} = dv/dt$ and $i/C_{\text{X}} = dv_{\text{C}}/dt$, the fixed capacitor can be determined using Eq. (9.1) as

$$C_{\text{X}} = C_0 \frac{\phi}{1 - n}. \tag{9.4}$$

The model parameters $R_{\text{on}}$ and $R_{\text{Co}}$ can be measured or estimated from the device data sheet. The sub-circuit shown in Fig. 9.33 must be connected to nodes DorC (drain or collector), SorE (source or emitter), and GorB (gate or base). A VSWITCH element should be used for the ideal switch SW, with two resistance values (low and high) following the control voltage applied to the gate terminal. If this voltage is equal or greater than VON (default value 4 V), the switch turns on to low resistance RON (default value 0.01 Ω). Otherwise, the switch turns off to a high resistance ROFF (default value 1E8 Ω). The diode DSW (D in the circuit diagram of Fig. 9.33)

parameters can be adjusted through its .MODEL description. The parameters $C_0$, $n$, $\phi$, $R_{C0}$, and $R_{on}$ can be more accurately modeled using the optimization procedure based on a discrete-time technique for the steady-state analysis of the nonlinear switched circuits with inconsistent initial conditions [12]. Using NGSPICE which is a latest version of Berkeley SPICE, the optimization procedure for the entire Class-E power amplifier (including input circuit), based on the time-domain shooting method for finding the steady-state responses, can be fully implemented [13].

## 9.7 ADS Circuit Simulator and Its Applicability to Switched-Mode Class E

The Agilent Advanced Design System (ADS) circuit simulator is a comprehensive simulator of linear and nonlinear circuits in the frequency and time domains. It can be used directly to model and simulate the performance of the switched-mode Class-E power amplifiers. This can be done using both the transient and harmonic-balance simulation engines.

Fig. 9.34 shows the simulation setup for ideal parallel-circuit Class-E operation in the time domain. The active device is represented by a voltage-controlled switch with off-resistance of 1 MΩ and small finite on-resistance, the value of which can generally be varied. The input source represents a voltage source with pulse train defined at discrete time steps used in envelope and transient simulators. The use of discrete time pulse source, as opposed to a standard pulse source, can guarantee that there is no timing jitter in the pulse edge due to the waveform being sampled asynchronously by a fixed-time interval simulation. The simulation time is significantly faster than the period of a square wave.

To provide the circuit simulation in the time domain, the transient simulator is added to the simulation template. The stop time of 20 sec is chosen for a normalized frequency of 1 Hz; that is sufficient to reach a steady-state mode for a simulated operating frequency normalized to unity, as shown on the example of the waveforms of the switch voltage and load current shown in Fig. 9.35(*a*) and Fig. 9.35(*b*), respectively. The inductors and capacitors are lossless and the loaded quality factor $Q_L$ of the series resonant circuit is chosen to be as high as 20. The measure equations MeasEqn include the conditions when the switch voltage V_sw and its voltage derivative V_sw_der must take zero values at the instant just before the switch is turned on. The efficiency is calculated in the 19th+20th period since the products of instantaneous current and voltage are integrated over these two periods and divided by two. The function ''integrate'' automatically deals with the non-constant time steps in the transient simulation results. The term ''switch_index'' is the number (index) of the simulation points for 19 seconds, the instant when the switch is turned on, while the term ''switch_index-1'' is therefore the simulation point just before the switch is turned on.

After the transient simulation has settled to a steady-state mode, the simulation results for the optimum parallel-circuit Class-E load network parameters calculated from Eqs. (6.79) to (6.81) in Chapter 6 demonstrate the ideal Class-E voltage and current waveforms. The optimization

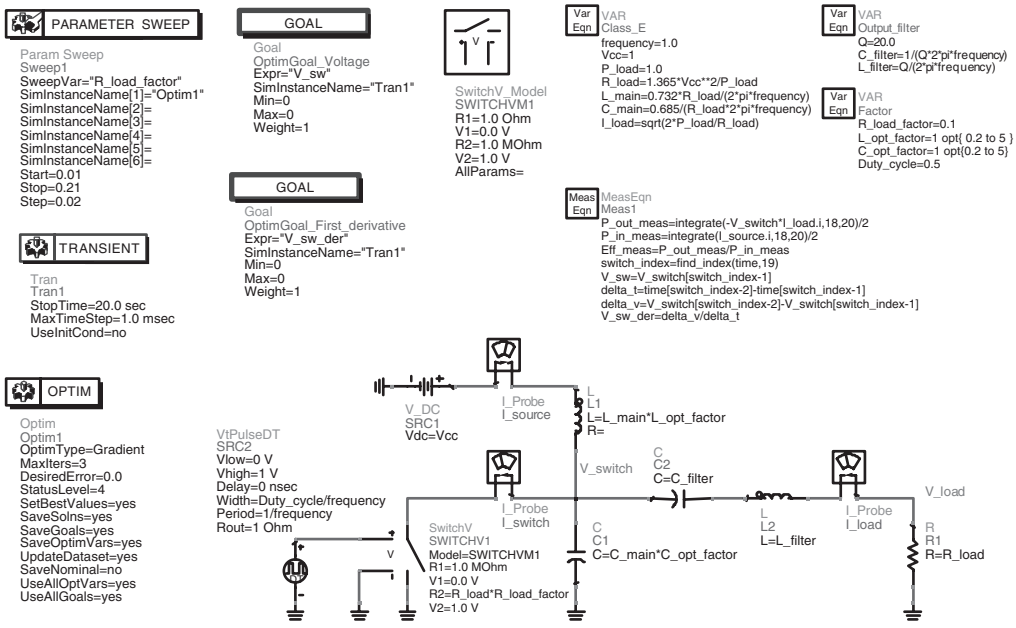



**Figure 9.34: Simulation setup to maintain Class-E mode in time domain.**

simulator added to the simulation template shown in Fig. 9.34 is necessary to optimize the load-network parameters by varying their factors for a non-ideal switch with finite on-resistance. The optimization is performed to minimize the switch voltage and voltage derivative values to zero.

Figs. 9.36 (*a*) and (*b*) shows a set of the switch voltage and current waveforms obtained for zero voltage and voltage derivative conditions by sweeping the switch resistance load factor from 0.01 to 0.21 with steps of 0.02. The total simulation time for a 1.6 GHz processor is 1.2 hours. (Making the same computation with HEPA-PLUS [see last paragraph on p. 383], would take about 8 seconds of computing time plus about 10 seconds to manually change the resistance value nine times, faster than 1.2 hours by a factor of 4320 seconds/18 seconds = 240:1, running on a Pentium III/667 MHz [processor slower than 1.6 GHz by a factor of 1.6 GHz/667 MHz = 2.4:1]. The overall speed advantage of HEPA-PLUS over ADS is approximately 240:1 $\times$ 2.4:1 = 576.1 overall. Of course, ADS is a general-purpose program that can simulate and optimize anything, and it can do many things that HEPA-PLUS cannot do.) In this case, the peak voltage and current values are the smallest for maximum values of the switch on-resistance, and the saturation voltage becomes significant resulting in a lower output power and efficiency. The output power and efficiency drop by approximately 45% and 39% respectively, when a ratio $r_{\text{sat}}/R$ reaches the value of 0.15, as shown in Fig. 9.37(*a*). This is achieved for an increased capacitance by 29% and a reduced inductance by 29%, as shown in Fig. 9.37(*b*). When $r_{\text{sat}}/R = 0.1$, the efficiency is equal to 73.4%.

However, the Class-E zero voltage and zero voltage derivative conditions become non-optimum for finite values of the on-resistance. This means that higher efficiency can be achieved when these Class-E conditions are non-zero. Consequently, some voltage is present at

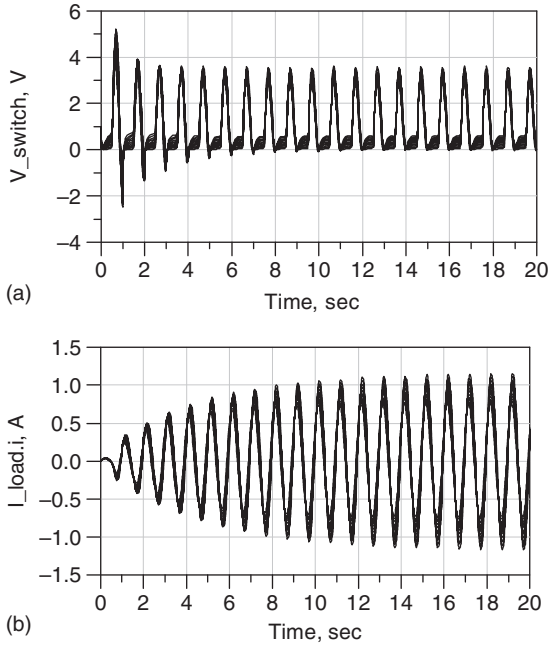



**Figure 9.35: Transient response of switch voltage and load current.**

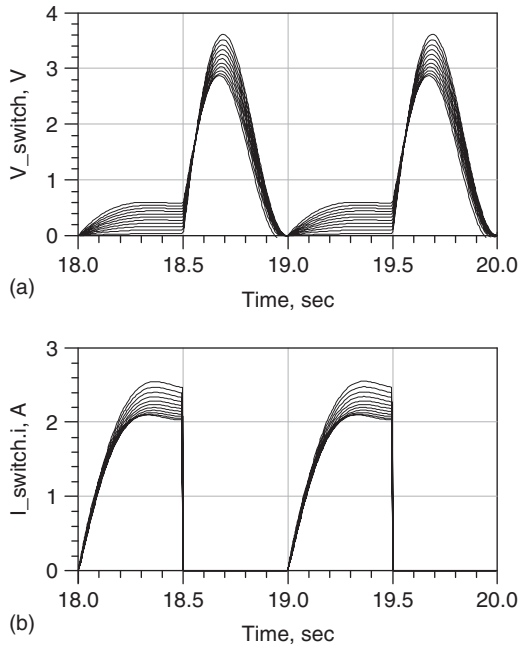



**Figure 9.36: Parallel-circuit Class-E nominal waveforms with finite on-resistance.**

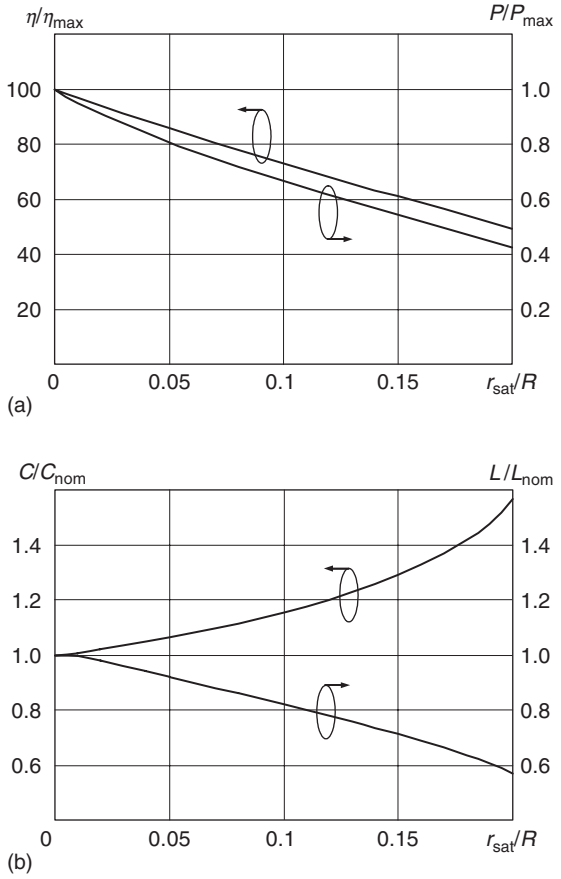



**Figure 9.37: Optimum parameters versus on-resistance.**

the capacitor before the switch is turned on. By maintaining the switch transient time to almost zero and the optimum parameters of the load network, one can observe the discharge of this voltage in the shape of a current spike. Figs. 9.38(*a*) and (*b*) shows the switch voltage and current waveforms as a function of the normalized switch saturation resistance $r_{\text{sat}}/R_{\text{L}}$ varying from 0.05 to 0.3 with steps of 0.05. Here, higher spikes correspond to lower values of $r_{\text{sat}}/R_{\text{L}}$, and then decreases with larger values of $r_{\text{sat}}/R_{\text{L}}$. As a result, for $r_{\text{sat}}/R = 0.1$, the efficiency is equal to 75.7%, which is 2.3% greater than in a nominal case; for $r_{\text{sat}}/R = 0.15$, the efficiency is equal to 67.2%, which is 6.2% greater than in a nominal case. This means that, for the normalized saturation resistance $r_{\text{sat}}/R$ equal or smaller than 0.1, it makes sense to use the nominal values of a parallel-circuit Class-E load network, since it will simplify significantly the entire design procedure (no need for optimization) and the efficiency will be close to the theoretically achievable maximum.

Fig. 9.39 shows the simulation setup for ideal parallel-circuit Class-E operation in the frequency domain. Using the frequency domain enables the overall simulation procedure to be much faster

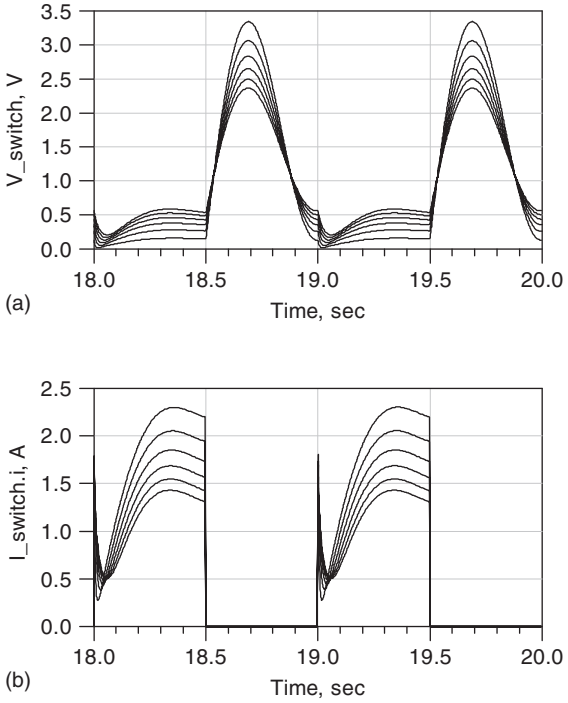



**Figure 9.38: Parallel-circuit Class-E waveforms with finite on-resistance.**

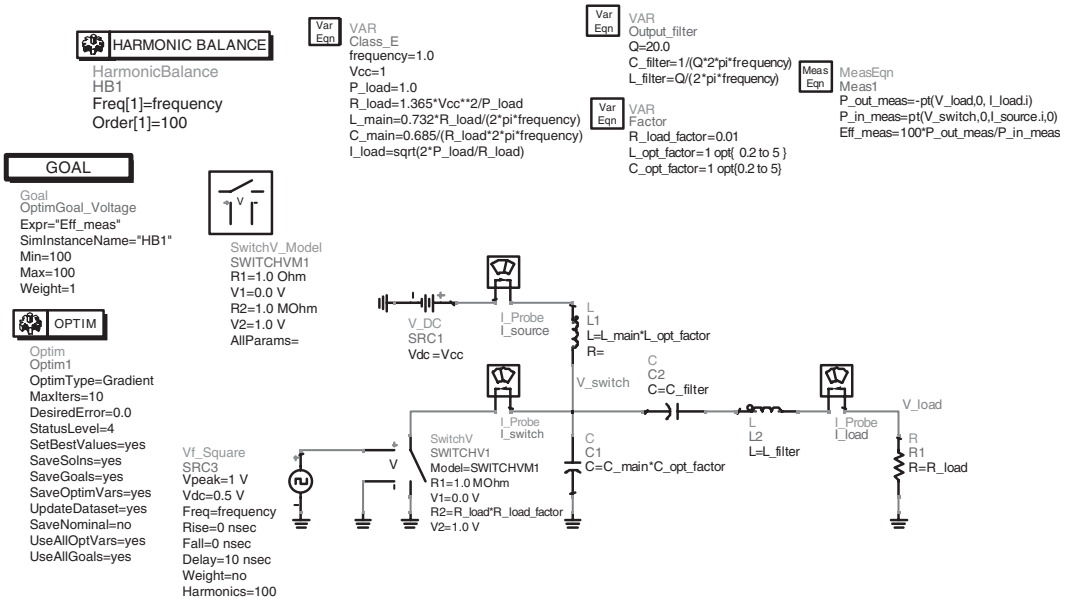



**Figure 9.39: Simulation setup to maintain Class-E mode in frequency domain.**

than that in time domain and can take a few seconds. However, because the number of harmonic components is not infinite, the simulation waveforms and numerical results for the optimum load network parameters are not so accurate. In this case, the input source is changed and represents a voltage source with Fourier-series expansion of periodic square wave used in a harmonic-balance simulator. The harmonic order is chosen to 100. The optimization procedure can be applied with respect to the efficiency as an optimization parameter. Since the simulation time is very short, the number of iterations can be increased significantly for more accuracy. Figs. 9.40(*a*) and (*b*) shows the switch voltage and current waveforms obtained for the nominal parameters of the parallel-circuit Class-E load network. Unlike the time-domain simulations, there are smoother transitions between the positions when switch is turned on and switch is turned off. Nevertheless, for $r_{sat}/R = 0.01$, the efficiency is equal to 96.9%, which is only about 0.1% smaller than that using time-domain simulation.

## 9.8 ADS CAD Design Example: High-Efficiency Two-Stage L-Band HBT Power Amplifier

Since the ADS harmonic-balance circuit simulator gives a real possibility to accurately describe the nonlinear circuit behavior in the frequency domain, including active device and passive circuits, it can be very useful to simulate the entire high-efficiency power

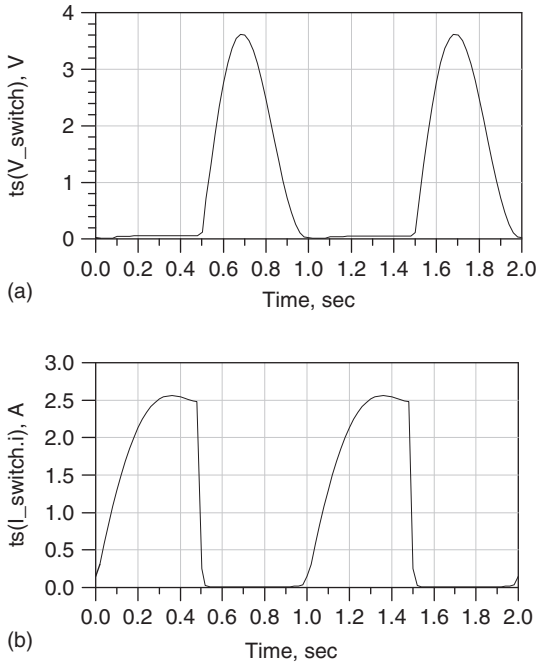



**Figure 9.40: Parallel-circuit Class-E optimum switch waveforms.**

amplifier in a switched-mode approximation as well. Generally, the high-efficiency power-amplifier design procedure can include the following several basic steps:

- The proper selection of the active device, accurate measurements of its small-signal *S*-parameters under different bias conditions in a wide frequency range, transformation of the *S*-parameters to the impedance *Z*- and admittance *Y*-parameters to describe the device electrical behavior through the nonlinear model in the form of its equivalent circuit with generally nonlinear parameters.

- The analytical calculation of the optimum parameters of the proper load network in a high-efficiency mode for given output power, supply voltage, and device output capacitance to provide the maximum collector efficiency and required harmonic suppression.

- The choice of a proper bias circuit to optimize the quiescent current and minimize the reference current and variations over temperature for maximum power gain and power-added efficiency.

- The design of the input and interstage matching circuits to provide the minimum input return loss, maximum power gain and power-added efficiency- and stable, operating conditions.

- The final circuit parameter optimization to maximize power-added efficiency.

As an example, our design objective is to design a high-efficiency monolithic Class-E bipolar power amplifier operating at 1.75 GHz with an output fundamental-frequency power $P_{out} = 33\,\text{dBm}$, power gain $G_p = 27\,\text{dB}$ and supply voltage $V_{cc} = 5\text{V}$. To satisfy these requirements, our decision is to choose a two-stage topology and HBT devices with the minimum saturation voltage at low supply voltage and the transition frequency $f_T > 25\,\text{GHz}$. Fig. 9.41 shows the nonlinear equivalent circuit of the HBT transistor with the circuit parameters corresponding to the device emitter area A-90 $(3 \times 30)\ \mu\text{m}^2$. The most nonlinear parameters as $R_{be}$ and $C_{be}$ representing the input diode forward-biased junction can be found by *S*-parameter simulation as a result of the *S*-parameter transformation to the input impedance $Z_{in}$ or input admittance $Y_{in}$. Since, in a high-efficiency mode, the voltage swing is very high, the junction collector capacitance $C_{bc}$ can be chosen at some middle bias point, between the base and collector dc voltages. In our case, $C_{bc} = 4.25\text{e-}14^{*}\text{A}$.

Ideally, in switched-mode operation, the active device should act as an ideal switch, driven to be turned on or off by the input RF signal. Assuming the collector efficiency of the second-stage transistor of 80%, the dc power is equal to $P_0 = 2\,\text{W}/0.8 = 2.5\,\text{W}$ with the dc supply current $I_0 = P_0/V_{cc} = 2.5\,\text{W}/5\ \text{V} = 500\,\text{mA}$. Since, for an HBT device selected, the recommended dc current density for reliable operation over a wide temperature range should

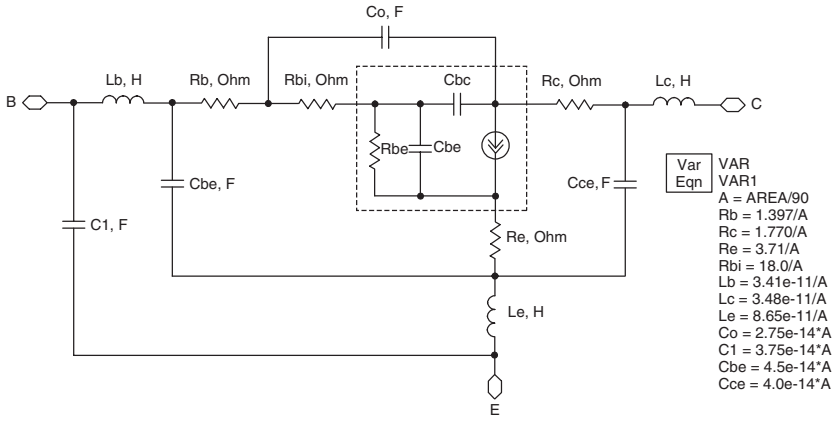



**Figure 9.41: Small-signal high-frequency HBT equivalent circuit.**

not exceed 15 mA per 90 $\mu$m$^2$, the overall emitter area was chosen with some margin to be equal to 5400 $\mu$m$^2$. The dc output characteristics $I_{ce}(V_{ce})$ (amperes and volts) of such an HBT transistor for different base bias voltage $V_{be}$ varying from 1.2 to 1.5 V are shown in Fig. 9.42. In this case, the peak collector current for a parallel-circuit Class-E mode according to Eq. (6.84) given in Chapter 6 is equal to $I_{max} = 2.647I_0 = 2.15$ A. The idealized Class-E load line (with instant transition between pinch-off and saturation regions) is shown as a heavy line in two sections: horizontal at zero current at the bottom of the figure (transistor pinched-off), and slanted upwards to the right at the left end of the figure (transistor conducting current). It can be seen that the operating point moves along the horizontal $V_{ce}$ axis (pinch-off region) and then along the collector current saturated line (voltage-saturation region) until $I_{ce} = 2.15$ A. At this final point, the saturation voltage can be found as equal to $V_{sat} = 0.3$ V. This means that the power loss due to the finite device saturation resistance can be calculated as $P_{sat} = I_0 V_{sat} = 150\,\text{mW}$ with degradation in the collector efficiency of $(1 - P_{sat}/P_0) = 0.06$ or 6%.

First, we shall design the second stage for a maximum collector efficiency with some intermediate value of the source resistance much less than 50 $\Omega$. The optimum parameters of a

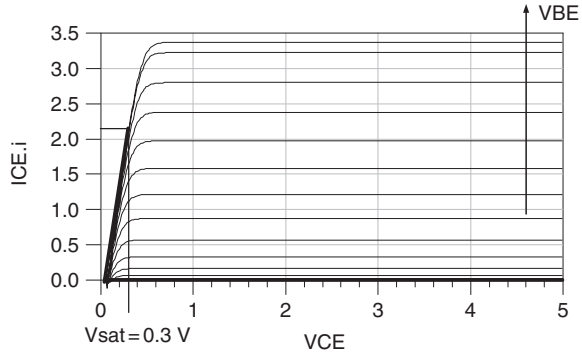



**Figure 9.42: Device output current-voltage characteristics and load line.**

parallel-circuit Class-E load network can be calculated using Eqs. (6.79) to (6.81) given in Chapter 6, taking into account the saturation voltage $V_{sat}$ as

$$R = 1.365\frac{(V_{cc} - V_{sat})^2}{P_{out}} = 15\,\Omega$$

$$L = 0.732\frac{R}{\omega} = 1.0\,\text{nH}$$

$$C = \frac{0.685}{\omega R} = 3.9\,\text{pF}.$$

It should be noted that, in view of a saturation voltage, the calculated parameters of the Class-E load network generally cannot be considered optimum unlike the ideal case of zero saturation voltage. However, they can be considered as a sufficiently accurate initial guess for final design and optimization when efficiency is sufficiently high. In addition, the collector capacitance can be larger than required, especially at higher frequencies and for the transistor with large emitter area required for high output power. In our case, the total output capacitance can be estimated as $C_{out} = C_{ce} + C_0 + C_{bc} = 6.6\,\text{pF}$ for emitter area of $5400\,\mu\text{m}^2$, which is 1.5 times greater than required for optimum parallel-circuit Class-E mode. The excessive output capacitance of $(6.6 - 3.9) = 2.7$ pF is responsible for additional switching losses which occur during the transitions from the saturation to pinch-off modes of the device operation. To compensate for this capacitance at the fundamental frequency, it is necessary to connect the inductance in parallel, which value is equal to 3 nH. Hence, the parallel connection of the two inductors with values of 1 nH and 3 nH results in a final value of $(1 \times 3)/(1 + 3) = 0.75$ nH.

Assuming the quality factor of the series filter of $Q_L = 10$, the series capacitance $C_0$ and inductance $L_0$ are calculated as

$$C_0 = \frac{1}{\omega R Q_L} = 0.6\,\text{pF}$$

$$L_0 = \frac{1}{\omega^2 C_0} = 13.8\,\text{nH}.$$

Since the input-device impedance is sufficiently low, the intermediate source resistance is chosen to be equal to $5\,\Omega$. In this case, it will be enough to use only one input-matching section. The input-matching circuit is composed in the form of a high-pass L-type section with a shunt inductor and a series capacitor. The parameters of this matching circuit can be simulated in a large-signal mode to minimize input return loss as a criterion by using Smith chart tuning procedure.

Fig. 9.43 shows the simulation setup of the second power-amplifier stage designed to operate in a parallel-circuit Class-E mode. To simulate the electrical characteristics and waveforms, the corresponding current probes and voltage wire labels are incorporated into the circuit. As a current controlled device, the bipolar transistor requires the dc base driving current, the value of which depends on the output power and device parameters. Because technologically the bipolar device represents a parallel connection of the basic cells, the important issue is to use the ballasting series resistors to avoid the current imbalance and possible device collapse at higher current density levels. Generally, different types of the current-mirror bias circuits can be used effectively to bias a transistor. In our case, the emitter-follower bias circuit that provides the temperature compensation and minimizes the reference current is used [14]. It is very important to provide the proper ratio between the ballasting resistors $R_{34}$ and $R_{33}$, equal to the ratio of the corresponding device areas equal to $5400/270 = 20$. The emitter follower bias circuit normally requires only several tens of microamperes of reference current.

Fig. 9.44 shows the measurement equations required to plot the small- and large-signal power-amplifier characteristics. The small-signal frequency dependence of the stability factor $K$ is shown in Fig. 9.45($a$) demonstrating the stable conditions over the entire frequency range with $K > 1$. However, it is not enough to just simulate the small-signal performance. It is important also to verify the potential instability that can occur in the form of injection-locking

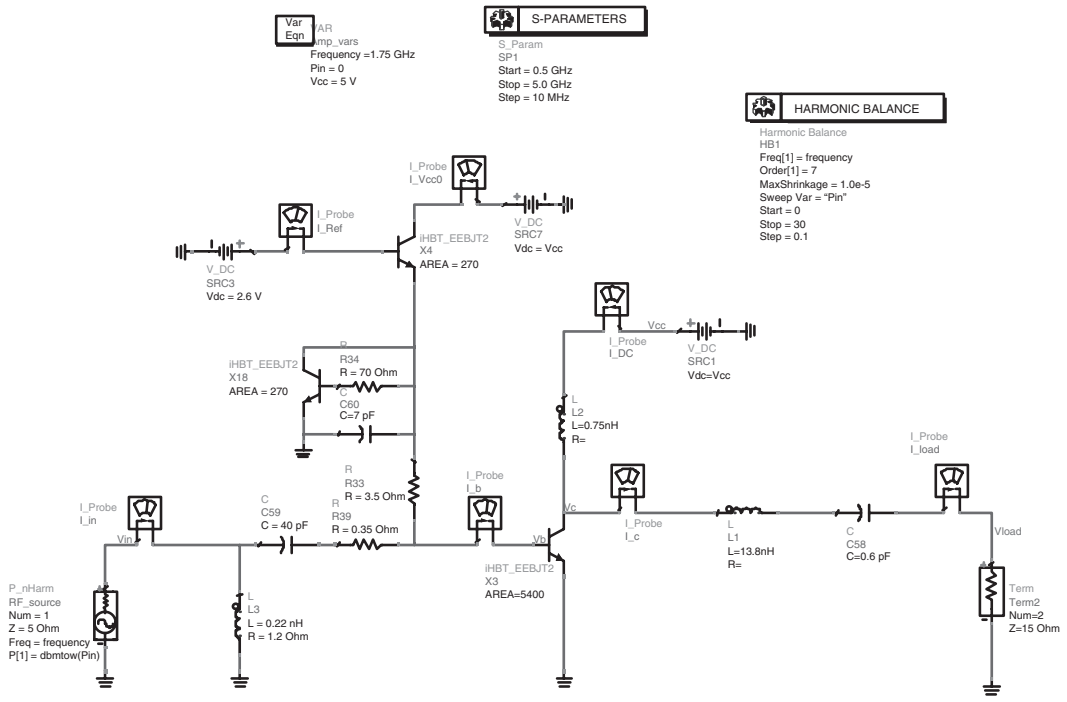



**Figure 9.43: Simulation setup for Class-E second stage.**

```
Eqn P_DC=Vcc[0]*(I_Ref.i[::,0]+I_Vcc0.i[::,0]+I_DC.i[::,0])
Eqn Pload_W=mag(Vload[::,1])*mag(I_load.i[::,1])/2
Eqn Pload_dBm=10*log(Pload_W)+30
Eqn Efficiency=100*Pload_W/(Vcc[0]*I_DC.i[::,0])
Eqn Gain=Pload_dBm-Pin
Eqn K=stab_fact(S)
Eqn Pin_W=mag(Vin[::,1])*mag(I_in.i[::,1])/2
Eqn PAE=100*(Pload_W-Pin_W)/P_DC
```

**Figure 9.44: Measurement equations.**

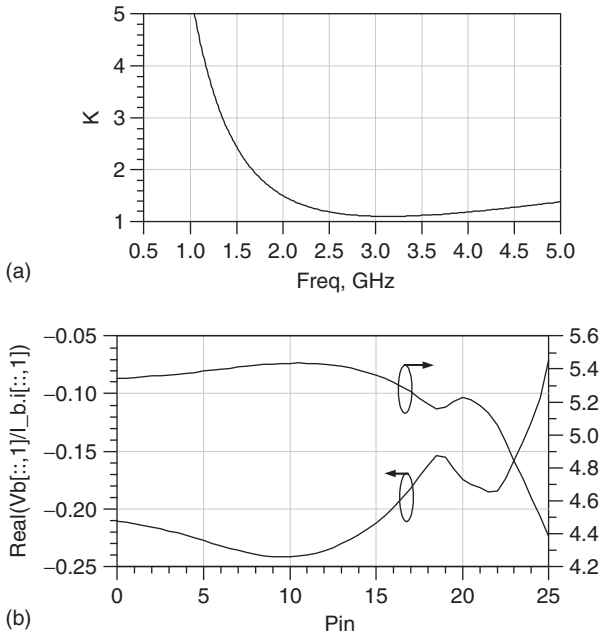



**Figure 9.45: Input impedance and stability.**

effect at large-signal mode near the operating frequency. The dependencies of the real parts of the device impedance at the base and the input impedance seen by the source are shown in Fig. 9.45(*b*). It is seen that the real part of the base impedance is slightly negative. In order to compensate for this negative resistance, it is necessary to connect the resistance of 0.35 Ω in series to the base compromising the stable operation and sufficient power gain. The real part of the input impedance seen by the source is close to the required 5 Ω at nominal large-signal operation.

As a result, the second power-amplifier stage exhibits a linear power gain of about 13 dB and saturated output power of 33.1 dBm, which dependencies are shown in Fig. 9.46(*a*), with a

maximum collector efficiency of 85.3% and a maximum power-added efficiency of 60.5%, which dependencies are shown in Fig. 9.46(*b*). It is seen that the collector-efficiency improvement is achieved at the expense of the significant power-gain reduction. However, the maximum power-added efficiency occurs when the power gain is reduced by about 3 dB, which is a result of the contribution of the driving power.

Fig. 9.47 shows the collector and base voltage waveform corresponding to a Class-E approximation. The collector voltage waveform with a peak factor of about 18/5 = 3.6 was achieved for a maximum collector efficiency with the base voltage waveform having

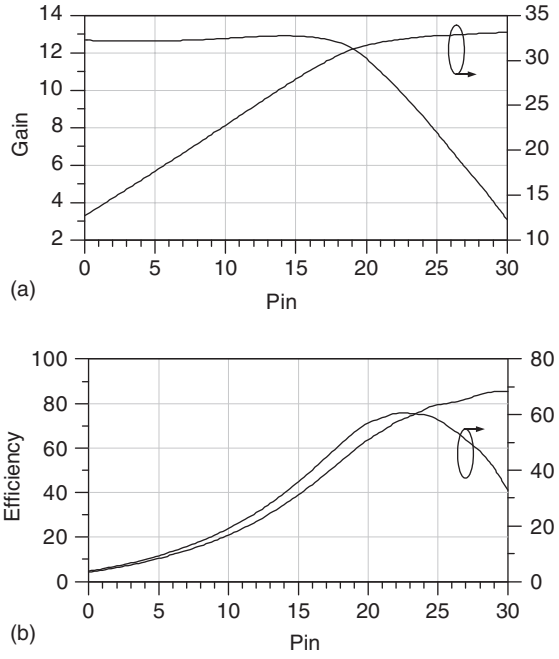



**Figure 9.46: Power gain, output power, and efficiency.**

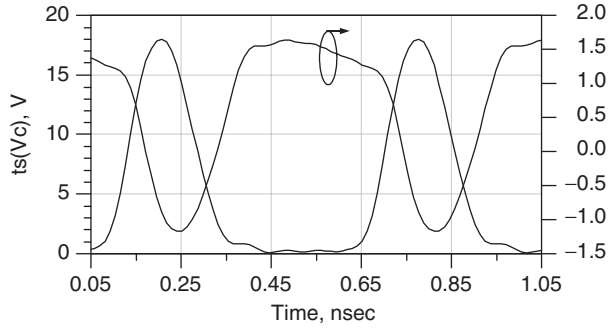



**Figure 9.47: Collector and base voltage waveforms.**

a flattened top part and causing the device to operate in a switching mode with minimum switching loss.

To match the Class-E load resistance $R = 15\,\Omega$ with a standard load resistance $R_{\mathrm{L}} = 50\,\Omega$, it is necessary to use a matching circuit with the series inductor as a first element to provide high impedance at the harmonics. Since the ratio of impedances is not so high, we can use the low-pass L-type matching section with design equations given by Eqs. (5.40) to (5.42) in Chapter 5. As a result,

$$Q_{\mathrm{L}} = \sqrt{\frac{50}{15} - 1} \cong 1.5$$

$$L = \frac{Q_{\mathrm{L}} R}{\omega} = 2.1\,\mathrm{nH}$$

$$C = \frac{Q_{\mathrm{L}}}{\omega R} = 2.9\,\mathrm{pF}.$$

Fig. 9.48 shows the simulation setup of the Class-E second stage with output-matching circuit. Since the loaded quality factor $Q_{\mathrm{L}}$ is sufficiently small, the conditions at the fundamental-frequency and harmonic components will be slightly different compared to the ideal case.

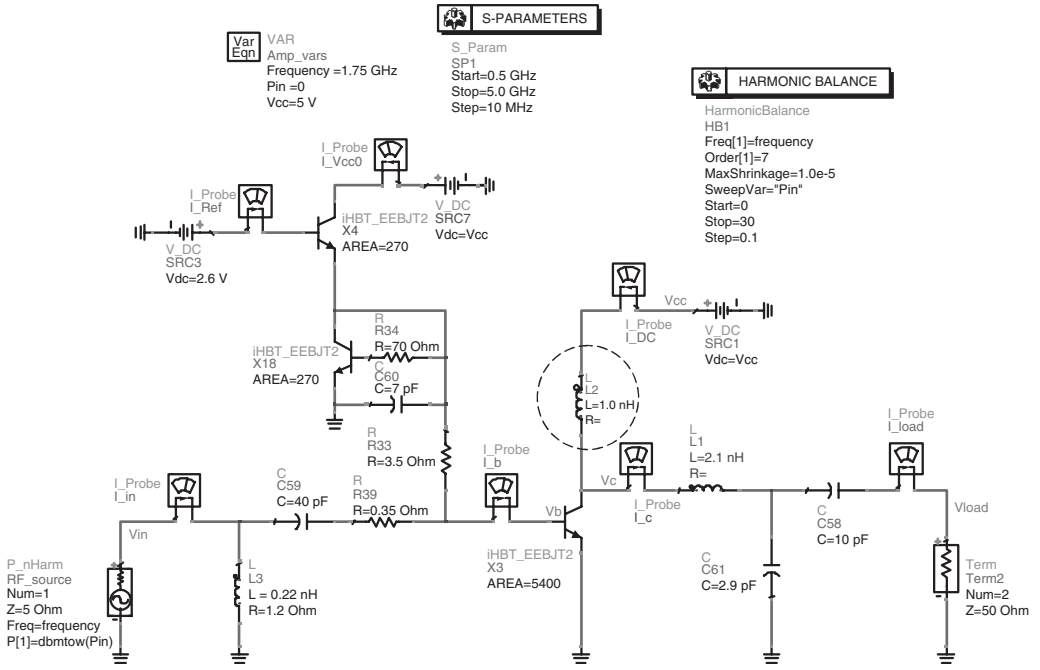



**Figure 9.48: Simulation setup for Class-E second stage with output-matching circuit.**

In this case, the easiest way to maximize collector efficiency is to tune manually the parameters of the basic elements like the parallel inductor. The maximum collector efficiency of 84.8% and power gain of about 13 dB were achieved, as shown in Fig. 9.49, by tuning the value of the parallel inductor from 0.75 nH to 1.0 nH. This inductor is shown in Fig. 9.48 inside the dashed circle. However, a single low-pass matching section can provide a second-harmonic suppression of about 20 dB. Consequently, to improve the spectral performance, it is necessary to use two or more low-pass sections in succession, better with equal quality factors, to provide a wider frequency bandwidth [15].

Fig. 9.50 shows the simulation setup of the first power-amplifier stage designed to operate in a Class-AB mode. Since it is sufficient to provide an output power from the first stage of not more than 200 mW, the device emitter area size was chosen to be $720\,\mu\text{m}^2$ and the output resistance is assumed to be $50\,\Omega$, which is close to the calculated value of $R_{\text{out}} = (V_{\text{cc}} - V_{\text{sat}})^2/2P_{\text{out}} = (4.7 \times 4.7)/0.4 = 55.2\,\Omega$. Then, to conjugately match the intermediate load resistance of $5\,\Omega$ with the chosen output resistance $R_{\text{out}} = 50\,\Omega$, it is convenient to use a high-pass L-type matching section with the shunt inductor as a first element followed by the series capacitor. In this case, the shunt inductor with a bypassing capacitor at its end in practical implementation also can serve as a dc power supply path. The parameters of the output-matching circuit are calculated as

$$Q_{\text{L}} = \sqrt{\frac{50}{5} - 1} = 3$$

$$L = \frac{R_{\text{out}}}{Q_{\text{L}}\omega} = 1.5\,\text{nH}$$

$$C = \frac{1}{5Q_{\text{L}}\omega} = 6.1\,\text{pF}.$$

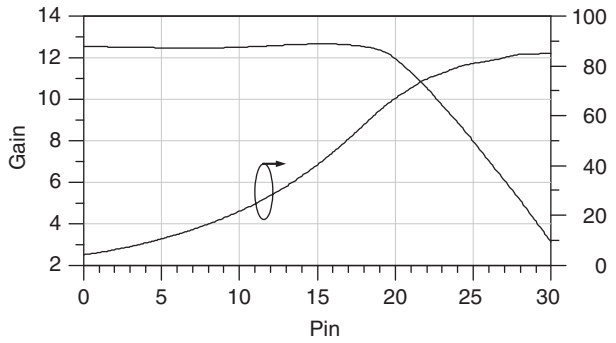



**Figure 9.49: Power gain and collector efficiency.**

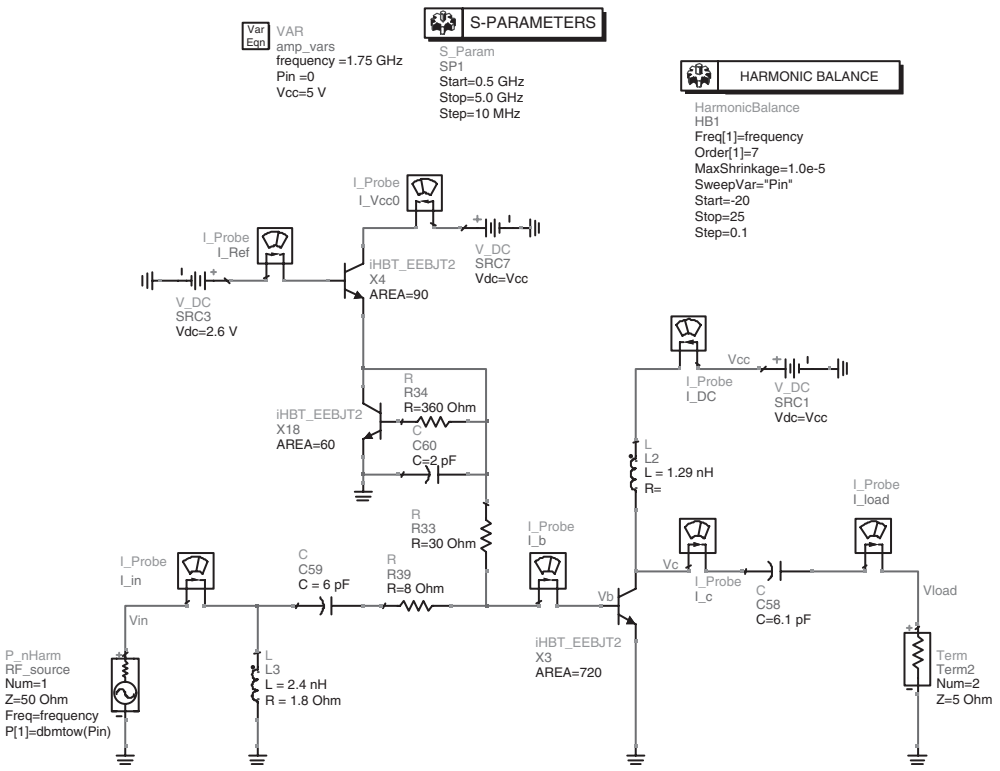



**Figure 9.50: Simulation setup for Class-AB first stage.**

To obtain a final value of the shunt inductor, it is necessary to take into account the device collector capacitance. In our case, the total output capacitance can be estimated as $C_{\text{out}} = 6.6/7.5 = 0.88\,\text{pF}$ for emitter area of $720\,\mu\text{m}^2$. To compensate for this capacitance at the fundamental frequency, it is necessary to connect the inductance of 9.4 pF in parallel. Hence, the parallel connection of the two inductors with values of 9.4 nH and 1.5 nH results in a final value of 1.29 nH. The input matching circuit is composed in the form of a high-pass L-type section, the parameters of which elements can be simulated in a large-signal mode to minimize input return loss as a criterion by using Smith chart tuning procedure. To improve stability factor and simplify the input matching, the resistance of $8\,\Omega$, connected in series to the transistor base terminal, was included.

The small-signal frequency dependence of the stability factor $K$ and $S_{11}$ are shown in Fig. 9.51($a$) demonstrating the stable conditions over entire frequency range with $K > 1$ and input return loss better than 20 dB at the operating frequency. Under large-signal operation, the first power-amplifier stage exhibits a linear power gain of about 15 dB and a maximum collector efficiency of about 72%, the dependencies of which on the input power are shown in Fig. 9.51($b$). It is seen that the collector efficiency improvement is achieved at the expense of

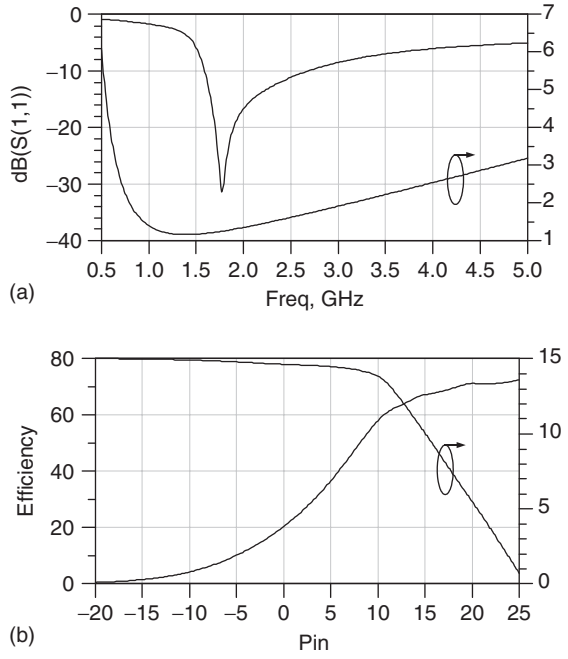



**Figure 9.51: Electrical performance of first power-amplifier stage.**

the significant power gain reduction. However, the sufficiently high efficiency of about 65% can be achieved at 3-dB compression point when the power gain is reduced by 3 dB from its linear value.

The next step is to combine the first power-amplifier stage with the load impedance of 5 Ω and the second power-amplifier stage with the source impedance of 5 Ω in a two-stage power amplifier. Fig. 9.52 shows the simulation setup of the two-stage Class-E power amplifier with lumped elements. The main attention should be paid to the interstage matching circuit consisting of the two high-pass matching sections since the impedances are not exactly the same, having also some certain values at the harmonics. In this case, it is necessary to provide some tuning of the elements around their initial values shown in a dashed circle. It can be done sufficiently fast even with manual tuning.

Fig. 9.53 shows the measurement equations required to plot the small- and large-signal power-amplifier characteristics including all dc power sources. The small-signal frequency dependences of the stability factor $K$ and $S_{11}$ are shown in Fig. 9.54($a$) demonstrating the stable conditions over entire frequency range with $K > 2$ and input return loss better than 12 dB at the operating frequency. Under large-signal operation, the two-stage parallel-circuit Class-E power amplifier exhibits a linear power gain of more than 29 dB and a maximum power-added efficiency of about 68%, the dependencies of which on the input power are

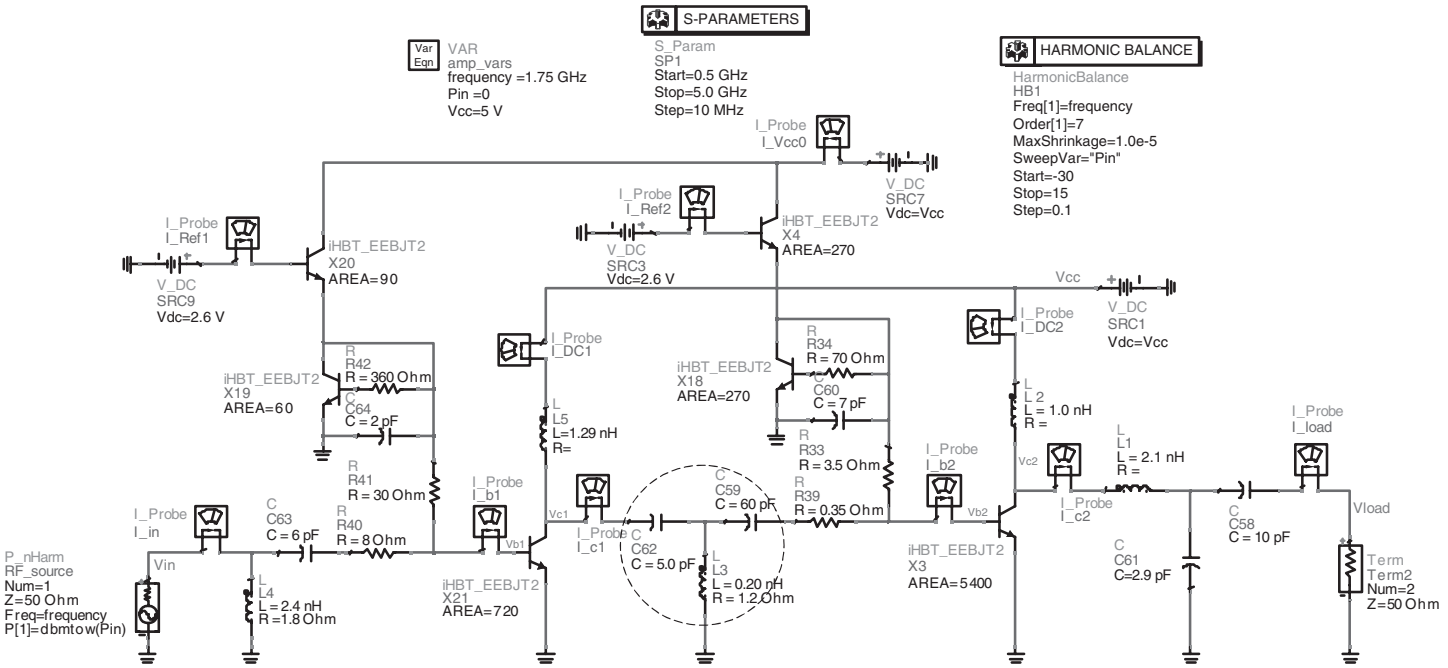



**Figure 9.52: Simulation setup for two-stage Class-E power amplifier with lumped elements.**

```
Eqn Pin_W=mag(Vin[::,1])*mag(I_in.i[::,1])/2
Eqn Pload_W=mag(Vload[::,1])*mag(I_load.i[::,1])/2
Eqn Pload_dBm=10*log(Pload_W)+30
Eqn Efficiency=100*Pload_W/(Vcc[0]*I_DC2.i[::,0])
Eqn Gain=Pload_dBm-Pin
Eqn K=stab_fact(S)
Eqn I_DC=I_Ref+I_Vcc0.i[::,0]+I_DC1.i[::,0]+I_DC2.i[::,0]
Eqn PAE=100*(Pload_W-Pin_W)/(Vcc[0]*I_DC)
Eqn I_Ref=I_Ref1.i[::,0]+I_Ref2.i[::,0]
```

**Figure 9.53: Measurement equations.**

shown in Fig. 9.54(*b*). The sufficiently high efficiency of about 57.5% can be achieved at 1-dB compression point when the power gain is reduced by 1 dB from its small-signal linear value.

Finally, the lumped inductors must be replaced by the microstrip lines using standard FR4 substrate. The lumped capacitors in the output-matching circuit can be implemented as the MIM capacitors with using a separate die to provide their high quality factors. To calculate the parameters of the microstrip lines, let us represent the input impedance of a transmission line with arbitrary load impedance as

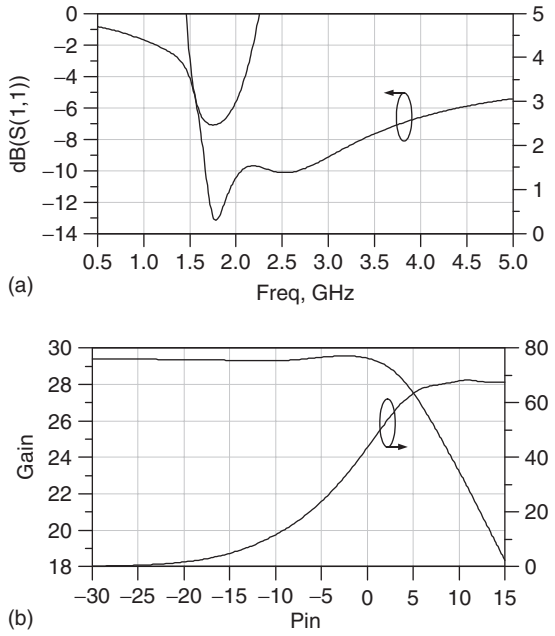



**Figure 9.54: Electrical performance of two-stage power amplifier with lumped elements.**

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\theta}{Z_0 + jZ_L \tan\theta} \tag{9.5}$$

where $\theta$ is the electrical length, $Z_0$ is the characteristic impedance and $Z_L$ is the load impedance [15]. For a short-circuited condition of $Z_L = 0$ or when $Z_0 >> Z_L$, we can write a simple equation

$$Z_{in} = jZ_0 \tan\theta. \tag{9.6}$$

Since the input impedance of a lumped inductance $L$ is written as $Z_{in} = j\omega L$, the electrical length $\theta$ can be written as

$$\theta = \tan^{-1} \frac{\omega L}{Z_0}. \tag{9.7}$$

Then, the electrical lengths of the first-stage collector microstrip line, second-stage collector microstrip line and series microstrip line in an output matching circuit can be respectively calculated as

$$\theta_1 = \tan^{-1}(0.284) = 15.85^\circ$$

$$\theta_1 = \tan^{-1}(0.220) = 12.41^\circ$$

$$\theta_1 = \tan^{-1}(0.462) = 24.79^\circ$$

Using the LineCalc program, available in Tools displayed by the project menu, results in the following geometrical length of the microstrip lines with 26-mil width (characteristic impedance of approximately 50 Ω) implemented into the FR4 substrate with the parameters given in Fig. 9.55:

$$l_1 = 4.0\,\text{mm}$$

$$l_2 = 3.1\,\text{mm}$$

$$l_3 = 6.3\,\text{mm}.$$

Fig. 9.55 shows the simulation setup of the two-stage Class-E power amplifier with microstrip lines. In principle, there is no need to tune any circuit element. In this case, the maximum power-added efficiency of 67.1% and power gain of 22.5 dB with the output power of 33.6 dBm can be achieved, as shown in Fig. 9.56. At the same time, the output power of 33 dBm and power gain of 27 dB are provided with power-added efficiency as high as 62.7%. Some small additional tuning of circuit parameters around their nominal values, probably can slightly improve the performance. However, based on the example described above, you can

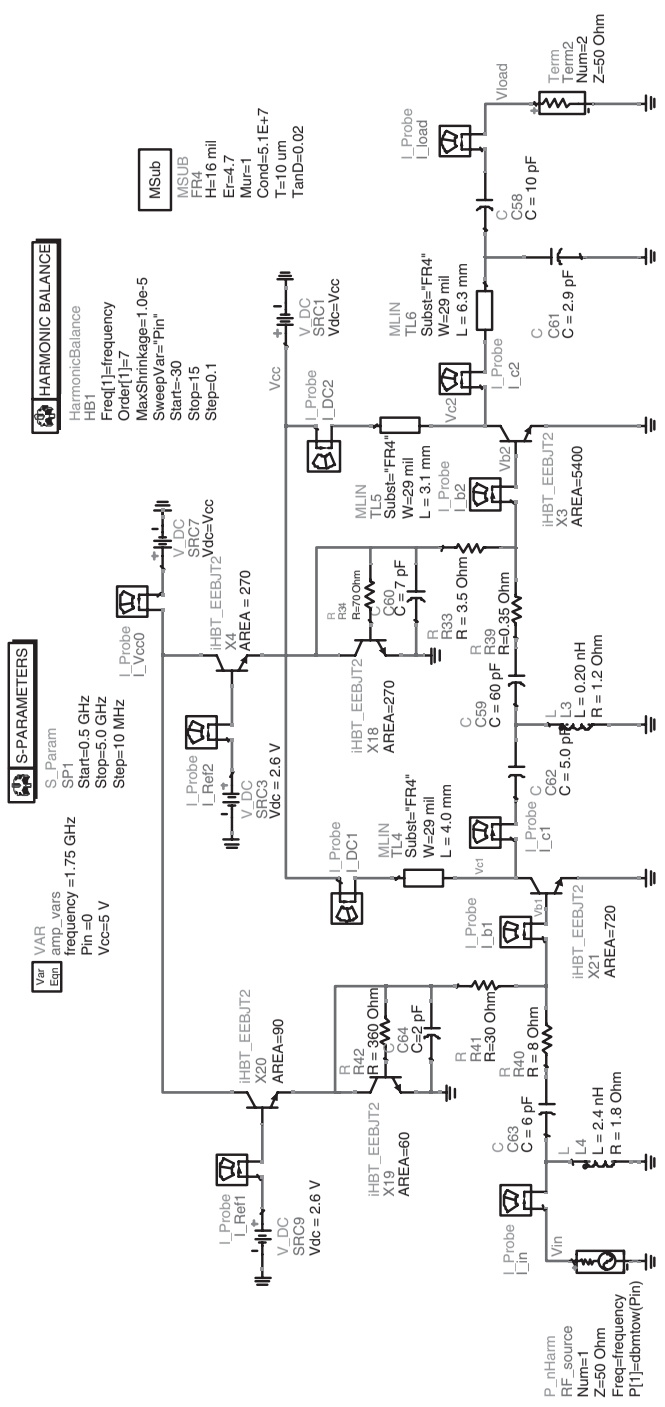



**Figure 9.55: Simulation setup for two-stage Class-E power amplifier with microstrip lines.**

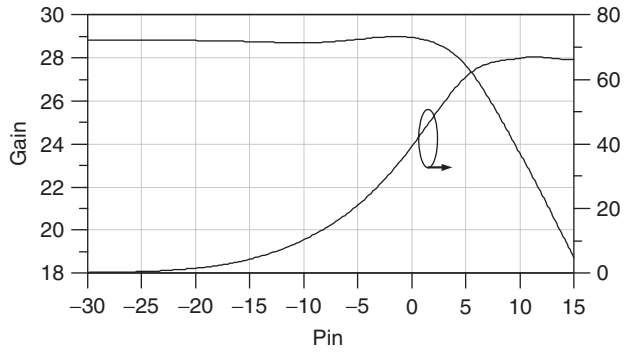



**Figure 9.56: Electrical performance of two-stage power amplifier with microstrip lines.**

see how effective a simple analytical approach with quick manual tuning (which can provide high performance and can significantly speed up the entire high-efficiency power-amplifier design procedure) is.

## References

[1] ''Tutorial Guide to the Demonstration Version of the HB-PLUS Computer Program for Simulating and Optimizing Resonant and Non-Resonant Voltage-Switching (Half-Bridge and Full-Bridge) Classes D and DE DC-DC Converters, DC-AC Inverters, and AC (including RF) Power Amplifiers and Power Generators,'' Design Automation, Inc., Lexington, MA 02420-2404, U.S.A., January 2007.

[2] N. O. Sokal and R. Redl, ''Power Transistor Output Port Model,'' *RF Design*, vol. 10, pp. 45–53, June 1987.

[3] P. J. Baxandall, ''Transistor Sine Wave LC Oscillators, Some General Considerations and New Developments'' *IEE Proc. Electric Power Appl.*, vol. 106, pp. 748–758, May 1959.

[4] S. A. Zhukov and V. B. Kozyrev, ''Push-Pull Switching-Mode Tuned Power Amplifier without Commutation Losses (in Russian),'' *Poluprovodnikovye Pribory v Tekhnike Elektrosvyazi*, vol. 15, pp. 95–106, 1975.

[5] D. C. Hamill, ''Class DE inverters and rectifiers for dc-dc conversion,'' *Proc. 27th IEEE Power Electronics Spec. Conf.*, vol. I, pp. 854–860, 1996.

[6] ''Tutorial Guide to the Demonstration Version of the HEPA-PLUS Program for Design, Simulation, and Optimization of High-Efficiency RF/Microwave Power Amplifiers,'' Design Automation, Inc., Lexington, MA 02420-2404, U.S.A., September 2006.

[7] F. H. Raab, ''Effects of Circuit Variations on the Class E Tuned Power Amplifier,'' *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 239–246, April 1978.

[8] N. O. Sokal, ''Class-E High-Efficiency RF/Microwave Power Amplifiers: Principles of Operation, Design Procedure, and Experimental Verification,'' in J. H. Huijsing, M. Steyaert, and A. van Roermund (Eds.), *Analog Circuit Design: Scalable Analog Circuit Design, High Speed D/A Converters, RF Power Amplifiers*, The Netherlands: Kluwer Academic Publishers, pp. 269–301, 2002.

[9] J. F. Davis and D. B. Rutledge, ''A Low-Cost Class-E Power Amplifier with Sine-Wave Drive,'' *1998 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 1113–1116.

[10] R. Frey, ''500 W, Class E 27.12 MHz Amplifier Using a Single Plastic MOSFET,'' *Application Note APT9903*, Advanced Power Technology, June 1999.

[11] A. Mediano, P. Molina, and J. Navarro, ''An Easy to Use PSPICE Model for Power Transistors in RF Switching Operation and Including Voltage Dependent Output Capacitance,'' *53rd Automatic RF Techniques Group (ARFTG) Conf. Dig.*, pp. 25–30, 1999.

[12] P. Molina, F. del Aguila, P. Pala, and J. Navarro, ''Simple Nonlinear Large Signal MOSFET Model Parameter Extraction for Class E Amplifiers,'' *Proc. 9th Int. Conf. Electronics, Circuits and Systems*, vol. 1, pp. 269–272, 2002.

[13] Y. Tanji, H. Sekiya, and H. Asai, ''Optimization Procedure of Class E Amplifiers Using SPICE,'' *Proc. 2005 Europ. Conf. Circuit Theory and Design*, vol. 3, pp. 133–136.

[14] T. Sato and C. Grigorean, ''Design Advantages of CDMA Power Amplifiers Built with MOSFET Technology,'' *Microwave J.*, vol. 45, pp. 64–78, October 2002.

[15] A. V. Grebennikov, *RF and Microwave Power Amplifier Design*, New York: McGraw-Hill, 2004.

This page intentionally left blank

# Index


Admittance 35, 37, 125, 166, 271

Bipolar junction transistor (BJT)
  base resistance 20, 37, 68, 137
  base-emitter capacitance 37, 46, 137
  collector-base capacitance 17, 122, 123
  collector-emitter capacitance 17, 181
  current source
    ideal 7, 20, 100, 102, 108
    multiharmonic 125
  transconductance 3, 37, 265
  transition frequency 21, 37, 405
Bondwire inductance 131, 165, 172, 233, 260, 294

Circuit
  full-bridge 364, 366
  half-bridge 364, 366, 367
  multi-resonant 95, 151
  single-resonant 49, 95, 151, 269
Class A 8–12, 38, 39
Class AB 10–13, 25, 133, 172, 201, 412
Class B 9–13, 25, 31, 96, 108, 129, 134, 280–282
Class C
  negative bias 45
  zero bias 44, 137
Class D
  current-switching
    symmetrical 71–74, 89
    transformer-coupled 55, 59–61, 74–75, 80, 89
  voltage-switching
    complementary 55, 65, 69, 72–73, 78, 88
    quasi-complementary 67, 78, 90
    transformer-coupled 61, 69, 74–75, 80
    true-complementary 67
    with reactive load 78, 81
  with resistive load 55, 62
Class DE
  voltage-switching 317–326, 364
  with rectangular drive 328
  with sinusoidal drive 329
Class E
  even-harmonic 233, 250, 257–258, 260, 308, 334
  generalized 233, 242–243, 261
  inverse 344, 348–351
  parallel-circuit 233–234, 247–250, 253–256, 260–274, 308, 398–407, 413
  subharmonic 233, 248, 250–253, 308
  with one capacitor and one inductor 233–234, 239, 241
  with quarterwave line
    parallel 293, 301, 308–310
    series 312–313
  with shunt capacitance 179, 183–184, 188, 206, 257, 282, 307–308, 342, 371
Class $E_M$
  biharmonic 315, 338–344
  second-harmonic injection 343
Class E/F
  dual-band 337–338
  generalized 330, 336
  push-pull 332
  with third harmonic trap 337
Class F
  conventional 95, 104–115, 159, 164, 167, 330–331, 352, 356
  inverse 151, 158–175, 330–331, 352, 357
  with quarterwave line
    series 115
    shunt 116, 139

CMOS technology 141–142, 224–225, 233, 283–287
Collector capacitance
  nonlinear effect 27, 46
  parametric generation 46
Conduction angle 4–5, 10–13, 20–25, 100–102
Conjugate matching 37–39

Device operation mode
  active 21–25, 46, 121–123, 203
  inverse 96
  pinch-off 22–25, 64, 71, 198, 202–203
  saturation 64, 71, 84, 88, 120–122, 156, 174, 180, 198, 202–204, 235
Dead time 317–329, 375–376
Diode
  anti-parallel 365, 370
  protection 80–81
  reverse-recovery current 80
Driving
  circuit 82–84
  voltage 23, 27, 82, 88, 153, 280, 286
  signal
    biharmonic 100, 103, 155
    sinusoidal 88, 155, 198, 204, 258, 282, 356
Duty cycle (or ratio) 55–65, 85, 105, 137, 183, 201, 234, 340, 369

Effect
  charging 87
  discharging 87
Efficiency
  anode 96, 104, 153, 156
  collector 8–12, 30, 33, 71, 74, 78, 89, 107,
  drain 101–102, 114, 135–137, 168–170
  power-added (*PAE*) 11, 343–344, 408–409, 415

Feedback
  capacitance 17, 20–22, 27, 35–38, 80, 329
  negative 103
Filter
  low-pass 62, 98–99, 144, 226, 358, 388
  parallel 72, 74, 76
  series 65–70, 108, 174, 179, 183, 241–243, 253, 316, 328, 406
Filter-diplexer 62–63

Harmonic
  control 100–103, 139, 141, 148, 156, 169, 176, 213–214
  peaking 97, 108–114, 124–125, 129–131, 164–167, 194
  termination 136, 164, 167, 214, 356, 358
  tuning 95, 103, 176, 250, 315, 330–331, 336–337, 352–358, 361–362
HBT (hetero-junction bipolar transistor) 17, 91, 264–269, 363, 403–405
HEMT (high-electron mobility transistor) 17, 103, 2205, 211–212, 343, 351, 358

Immittance 35–36, 39–40, 44–45
Instability
  domains 40–44, 49
  feedback
    external 41, 44
    internal 40, 44
  low-frequency 44
  negative resistance 41, 46

Kirchhoff voltage law 85

Large-signal mode 21, 50, 406–407, 411
LDMOSFET (laterally diffused MOSFET) 136, 169, 265–266, 273
Load
  impedance 7, 14, 35, 40, 95, 115, 151, 161, 192
  line 12–15, 96, 405
  network
    with lumped elements 115, 123, 162, 354
    with quarterwave line
      series 312
      parallel 313
    with shunt capacitance 120, 190, 209, 283, 372
    with transmission lines 129, 164, 213, 261
  slope angle 12–14
Load-pull system
  active 354, 361
  passive 358
Load-pull technique
  harmonic reaction 352–354
  harmonic tuning 352–357
Loss
  insertion 213, 359
  return 92, 273, 279–280, 359, 412–413

Matching circuit 27, 50, 168, 174, 183, 192–194, 309–311, 405, 412–416
MESFET (metal-semiconductor field-effect transistor)
  dispersion 17
  drain-source capacitance 16, 124, 144, 162, 220
  gate resistance 16, 199
  gate-drain
    avalanche current 17
    capacitance 17, 37, 162, 199
    diode 17
  gate-source
    capacitance 17, 38, 102–103
    diode 17, 199
  transconductance 38
  transition frequency 37, 199
MMIC (microwave monolithic integrated circuit) 224, 226, 263–267, 283, 363–364
Mode
  hard-switching 363, 368, 376, 380
  soft-switching 363, 366, 376–377
Model
  Angelov 17
  Giacoletto 21
  Gummel-Poon 17
  Materka 17
MOSFET (metal-oxide silicon field-effect transistor)
  gate resistance 16, 85, 137, 199, 279
  gate-drain capacitance 16, 37, 43, 46, 50, 85, 162, 199
  gate-source capacitance 16, 38, 85, 322, 394
  drain resistance 17, 135
  drain-source capacitance 16–17, 46, 50, 124, 162, 325, 337, 392
  oxide capacitance 16
  transconductance 19, 38, 85, 100, 200
  transit time 16, 19, 41
  transition frequency 15, 38, 67, 136, 199, 265, 273, 281

Nominal conditions 235

Objective function 368
Operation mode
  biharmonic 95, 179
  lossless 182, 186, 235, 243, 296
  polyharmonic 179
Optimum
  capacitance 190, 197, 251, 254, 259, 301, 307
  conditions
    zero current 315, 346, 351
    zero voltage 182, 186, 210, 235, 243, 253, 296
    zero current-derivative 315, 346, 351
    zero voltage-derivative 182, 186, 210, 235, 243, 253, 296
  inductance 190, 197, 251, 254, 258, 301, 306–307
  load resistance 190, 251, 254, 258, 301–302, 307
Optimization 175, 191, 273, 278–280, 364, 369–370, 386–389

Parametric oscillation
  large-signal driving 46
  Mathieu equation 49
  modulation factor 48–50
  negative resistance 41, 46, 408
  nonlinear capacitance 28, 47–49
  parametric resonance 48
  subharmonic component 46
  varactor diode 46
Parasitic oscillator
  boundary frequency 41–43
  parasitic series inductance 42–44
  Hartley oscillator 42
Piecewise-linear approximation 2–4, 7, 21, 154
Power gain
  maximum available 38
  operating 11, 36–40, 233, 280–282
  transducer 36–40
Push-pull amplifier
  balanced circuit 33, 61, 209
  midpoint 33, 61, 90
  virtual ground 33, 332

Quality factor 66–67, 71, 90, 117, 156, 162, 180
Quiescent current 7, 10–12, 31, 133, 222, 404

Reactance compensation
  double 272–274
  single 270–273
  transmission-line 275–279
Reflection coefficient 192, 215, 355
Region
  accumulation 16
  active 10, 21, 121, 156, 202, 284, 293

Region (*Continued*)
charge depletion 17
inversion 16
pinch-off 2, 10, 21, 85, 131, 405
quadratic 16
saturation 2, 13, 16, 131, 405
Resonant circuit
detuned 179, 227
parallel 20, 30, 50, 97, 127, 142, 151, 165, 179, 270, 350
series 27, 78, 108, 127, 140, 161, 183, 270, 284, 348, 398
third-harmonic 104
Resonator
harmonic 96, 153, 174, 194
parallel 98, 156, 367–389
series 331, 370

*S*-parameters 354
Saturation
resistance 4, 55, 120, 140
voltage 9, 32, 56, 133, 196–198, 268, 318, 344, 399, 405
Simulator
harmonic balance 398, 403
transient 398–401
Smith chart 192, 354, 394, 406
Spectral-domain analysis
conduction angle 4–5, 10–13, 20–25, 100–102
current coefficient 5, 12, 96, 155
Fourier
series expansion 4–5, 10, 14, 261, 347, 403
transform 57, 59, 61, 66, 73
harmonic balance technique 2, 403, 414, 417
piecewise-linear approximation 2, 7, 21, 154
voltage-ampere characteristic 133–134, 405
Stability
circuit 40, 44
factor 40, 44, 407, 412
margin 39
unconditional 39, 40
Susceptance 125, 191, 271, 281, 311, 338, 372
Switching
loss 80, 205, 317, 410
time 80, 88, 120, 133, 140, 179, 205, 268, 293, 315, 343, 396

Tank resonator
odd-harmonic 95, 104
parallel 125–128, 194
Threshold voltage 83, 85, 199, 218, 224, 281, 365, 370
Time-domain analysis
Taylor series expansion 29, 38
transient response 23, 25, 196, 364–370, 400
Transfer function 1–2, 172
Transformer
*L*-type 216, 284, 311
*T*-type 222, 265
unbalanced-to-balanced 33–35, 59, 69, 74, 337
winding
primary 75
secondary 83, 218
Transmission line
characteristic impedance 33, 115, 130, 144, 162, 217, 263, 275, 310, 416
coaxial 33, 91
electrical length 34, 45, 116, 129, 144, 165, 173, 217, 263, 275, 310, 355, 416
microstrip 92, 136, 167, 173, 213, 221, 264, 416
open-circuited 124, 129–134, 163, 261, 331, 334
quarterwave 95, 115–119, 129–130, 138, 151, 161, 174, 276, 293–312
short-circuited 35, 80, 124, 130, 139, 165, 217, 261, 331, 416
Tuning method
cascaded 359
stub resonator 358
triplexer 358

Voltage
incident 117
reflected 117
*VSWR* (voltage standing wave ratio) 45, 192, 218, 228, 274, 396

*W*-parameters 35–36
Waveform
asymmetrical 14, 201
flattened 96, 104, 108, 152, 179
half-sinusoidal 66, 106, 108, 118, 136, 158, 204
maximally flat 108, 114, 146
rectangular 97, 204, 334, 336
symmetrical 179, 201
trapezoidal 88, 199, 204, 336
*Y*-parameters 35, 37, 281, 404

*Z*-parameters 35, 37