Extending SuperSpeed USB to Higher Performance Applications – 10Gbps SuperSpeed USB

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HSTS004
Agenda

• Motivation and Goals
• Architectural Approach
• Technical Details
• Industry Timeline and Compliance
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Motivation for SuperSpeed USB @ 10Gbps

• SuperSpeed USB 3.0 @ 5Gbps is enabling new usages
  – Compelling video display – 1080p/60fps
  – High-performance storage – 450MB/sec SSDs
  – USB docking – multi-function hubs

• Usage assessment indicates increase in bandwidth needed to dramatically improve USB experience
  – Display + storage + other functions collectively can saturate a 5Gbps SuperSpeed USB link
  – SSD and hybrid HDD storage on track to break 500MB/sec within three years

• Technical analyses indicated that a doubling of data rate “within” the existing ecosystem is feasible
Use Cases for SuperSpeed USB @ 10Gbps

• Support attach of much higher performance peripherals
  – A/V Display beyond 1080p and multi-displays
  – SSD, RAID HDD or Hybrid HDD
• Blazing fast data sync
• Enable multi-function, single port connections
  – SuperSpeed Hubs with fatter system pipe supporting multiple SuperSpeed downstream devices
  – Display Dock enabling mix of SuperSpeed-based A/V, webcam, storage, etc. over a single connection
Goals/Objectives Given to the Team

• Double the delivered bandwidth
  – Both on the link and through the topology

• Preserve/improve power efficiency
  – For a given workload, match or improve upon power consumed for the USB aspects of data transfer

• No OS driver software changes required
  – Just works by default
  – Driver enhancements would allow devices to take advantage of new capabilities (e.g. 750 MB/s ISOC)

• Consider inclusion of more design guidance
  – Increase implementation consistency and success

• Consider system interaction factors (EMI/RFI, etc.)
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General Approach

• More than double SuperSpeed USB bandwidth by adding a 10Gbps data rate and improving data encoding
  – Enable across existing USB connectors with full backward compatibility
    ▪ Normalize requirements based on 1m cable usage
  – Auto configuration of data rates, graceful fall back as needed
  – Enhance hub definition to address rate matching and optimize upstream channel utilization
  – Achieve power efficiency better than 5Gbps SuperSpeed from a workload perspective

• No anticipated changes to be required in software stack because xHC comprehends bandwidth scaling

• Update compliance plans/specs

• Develop additional design guidance/specs to aid successful platform and device implementation
Functional Update Highlights

- **SuperSpeed USB Communication Layers**

- **Multiple Ins, new speed TP and new traffic type classes**

- **Link speed training and error performance enhancements**

- **New data rate and encoding for 10Gbps operation, and new LFPS-based messaging**

- **New store and forward model/buffering and upstream traffic optimization**
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Terminology

Enhanced SuperSpeed System

USB Host
- USB Connector(s)
- USB 2.0 Bus
- Composite cable

USB Hub Device
- USB 2.0 Hub
- Enhanced SuperSpeed Hub
- Enhanced SuperSpeed Bus

USB Peripheral Device
- Enhanced SuperSpeed Function
- USB 2.0 Function
Updates for Cables and Connectors

- Continued use of existing mechanical interface
  - Backward-compatible connectors
- New channel budget for 10Gbps (Gen2) signaling
  - The mated cable assembly insertion loss is budgeted to be ≤6dB @ 5 GHz
    - Targeted for 1 meter cables, not 3 meter cables
    - Longer than 1 meter may require an active cable
    - Both raw cable and connector performance need to improve to achieve this
- EMI/RFI performance improvement required
  - Improved shielding and grounding, defined EMI contact zones
- Reference Footprint Pad Stack-ups for PCB designs defined to ensure good high-speed signal performance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>Finished hole radius</td>
<td>0.35</td>
</tr>
<tr>
<td>b</td>
<td>Annular ring radius</td>
<td>0.50</td>
</tr>
<tr>
<td>R</td>
<td>Antipad radius to center</td>
<td>0.75</td>
</tr>
<tr>
<td>P</td>
<td>Antipad center to center distance</td>
<td>2.00 (Std-A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.75 (Std-B)</td>
</tr>
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</table>
New Compliance Methodology for Cables and Connectors

- A new compliance methodology will be used for the certifying USB 3.1 cable assembly performance
  - Will use reference PHYs for the host and device
  - Metrics include:
    - Insertion loss fit at Nyquist frequency (ILfitatNq)
    - Integrated multi-reflection (IMR)
    - Integrated crosstalk (IXT)

New compliance methodology aids in avoiding margin loss or the failing of assemblies that would otherwise function properly
Updates for Physical Layer

• More than doubled the useable bandwidth
  – 10Gbps signaling rate \( \rightarrow \) Twice as many bits per second
  – 128b/132b line code \( \rightarrow \) ~20% better use of those bits

• New channel definition: ~equal allocation for both host and device
  – 20dB overall channel budget split between host, cable and device

• Reference transmitter and reference receiver are defined

TX w/3 taps

RX w/7 CTLE boost settings and a 1-tap DFE

• Updated Jitter budget model and tolerance requirements
  – PLL bandwidth raised to 7.5MHz
Repeaters

- 10Gbps compliance testing environment will be built around a revised loss budget
  - Cable assembly includes the mated pairs at both ends
- May need a repeater if your host or device loss exceeds 7dB at 5GHz

- Requirements for on-board re-timing repeaters are being defined – will be released Q4’13 in Appendix E
Updates for Link Layer

• Minimal LTSSM change
  – Added speed negotiation as part of Polling sub-state

• Link Speed training
  – Defined LFPS Based PWM Message
  – LBPM used for port capability announcement and negotiation

• Retained SuperSpeed USB packet structure
• Two credit classes: Type 1 (control/periodic), Type 2 (async)
• Ensured equivalent or better error rates
  – Frame markers – single symbol error tolerant
  – Data packet header – length field single-bit error tolerant
## Link Performance Summary

<table>
<thead>
<tr>
<th></th>
<th>5Gbps</th>
<th>10Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line code</td>
<td>8b/10b</td>
<td>128b/132b</td>
</tr>
<tr>
<td>Bandwidth encoding overhead</td>
<td>20%</td>
<td>3%</td>
</tr>
<tr>
<td>Random BER</td>
<td>1e-12</td>
<td></td>
</tr>
<tr>
<td>Probability of Recovery entry due to single-bit error</td>
<td>5.7e-15</td>
<td>0</td>
</tr>
<tr>
<td>Probability of Recovery entry due to single/multi-bit error</td>
<td>&gt;5.7e-15</td>
<td>1.8e-22</td>
</tr>
</tbody>
</table>

- Error performance improves with 128b/132b code and 4-bit sync header
  - Compliments SuperSpeed USB’s strong packet framing to achieve single-bit error not going to Recovery
  - Preserves the link layer architecture with minimum change
- LFPS-based start-up speed negotiation protocol minimizes the initialization latency while offering maximum flexibility for port configuration
Updates for Protocol Layer

• Added support for multiple INs
  – Used by hubs to maximize throughput in mixed speed topology
  – Defined arbitration rules for multiple in-flight INs

• Expanded header definition
  – Added transaction type field
  – Extended the use of the Route String field on return packet to include Data Packet Weight for device to host packets

• Defined new priority rules for TPs and periodic/async DPs

• Doubled maximum isochronous bandwidth

• Deprecated features
  – Num HP, Link Speed fields in configuration LMPs
  – Bus Interval Adjustment (BIA) Message

• Added Precision Time Management to USB 3.0
  – Precisely measure link delay time
Updates for Hub

• Defined new store and forward model for data packets
• Maximized use of upstream link
  – Multiple in-flight INs
  – Reordering of data packets
• Enabled fair share of bandwidth to devices regardless of position in topology
  – Weighted fair share round robin arbitration
• Defined two link credit classes to ensure smooth flow of link/connection management TPs and periodic traffic
• Increased buffering requirements
• Updated upstream and downstream port state machines
Enhanced SuperSpeed Hub Architecture

- **Upstream Controller**
  - \(\downarrow\) Buffers and routes packets being received from the upstream link
  - \(\uparrow\) Arbitrates packets waiting to be transmitted on the upstream link

- **Downstream Controller**
  - \(\uparrow\) Buffers and routes packets being received from the downstream link
  - \(\downarrow\) Buffers and arbitrates packets waiting to be transmitted on the downstream link

- **Hub Controller**
  - Responsible for host-to-hub communication
Enhanced SuperSpeed Hub Arbitration

- TPs prioritized over DPs – both upstream and downstream
- Periodic DPs prioritized over Asynchronous DPs – both upstream and downstream
- Weighted Sum Round Robin Algorithm
  - Upstream DPs carry summed weight
    - 16 bit weight field using bits in the previously reserved RouteString space
- Arbitration decisions occur close to the end of current packet transmission

All devices get approx. same bandwidth
xHC Design Updates

• Link Speed Device Notification TP
  – Sent by the device after it enters the Address State
  – xHC matches the Link Speed Notification to closest Speed ID
    ▪ Updates Slot Context
  – xHC uses the new Speed to adjust its scheduling algorithm to the device
  – Software can optionally enable Link Speed Device Notification Events

• Enable xHC to schedule 10Gbps SuperSpeed USB devices to maximize bus utilization
  – Support multiple INs for devices operating at 10Gbps
  – Take advantage of additional bandwidth
USB 3.1 PIPE Updates

- PIPE 4.2 with USB 3.1 updates based on 0.9 rev USB 3.1 specification available or review

- USB 3.1 updates use same signals as PCI Express* 3.0
  PIPE 128/130 support with two additional header bits
  - TxDataValid, RxDataValid
  - TxStartBlock, RxStartBlock
  - TxSyncHeader[3:0], RxSyncHeader[3:0]
  - Header error detection/reporting handled by controller
  - Polarity detection handled by controller

- PIPE 4.3 with USB 3.1 comments and updates for 1.0 planned release Q3/Q4 2013
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Specification Timeline

**Specification Development**
- **Jan**: Initial Product Development
- **Q3**: Initial Silicon Development
- **Q4**: Compliance Development

**Compliance Development**
- **Feb**: Industry Review #1
- **May**: Industry Review #2

**Initial Silicon Development**
- **Q3**: Initial Product Development

**Initial Product Development**
- **Q4**: Final Release

**Technically comprehensive**
- **0.7 Draft**
- **0.9 Draft**
- **1.0 Final**
- **Final Release Candidate**

**Next DevCons**:
- **October 1-2, 2013** in Dublin, Ireland
- **December 10-11, 2013** in Asia
USB 3.1 Compliance

• 10Gbps Hosts/Devices will be tested for:
  – Compliance at the USB 2.0 speeds supported
  – Compliance to 5Gbps SuperSpeed USB requirements
  – Compliance to new 10Gbps SuperSpeed USB requirements

• USB 3.1 Compliance Requirements
  – Interoperability testing will be updated to include support for USB 3.1 hosts/devices
  – Updated framework tests
  – New link layer tests
  – New electrical tests for the physical layer
  – New cable and connector tests
    ▪ Includes USB Power Delivery (USB PD) requirements
## USB 3.1 Compliance Timeline

<table>
<thead>
<tr>
<th>Version</th>
<th>Milestones</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>Test Assertions</td>
</tr>
<tr>
<td>0.7</td>
<td>Test Assertions + Test Descriptions</td>
</tr>
<tr>
<td></td>
<td>Test Specification</td>
</tr>
<tr>
<td>0.9</td>
<td>Tests coded and Test Specification updated</td>
</tr>
<tr>
<td></td>
<td>Begin testing at PIL</td>
</tr>
<tr>
<td>0.95</td>
<td>Beta tool release</td>
</tr>
<tr>
<td></td>
<td>Ready to certify products</td>
</tr>
<tr>
<td>1.0</td>
<td>Final tool release</td>
</tr>
<tr>
<td></td>
<td>Release to ITLs</td>
</tr>
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**Timeline:**

- **Q1 2013:** Test Assertions
- **Q2 2013:** Test Descriptions
- **Q3 2014:** Product Integration Lab (PIL) Testing
- **Q4 2014:** Test Tool Development
- **Q1 2015:** Test Tool Refinement
- **Q2 2015:** First USB-IF workshop
- **Q3 2015:** ITL rollout
- **Q4 2015:** 1.0 Compliance Spec Release
Summary

• Trends in USB storage, display and docking applications with be driving demand for increased USB data bandwidth
• USB 3.1 will deliver a compelling performance boost within the existing USB cable and connector ecosystem

• Engage in USB 3.1 development
  – The spec and more information available at: http://usb.org/developers/ssusb/
• Attend USB 3.1 Developer’s Days
  – Oct 1/2 in Dublin, Ireland and Dec 10/11 in Asia (tentative) http://www.usb.org/developers/events/USB_3_1_DD/
Q&A
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