A ZVS PWM Half-Bridge Voltage Source Inverter With Active Clamping

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***Abstract*—This paper presents a zero-voltage (pulsewidth modulation) half-bridge inverter with active voltage clamping using only a single auxiliary switch. The structure is particularly simple and robust. It is very attractive for single-phase high-power applications. Switching losses are reduced due to implementation of the simple active snubber circuit that provides zero-voltage-switching conditions for all switches, which includes the auxiliary one. Its main features are simple modulation strategy, robustness, low weight and volume, low harmonic distortion of the output current, and high efficiency. The principle of operation for steady-state conditions, mathematical analysis, and experimental results from a laboratory prototype are presented.**

***Index Terms*—Active clamping, inverters, soft commutation.**

I. Introduction

With the appearance of the bipolar transistors in the 1950s and the metal–oxide–semiconductor field-effect transistors in the 1980s, pulsewidth modulation (PWM) techniques could be used together with the increase of the commutation frequency, aiming to reduce the harmonic distortion at the output voltage waveform of inverters [1]–[6]. These measures lead to some benefits like the reduction of volume and weight of filters and magnetic elements; nevertheless, they cause some difficulties due to the high commutation losses in the switches, which reduce the efficiency of the converter, and the appearance of electromagnetic interference. These factors mainly occur in inverter topologies that use the bridge configuration, where the main switch is affected by the reverse recovery phenomenon of the antiparallel diode of the complementary switch. During this stage, the switches are submitted to a high current ramp rate (di/dt) and a high peak reverse recovery current i_r. Both significantly contribute to increasing the commutation losses and produce electromagnetic interference.

A great number of works have been realized by power electronics scientific community, with the aim to diminish these problems. They can be divided in two groups, which are: 1) passive techniques [7]–[13] and 2) active techniques [14]–[27]. The passive techniques are characterized by the absence of controlled switches in the auxiliary circuit, whereas the active techniques are characterized by circuits that use controlled switches.

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Among the passive solutions, perhaps the most widely known is the Undeland snubber [7], which provides a good performance in the majority of its applications but is not capable of regenerating the energy of the switching process. To try to minimize the switching losses, some works have considered modifications in the Undeland snubber, which aim at the regeneration of the energy lost in the switching [8]–[13].

Among the active solutions, the main ones are those that use conventional PWM modulation without the need for special control circuits. One of these works is the auxiliary resonant diode pole inverter [14]. This topology matches the use of PWM modulation, with the soft switching attained through a relatively simple circuit. On the other hand, it needs a high current circulating in the circuit, about 2.5 times the load current, which raises the current stress in the switches. A topology very similar to the previous one is the auxiliary resonant pole inverter [15]. Theoretically, this circuit reduces the current levels that are necessary for switching; however, it involves a complex control strategy. Another circuit found in literature is the auxiliary resonant commutated pole inverter [16]–[18]. This inverter has auxiliary switches that are only turned on when the load current is not sufficient to realize the soft switching, which causes the control circuit to become very complex and dependent on the sensors. The works presented in [19] and [20] show an interesting idea, where the reverse recovery energy from the diodes is used to obtain soft commutation in the switches of the preregulated rectifiers with high power factor.

In this paper, the analysis of a zero-voltage-switching (ZVS) PWM full-bridge inverter with active clamping technique using the reverse recovery energy of the diodes to improve the efficiency of the converter is presented. The proposed structure uses only a single auxiliary switch and the diode reverse recovery energy technique to obtain soft commutation in all switches such as the rectifier shown in [20].

II. Proposed Circuit

The proposed circuit is shown in Fig. 1. It presents a half-bridge inverter configuration, where Q_1 and Q_2 are the main switches, and Q_A is the auxiliary switch. C_1, C_2, and C_A are the commutation capacitors.

The snubber circuit is formed by one controlled switch, Q_A, with antiparallel diode D_A, one small inductor L_S, and one clamping capacitor C_S. Capacitor C_S is responsible for the storage of the diode reverse recovery energy and for the clamping of the voltage across the switches. Inductor L_S is responsible for the control of di/dt during the diode reverse recovery time.

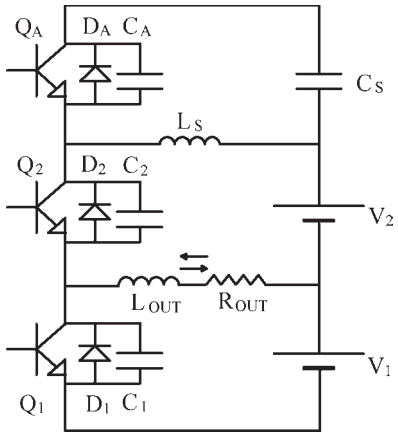

Fig. 1. Proposed circuit.

The auxiliary switch works with constant duty cycle in all operation range. One of the main advantages of this converter consists in the use of only one auxiliary switch, which provides the clamping of the voltage and the ZVS conditions for all switches, including the auxiliary switch in the snubber circuit.

III. Operation Stages (for the First Half-Cycle)

To simplify the analysis, the following assumptions are made: the circuit operates in steady state; the components are considered ideal; and the reverse recovery characteristic of diodes D_1 and D_2 is excluded. The voltage across the capacitor C_S and the current in the output inductor $L_{\rm OUT}$ are considered constant during the switching period. The parameter E represents the bus voltage $(E = V_1 + V_2)$, and vC_S is the voltage across the clamping capacitor C_S. In the following paragraphs, the operation stage of the first positive half-cycle of the output current is described in detail. The main operation stages are shown in Fig. 2. Fig. 3 shows the main waveforms.

First stage $(t_0 - t_1)$: During this interval, the output current $i_{\rm OUT}$ is delivering energy to the source V_2 via diode D_2. At the same time, additional current $(iL_S - i_{\rm OUT})$ circulates through C_S and Q_A. At the end of this stage, the current through inductor L_S reaches its maximum value, $i_f + i_{\rm OUT}$.

Second stage $(t_1 - t_2)$: This stage starts when the auxiliary switch Q_A is blocked. Current iL_S charges capacitor C_A from zero to $E + vC_S$ and discharges C_1 from $E + vC_S$ to zero.

Third stage $(t_2 - t_3)$: During this stage, the voltage across C_1 is clamped by the antiparallel diode D_1. At this moment, the voltage $E = V_1 + V_2$ is applied across the inductor L_S, and the current iL_S linearly decreases. The diode D_2 conducts the current iL_S, whereas D_1 conducts the current $iL_S - i_{\rm OUT}$.

Fourth stage $(t_3 - t_4)$: This stage begins when current iL_S reaches $i_{\rm OUT}$ and flows through switch Q_1. The turn-on occurs at zero voltage. Current iL_S continues to decrease until inverting its direction, which begins the reverse recovery phase of diode D_2. The inductor L_s limits the di/dt.

Fifth stage $(t_4 - t_5)$: This stage starts when diode D_2 finishes its reverse recovery phase. Current iL_S begins the charging of capacitor C_2 from zero to $E + vC_S$ and discharging of C_A from $E + vC_S$ to zero.

Sixth stage $(t_5 - t_6)$: At this stage, the voltage across capacitor C_A reaches zero, and it is clamped by diode D_A. Current iL_S increases due to the application of voltage vC_S across inductor L_S. In this stage, switch Q_A must be turned on. It is important to emphasize that the drive time of switch Q_A is previously estimated and kept constant during the entire inverter operation range. Therefore, the use of current sensor is not necessary. This stage finishes when the current in L_s reaches zero.

Seventh stage $(t_6 - t_7)$: This stage begins when current iL_S changes its direction and flows through switch Q_A. Current iL_S continues to linearly increase.

Eighth stage $(t_7 - t_8)$: During this stage, switch Q_1 is blocked, and the current through C_S decreases, inverts its direction, and flows through diode D_A. Capacitor C_1 is charged from zero to $E + vC_S$, and capacitor C_2 is discharged from $E + vC_S$ to zero.

Ninth stage $(t_8 - t_0)$: This stage begins when the voltage across capacitor C_2 reaches zero, and it is clamped by diode D_2. Current iL_S continues to increase. This stage finishes when iL_S is equal to $i_{\rm OUT}$, and the additional current $(iL_S - i_{\rm OUT})$ flows through the auxiliary switch Q_A, which restarts the first operation stage.

For the second half-cycle, the operation stage is analogous and can be described in an identical way.

IV. Mathematical Analysis of the Soft-Switching Circuit

To guarantee ZVS conditions, in the second stage, it is necessary that the stored energy in the inductor L_S due to the additional current iC_S be sufficient to discharge capacitor C_1 and to charge C_A. Thus, by inspection of Fig. 2 (interval $t_1 - t_2$), the following condition can be formulated:

$$L_S \cdot i_f^2 \geq (C_A + C_1)(E + vC_S)^2 \tag{1}$$

where i_f is the maximum current in C_S, and vC_S is maintained constant during the switching period. The current i_f must be sufficient to promote the charge and discharge of the commutation capacitors. Assuming $vC_S \ll E$ results to

$$i_{f\,\min} \geq E\sqrt{\frac{C_1 + C_A}{L_S}}. \tag{2}$$

It is necessary to know the clamping voltage behavior for the design of the switches and capacitor C_S. In the steady-state conditions, the clamping capacitor average current must be zero. Thus,

$$iC_{\rm Sav} = \frac{1}{T_S}\left[\int_{t_5}^{t_7}\left(\frac{vC_S}{Ls}t - i_r\right)dt + \int_{t_7}^{Ts}\left(\frac{vC_S}{Ls}t - i_{\rm OUT} - i_r\right)dt\right] \tag{3}$$

where T_S is the switching period.

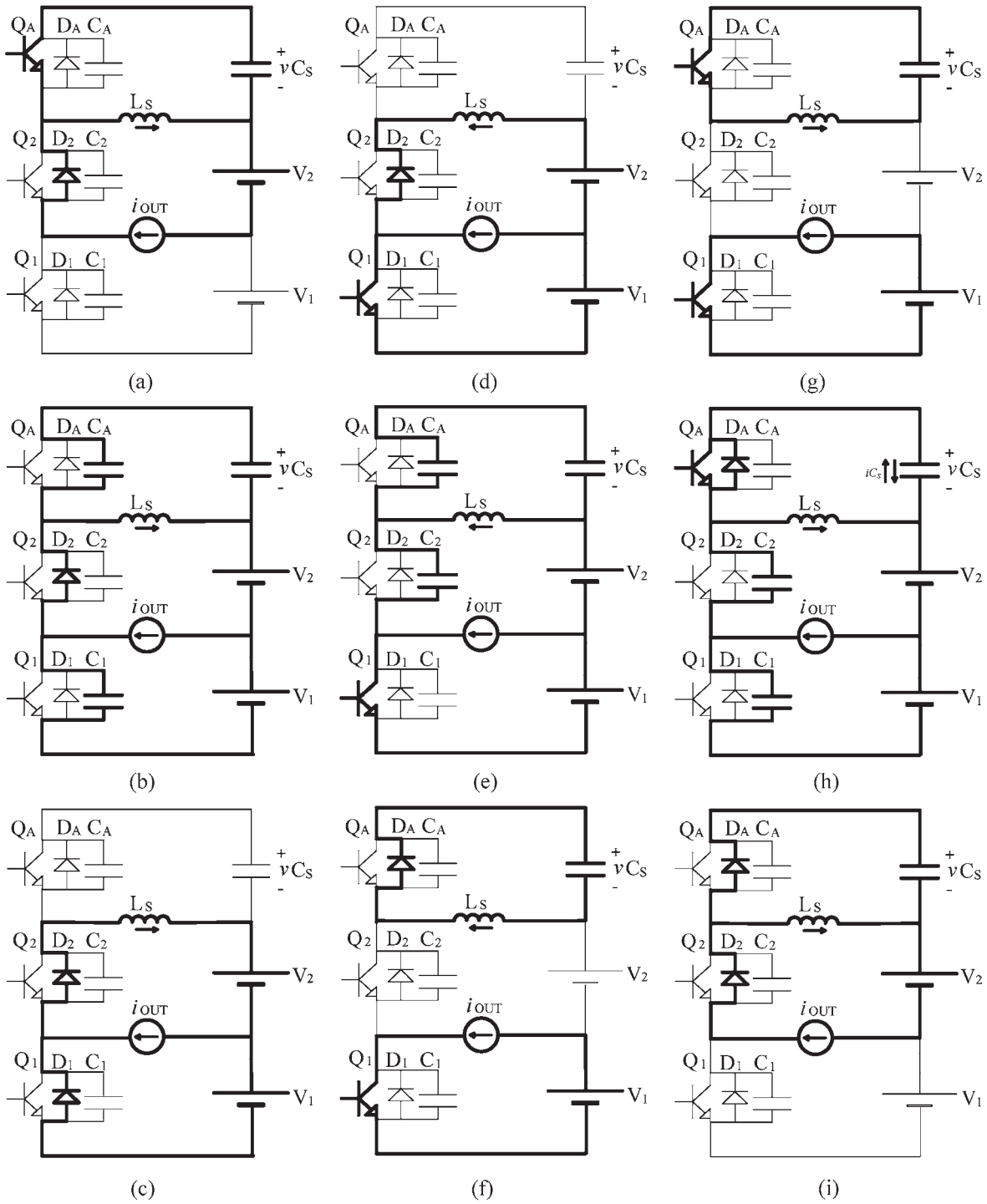

Fig. 2. Operation stages. (a) First stage ($t_0 - t_1$). (b) Second stage ($t_1 - t_2$). (c) Third stage ($t_2 - t_3$). (d) Fourth stage ($t_3 - t_4$). (e) Fifth stage ($t_4 - t_5$). (f) Sixth stage ($t_5 - t_6$). (g) Seventh stage ($t_6 - t_7$). (h) Eighth stage ($t_7 - t_8$). (i) Ninth stage ($t_8 - t_0$).

In relation to the switching period, the commutation time is very short. Therefore, the following simplifications can be made:

$$t_5 = t_1 = 0 \tag{4}$$

$$t_7 - t_5 = D \cdot T_S \tag{5}$$

$$t_7 = D \cdot T_S \tag{6}$$

where D is the duty cycle to the switching period.

From (4)–(6), (3) can be rewritten as follows:

$$iC_{\text{Sav}} = \frac{1}{T_S}\left[\int_0^{D\cdot T_S}\left(\frac{vC_S}{L_S}t - i_r\right)dt + \int_{D\cdot T_S}^{T_S}\left(\frac{vC_S}{L_S}t - i_{\text{OUT}} - i_r\right)dt\right]. \tag{7}$$

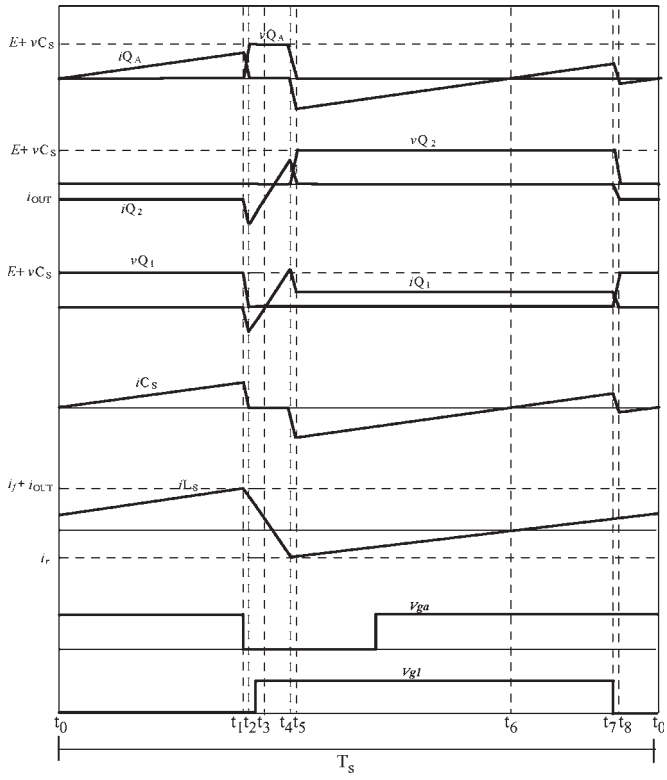

Fig. 3. Main waveforms.

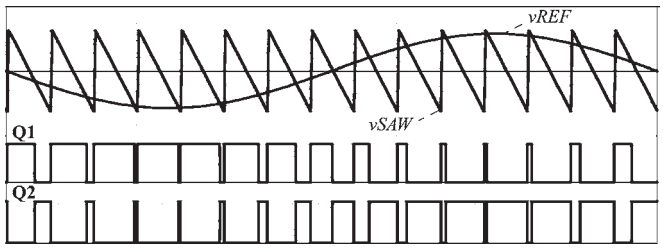

Fig. 4. Modulation strategy.

Solving the integral equation and considering

$$iC_{\mathrm{Sav}} = 0 \tag{8}$$

we have

$$vC_S = \frac{2 \cdot L_S}{T_S}\left[i_r + i_{\mathrm{OUT}}(1-D)\right]. \tag{9}$$

Considering that the load current is a sinusoidal function and is in phase with the output voltage, then,

$$i_{\mathrm{OUT}}(\omega t) = \frac{E \cdot ma}{2 \cdot Z_{\mathrm{OUT}}} \cdot \sin \omega t \tag{10}$$

where Z_{OUT} is the load impedance.

Fig. 4 shows some signals of the modulation strategy used to drive the main switches.

The sawtooth waveform is lined on the left edge. This facilitates the synchronism between the auxiliary switch and the main switches. The converter output voltage is controlled by the amplitude modulation factor (ma), which is obtained through the relation between the peak value of the sinusoidal reference signal and the peak value of the sawtooth waveform (11), i.e.,

$$ma = \frac{v_{\mathrm{ref_{pk}}}}{v_{\mathrm{saw_{pk}}}}. \tag{11}$$

The inverter output voltage for a switching period can be expressed by

$$v_{\mathrm{OUT}} = E\left(D - \frac{1}{2}\right). \tag{12}$$

From (12), we can obtain the duty cycle D, i.e.,

$$D = \frac{v_{\mathrm{OUT}}}{E} + \frac{1}{2}. \tag{13}$$

The inverter output voltage for an output period is given by

$$v_{\mathrm{OUT}}(\omega t) = \sqrt{2} \cdot v_{\mathrm{OUT_{rms}}} \cdot \sin \omega t \tag{14}$$

where ω is expressed by

$$\omega = 2 \cdot \pi \cdot f \tag{15}$$

and f represents the output frequency.

The maximum output voltage is given by

$$v_{\mathrm{OUT_{pk}}} = \frac{E \cdot ma}{2}. \tag{16}$$

The root-mean-square (rms) output voltage is obtained from

$$v_{\mathrm{OUT_{rms}}} = \frac{E \cdot ma}{2 \cdot \sqrt{2}}. \tag{17}$$

Equation (18) shows the inverter duty cycle obtained from (13), (14), and (17), i.e.,

$$D(\omega t) = \frac{ma}{2} \cdot \sin \omega t + \frac{1}{2}. \tag{18}$$

Combining (9), (10), and (18), we obtain the expression of the snubber capacitor voltage vC_S given by

$$vC_S(\omega t) = \frac{2 \cdot L_S}{T_S}\left[i_r + \frac{E \cdot ma}{4 \cdot Z_{\mathrm{OUT}}} \cdot \sin \omega t - \frac{E \cdot ma^2}{4 \cdot Z_{\mathrm{OUT}}} \cdot \sin^2 \omega t\right] \tag{19}$$

where i_r is the peak reverse recovery current of the antiparallel diode, which can be given by [25]

$$i_r = \sqrt{\frac{4}{3} \cdot Q_{\mathrm{rr}} \cdot \frac{E}{L_S}}. \tag{20}$$

Q_{rr} represents the reverse recovery charge of the diode.

From the analysis of the current behavior in capacitor C_S, the expression of current i_f can be obtained

$$i_f(\omega t) = \frac{vC_S(\omega t)}{L_S} \cdot T_S - i_{\mathrm{OUT}}(\omega t) - i_r. \tag{21}$$

TABLE I
MAIN SPECIFICATIONS

E = 400V	Bus Voltage
V_{OUT} = 127 V	RMS Output Voltage
P_{OUT} = 7.5kVA	Output Power
i_{OUT} = 59A	Output Current
f_S = 20kHz	Switching Frequency
f = 60Hz	Output Frequency
L_{OUT} = 500 μH	Load Inductance
R_{OUT} = 2.15Ω	Load Resistance
ma = 0.9	Modulation Factor
C_1, C_2, C_A = 1.5nF	Commutation Capacitance

Combining (10) and (19) with (21), we obtain the expression that represents the evolution of current i_f, i.e.,

$$i_f(\omega t) = i_r - \frac{E \cdot ma^2}{2 \cdot Z_{\rm OUT}} \cdot \sin^2 \omega t. \tag{22}$$

The minimum value of expression (22) is located in $\pi/2$. Then,

$$i_{f\,\min} = i_r - \frac{E \cdot ma^2}{2 \cdot Z_{\rm OUT}}. \tag{23}$$

To guarantee the ZVS condition in all load range, the minimum value of current i_f obtained from (23) must be greater than the value obtained from (2), i.e.,

$$i_r - \frac{E \cdot ma^2}{2 \cdot Z_{\rm OUT}} \geq E\sqrt{\frac{C_1 + C_A}{L_S}}. \tag{24}$$

V. DESIGN EXAMPLE

A. Input Data

The main specifications are shown in Table I.

B. Calculation of the Auxiliary Inductors

The auxiliary inductor is responsible for the di/dt limit during the turnoff of the main diodes. The di/dt is directly related to the peak reverse recovery current i_r of the antiparallel diodes. A "snappy" di/dt produces a large amplitude transient voltage and significantly contributes to electromagnetic interference.

In the design procedure, a di/dt that is usually found in the diode datasheet was chosen. This is a simple way to obtain the diode's fundamental parameter for the design of the inverter. In this case, the di/dt chosen for the example was 40 A/μs. We know that the current ramp rate is determined by the external circuit. Thus,

$$L_S = \frac{E}{di/dt} = \frac{400}{40} = 10\ \mu\text{H}. \tag{25}$$

TABLE II
DIODE SPECIFICATIONS

V_{rrm} = 1.200V	Maximum Reverse Voltage
I_{av} = 80A	Diode Average Current
Qrr = 130μC	Reverse Recovery Charge

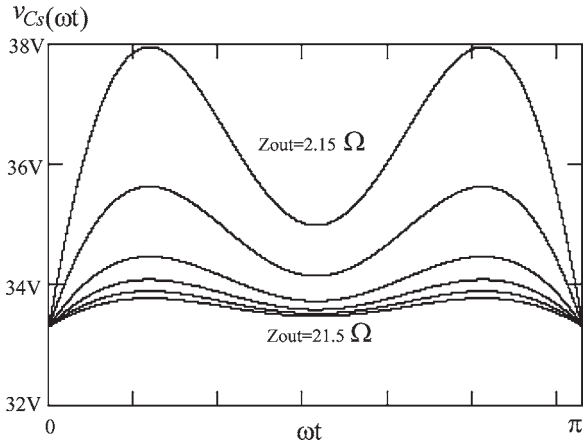

Fig. 5. Capacitor clamping voltage behavior.

C. Load Impedance

The load impedance is obtained from

$$Z_{\rm out} = \sqrt{2.15^2 + (2 \cdot \pi \cdot 60 \cdot 500\mu)^2} \cong 2.15\ \Omega. \tag{26}$$

D. Diode Selection

For satisfactory performance of the inverter, it is important to choose a slow recovery diode. Therefore, it has been decided to use the diode SEMIKRON SKKD 81/12 (its characteristics are shown in Table II).

E. Switching Period

$$T_S = \frac{1}{f_S} = \frac{1}{20} = 50\ \mu\text{s}. \tag{27}$$

F. Reverse Recovery Current

The reverse recovery current is given by

$$i_r = \sqrt{\frac{4}{3} \times 120\mu \times \frac{400}{10\mu}} = 83.2\ \text{A}. \tag{28}$$

G. Clamping Voltage Capacitor Behavior

Using (19), the curves described in Fig. 5 are obtained. For $Z_{\rm OUT} = 2.15\ \Omega$, the maximum clamping voltage is 38 V. We can observe that the voltage increment across the switches is smaller than in a conventional inverter.

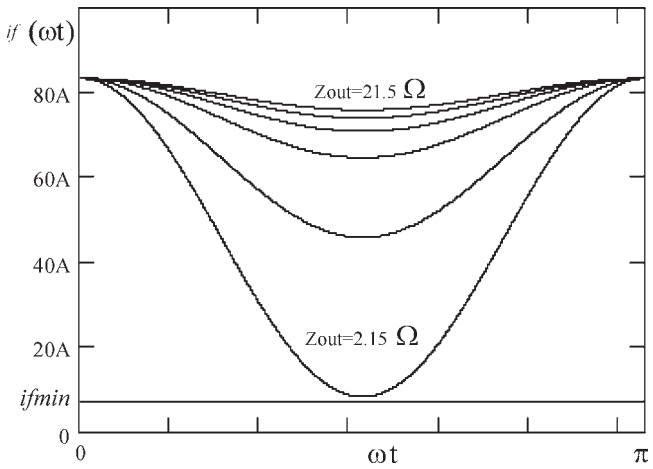

Fig. 6. Current i_f behavior.

TABLE III
PROTOTYPE SPECIFICATIONS

Q_1, Q_2, Q_A	(IGBT GA250TS60U) Manufactured by IR
D_1, D_2, D_A	(SKKD81/12) Manufactured by SEMIKRON
C_1, C_2, C_A	(Component's Intrinsic Capacitance ≈1.5nF)
L_S	(10μH; Ferrite Core EE55/39; N=20 turns)
C_S	(4 x 1000μF/350V; Electrolytic Capacitor)
L_{OUT}	(500μH, Output Inductor)
R_{OUT}	(2.15Ω; Output Resistor)

H. Behavior of the Current i_f

The behavior of the current i_f, which is obtained from (2) and (22), can be seen in Fig. 6.

It can be seen that current i_f has a minimum point that is located at $\pi/2$, and the intensity of the current is reduced with the increase of the load. To guarantee a ZVS condition in all load ranges, the minimum value of current i_f, which is obtained from (23), must be greater than the value obtained from (2), i.e.,

$$i_{f\min} = 83.2 - \frac{400 \cdot 0.9^2}{2 \cdot 2.15} = 7.85 \text{ A} \tag{29}$$

$$i_{f\min} \geq 400\sqrt{\frac{1.5n + 1.5n}{10\mu}} = 6.93 \text{ A} \tag{30}$$

$$7.85 \text{ A} \geq 6.93 \text{ A}. \tag{31}$$

VI. EXPERIMENTAL RESULTS

An inverter prototype rated 7.5 kW, which operates with PWM strategy, was built to evaluate the proposed circuit. The main specifications and components are given in Table III.

A. Experimental Waveforms

In the figures presented below, we can observe the experimental waveforms obtained from the laboratory prototype.

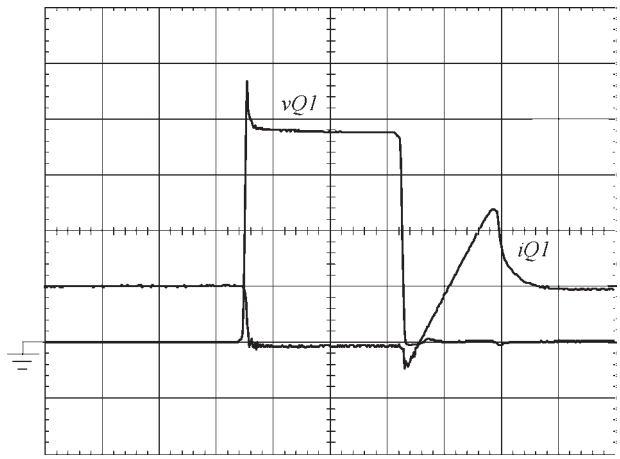

Fig. 7. Voltage and current in Q_1, including D_1 and C_1. 100 V/div, 50 A/div, 2 μs/div.

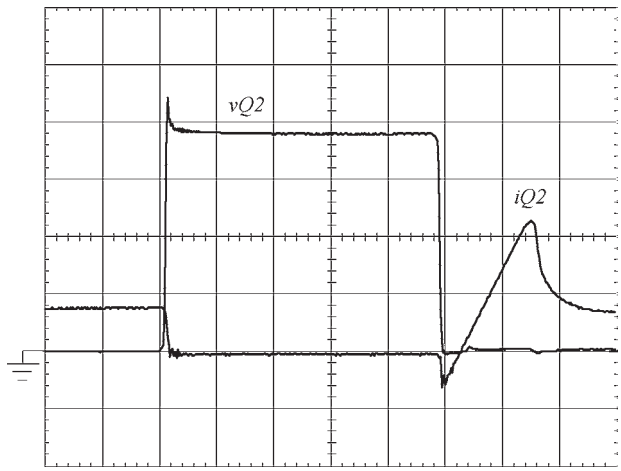

Fig. 8. Voltage and current in Q_2, including D_2 and C_2. 100 V/div, 50 A/div, 2 μs/div.

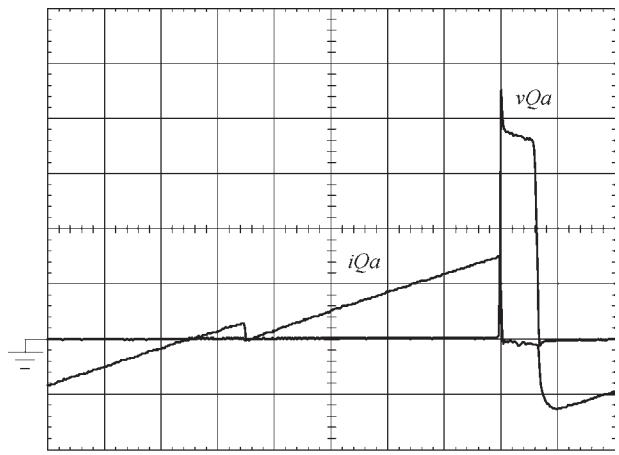

Fig. 9. Voltage and current in Q_A, including D_A and C_A. 100 V/div, 50 A/div, 10 μs/div.

Figs. 7–9 show the voltage across and the current through the switches. We can observe that for all switches, including the auxiliary one, the commutation occurs under ZVS conditions, which confirms the theoretical analysis. In Fig. 10, the current in the commutation auxiliary inductor for a switching period can be observed.

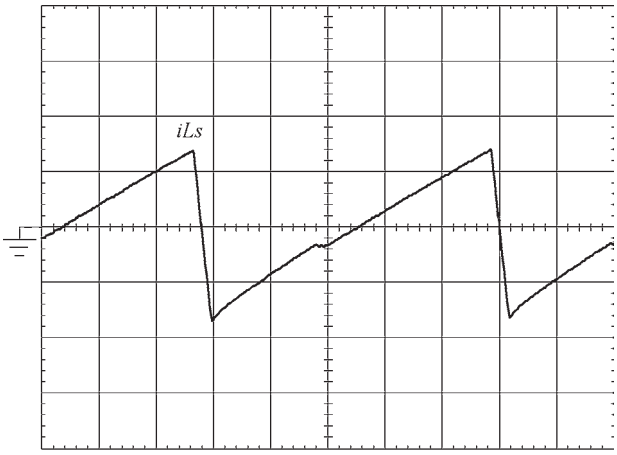

Fig. 10. Current in L_S (50 A/div, 10 μs/div).

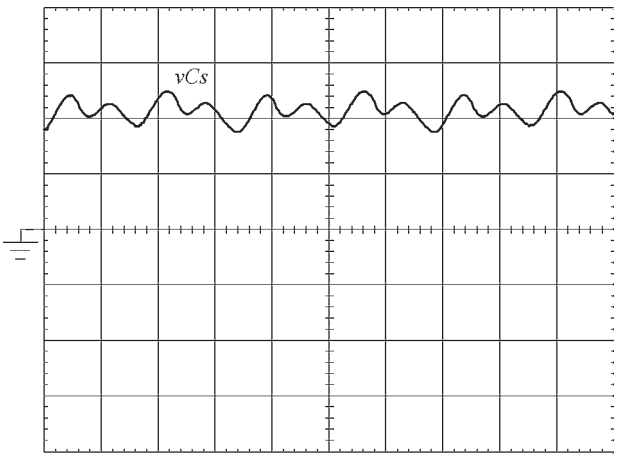

Fig. 11. Voltage in C_S (10 V/div, 5 ms/div).

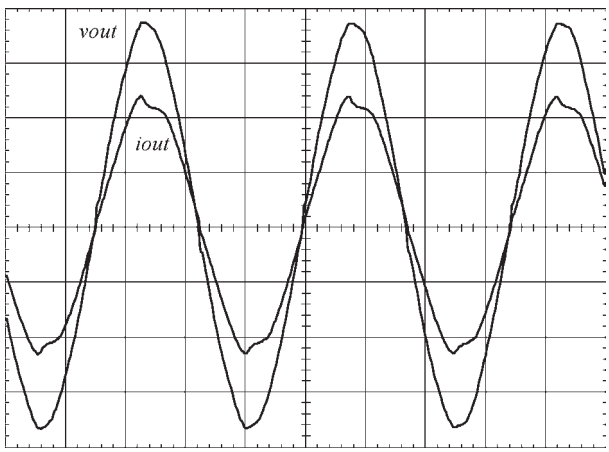

Fig. 12. Output voltage and current (50 V/div, 50 A/div, 5 ms/div).

The voltage across clamping capacitor C_S is shown in Fig. 11. We can note a very low voltage across C_S, which represents a minimal voltage stress across the devices. The output voltage and the current are presented in Fig. 12. Fig. 13 shows the efficiency as a function of the load range.

The efficiency was obtained using two wattmeters (Yokogawa Digital Power Meter WT230). One was put in the dc bus, and the other was put in the load resistance after the filter.

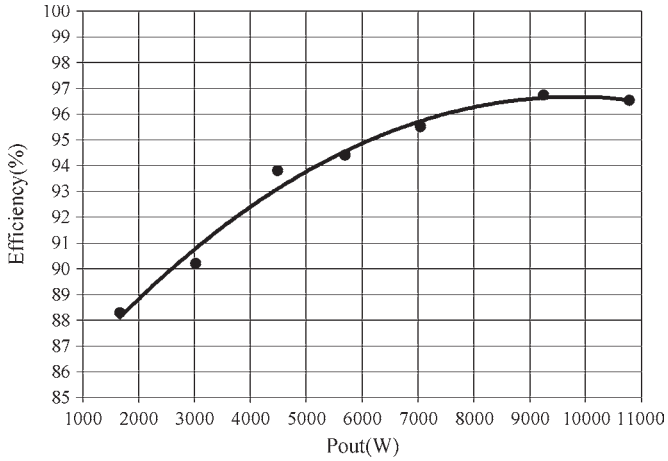

Fig. 13. Efficiency over the output range.

VII. Conclusion

A ZVS PWM inverter with active voltage clamping technique using the reverse recovery energy of the diodes has been developed. The operation stages for a steady-state condition, mathematical analysis, main waveforms, and experimental results were presented. The experimental results show a low voltage across the clamping capacitor. Switching losses are reduced due to the implementation of a simple active snubber circuit, which provides ZVS conditions for all the switches, including the auxiliary one. The reduced number of components and the simplicity of the structure increase its efficiency and reliability and make it suitable for practical applications. The proposed circuit presents soft commutation for all load ranges, which confirms the theoretical studies.

This topology presents certain advantages when compared to the conventional soft commutation inverters presented in the literature:

- soft commutation in all load ranges;
- simple structure with a low number of components;
- the use of a classical PWM modulation;
- auxiliary switch works with a constant duty cycle in all operation stages;
- the use of slow and low-cost rectifier diodes;
- low clamping voltage across the capacitor;
- simple design procedure with few restrictions;
- high efficiency.

With these characteristics, the authors believe that the proposed inverter circuit can be very useful for several industrial applications such as ac drive systems, power factor correction, uninterruptible power system, active filters, and induction heating.

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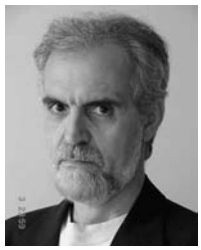

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