Zero-Voltage-Switching Half-Bridge DC–DC Converter With Modified PWM Control Method

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***Abstract*—Asymmetric control scheme is an approach to achieve zero-voltage switching (ZVS) for half-bridge isolated dc–dc converters. However, it is not suited for wide range of input voltage due to the uneven voltage and current components stresses. This paper presents a novel "duty-cycle-shifted pulse-width modulated" (DCS PWM) control scheme for half-bridge isolated dc–dc converters to achieve ZVS operation for one of the two switches without causing the asymmetric penalties in the asymmetric control and without adding additional components. Based on the DCS PWM control scheme, an active-clamp branch comprising an auxiliary switch and a diode is added across the isolation transformer primary winding in the half-bridge converter to achieve ZVS for the other main switch by utilizing energy stored in the transformer leakage inductance. Moreover, the auxiliary switch also operates at ZVS and zero-current switching (ZCS) conditions. Furthermore, during the off-time period, the ringing resulted from the oscillation between the transformer leakage inductance and the junction capacitance of two switches is eliminated owing to the active-clamp branch and DCS PWM control scheme. Hence, switching losses and leakage-inductance-related losses are significantly reduced, which provides the converter with the potential to operate at higher efficiencies and higher switching frequencies. The principle of operation and key features of the proposed DCS PWM control scheme and two ZVS half-bridge topologies are illustrated and experimentally verified.**

***Index Terms*—Duty-cycle-shifted (DCS), half bridge (HB), metal oxide semiconductor field effect transistors (MOSFETs), pulse-width modulated (PWM), zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

SEVERAL new techniques for high frequency dc–dc conversion have been proposed to reduce component stresses and switching losses while achieving high power density and improved performance [1]–[11]. Among them, the phase-shifted zero-voltage-switching (ZVS) full bridge [1]–[3] is one of the most attractive techniques since it allows all switches to operate at ZVS by utilizing transformer leakage inductance and metal oxide semiconductor field effect transistors' (MOSFETs) junction capacitance without adding an auxiliary switch. However, the complexity of the full-bridge is almost highest among the conventional topologies due to its large switch count and complicated control and driving. Active-clamp forward topology [4]–[6] is another typical example to successfully realize ZVS for the switches by utilizing the leakage inductance, magnetizing inductance and junction capacitance. However, the topology of the converter is asymmetric and the energy-delivery is unidirectional. In other words, voltage and current stresses are unevenly distributed, which results in the individual switch and rectifier stresses being higher compared to symmetric half-bridge and full-bridge converters. This disadvantage limits power level of the active-clamp forward topology applications. In addition, dc bias of magnetizing current may exist in the transformer [5].

Half bridge (HB) dc–dc converter is an attractive topology for middle power level applications owing to its simplicity. There are two conventional control schemes for the HB dc–dc converter, namely, symmetric control and asymmetric (complimentary) control. The main drawback of the conventional symmetric control is that both primary switches in the converter operate at hard switching condition. Moreover, during the off-time period of two switches, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and electromagnetic interference (EMI) emissions due to reverse recovery of MOSFETs body diodes. To suppress the ringing, resistive snubbers are usually added. As a result, energy in the transformer leakage inductance is significantly dissipated in snubbers. Therefore, the symmetric-control half bridge is not a good candidate for high switching frequency power conversion.

The asymmetric (complementary) control was proposed to achieve ZVS operation for HB switches [7]–[11]. Two drive signals are complementarily generated and applied to high side and low side switches. Thus, the two HB switches may be turned on at ZVS conditions owing to the fact that the transformer primary current charges and discharges the junction capacitance. However, asymmetric stresses distribution on the corresponding components may occur due to the asymmetric duty cycle distribution for the two primary switches. In other words, current stresses in the two primary switches are not identical and voltage and current stresses on secondary rectifiers are not equal. As a result, diodes or synchronous rectifiers with higher voltage rating are needed at the penalty of degrading the performance and efficiency of the rectifier stage [10]. Furthermore, the dc gain ratio of the converter is nonlinear, thus higher duty cycle variation is needed for the same input voltage variation in comparison with symmetric PWM control scheme, which makes the converter operate further beyond the optimum operating point at high

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input voltage [10]. Therefore, the complementary (asymmetric) PWM control is more suitable for applications where the input voltage is fixed. As a solution to reduce the duty cycle variation for wide input voltage range, an asymmetric transformer turns ratio together with integrated-magnetic structure was proposed in [10], such that rectifiers with lower withstanding voltage may be used to improve the performance. However, the power delivery of the transformer and current stresses in the switches and rectifiers are still uneven [10].

In this paper, a new control scheme, to be known as duty-cycle shifted PWM (DCS PWM) control, is proposed and applied to the conventional HB dc–dc converters to achieve ZVS for one of the two switches without adding extra components and without adding asymmetric penalties of the complementary control. The concept of this new control scheme is shifting one of the two symmetric PWM driving signals close to the other, such that ZVS may be achieved for the lagging switch due to the shortened resonant interval. Unlike the asymmetric control, the width of the duty cycle for the two switches is kept equal, such that all corresponding components work at the conditions with even stresses as the case in the symmetric control scheme.

Moreover, based on the DCS PWM control, a new half-bridge topology is proposed to achieve ZVS for the other switch and auxiliary switch by adding an auxiliary switch and diode in the conventional half bridge. ZVS for the other switch is achieved by utilizing the energy trapped in the leakage inductance. In addition, the proposed topology with DCS PWM control eliminates the ringing resulting from the oscillation between the transformer leakage inductance and the switches junction capacitances during the off-time period. Therefore, the proposed converter has a potential to operate at higher efficiencies and switching frequencies. The principle of operation and features of the DCS PWM control and proposed topologies are illustrated and verified experimentally on 36–75 V input voltage prototypes.

Section II describes the DCS PWM control scheme. Section III presents the principle of operation and features of the proposed ZVS half-bridge topology with the DCS PWM control scheme. In Section IV, a modified DCS controlled ZVS HB topology is presented. Experimental results and comparisons are presented in Section V and the conclusion is given in Section VI.

II. DCS PWM Control Scheme

Fig. 1 shows the half-bridge dc–dc converter with current doubler rectifier. The ideal waveforms for the symmetric PWM control is sketched in Fig. 2(a), where L_k, is the leakage inductance; ip, i_M are the transformer primary-side input and magnetizing currents, respectively; and $i_{\rm D1}$ is the forward current through rectifier diode D_1. Besides the hard switching, conventional symmetric PWM control has transformer-leakage-inductance related disadvantages. During the off-time period when both switches are off, the energy stored in the transformer leakage inductance may be recycled to primary dc bus through body diodes of MOSFETs. However, because of reverse recovery current of body diodes, the oscillation between the transformer leakage inductance and the MOSFETs' junction capacitance is significant on the primary side. To suppress the ringing, usually, snubber circuits are necessarily added, but losses dissipated in the snubber become dramatically large, especially at high input current and high switching frequencies.

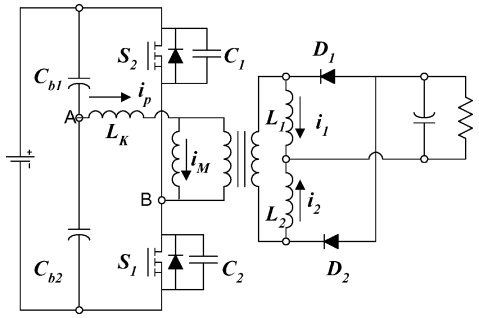

Fig. 1. Conventional half bridge converter with a current doubler rectifier.

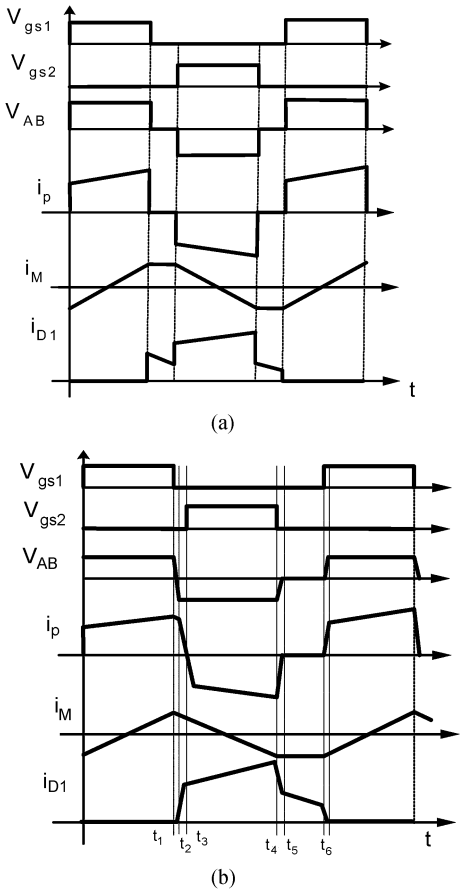

Fig. 2. Waveforms comparison of the half bridge dc–dc converter: (a) symmetric PWM control and (b) DCS PWM control.

A. Proposed DCS PWM Control Scheme

Fig. 2(b) shows the key waveforms of the half-bridge converter with the proposed DCS PWM control. Based on symmetric PWM control, S_2 driving signal $V_{\rm gs2}$ is shifted left such that the $V_{\rm gs2}$ rising edge is close to the falling edge of S_1 driving signal $V_{\rm gs1}$. When S_1 is turned off, the transformer primary current charges the junction capacitance of switch S_1 and discharges the junction capacitance of switch S_2. After the voltage across drain-to-source of S_2 drops to zero, the body diode of S_2 conducts to carry the current. During the body diode conduction period, S_2 may be turned on at zero-voltage switching. No ringing occurs during the transition period.

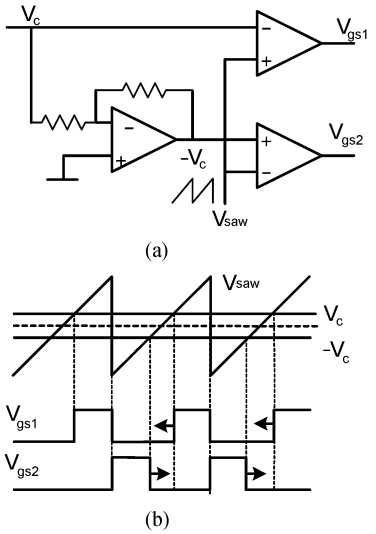

Fig. 3. DCS PWM modulation scheme: (a) modulation circuits and (b) key waveforms.

Fig. 3 shows a possible modulation approach for the realization of DCS PWM control. Where, Vsaw is the SAW carrier waveform for modulation; V_c and $-V_c$ are control voltages derived from the front voltage or current controller. By modulating V_c and $-V_c$, driving signals for S_1 and S_2 can be generated, respectively. Because the falling time of the saw waveform is short, the falling edge of S_1 is always close to the rising edge of S_2, which provide a possibility of ZVS for S_2. This modulation method differs from the conventional symmetric PWM method in that the direction of variation of the two duty cycles is opposite as shown in Fig. 3(b) by the arrows shown on the driving signals waveforms. In other words, since V_c and $-V_c$ are symmetrically centered around zero, the duty cycle of S_1 is regulated by moving its rising edge left and right, while the duty cycle of S_2 is regulated by moving its falling edge right and left, keeping S_1 and S_2 with the same duty cycle.

B. Principle of Operation

To simplify the analysis of operation, components are considered ideal except otherwise indicated. The main operation modes are described as follows.

Mode 1 $(t < t_1)$: Initially, S_1 is conducting, and the input power is delivered to the output. L_1 is charged and L_2 freewheels through D_2.

Mode 2 $(t_1 < t < t_2)$: S_1 is turned off at $t = t_1$, causing the primary current i_p to charge C_1 and discharge C_2. During the interval, the reflected secondary inductor current dominates the primary current ip. Thus, C_2 may be discharged to zero at wide load range, which means wide ZVS range can be achieved for S_2.

Mode 3 $(t_2 < t < t_3)$: When the voltage across C_2 is discharged to zero at $t = t_2$, the body diode of S_2 conducts to carry the current, which provides ZVS condition for switch S_2. During this period, leakage inductance is reset and secondary current i_1 and i_2 freewheel through D_1 and D_2, respectively.

Mode 4 $(t_3 < t < t_4)$: S_2 is turned on with ZVS at $t = t_3$; the primary current decreases to zero and then becomes negative. When the negative peak current equals to the reflected L_2 current, the diode D_2 is blocked and the converter starts to deliver power to the output. The inductor L_2 is charged and inductor L_1 current continues to freewheel.

Mode 5 $(t_4 < t < t_5)$: S_2 is turned off at $t = t_4$, causing the primary current i_p to charge C_2 and discharge C_1. When the secondary D_1 and D_2 start to freewheel, leakage inductance and junction capacitance of switches S_1 and S_2 start to oscillate on the primary side. During the interval, body diodes may be involved, which worsens the ringing and results in reverse recovery losses. (The ringing waveforms are not shown in the Figure.)

Mode 6 $(t_5 < t < t_6)$: The oscillation comes to the end with equal voltage across switches S_1 and S_2. On the secondary side, L_1 and L_2 keep freewheeling. At $t = t_6$, S_1 is turned on again going back to Mode 1.

C. Main Features Compared With Symmetric and Asymmetric PWM Control

Compared with the conventional symmetric PWM control, DCS PWM controlled HB has the same voltage and current stresses in the primary switches, and although the transformer voltage and current waveforms are different from those of the symmetric PWM control, the voltage-second value and magnetizing B-H loop of the transformer are identical. The peak and *rms* currents through the transformers are also the same for both schemes. Hence, there is no change in characteristics and design of the transformer from the symmetric PWM control to DCS PWM control.

In the secondary side, as shown in Fig. 2, even though the currents through rectifiers have different waveforms in the two schemes, the peak and *rms* values of the waveforms are equal. Moreover, the inductors voltage-second value, current peak and current *rms* values are the same for both schemes. Therefore, the voltage and current stresses for the secondary-side switches and inductors are the same for both schemes. Consequently, there is no change in the components selection and converter design with the change of control scheme from symmetric PWM control to the proposed DCS PWM control.

As mentioned above, both symmetric PWM and DCS PWM have even voltage and current stresses in corresponding components thanks to the identical duty cycle width for two switches. Hence, there are no asymmetric penalties in asymmetric PWM control, which allows DCS PWM control to be employed in applications for wide input voltage range. Furthermore, in the DCS PWM control, ZVS for switch S_2 is achieved without adding additional components. In addition, wide ZVS range operation may be achieved because the secondary inductor current is reflected to transformer primary side to the discharge the output capacitor of switch S_2 to create ZVS condition for switch S_2. Because switching losses and transformer leakage-inductance-related losses are reduced, higher efficiency is expected with the DCS PWM control method.

A comparison between the asymmetric HB, symmetric HB and DCS HB under same design conditions is shown in Table I, where N is the transformer turn ratio, D is the duty cycle of the switch S_1, I_o is the load current, V_{in} is the input voltage, and V_{out} is the output voltage. The filter inductance and output capacitance values are assumed large enough such that the

TABLE I
COMPARISONS OF HALF BRIDGE CONVERTERS UNDER SEVERAL CONTROL SCHEMES

	Symmetric HB	Asymmetric HB	DCS HB
DC gains	$V_{out}=\frac{DV_{in}}{2N}$	$V_{out}=\frac{D(1-D)V_{in}}{N}$	$V_{out}=\frac{DV_{in}}{2N}$
DC Bias of magnetizing current	$I_{DC}=0$	$I_{DC}=\frac{(1-2D)}{2}I_O$	$I_{DC}=0$
Stresses of switch S_1	$V_{ds1}=V_{in}$ $Irms=\frac{I_o}{2N}\sqrt{D}$	$V_{ds1}=V_{in}$ $Irms=\frac{I_o(1-D)\sqrt{D}}{N}$	$V_{ds1}=V_{in}$ $Irms=\frac{I_o}{2N}\sqrt{D}$
Stresses of switch S_2	$V_{ds1}=V_{in}$ $Irms=\frac{I_o}{2N}\sqrt{D}$	$V_{ds2}=V_{in}$ $Irms=\frac{I_oD\sqrt{1-D}}{N}$	$V_{ds1}=V_{in}$ $Irms=\frac{I_o}{2N}\sqrt{D}$
Stresses of rectifier D_1	$V_{d1}=\frac{V_{in}}{2N}$ $Irms=\frac{I_o}{2}\sqrt{2D+1}$	$V_{d1}=\frac{(1-D)V_{in}}{N}$ $Irms=I_o\sqrt{1-D}$	$V_{d1}=\frac{V_{in}}{2N}$ $Irms=\frac{I_o}{2}\sqrt{2D+1}$
Stresses of rectifier D_2	$V_{d2}=\frac{V_{in}}{2N}$ $I_{rms}=\frac{I_o}{2}\sqrt{2D+1}$	$V_{d1}=\frac{DV_{in}}{N}$ $I_{rms}=I_o\sqrt{D}$	$V_{d2}=\frac{V_{in}}{2N}$ $I_{rms}=\frac{I_o}{2}\sqrt{2D+1}$

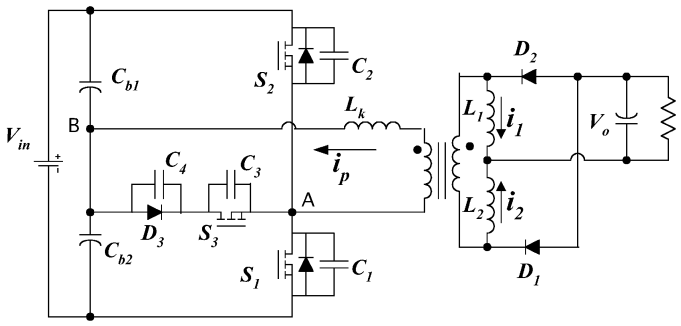

Fig. 4. Proposed DCS controlled ZVS HB dc–dc converter.

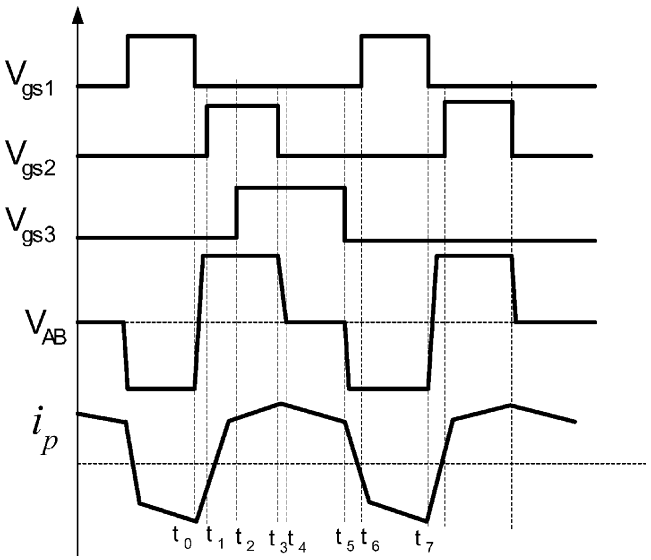

Fig. 5. Key waveforms for the DCS controlled dc–dc converter.

inductor currents and output voltage is regarded as constant current source and constant voltage source, respectively. From Table I, it can be observed that DCS HB has the same stresses distribution as the symmetric HB, while asymmetric HB has asymmetric stresses distribution, dc bias of the magnetizing current and nonlinear dc gain. These features make asymmetric HB unsuitable for applications with wide input voltage range.

In the DCS controlled HB converter, the current waveforms and values through inductors L_1 and L_2 are same as those of the symmetric HB converter. In the symmetric HB converter, the inductor current ripples are interleaved, thus the output current ripple cancellation is achieved at the whole duty cycle range $(0 < D < 0.5)$. In other words, output current ripple is always smaller than individual inductor current ripple. However, in the DCS HB converter, the current cancellation is weakened due to the shifted duty cycle. Analysis shows that the current cancellation takes effect only at the duty cycle range of $0.33 < D < 0.5$, which means the current cancellation is lost at the duty cycle range of $0 < D < 0.33$.

III. ZVS HALF BRIDGE TOPOLOGY WITH DCS PWM CONTROL

As described in Section II, ZVS of switch S_2 is achieved by using the DCS PWM control scheme. However, switch S_1 still

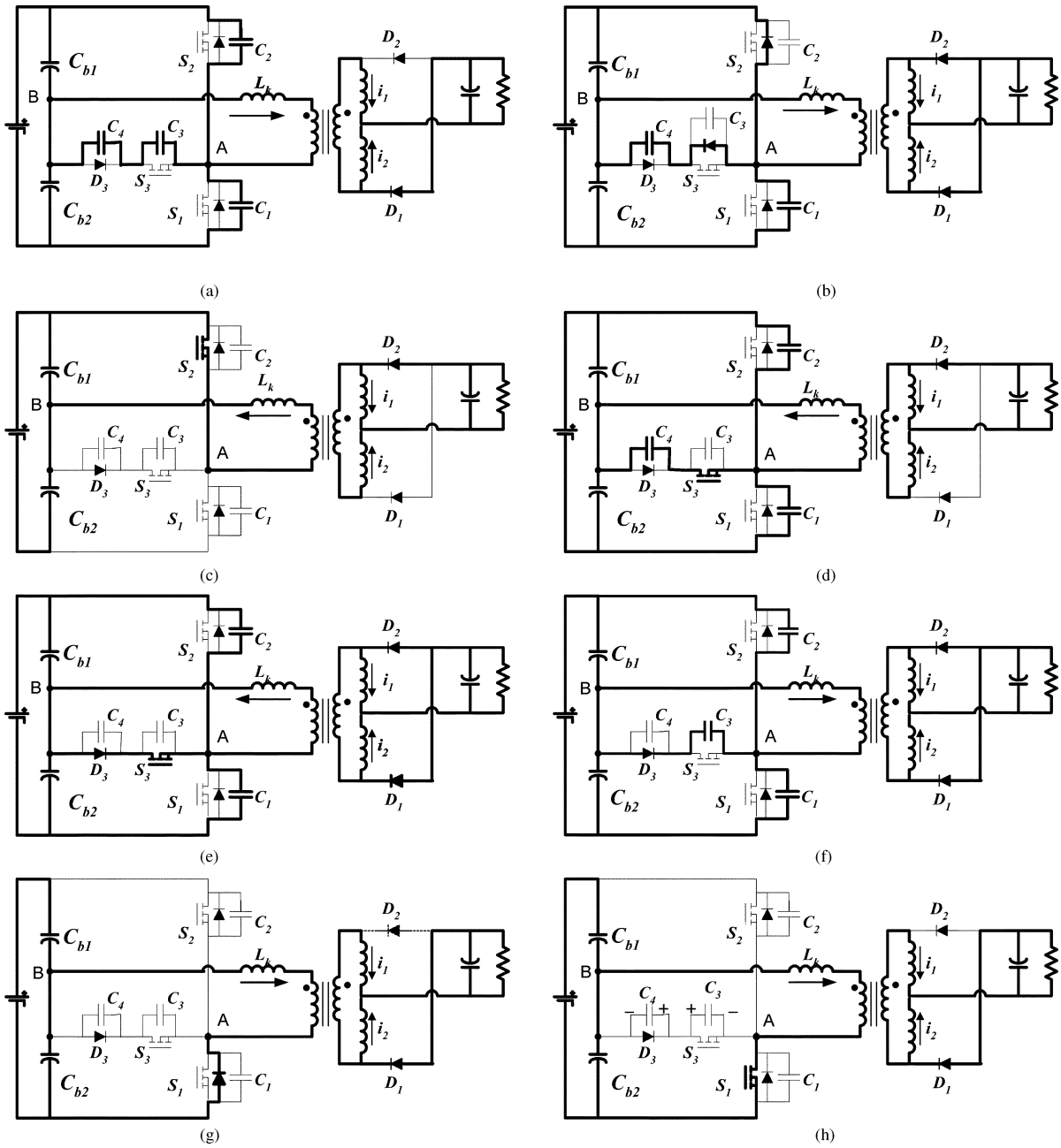

Fig. 6. Operation modes of the proposed ZVS converter (mode 1–mode 8).

operates at hard-switching condition. To achieve ZVS for S_1, a new ZVS topology is proposed as shown in Fig. 4, where L_k is the transformer leakage inductance, C_1, C_2 and C_3 are the external capacitors including junction capacitance of the associated switches, and C_4 is the external capacitor across the diode D_3. The key waveforms of the topology are showed in the Fig. 5. Basically, energy stored in the leakage inductance can be employed to discharge junction capacitances to achieve ZVS. Auxiliary switch S_3 and diode D_3 are added to provide a path for the leakage inductance current during the period when both S_1 and S_2 are off (off-time interval). In other words, leakage inductance energy is trapped via the path during the off-time interval until it is needed. As shown in Fig. 5, before S_1 is turned on, S_3 is turned off to release the trapped energy in the leakage inductance to discharge output capacitances of switches to create ZVS for the switch S_1.

A. Principal of Operation

To simplify the analysis of operation, components are considered ideal except otherwise indicated. The main equivalent circuits for main operation modes are shown in Fig. 6.

Mode 1 $(t_0 < t < t_1)$: Before this mode, $t < t_0$, S_1 was turning on and the transformer delivers power to the output; At $t = t_0$, S_1 is turned off, causing the current i_p to charge C_1 and C_4 and discharge C_2 and C_3.

Mode 2 $(t_0 < t < t_1)$: When the C_3 voltage is discharged to zero, the body diode of switch S_3 conduct to continually charge C_4. Then the voltage across C_2 is discharged to zero, and the body diode of S_2 conducts to carry the current, which provides ZVS condition for the switch S_2. During this interval, inductor current i_1 and i_2 freewheel through D_2 and D_1, respectively.

Mode 3 $(t_1 < t < t_3)$: S_1 is turned on with ZVS at $t = t_1$, and the transformer leakage inductance current is reset to zero and reverse-charged. When the transformer primary current reaches the reflected current of i_2, diode D_1 is locked and the inductor L_2 start to be charged. At $t = t_2$, switch S_3 is turned on with zero voltage and zero current, i.e., ZVZCS.

Mode 4 $(t_3 < t < t_4)$: At $t = t_3$, S_2 is turned off, the primary transformer current discharges C_1 and C_4 while charging C_2.

Mode 5 $(t_4 < t < t_5)$: At $t = t_4$, the voltage across C_4 is discharged to zero forcing the leakage inductance current to flow through D_3 and S_3. During this interval, the leakage inductance current freewheels through D_3 and S_3 such that the energy in the leakage inductance is trapped. On the secondary side, inductor L_1 and L_2 currents freewheel through D_2 and D_1, respectively.

Mode 6 $(t_5 < t < t_6)$: At $t = t_5$, S_3 is turned off, causing C_2 and C_3 to be charged and C_1 to be discharged by the leakage inductance current.

Mode 7 $(t_5 < t < t_6)$: When the voltage across C_1 is discharged to zero, the body diode of S_1 conducts to recycle the energy in the transformer leakage inductance.

Mode 8 $(t_6 < t < t_7)$: At $t = t_6$, S_1 is turned on with ZVS, and then the leakage inductance current is reset to zero and reverse-charged. When the transformer primary current increases to the reflected current of i_1, D_2 is blocked and the converter starts to deliver power to the output.

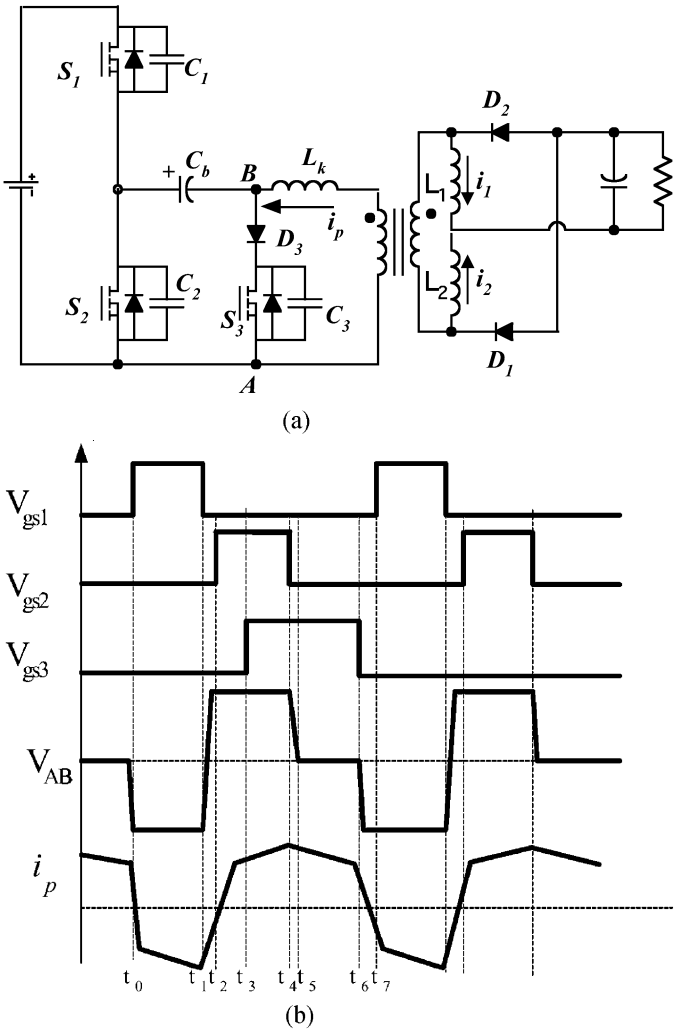

Fig. 7. Modified DCS PWM ZVS Hb dc–dc converter: (a) dc–dc converter and (b) key waveforms.

B. Features of the Proposed Topology

1) Generation of Driving Signals: Driving signals of switch S_1 and S_2 are generated as discussed in Section II for the DCS PWM modulation method and as shown in Fig. 3. Timing of driving signal for switch S_3 is not critical due to the fact that switch S_3 may be turned on at any time during the interval when switch S_2 is on. Driving signal for switch S_3 is simply obtained only by inverting the driving signal of switch S_1 and adding some delay time at the rising edge.

2) Voltage and Current Stresses: With DCS PWM control, the duty cycle width of the two half-bridge main switches are identical, and the voltage across the two leg-capacitors are equal, thus all voltage and current stresses in the corresponding components are evenly distributed. The asymmetric problems incurred to complimentary PWM control are eliminated. Concerning the voltage and current stresses in auxiliary switch S_3 and diode D_3, the voltage stresses are only half of those of the main switches and the current stresses are the same as those of the main switches. It is noted that there is no reverse recovery problem for the diode D_3, and that switch S_3 operate at ZVZCS turn-on and nearly ZVS turn-off.

3) ZVS Range for Main Switch S_1 and S_2: In the phase-shifted full-bridge converter, the load current reflected to the primary side is used to achieve the ZVS for the leading-leg switches [3]. Similarly, in the proposed topology, the reflected secondary inductor current may be used to achieve ZVS of switches. Specifically, the ZVS of switch S_2 is achieved by the same manner as that of the leading-leg switches in the phase-shift full-bridge converter, thus the realization of ZVS is easy to obtain. However, the ZVS behavior of switch S_1 is not exactly the same as that of lagging-leg switches in the phase-shift full-bridge converter. ZVS range equation for two topologies is compared as follows:

In a full-bridge converter, in order to achieve ZVS of lagging-leg switches, the energy stored in the leakage inductance has to be larger enough to charge and discharge output capacitance [3]. Neglecting the transformer winding capacitance, the energy stored in the leakage inductance L_k has to satisfy [3]

$$E = \frac{1}{2} L_k I_p^2 \geq \frac{1}{2}(C_1 + C_2) V_{in}^2 \tag{1}$$

where I_p is the current through the transformer primary winding at the time when one of lagging switches is turned off; C_1 and C_2 are the output capacitance across the switches, respectively.

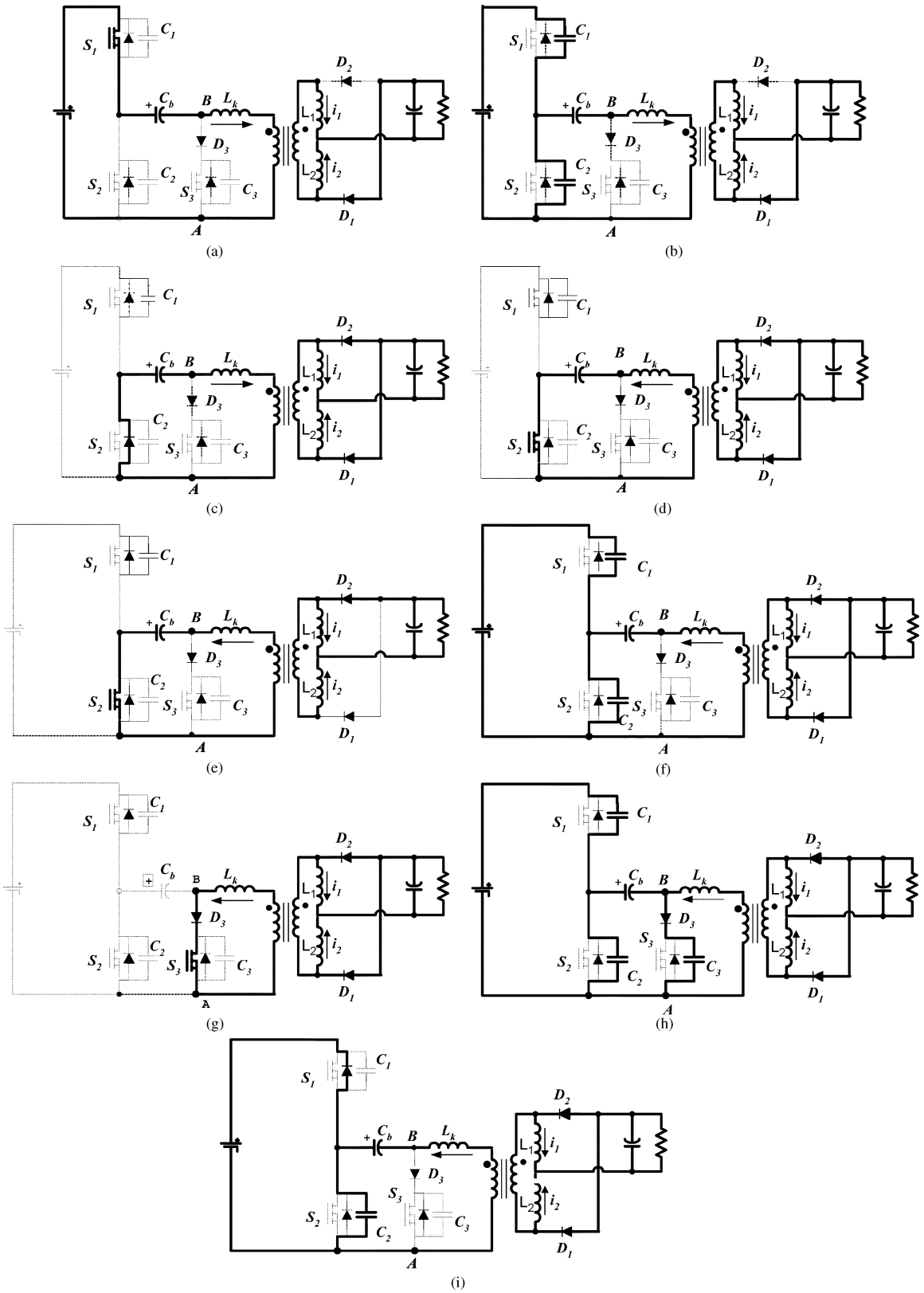

Fig. 8. Operation modes of the modified DCS HB dc–dc converter (mode 1–mode 9).

Assuming $C_1 = C_2 = C$, it follows that

$$E = \frac{1}{2} L_k I_p^2 \geq C V_{in}^2. \tag{2}$$

In the proposed topology, when switch S_2 is turned off, reflected secondary inductor current discharges C_1 and C_4 and charges C_2 until

$$v_{c1} = v_{c2} = \frac{V_{in}}{2} \text{ and } v_{c4} = 0. \tag{3}$$

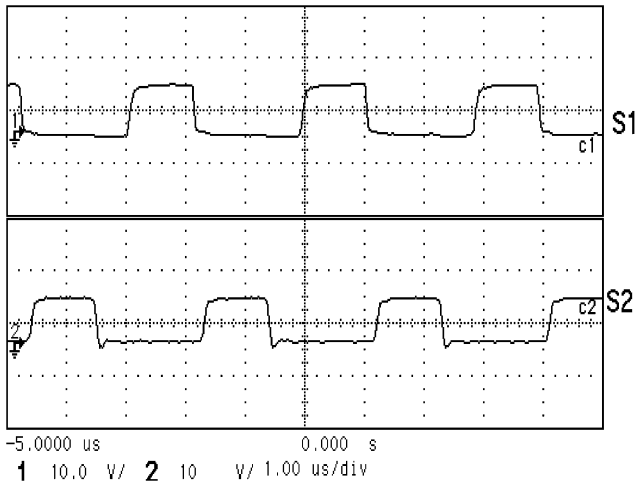

Fig. 9. Gate signals of the switches S_1 and S_2.

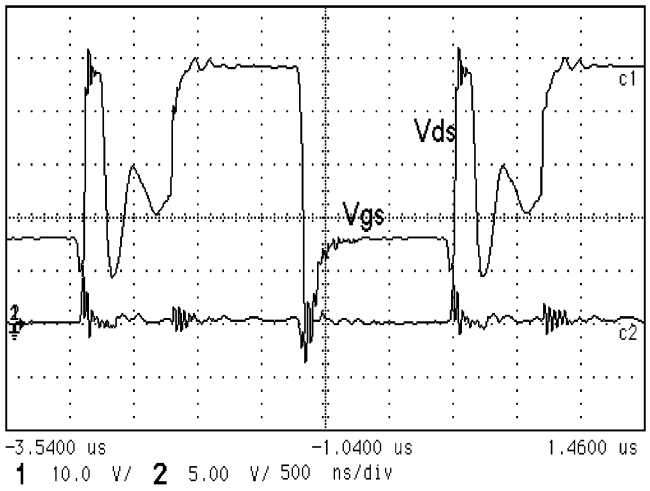

Fig. 10. Zero-voltage switching of the switch S_2.

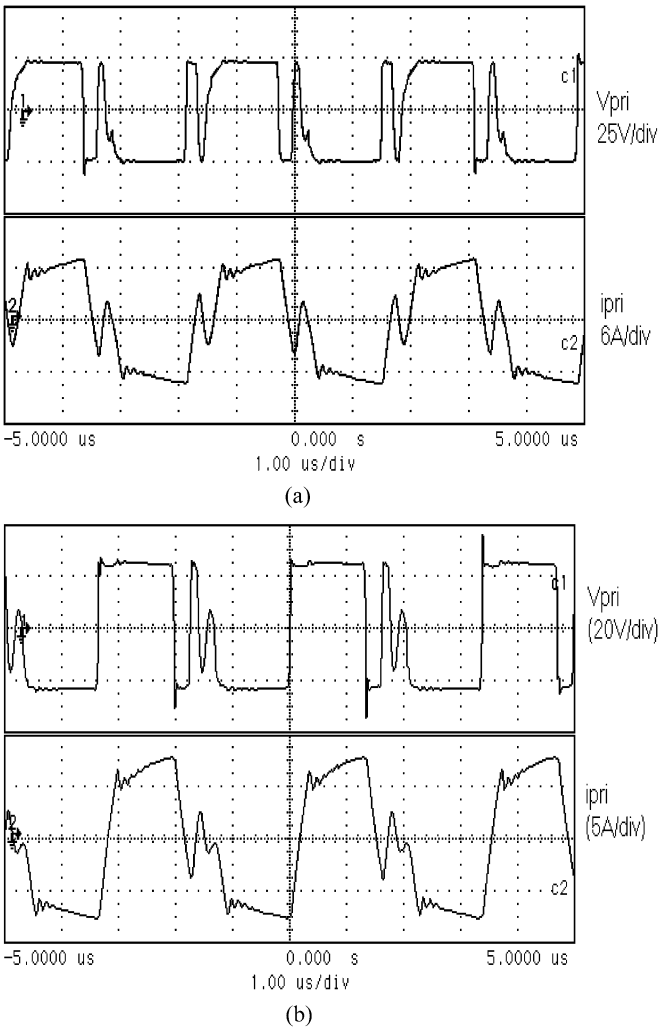

Fig. 11. Waveforms of transformer primary voltage and current: (a) Conventional symmetric PWM control and (b) DCS PWM control.

For this interval, because the primary current is the reflected output current, (3) is easily satisfied at wide load range. After the freewheeling mode, switch S_3 is turned off, the energy stored in the transformer leakage inductance is released to continue discharging C_1 and charging C_2 and C_3. In order to achieve ZVS for S_1, the energy in the leakage inductance L_k has to satisfy

$$E = \frac{1}{2}L_k I_p^2 \geq \frac{1}{8}V_{in}^2(C_1 + C_2 + C_3) \tag{4}$$

where C_3 is the junction capacitance of switch S_3. Assuming $C_1 = C_2 = C_3 = C$. It follows that:

$$E = \frac{1}{2}L_k I_p^2 \geq \frac{3}{8}CV_{in}^2. \tag{5}$$

Comparing (2) and (5), assuming that output capacitances across the switches in the proposed converter is equal to those of the full bridge, and that the energy stored in the leakage inductance is equal for the two topologies. The ZVS of switch S_1 in the proposed topology is more easily achieved than that of the lagging-leg switches in the full bridge.

4) ZVS and ZCS Behavior of the Switch S_3: Concerning the switching behavior of switch S_3, the ZVS of the switch S_3 depends on the capacitance of C_3 and C_4. In the analysis, it is assumed

$$V_{cb1} = V_{cb2} = \frac{V_{in}}{2}. \tag{6}$$

In mode 8 shown in Fig. 6, the voltages across C_3 and C_4 are

$$V_{c3} = \frac{V_{in}}{2}; V_{c4} = 0. \tag{7}$$

After S_1 is turned off, the capacitor C_3 is discharged and capacitor C_4 is charged as shown in mode 1 of Fig. 6. Because C_3 and C_4 are in series, the voltage across C_3 is

$$v_{c3}(t) = \frac{V_{in}}{2} - \frac{1}{C_3}\int i_c dt. \tag{8}$$

The voltage across C_4 is

$$v_{c4}(t) = \frac{1}{C_4}\int i_c dt. \tag{9}$$

It can be noted that when the voltage v_{c3} is discharged to zero, if the following inequality is satisfied:

$$v_{c4}(t) \leq \frac{V_{in}}{2}. \tag{10}$$

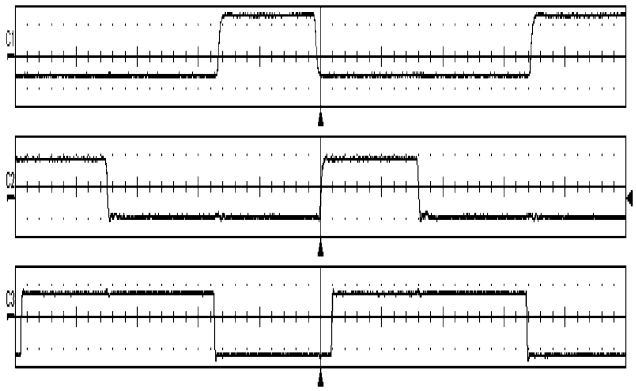

Fig. 12. Gate signals waveforms ($f_s = 400\,\mathrm{kHz}$) (from top to bottom: S_1, S_2, S_3, 500 nS/div).

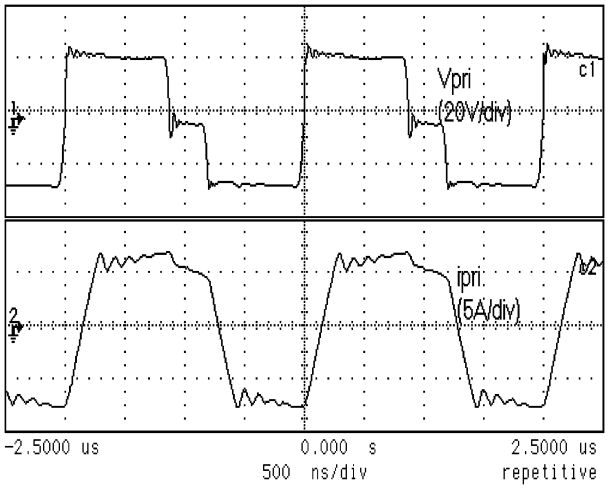

Fig. 13. Transformer primary voltage and current.

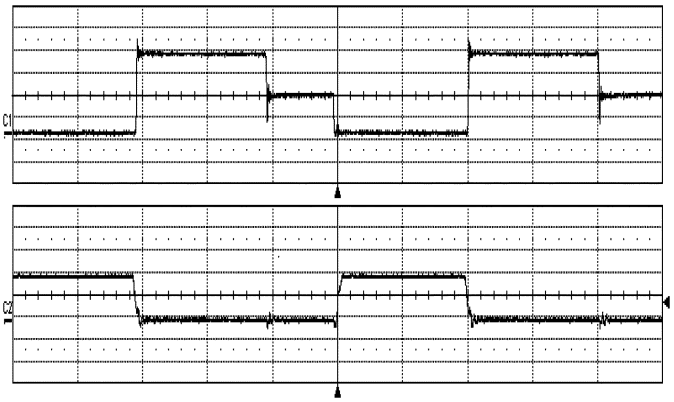

Fig. 14. ZVS waveforms of switch $S_1(f_s = 400\,\mathrm{kHz})$ [top trace: Vds (10 V/div); bottom trace: Vgs (5 V/div)].

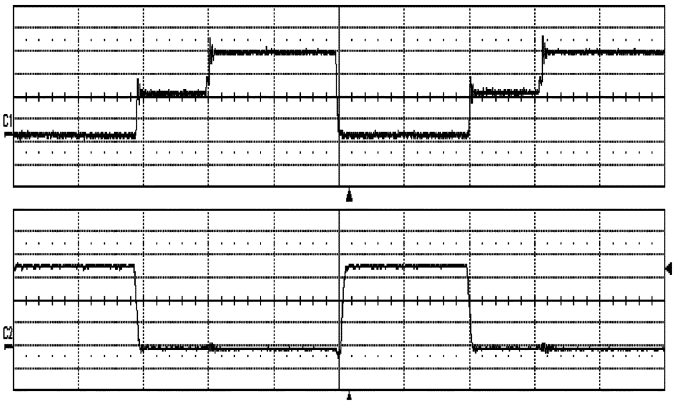

Fig. 15. ZVS waveforms of switch $S_2(f_s = 400\,\mathrm{kHz})$ [top trace: Vds (10 V/div); bottom trace: Vgs (2.5 V/div)].

Then the body diode of switch S_3 conducts to carry the current to charge C_4 continually until

$$V_{c4}(t) = \frac{V_{in}}{2}. \tag{11}$$

After that, the voltage across C_4 is clamped at the half of the input voltage and the C_3 voltage keeps zero, thus the switch S_3 may be turned on at zero voltage. From (8) through (10), the ZVS condition for the switch S_3 can be derived as

$$C_4 \geq C_3. \tag{12}$$

To achieve ZVS, an extra capacitor is added across the diode D_3. When S_3 is turned on at ZVS, also, there is no current flowing through the switch S_3, thus zero-voltage zero-current switching (ZVZCS) is achieved for the switch S_3.

IV. Modified ZVS Half Bridge DC–DC Converter With DCS Control

For the DCS HB dc–dc converter proposed in Sections II and III, the added switch S_3 is floating to the ground, and the bootstrap technique is usually used to drive floating switches. To simplify the architecture, a modified DCS ZVS HB dc–dc converter is proposed as shown in Fig. 7(a), where S_1 and S_2 are two main switches, and an auxiliary branch consists of S_3 and D_3. It is noted that the switch S_3 is grounded instead of floating in Fig. 4, and thus the drive circuitry becomes simple and reliable. The principle of operation is similar to the previous topology described in Section III, and the key waveforms are shown in Fig. 7(b), where drive signal of the switch S_2 is shifted left close to the falling edge of S_1 driving signal so that S_2 may achieve ZVS. During the on time of the switch S_2, switch S_3 turns on with ZVZCS. The transformer leakage inductance current freewheels through the auxiliary branch when the switch S_2 turns off. Later on, the switch S_3 turns off, and the leakage inductance energy is released to achieve ZVS for the switch S_1.

To simplify the analysis of operation, components are considered ideal except otherwise indicated. The main equivalent circuits for main operation modes are shown in Fig. 8.

Mode 1 $(t_0 < t < t_2)$: At $t = t_0$, S_1 turns on with ZVS. During the interval, the transformer primary current i_p was negative, and the secondary side diode D_2 was reverse-biased.

Mode 2 $(t_1 < t < t_2)$: At $t = t_1$, S_1 turns off causing the current i_p to charge C_1 and discharge C_2.

Mode 3 $(t_1 < t < t_2)$: When the voltage across C_2 is discharged to zero, the body diode of S_2 conducts to carry the current, which provides ZVS condition for the switch S_2. During this subinterval, the secondary side current i_1 and i_2 freewheel through D_2 and D_1, respectively.

Mode 4 $(t_2 < t < t_3)$: S_1 is turned on with ZVS at $t = t_2$, which causes the transformer leakage inductance current

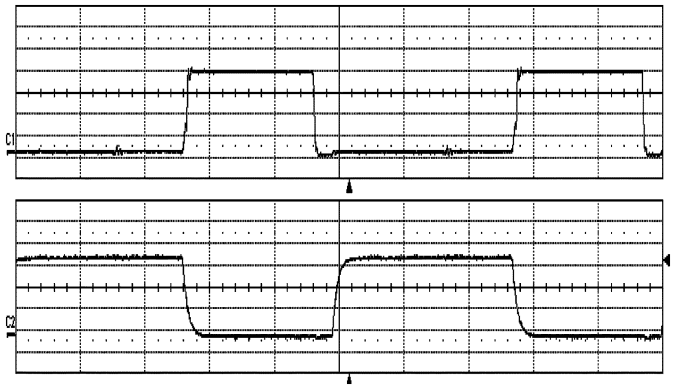

Fig. 16. ZVS waveforms of switch S_3 [top trace: Vds (5 V/div); bottom trace: Vgs (2.5 V/div)].

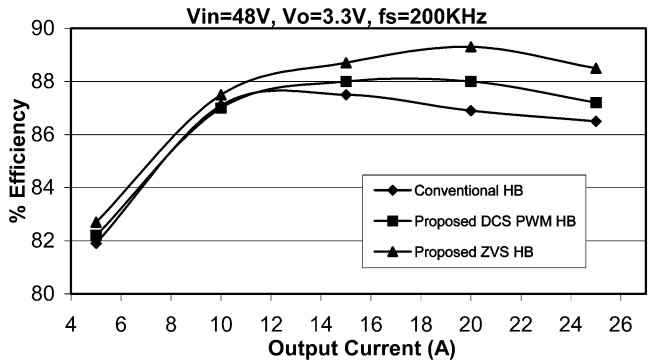

Fig. 17. Efficiency comparison ($f_s = 200\,\mathrm{kHz}$).

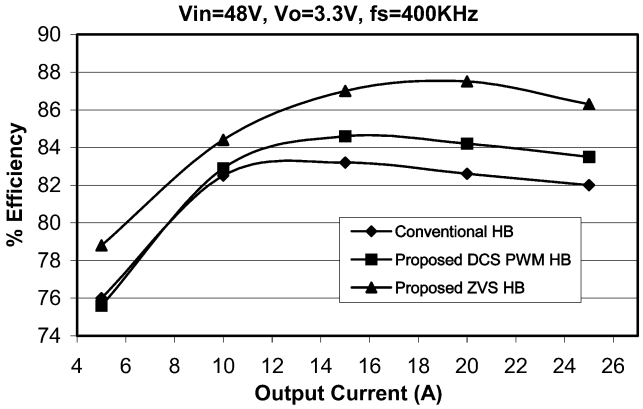

Fig. 18. Efficiency comparison ($f_s = 400\,\mathrm{kHz}$).

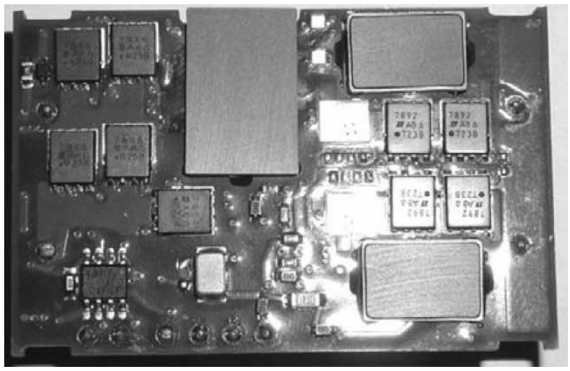

Fig. 19. Quarter-brick prototype of the modified DCS HB dc–dc converter.

to be reset to zero and reverse-charged while the output inductor currents keep freewheeling.

Mode 5 $(t_2 < t < t_4)$: When the primary transformer current reaches the reflected current of i_2, diode D_1 is blocked and the inductor L_2 is charged. At $t = t_3$, the switch S_3 turns on with ZCS, because D_3 is reverse-biased and no current goes through S_3 until S_2 is turned off.

Mode 6 $(t_4 < t < t_5)$: At $t = t_4$, S_2 is turned off, and the primary transformer current discharges C_1 while charging C_2.

Mode 7 $(t_5 < t < t_6)$: At $t = t_5$, the voltage across C_2 is charged to the voltage across the capacitor C_b, and then the leakage inductance current flows through D_3 and S_3. During this interval, the leakage inductance current freewheels through D_3 and S_3 such that the energy in the leakage inductance is trapped. On the secondary side, inductor L_1 and L_2 currents freewheel through D_2 and D_1, respectively.

Mode 8 $(t_6 < t < t_7)$: At $t = t_6$, S_3 is turned off, causing C_2 and C_3 to be charged and C_1 to be discharged by leakage inductance current.

Mode 9 $(t_6 < t < t_7)$: When the voltage across C_1 is discharged to zero, the body diode of S_1 conducts to recycle the energy in the transformer leakage inductance and offer a ZVS condition for switch S_1. Then it returns to Mode 1.

V. Experimental Verification and Comparison

An experimental prototype with 3.3 V/25 A output and 36 V–75 V input voltage was built in the laboratory to evaluate the proposed DCS PWM control and ZVS topology. For comparison, the symmetric PWM control and DCS PWM control are separately applied to the same conventional half bridge prototype as shown in Fig. 1; and the DCS PWM control is applied to the proposed ZVS half bridge topology shown in Fig. 4. Because of the low output voltage, synchronous rectifiers were used instead of the rectifier diodes in the converter. To make the comparison fair, closed-voltage-loop control is employed to tightly regulate the output voltage. In the prototype, IRFS59N10D is used for switch S_1 and S_2, 30CTQ060S is selected for D_3, Si4470EY is used for S_3, and Si4420DY is used for synchronous rectifiers. The transformer turns ratio is 4:2 and the measured primary-side leakage inductance is 180 nH.

Figs. 9 and 10 show experimental waveforms for the conventional half bridge converter with the DCS PWM control. Fig. 9 shows the experimental gate signals of the switches S_1 and S_2, while Fig. 10 shows the gate signal and drain-to-source voltage waveforms of switch S_2. It is clear that switch S_2 turns on at zero voltage. In Fig. 11, the transformer primary voltage and current waveforms for both DCS PWM control and symmetric PWM control are shown and compared on the conventional half bridge topology. It is noted that ringing is reduced to half in the DCS PWM control.

Figs. 12–16 show the waveforms for the proposed DCS-PWM-based ZVS half bridge topology. Fig. 12 shows the gate signals for switches S_1, S_2 and S_3. Fig. 13 shows waveforms of the transformer primary voltage and current at full load. Cleaner waveforms can be observed compared with waveforms of the conventional HB topology due to the

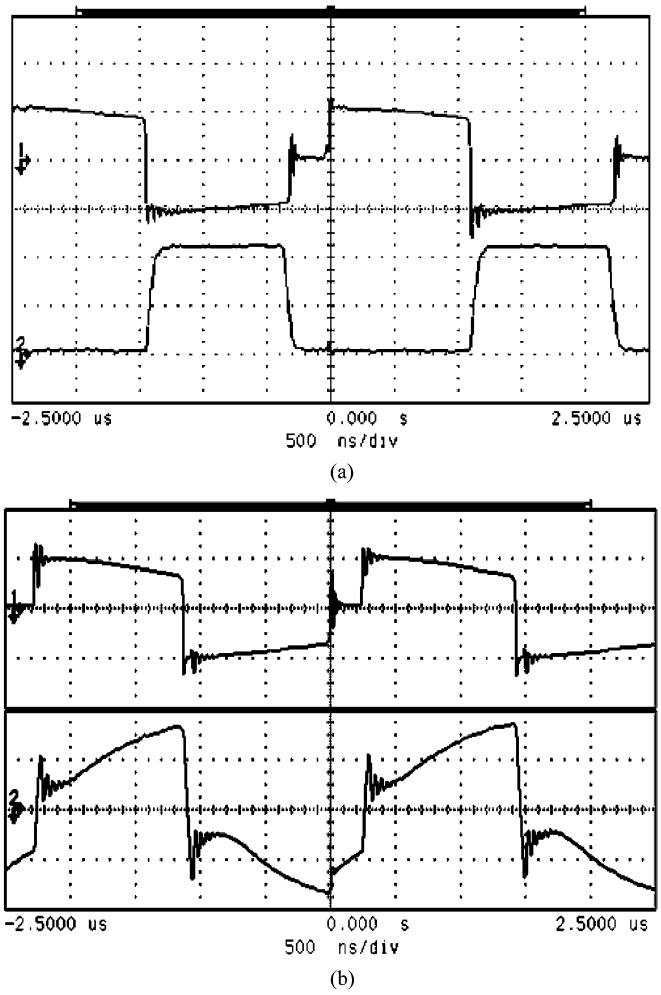

Fig. 20. Experimental waveforms of the modified DCS HB prototype: (a) ZVS of the switch S_2 and (b) transformer primary voltage and current.

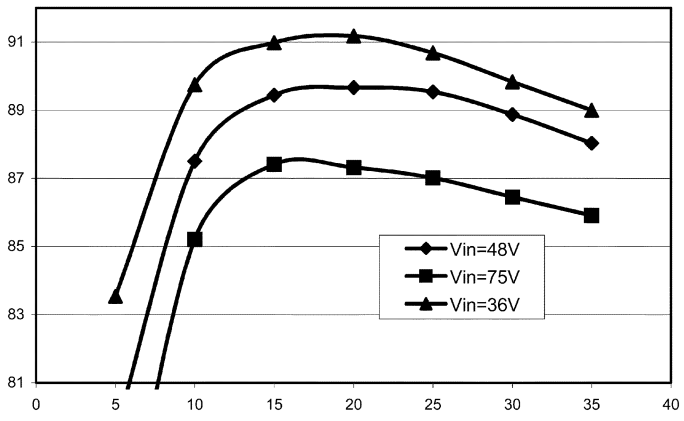

Fig. 21. Efficiency curves of the modified DCS HB dc–dc converter ($f_s = 400\ \mathrm{kHz}$).

fact that the ringing during the off-time interval of two main switches is almost eliminated. Figs. 14–16 show the gate signals and drain-to-source voltage of switches S_1, S_2, and S_3, respectively. It is clear that switches S_1, S_2 and S_3 are turned on at zero voltage.

As the experimental results verified, all primary-side switches operate at ZVS condition, and the leakage-inductance-related ringing and reverse recovery losses in the primary side are almost eliminated. Therefore, higher efficiency and an ability to operate at higher switching frequency are achieved with the DCS PWM control and the proposed DCS- PWM-control based ZVS topology.

The efficiency values were measured for three experimental cases: conventional half bridge with symmetric PWM control, conventional half bridge with DCS PWM control, and the proposed ZVS topology with DCS-PWM control. Figs. 17 and 18 show the efficiency comparison curves at 200 kHz and 400 kHz switching frequencies, respectively. From these figures, it can be observed that the DCS PWM control improves the efficiency of conventional half bridge converter, and the DCS-PWM-based ZVS half bridge topology improves the efficiency further. With the increase in switching frequency, the efficiency improvement becomes more significant. At 400 kHz switching frequency, the efficiency of the DCS-PWM-based ZVS half bridge topology is 4% higher than that of symmetric PWM controlled half bridge converter. This is because switching losses and leakage-inductance-related losses in a conventional half bridge is positively proportional to switching frequency; and in the proposed ZVS half bridge, the losses were almost eliminated. Hence, the DCS-PWM-based ZVS topology is a good candidate for higher frequency applications.

A standard quarter-brick multilayer-PCB prototype with 3.3 V/35 A output as shown in Fig. 19 is built with the modified DCS controlled ZVS HB dc–dc converter as shown in Fig. 7(a), where the secondary-side diodes are replaced with the synchronous rectifiers: Si7892 MOSFETs. The experimental waveforms are shown in Fig. 20, and the efficiency curves at different input voltages are shown in Fig. 21. It can be observed that the converter achieves high efficiencies at 36 V and 48 V inputs, however, the converter has lower efficiency at 75 V input voltage because of the larger circulating energy that occurs at higher input voltage.

VI. Conclusion

A simple and effective PWM control method known as "duty-cycle-shifted PWM" (DCS PWM) was proposed to reduce switching losses and transformer-leakage-inductance-related losses in half-bridge dc–dc converters. By employing the proposed DCS PWM control scheme, ZVS is achieved for one of the two switches without adding extra components and without asymmetric penalties of the complementary control. Based on the DCS PWM control scheme, two ZVS half-bridge topologies are presented and analyzed. Theoretical analysis and experimental results verify that all switches in the converters operate at soft switching such that switching losses are significantly reduced. Furthermore, the energy stored in the transformer leakage inductance is recycled to the input dc bus and utilized for ZVS operation of the switches instead of being dissipated in snubbers. Therefore, switching-frequency-related losses are significantly reduced, which provides converters with the potential to operate at higher frequencies and higher efficiencies. The proposed DCS PWM control and ZVS half-bridge topologies may also be used for high-voltage-input dc–dc applications. The proposed topologies may compete with phase-shifted full bridge in term of complexity and ZVS range for some applications.

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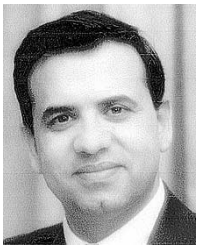

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