

## Design of Efficient ZVS Half-Bridge Series Resonant Inverter with Suitable Control Technique

Harish Vegolam, P. Sucharitha, Durgam Kumaraswamy

2Assistant Professor, Department of EEE, Aurora's Research & Technological Institute, Warangal Institute, Warangal.

3Associate Professor, Department of EEE, Aurora's Research & Technological Institute, Warangal Institute, Warangal.

### ABSTRACT:-

During certain load conditions there will be considerable reduction or decrease in the efficiency of zero voltage switching half-bridge series resonant inverter and this is mainly because of high switching frequencies. In order to improve efficiency, the technique named variable frequency duty cycle (VFDC) control is used for both the medium and low output power levels with the decreased switching frequencies.

VFDC strategy efficiency improvement is achieved by means of a switching-frequency reduction, mainly at low-medium power range, and with low quality factor loads. And this technique is used in Domestic induction heating application because of its special load characteristics.

This paper includes a theoretical analysis of power balance as a function of control parameters, an efficiency analysis to determine the optimum operation point, Switching and conduction losses to examine the overall efficiency improvement are discussed. In addition, restrictions due to snubber capacitors and dead time, and variability of the loads have been considered.

**Index Terms**—Home appliances, induction heating, inverters, resonant power conversion

### I. INTRODUCTION

Home appliances represent a substantial part of the residential energy consumption. For this reason the efficiency of the power converter is a key design aspect, as it defines not only the environmental impact but also the final appliance performance and reliability. As a consequence, researches and developments on induction cookers, as one of the more consuming appliances, pursue further efficiency improvements.

Domestic induction heating technology has become more important in recent years due to advantages such as its improved efficiency, safety and performance. The main blocks of an induction cooking appliance are outlined in Fig. 1. The mains voltage is rectified and filtered, generating a DC bus. Afterwards, the resonant inverter supplies variable frequency current (20 to 75 kHz) to the induction coil. This current produces an alternating magnetic field, which causes eddy currents and magnetic hysteresis heating up the pan.

Traditional Square Wave (SW) modulation implies operation at high switching frequencies to deliver low-medium power. This entails inverter efficiency reductions, which is a basic fact to ensure reliability,

Maximize output power capabilities and minimize heat sink and fan size. In the past, Pulse Density Modulation has been proposed to improve the efficiency. However, it has some limitations regarding flicker emissions and user performance. The aim of this paper is to propose a control algorithm optimization leading to an efficiency improvement with no hardware changes required. To achieve this goal, a theoretical analysis of Variable Frequency Duty Cycle (VFDC) modulation scheme has been carried out. Afterwards, efficiency obtained at different operation conditions has been estimated for different switching devices. Finally, experimentation with a typical induction heating inverter has been used to validate the simulation results.

### PROJECT DESCRIPTION:

The efficiency of ZVS half-bridge series resonant inverter can be decreased under certain load conditions due to the high switching frequencies required. The proposed Variable Frequency Duty Cycle (VFDC) control is intended to improve the efficiency in the medium and low output power levels because of the decreased switching frequencies.

### EXISTING SYSTEM:

Traditional Square Wave (SW) modulation implies operation at high switching frequencies to deliver low medium power. This entails inverter

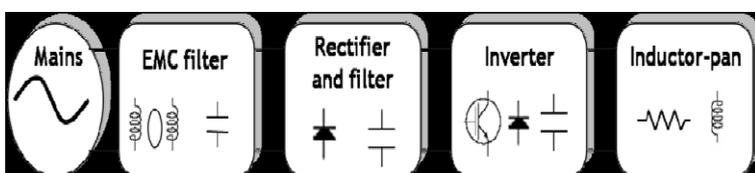


Fig. 1. Block diagram of a domestic induction cooking appliance

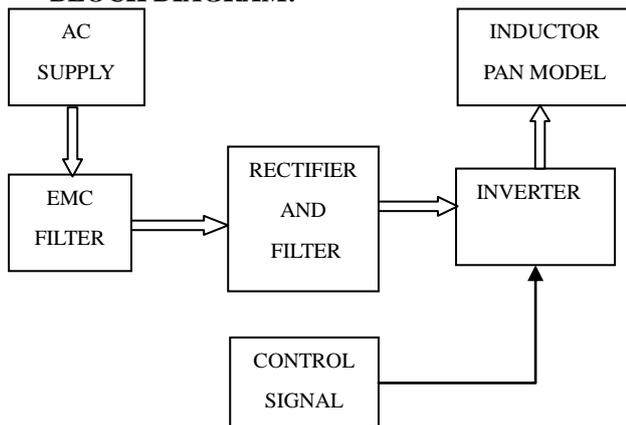
efficiency reductions, which is a basic fact to ensure reliability, maximize output power capabilities and minimize heat sink and fan size. In the past, Pulse Density Modulation has been proposed to improve the efficiency. However, it has some limitations regarding flicker emissions and user performance.

But the disadvantage of the existing system is that the efficiency of ZVS half-bridge series resonant inverter can be decreased under certain load conditions due to the high switching frequencies required.

**PROPOSED SYSTEM:**

The proposed Variable Frequency Duty Cycle (VFDC) control is intended to improve the efficiency in the medium and low output power levels because of the decreased switching frequencies. The study performed in this paper includes, in a first step, a theoretical analysis of power balance as a function of control parameters. In addition, restrictions due to snubber capacitors and dead time, and variability of the loads have been considered. Afterwards, an efficiency analysis has been carried out to determine the optimum operation point. Switching and conduction losses have been calculated to examine the overall efficiency improvement. VFDC strategy efficiency improvement is achieved by means of a switching frequency reduction, mainly at low-medium power range, and with low quality-factor loads.

**BLOCK DIAGRAM:**



**II. VARIABLE FREQUENCY DUTY CYCLE**

The half-bridge series resonant inverter (Fig. 2) is the most used topology due to its simplicity, efficiency, and its cost-effectiveness. The resonant load consists of the pan, the induction coil and the resonant capacitor. Induction coil and pan coupling is modeled as the series connection of an inductor and a resistor, based on its analogy with respect to a transformer, and it is defined by the values of  $L_{eq}$  and  $R_{eq}$ . VFDC control is a generalization of SW and classical Asymmetrical Duty Cycle controls. Its

modulation parameters (Fig. 2 (b)) are switching frequency ( $f_s$ ) and duty cycle ( $D$ ). Reduction in  $D$  allows reducing  $f_s$  and, as a consequence, switching losses can be minimized. Minimum  $D$  and  $f_s$  are limited by Zero Voltage Switching (ZVS) commutation conditions

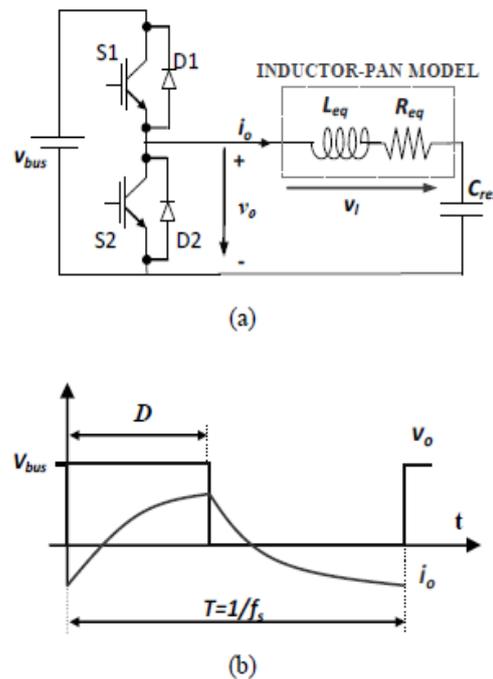


Fig. 2 The half-bridge series resonant inverter: (a) schematic and (b) main waveforms and parameters

**A:- SIMULATION PROCEDURE:**

A versatile simulation tool has been developed using MATLAB to allow varying modulation parameters and performing the required calculus. The power stage has been simulated using the harmonic decomposition. Since voltage  $v_o(t)$  and its harmonics composition  $V_{oh}$  are known, the output power can be calculated as follows.

$$P_o = \sum_{h=0}^{\infty} V_{oh,rms} I_{oh,rms} \cos \phi_h = \sum_{h=0}^{\infty} R_{eq} \left( \frac{V_{oh,rms}}{Z_h} \right)^2$$

$$= \sum_{h=0}^{\infty} R_{eq} \frac{V_{oh,rms}^2}{R_{eq}^2 + (h\omega L_{eq} - 1/h\omega C_{res})^2} \tag{1}$$

Besides, a temporal analysis can be achieved obtaining  $i_o(t)$  through Fourier series.

$$i_o(t) = \sum_{h=0}^{\infty} i_{oh}(t) = \sum_{h=0}^{\infty} \sqrt{2} I_{oh,rms} \sin(h\omega t - \phi_{ih}) \tag{2}$$

where  $i_h$  represents phase delay between h-order harmonic and main harmonic, and it is given in (3).

$$\begin{aligned} \varphi_{in} &= \varphi_{vh} - h \quad \varphi \\ &= \tan^{-1}\left(\frac{1}{\tan(h\pi D)}\right) - \tan^{-1}\left(\frac{h\omega L_{eq} - \frac{1}{h\omega C_{res}}}{R_{eq}}\right). \end{aligned} \quad (3)$$

**B:- INFLUENCE OF LOAD, SNUBBER NETWORK AND DEAD TIME**

Equivalent load parameters  $L_{eq}$ ,  $R_{eq}$  and  $C_r$  compose the inverter resonant tank and, hence, the load has a direct influence on the operation conditions. Different loads can be classified by their quality factor (Q), defined as usual (4), and the resonant frequency  $f_0$ . For domestic induction heating  $Q = 1.66$  is considered as a common value for ferromagnetic pots, although this analysis has been extended for  $Q = 1, 2, 4$  and  $8$ .

$$Q = \frac{X_{eq}}{R_{eq}} = \frac{\omega L_{eq}}{R_{eq}}. \quad (4)$$

In addition, commercial power stages use snubber networks and minimum-fixed dead time to minimize the power losses and to ensure the reliability of the appliance. This entails temporal restrictions, given in the following expression, which must be satisfied to keep ZVS operation. As a consequence, potential fs reduction and efficiency improvements are limited.

$$t_{snubber} = \frac{2C_s V_{bus}}{i_{fall}} < t_d \quad \min(t_{diode}), \quad (5)$$

Where  $t_{diode}$  is the diode conduction time,  $t_d$  is the dead time,  $t_{snubber}$  the time until snubber capacitor reaches bus voltage,  $C_s$  the snubber capacitor and  $i_{fall}$  all the turn-off current.

The influence of both the load and the snubber network has been analyzed through the power distribution shown in Fig. 3, where output power as a function of fs for duty cycle from 0.5 to 0.15 is represented. All the magnitudes have been normalized to their values at resonance frequency and  $D = 0.5$ . In addition, the minimum D value to

ensure ZVS operation has been included. It is shown that maximum fs reductions are achieved with loads with low Q (Fig. 3 (a), (c)) operating with low snubber capacitor values (Fig 3. (a), (b)).

**III. EFFICIENCY ANALYSIS**

An efficiency analysis has been carried out considering the contribution of conduction ( $P_{on}$ ) and switching losses ( $P_{sw}$ ) to total losses ( $P_{loss}$ ). Conduction losses analysis has been computed modeling the switch as the series connection of a resistance ( $R_{on}$ ) and a voltage source ( $V_{on}$ ). Thus, power losses are calculated as follows

$$P_{on} = V_{on} I + R_{on} I_{rms}^2, \quad (6)$$

where I and  $I_{rms}$  are the device average and rms currents respectively.

Switching losses have been calculated assuming linear current and voltage turn-off characteristics of the switching devices, so  $P_{sw}$  for a transistor with current fall time  $t_f$  all are given by

$$P_{sw} = \frac{f_s V_{bus} t_{fall}}{2} \sum_j i_{fall,j} \cdot \psi_j(q_j) \quad f_s \quad E_{off}, \quad (7)$$

$$\psi_j(q_j) = \left(1 - \frac{4}{3} q_j \frac{q_j^2}{2}\right) \text{ where } q_j = \frac{\sqrt{2C_s V_{bus}}}{\sqrt{t_{fall} i_{fall,j}}}. \quad (8)$$

VFDC control scheme achieves power loss reduction by decreasing switching frequency. Fig. 4 shows switch-off power loss improvement for different transistor  $t_f$  all times (a) and total power loss improvement (b). The power losses have been normalized with the value operating with  $D = 0.5$  to provide a clear evaluation of VFDC control scheme. Simulation results show a reduction of the switching losses up to 14% for high commutation speed devices (Fig. 4 (a)).

Besides, the overall importance of switching losses reduction and, hence, efficiency improvement, depends on the relative weight of switching and conduction losses.

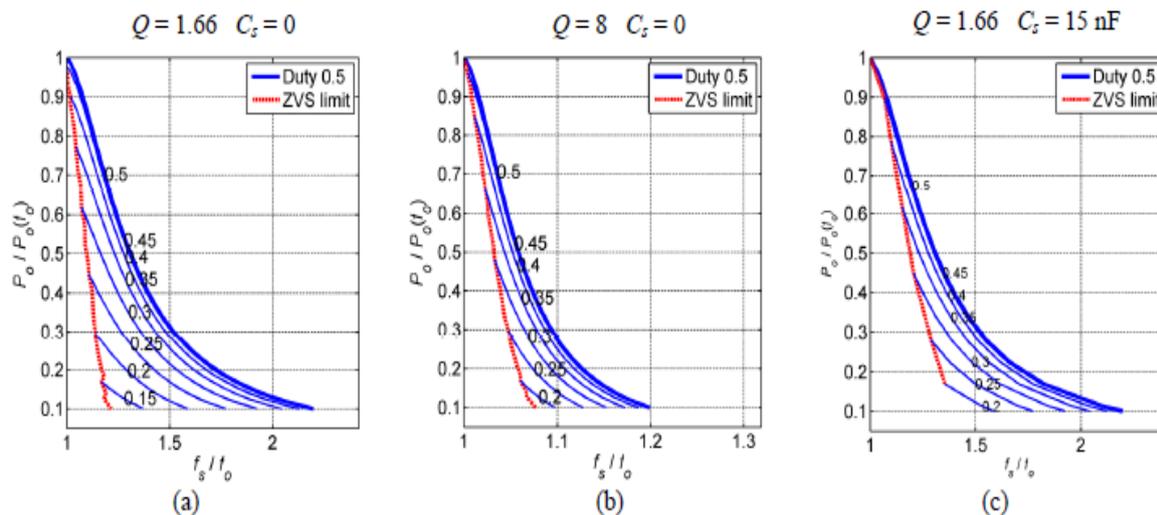


Fig. 3 Normalized output power as a function of normalized switching frequency with different duty cycles for loads with  $Q = 1.66$  (a) and  $Q = 8$  (b) operating without snubber, and  $Q = 1.66$  operating with 15 nF snubber capacitor (c)

This is characteristic of the switching device and, as a consequence, it must be previously defined. For this analysis it has been considered the commercial device Fairchild 20N60 IGBT which includes anti-parallel diode. Fig. 4 (b) shows the normalized power losses and the  $D$  selected to minimize it. The maximum efficiency benefits are obtained in the low-medium power range and, as previously shown, with low  $Q$  loads, because of the higher  $f_s$  reduction feasible.

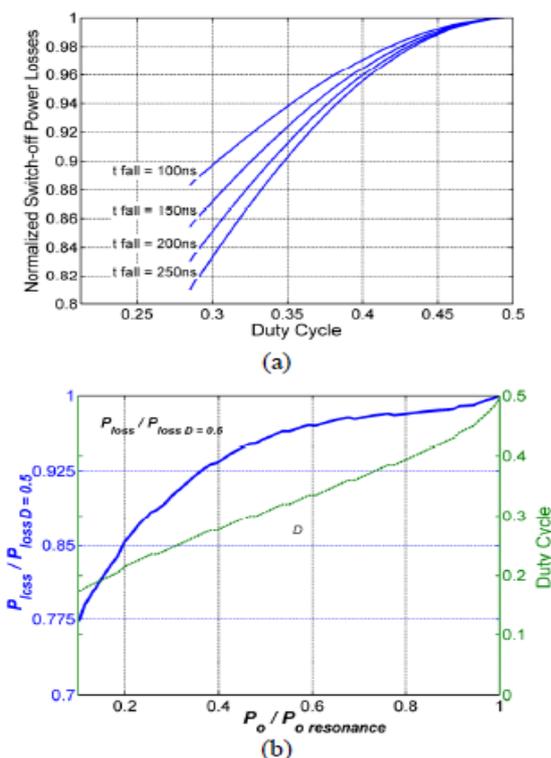


Fig. 4 Simulation results for different duty cycles and load with  $Q = 1.66$ : (a) normalized switching power losses to supply 2200 W and (b) total power loss reduction and its optimum duty cycle associated for the whole output power range.

#### IV. EXPERIMENTAL VERIFICATION

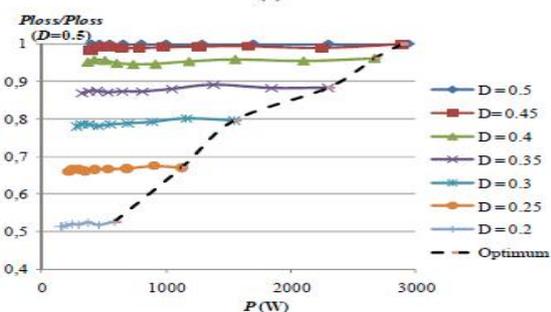
A half-bridge series resonant inverter has been used to test the proposed control scheme. In order to avoid second order effects with temperature and frequency when using commercial pots, a discrete RL load has been implemented ( $Q = 1.4$ ). It has been designed with forced-cooling in order to operate with output powers up to 3500 W. Measurements have been carried out with a digital oscilloscope and power analyzer YOKOGAWA PZ4000. The power converter is controlled in open loop through a PC interface (Fig. 5 (a)). Digital control has been implemented in a PIC18F2520, which controls a versatile PWM modulator implemented in an ASIC. The main inverter specifications are summarized in Table I

Table I. Inverter specifications

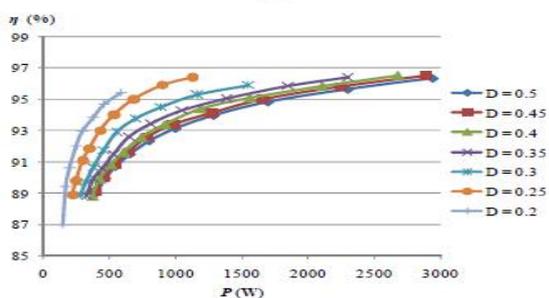
Parameter	Value
$V_{bus}$	230 V
$f_{s,min}$	20 kHz
$f_{s,max}$	100 kHz
Max. output power	3500 W
$C_z$	15 nF
$C_r$	1440 nF
$R_{eq}$	3 $\Omega$
$L_{eq}$	25 $\mu$ H
Power switch	2 x IGBT Fairchild 20N60



(a)



(b)



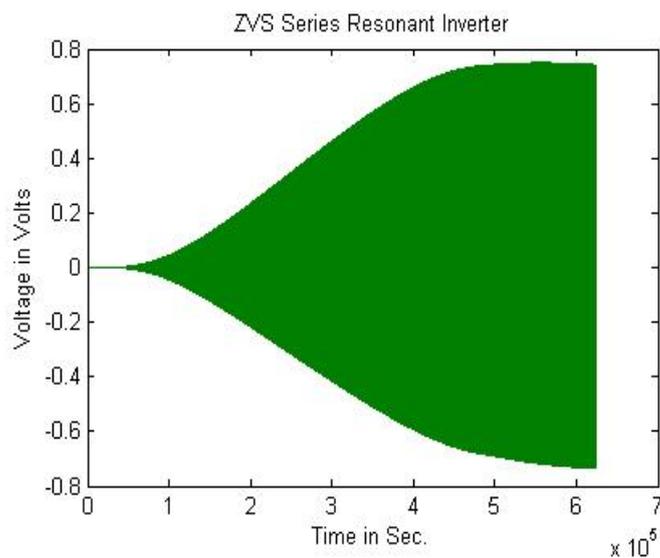
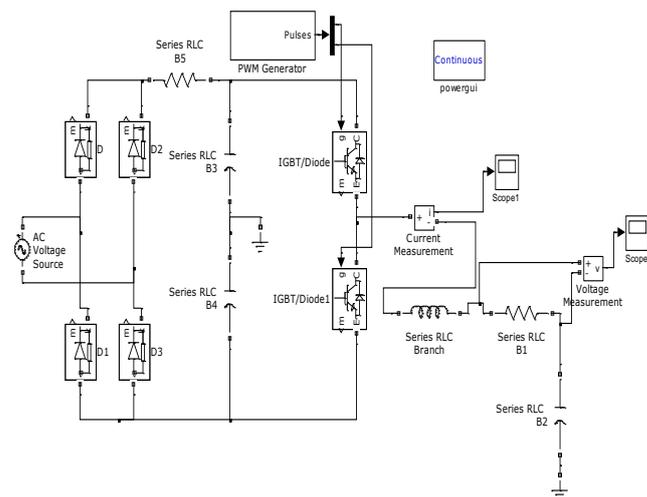
(c)

Fig. 5 Experimental verification: (a) experimental set up, (b) measured power loss reduction, and (c) efficiency for different output power and duty cycle.

Experimental measurements show the power loss reduction and efficiency improvement achievable with the use of VFDC modulation technique (Fig. 5 (b) and (c)). It is shown that the efficiency improvement is higher at the low/medium power range, and power loss reductions higher than 25%

are achieved with a load with  $Q = 1.4$ . For a final application, it should be also considered the effects of the dc-link voltage ripple, due to the non-linear behavior of both the induction load and the switching losses. Since the higher peak current increases significantly the switching losses, VFDC control is recommended to reduce the switching frequency. Besides, the maximum efficiency point for a certain output power is achieved with the lower D possible. Therefore, the maximum efficiency point tracking becomes simple and with a straightforward digital implementation.

V. SIMULATION MODEL AND RESULTS



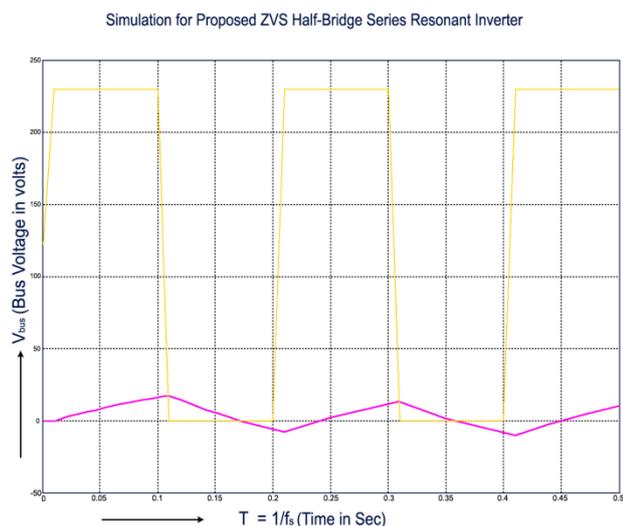


Fig. Extended Result for ZVS Series Resonant Inverter

## VI. CONCLUSION

The efficiency of the power converter determines the maximum output power and reliability of a domestic induction heating appliance. In this paper, a method to improve efficiency in the half-bridge series resonant inverter has been presented through a generalization of SW and ADC controls. VFDC control strategy is intended to replace classical SW and PDM strategies in order to get improved performance and user experience. It has shown efficiency improvements due to the switching frequency reduction which leads to reduced switching power losses. The most favorable operation range comprises loads with low  $Q$  operating in the low/medium power range. The analytical results presented in this paper have been verified through an induction heating test-bench. Experimental results confirm the benefits of VFDC control, improving efficiency in the whole power range, and achieving power loss reduction higher than 25% for a typical domestic induction heating load. As a consequence, VFDC control scheme is proposed as a solution to improve efficiency with easy digital control integration.

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