ES_LPC5410x

Errata sheet LPC5410x

Rev. 2.1 — 17 December 2015 **Errata sheet**

Document information

Info	Content
Keywords	LPC54102J512UK49; LPC54102J256UK49; LPC54101J512UK49; LPC54101J256UK49; LPC54102J512BD64; LPC54102J256BD64; LPC54101J512BD64; LPC54101J256BD64
Abstract	LPC5410x errata

Revision history

Rev	Date	Description
2.1	20151217	• Power ROM API.1 • Updated Section 1 “Product identification”. Added boot code revision.
2.0	20150501	• Added RTC.1 • Added ISP.1 • Frequency.1 • Updated product identification information
1	20141105	• Initial version

Contact information

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1. Product identification

The ES_LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The ES_LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

This Errata Sheet covers the following revisions of the LPC5410x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'1B'	Initial device revision with boot code version 17.1.
'1C'	Second device revision with boot code version 17.1.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
RTC.1	The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.	'1B', '1C'	Section 3.1
ISP.1	ISP (In-System Programming) command for UID (unique identification number) is not functional.	'1B', '1C'	Section 3.2
Frequency.1	The maximum operating system clock on the LPC5410x device is limited to 96 MHz.	'1B'	Section 3.3
POWER_API.1	The set-voltage ROM API call does not configure the internal regulator correctly for the desired operating frequency.	'1B', '1C'	Section 3.4

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 RTC.1: The RTC oscillator changes from bypass control mode to crystal mode when waking up from Deep power-down mode.

Introduction:

On the LPC5410x, the low power 32 KHz RTC oscillator can be configured to run in crystal oscillation mode or bypass control mode. In crystal oscillation mode, the RTC oscillator is driven by an external 32 KHz crystal and in bypass control mode, the RTC oscillator is driven by an external 32 KHz clock. Bypass control mode can be entered by setting the PDEN_32K_OSC bit in the PDRUNCFG register (bit 24).

Problem:

The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.

Work-around:

If using deep power-down mode, the crystal oscillation mode should be used instead of the bypass crystal mode. The bypass crystal mode can be used in active, sleep, deep-sleep, and power-down modes.

3.2 ISP.1: ISP (In-System Programming) command for UID (unique identification number) is not functional.

Introduction:

Each LPC5410x device contains a device serial number (four 32-bit words) for unique identification. The ISP call (ReadUID) can be performed via the USART interface to read the unique serial number where the word at the lowest address is sent first.

Problem:

On the LPC5410x, the read UID ISP command is not functional.

Work-around:

The unique serial number (four 32-bit words) can be directly read from address locations 0x01800100 to 0x0180010C.

3.3 Frequency.1: The maximum operating system clock on the LPC5410x device is limited to 96 MHz.

Introduction:

The LPC5410x data sheet specifies that the LPC5410x device can operate at CPU frequencies up to 100 MHz.

Problem:

To guard band for process, voltage, and temperature, the operating frequency is limited to ≤96 MHz.

Work-around:

None. Use CPU frequencies ≤96 MHz.

3.4 POWER_API.1: The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Introduction:

On the LPC5410x device, the following power API ROM calls are provided to configure the system clock, and to manage the power consumption::

- set_pll: Configures the system PLL.
- set_voltage: Controls the device power consumption and the internal regulator for desired operating frequency.
- power_mode_configure: Entry to and wake up from the low power modes.

Problem:

The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Work-around:

The power API library (power_lib) provided in NXP's LPC5410x LPCOpen v3.xx software platform must be used when calling the set_voltage API call. This library correctly configures the internal regulator for the desired operating frequency.

4. AC/DC deviations detail

No known errata.

5. Errata notes

No known errata.

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