nvSRAM - SRAM and EEPROM within a single chip

Powerful processor systems which place high demands on reliability require optimal data storage systems. The nvSRAM (non-volatile Static Random Access Memory) from ZMD offers unique and superior data storage features.

The nvSRAM not only provides the advantages of a fast SRAM (fast read and write operations), but also those of an EEPROM (non-volatile data retention). Each SRAM cell is equipped with a non-volatile EEPROM shadow cell. The nvSRAM also contains complex control logic, giving users convenient functions for reliable data security (Fig.1).

![Block diagram of the 256 Kbit nvSRAM](image)

Figure 1: Block diagram of the 256 Kbit nvSRAM

Typical applications of the nvSRAM are industrial and automotive electronics as well as diagnostic and measurement systems. The nvSRAM is the perfect solution where reliable data retention has to be guaranteed under extreme conditions.

The nvSRAM can be used to store critical process data in numerical controls. In miniaturized applications the nvSRAM can be used as combined program and data memory, reducing the number of ICs on board, increasing the flexibility and power of the system. The fast access nvSRAM is the ideal memory solution for measurement and diagnostic applications. The measured data can be stored in the SRAM and transferred to the EEPROM on demand, during normal system power down, or when the power supply is lost.
An important feature for microcontroller solutions is simple and fast reprogramming of the nvSRAM. This can be used in intelligent sensors / actuators and industrial networks with program and parameter download support. Another advantage is the random split of RAM / ROM area for microcontroller memory.

An SRAM from the outside - an EEPROM inside

In addition to the SRAM array, the nvSRAM contains an integrated shadow EEPROM array. Each SRAM cell has its own EEPROM cell.

The nvSRAM has two different modes of operation: SRAM mode and non-volatile mode. In **SRAM mode** the memory operates as an ordinary Static RAM. The SRAM can be read and written an unlimited number of times. The fastest memory access time for read and write is less than 25 ns. The nvSRAM products are byte organized.

In **non-volatile mode** the data are transferred from the SRAM to the EEPROM (the STORE operation) or from the EEPROM to the SRAM (the RECALL operation). STORE and RECALL operations may be initiated automatically at power-down / power-up of the power supply voltage; under user control via a software sequence or via a hardware signal to a control pin.

Once a STORE or RECALL cycle is initiated, further input to or output from the SRAM are disabled until the cycle is completed. The on-chip STORE/RECALL control unit enables data to be transferred between the SRAM and EEPROM.

The contents of the SRAM can be stored in the EEPROM at any time within a few milliseconds. Data can be written to the EEPROM at least 100,000 times, with no limitations on the frequency of its contents being read back into the SRAM. The nvSRAM guarantees that data is stored for at least ten years following the last STORE cycle to the EEPROM. This guarantees that data is neither lost when the part is switched off, nor when the feature voltage is suddenly interrupted.

Manufacturing Technology and Circuit Design

ZMD’s nvSRAMs are manufactured in a 0.8 µm CMOS technology. This technology has two polysilicon and two metal layers available. The non-volatile data storage capability is provided by an additional oxynitride layer (SiliconNitrideOxidSilicon). This storage principle is significantly different from common EEPROM and Flash technologies which are based on floating gates. High-voltage MOS transistors have been implemented on the chip to generate the voltages for the non-volatile data storage. According to the SRAM concept, highly-resistive load elements and buried polysilicon contacts are available. The complex functionality of the nvSRAM requires analog components like capacitors, resistors and bipolar transistors.
The volatile data storage is done with flip-flops using the four-transistor cell principle with highly-resistive load elements. This construction makes it possible to have an area efficient high-density memory array.

The non-volatile data storage is done with two EEPROM elements which are directly located at each SRAM cell. In the SRAM mode these EEPROM elements are electrically isolated from the SRAM cell. They are connected to the SRAM cell only in non-volatile STORE or RECALL operations.

The special advantage of this nvSRAM cell is the utilization of the differential information which is generated by two EEPROM elements located at one SRAM cell. This guarantees a very secure and long data retention over a wide temperature range. The non-volatile data storage is carried out in parallel for the whole memory array. A non-volatile STORE operation consists of two internal steps:

The first step erases the EEPROM cells by applying a negative voltage in the range of 10 V, while they are disconnected from the SRAM cells.

The second step connects the SRAM and EEPROM cells and the non-volatile STORE is accomplished by a positive voltage greater than 12 V. The program and erase voltages are generated on-chip by charge pumps. The pumps are controlled by an accurate band-gap reference circuit, which is very stable over a wide temperature and voltage range.

The RECALL of the non-volatile information is also done in parallel for the whole memory array. In order to transmit the non-volatile information into the SRAM cells the SRAM array is first erased completely at. Subsequently the EEPROM cells are connected to the SRAM cells and the RECALL takes place. In this case the programming gate of the EEPROM cell is strictly held at 0 V in order to avoid any influence upon the non-volatile stored information during recall.

In PowerStore nvSRAMs the integrated voltage sensor initiates an automatic non-volatile STORE when the power supply voltage is lost. The necessary accuracy of the voltage thresholds is maintained with the internal band gap reference.
nvSRAM types

**HardStore nvSRAM**
A signal to a control pin on the nvSRAM activates the data transfer from the SRAM to the EEPROM (STORE) or the reloading of the data from the EEPROM into the SRAM (RECALL).

**SoftStore nvSRAM**
A defined sequence of six consecutive SRAM read access operations activates the data transfer from the SRAM to the EEPROM or the reloading of the data from the EEPROM into the SRAM.

**PowerStore nvSRAM**
The data transfer from the SRAM to the EEPROM is initiated automatically once the integrated power sensor detects that the operating voltage has dropped below a minimum voltage. The power required to save the data is provided by an *external* capacitor, connected to a cap power pin, or by the intrinsic system capacitance. (Fig. 2)

**CapStore nvSRAM**
The data transfer from the SRAM to the EEPROM is initiated automatically once the integrated power sensor detects that the operating voltage has dropped below a minimum voltage. The power required to save the data is provided by an *internal* capacitor.

All types provide the automatic RECALL operation during power-up. *PowerStore* and *CapStore* nvSRAMs may provide hardware or software initiated STORE or RECALL operations, in addition to data transfer during power down/loss.

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**Figure 2: Power supply of the PowerStore nvSRAM U632H64 for the STORE operation at power-down**