Application Report
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BPSK Modem Implementation With MSP432™ MCUs

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ABSTRACT

This application report introduces how to implement a 125-kbps BPSK modem by taking advantage of the CMSIS DSP Library with on-chip timer and 1-Msps ADC on the MSP432P401R. The MSP-EXP432P401R LaunchPad™ development kit is used as the main development platform.

Source code and related collateral discussed in this document can be downloaded from http://www.ti.com/lit/zip/slaa681.

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1 Introduction

Many microcontroller-based applications can benefit from the use of an efficient digital signal processing (DSP) library. ARM has developed a set of functions called the CMSIS DSP Library compatible with all ARM® Cortex®-M3 and Cortex-M4 processors. CMSIS DSP library is designed to use ARM assembly instructions specific to each Cortex-M core implementation to quickly and easily handle various complex DSP functions. The Cortex-M4 processor has all of the features and the instruction set from the Cortex-M3 processor plus DSP extensions and an optional single-precision floating-point unit (FPU). Communication algorithms such as Binary Phase Shift Keying (BPSK) that require digital signal processing can benefit from CMSIS DSP especially when implemented on hardware-enabled DSP platforms such as Cortex-M4.

The MSP432™ microcontroller (MCU) family of devices is TI's latest efficient ultra-low-power mixed-signal MCUs. The MSP432 MCU family features the ARM Cortex-M4F processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount. MSP432 MCU is an ideal combination of the TI MSP430™ low-power DNA, advanced mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The devices ship with driver libraries and are compatible with standardized components of the ARM ecosystem.

This application report introduces how to implement a 125-kbps BPSK modem by taking advantage of the CMSIS DSP Library with the on-chip timer and 1-Msps ADC on the MSP432P401R. The MSP-EXP432P401R LaunchPad development kit is used as the main development platform.

2 BPSK Modem Algorithm

BPSK is a binary digital modulation scheme that conveys data by modulating the phase of a reference signal (the carrier). Binary digital modulation uses two distinct signals to represent binary digital data in two different phases for modulation. Usually, a carrier of one phase is used to represent bit 0, while a 180 degree different phase represents bit 1. As fixed phases are used for modulation, BPSK is sometimes known as *absolute* binary phase shift keying to distinguish it from *differential* binary phase shift keying. Figure 1 shows a typical BPSK signal.

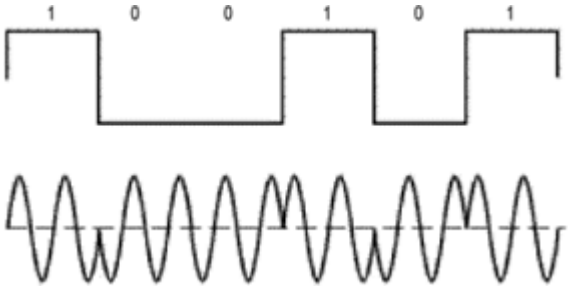

Figure 1. BPSK Waveform

In BPSK, a fixed-frequency signal is used as carrier, and the modulated information is carried by its different phases. Assuming that the carrier frequency is 100 kHz in Figure 1 with two periodic waveforms to present each bit, the baud rate is 50 kbps.

In modern communication systems, BPSK modem is widely used, because it has the best Bit Error Ratio (BER) performance in binary modulation. For more information about the BER of BPSK, see Section 7.1.

For demodulation, the receiver first recovers the clock from the received signals. The recovered clock is used to reconstruct raw data from the modulated signal by synchronous coherent demodulation. Costas loop is frequently used to recover the carrier from the modulated signal, because it is able to recover the raw data in parallel. Figure 2 shows the simple method that is applied in this application. DSP extension in Cortex-M4 takes the advantages of efficiency and low power while processing many multiply operations. The ADC acquires additional dynamic range for post digital processing, which is called *software demodulation*.

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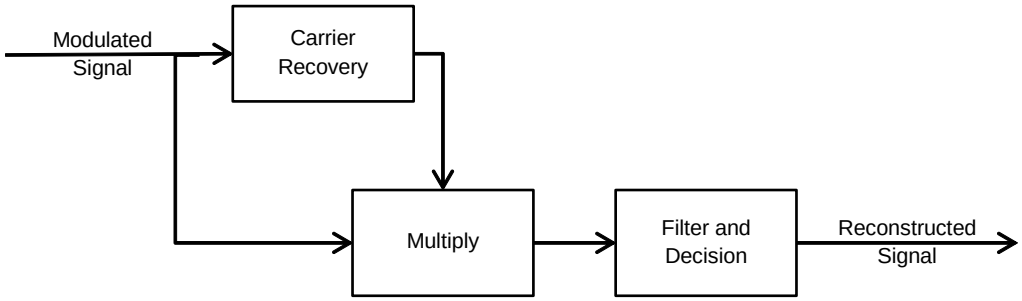

Figure 2. Block Diagram of BPSK Demodulation

A typical application is found in an optical communication system which uses the BPSK modem method to provide an additional path for a low-data-rate signaling link. The MSP432 MCU is selected to implement the two-way communication.

3 Modem Implementation on MSP432 MCU

This section describes the implementation of a BPSK modem on an MSP432 MCU, including BPSK modulation and demodulation, forward error correction (FEC) to improve BER, and digital signal conditioning.

The BPSK modulator has the following specifications:

- 125-kHz carrier frequency
- Up to 125-kbps bit rate
- A complete packet or frame of up to 600 bytes
- Using 500-kHz frequency for the ADC sampling (500 ksps), known as x4 oversampling

Figure 3 shows the system block diagram of the transmitter. The components that are marked with dotted lines are optional. The FEC encoder can be used to correct packet errors and to reduce retransmission by decoding redundancy bits at the receiver. The external RC filter is used to construct a sine waveform by suppressing the harmonics of a square wave generated by PWM. The BPSK modulator is described in Section 3.1. FEC codec implementation is described in Section 3.3.

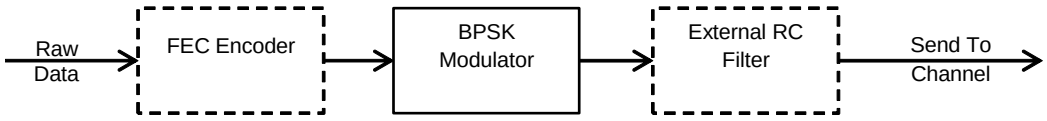

Figure 3. Block Diagram of Modulator

Figure 4 shows the receiver block diagram. The BPSK demodulator is described in Section 3.2, which includes an optional finite impulse response (FIR) low-pass filter (LPF) (see Section 3.4) to improve the signal-to-noise ratio (SNR) performance before demodulation.

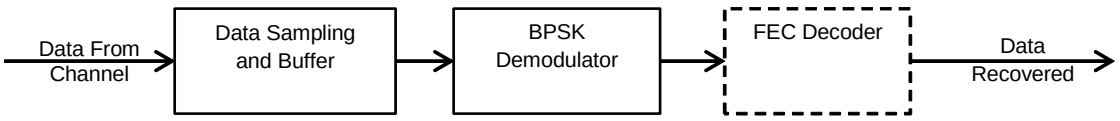

Figure 4. Block Diagram of Demodulator

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3.1 Modulation Implementation

In BPSK modulation (see Figure 5) two phases of carriers, which have a 180-degree differences, are used to present two types of signals.

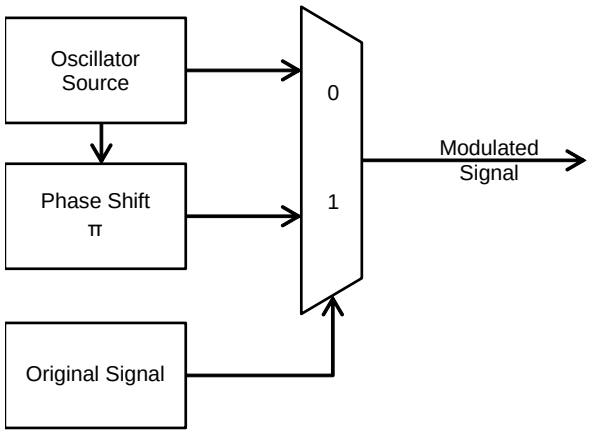

Figure 5. Block Diagram of BPSK Modulation

Section 3.1.1 describes the physical layer and data link layer implementation of BPSK modulation.

3.1.1 Physical Layer Implementation

In the diagram in Figure 5, a timer is used in the BPSK modulator to generate the carrier that has a phase difference of 180 degrees. In the MSP432 MCU, the Timer_A module supports several different PWM output modes. Output modes 2 and 6 can be configured to implement 180° phase difference in this application. Figure 6 shows the phase scheme.

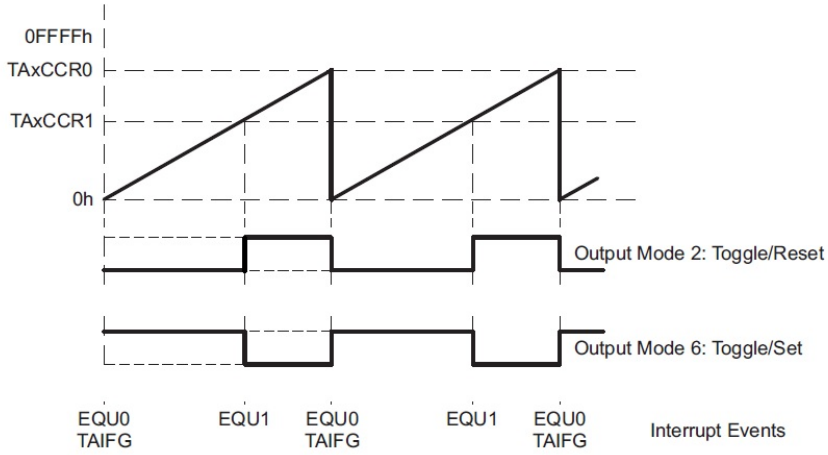

Figure 6. Timer_A Output Modes Used in This Application

Figure 7 shows how to generate the carrier with the Timer_A module. The clock signal is sourced from SMCLK through a divider. Timer_A works at stop mode normally, and when transmission starts, reconfigures its state to up mode and enables the counter. When the counter value matches the value in the TAxCCRn register, the output module is enabled and generates the output waveform. Output mode 2 or mode 6 is selected by whether the bit that needs to be modulated is 0 or 1, respectively. For further information, see the *MSP432P4xx Family Technical Reference Manual* (SLAU356).

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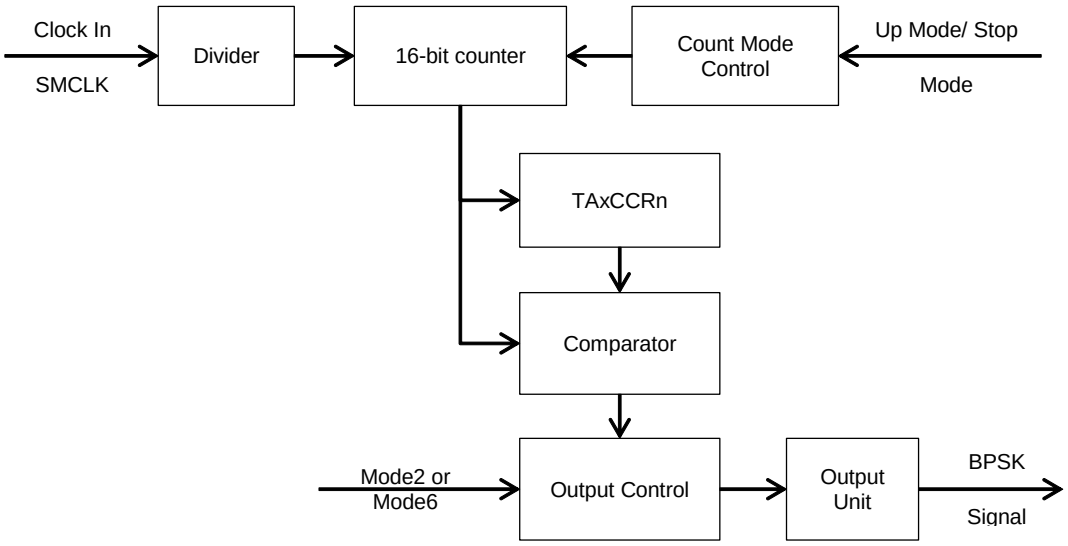

Figure 7. Flow Chart of BPSK Signal Generation by Timer_A

An external RC filter can be utilized to generate the sine wave for those applications that sine wave is required as carrier. The -3dB cut-off bandwidth is determined by Equation 1.

$$f_c = \frac{1}{2\pi RC} \quad (1)$$

A 1-kΩ resistor and 1-nF capacitor are selected to achieve the 160-kHz cut-off frequency in this design.

The following pseudocode shows how the MCU implements BPSK modulation using the timer interrupt and PWM output.

```
initial TA1 as carrier;
initial TA2 as bit generator, enable interrupt;
start modulation              //enable carrier output
if(TA2 interrupt)
{
    if(modulation not end)
    {
        if(bit == 0)          //for bit 0
            TA1 output mode2;
        else                  //for bit 1
            TA1 output mode6;
    }
    else
    {
        re-initialize;
        stop communication;   //stop carrier output
    }
}
```

3.1.2 Data Link Layer Implementation

Figure 8 shows the packet that is defined for handshake between transmitter and receiver. To manage data transmission in burst mode, the carrier is sent ahead of the actual data to wake up the receiver before the date packet is sent. A data packet contains a 4-byte preamble, 1-byte delimiter, length-variable Payload Data Unit (PDU), and 1-byte checksum. The receiver acquires the bit synchronization by recovering the clock from the preamble. Then, the receiver can identify the beginning of the PDU by recognizing the delimiter byte. The packet ends with a checksum using Exclusive-OR. Other data integrity check methodologies are also applicable depending on the systems requirements.

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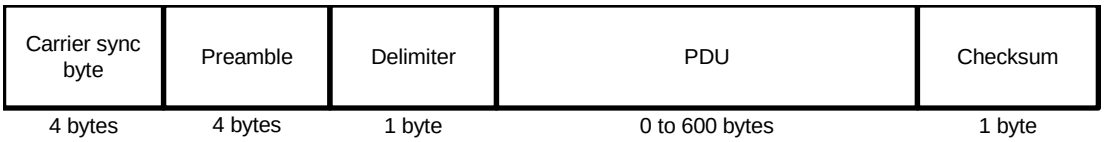

Figure 8. Data Packet Structure

3.2 Demodulation Implementation

In the demodulator, the ADC coverts the analog signal into digital, which provides better dynamic range performance and is easier to process in software. In addition, the ADC threshold compare function measures the Received Signal Strength Indicator (RSSI) and starts consecutive samplings.

In this application, because x4 oversampling is employed, the ADC sample rate is configured as 500 ksps. The threshold is set to 0.8 V as an RSSI. The ADC monitors the data line and ignores all signals below 0.8 V. When the input voltage is higher than the threshold, the ADC starts to sample continuously and store the result in SRAM using the DMA for post processing. The RSSI is averaged in parallel over a window of every six results. When the averaged RSSI is below a preset threshold, the receiver stops ADC sampling and the post processing of the data starts.

When a complete packet is received, the clock is first recovered from the carrier and preamble of the data packet. A mixer is used to implement the coherent demodulation with the inputs of the recovered clock and the filtered carrier. The bit sample and decision block takes the coherent result as inputs to demodulate the binary data. If the transmitter implements FEC, an FEC decoder must be applied at the receiver to recover the raw data. Figure 9 shows the demodulation flow chart.

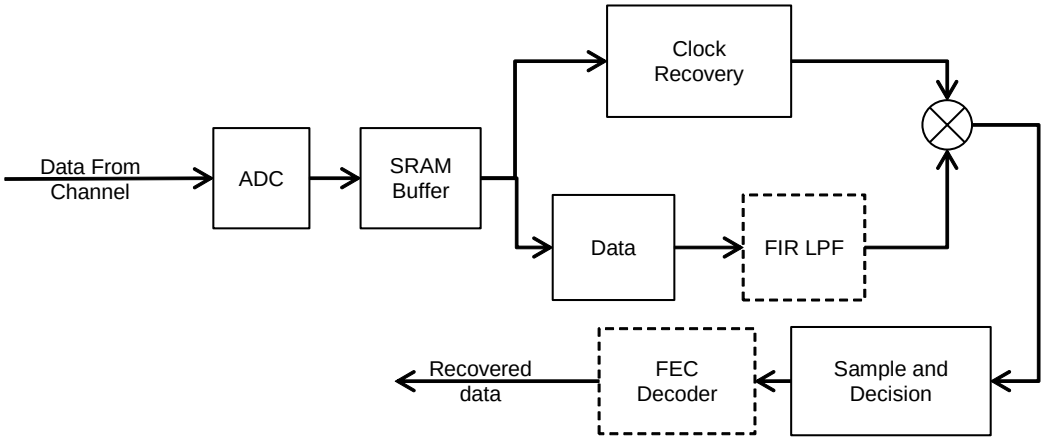

Figure 9. Flow Chart of Demodulation

The following pseudocode demonstrates demodulation.

```
initialize ADC high-threshold interrupt;
    //when input signal reaches RSSI
    if(ADC's high-threshold interrupt)
    {
        using TA1(500kHz) to sample;         //start adc sampling
        store data in SRAM;
        if((data[index] + data[index-1] + data[index-2] +
        data[index-3] + data[index-4] + data[index-
5]) < stopthreshold)//the window used for sampling stop decision
        {
            receiving stop;
            start demodulation;
        }
```


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```
}
if(start demodulation)
{
    recover clock from carrier sync bytes;
    stage1 = fir(data);//optional
    //synchronous coherent demodulation
    stage2 = stage1 * clock;
    stage3 = decision(stage2);
    recovered data = stage3;
    end demodulation;
}
if(end demodulation)
    re-initialize and wait for next data;
```

3.3 FEC Implementation

FEC allows constructing a more robust and efficient system by fixing the correctable error bits and reducing retransmission. An optional 5-bit redundant codec is used to correct single-bit error in every 8-bit raw data, which is called a Hamming (13, 8) code. A codeword contains 16 bits with 8-bit LSB raw data, 3-bit unused MSB bit, and 5-bit redundancy bit in the middle (see Figure 10). See Section 7.2 for more details.

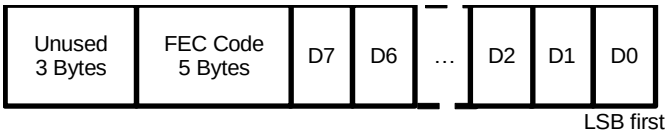

Figure 10. FEC Encoded Data Structure

3.4 Filter Used to Improve SNR

Figure 9 includes an optional FIR LPF to improve SNR performance by blocking out-of-band signals. The FIR filter can be designed and implemented using Matlab and CMSIS DSP Library functions, respectively. According to the Nyquist sampling theorem, the normalized cut-off frequency must be higher than 0.5. A 24-stage LPF is introduced with a normalized –3-dB cut-off frequency of 0.56. Figure 11 shows the magnitude response and impulse response of the filter. A phase delay of 11.5 must be managed when using this 24-stage filter. The filter coefficients are generated in Matlab by calling function *fir1(23, 0.56)*.

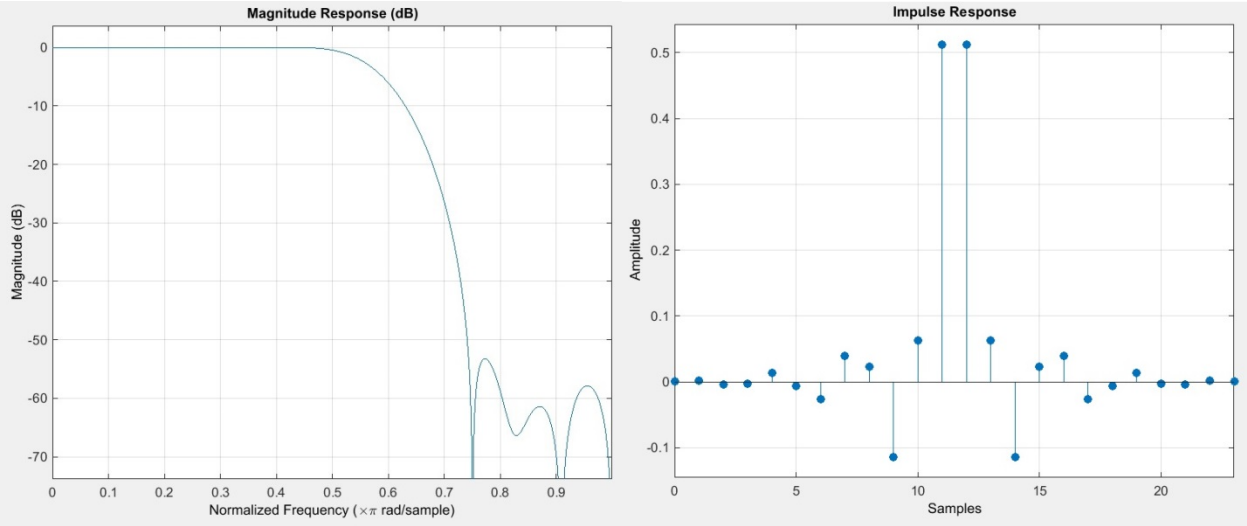

Figure 11. Magnitude and Impulse Response of FIR LPF

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This filter can be implemented by calling the FIR functions *arm_fir_init_f32* and *arm_fir_f32* in the CMSIS DSP Library with the filter coefficients generated by Matlab.

4 Test and Results

This section describes the results of the MSP432 MCU BPSK experiments. All tests were performed on two MSP-EXP432P401R LaunchPad development kits with Code Composer Studio IDE v6.1.0.

4.1 Test Bench Setup

One MSP-EXP432P401R works as the transmitter and the other as the receiver. Two boards are interconnected by two wires: one wire from the Timer_A output of the transmitter to the ADC input of the receiver, and the other wire connecting the GND signals on the two boards (see Figure 12 and Figure 13).

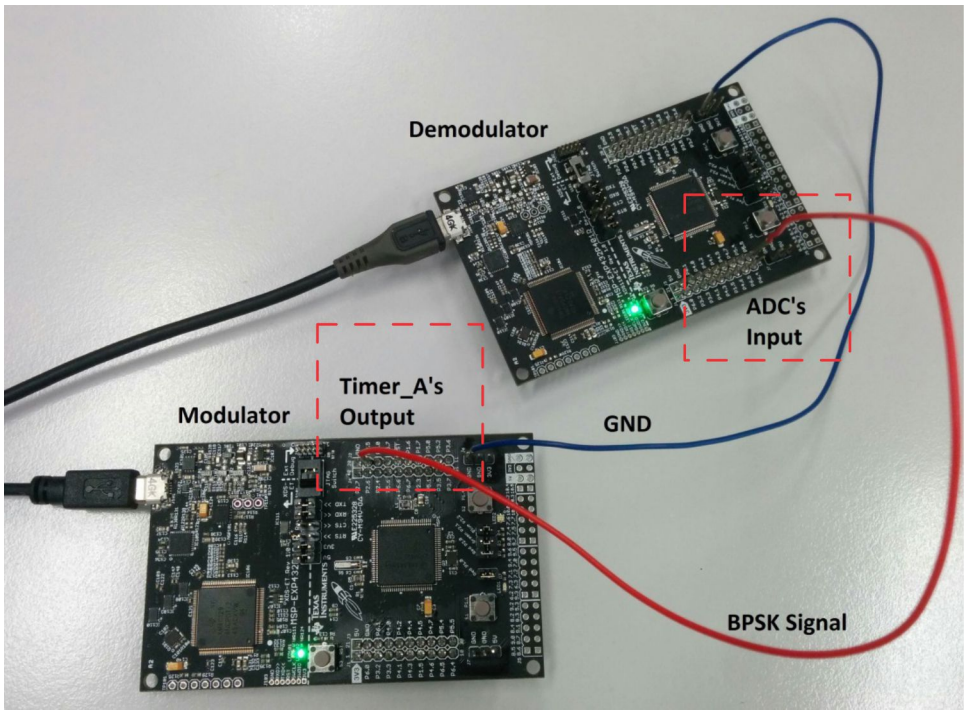

Figure 12. Hardware Test Bench

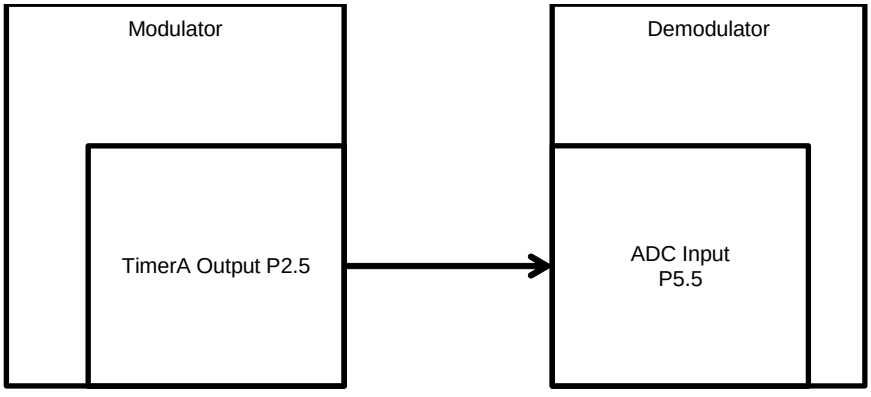

Figure 13. Hardware Connection Block Diagram

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The tool versions of the software platforms are:

- IDE: Code Composer Studio IDE v6.1.3
- Compiler: TI ARM Compiler v5.2.7
- Software Library: MSPWare v3.40.xx.xx and CMSIS v4.5.0

4.2 Modulator

Figure 14 shows the overview of a complete packet transmitted in BPSK waveform, which has a 22-ms duration. Figure 15 zooms in to show the modulation at bit level. The yellow waveform represents the modulated signal, and the blue waveform represents the carrier.

The test consists of a 30-byte data transmission without FEC. The entire transmission takes 1.92 ms (30 × 8 / 125 kHz = 1.92 ms) while the CPU loading is 41.5%. For CPU loading calculation, see Section 7.3.

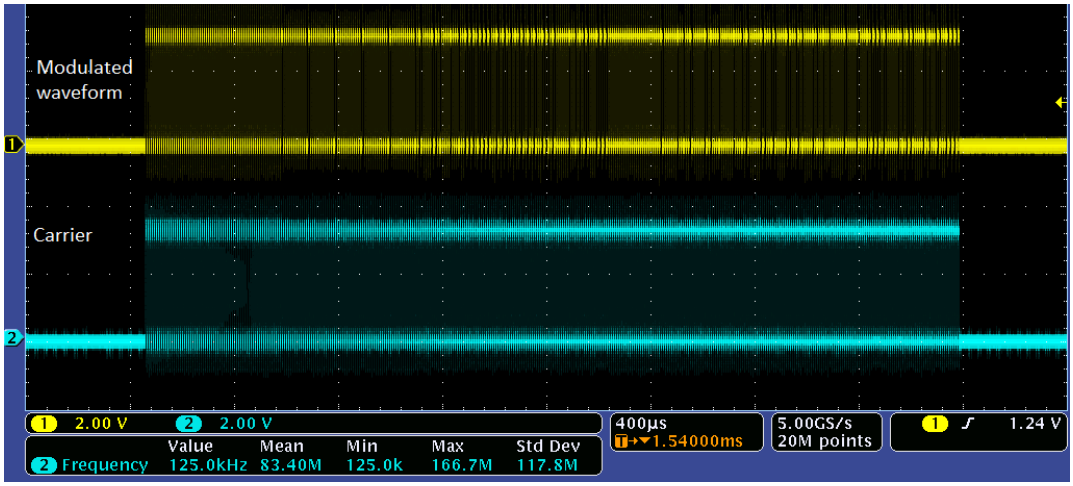

Figure 14. BPSK Waveform Generated by Modulator

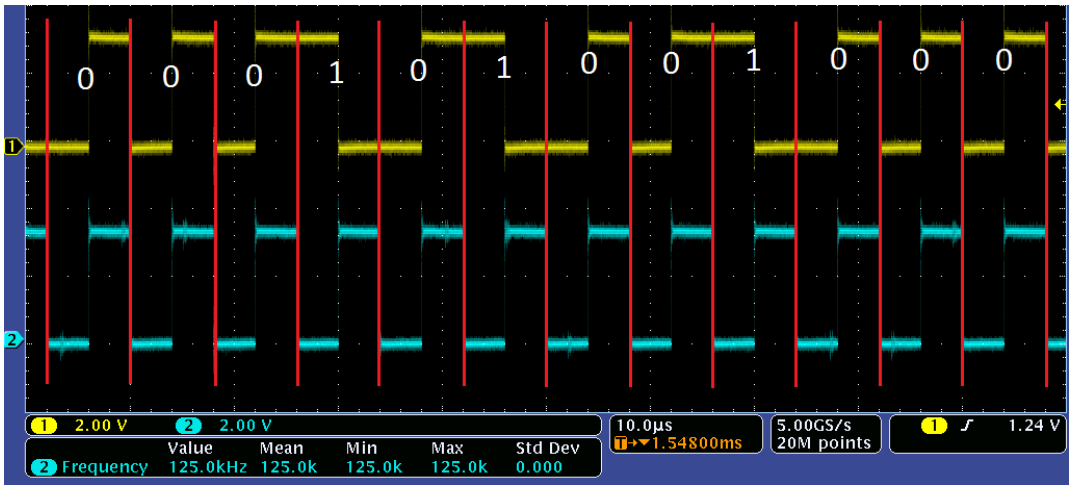

Figure 15. Detailed BPSK Waveform

All values are specified at 125 kbps of 240-bit data without FEC encoded, with 3.3-V V_{CC} and 48-MHz CPU clock.

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Table 1. Test Results for Modulator

Parameter	Value	Unit
CPU use	41.5%	
Current consumption	7	mA
Flash use	4120	bytes
SRAM use	630	bytes

The complete code requires 4120 bytes plus 630 bytes for the data buffer. The system consumes 7-mA current at 48 MHz and 3.3 V.

4.3 Demodulator

Transmitting a complete 210 byte encoded data requires 21.84 ms (see Table 2). In this complete configuration, the receiver takes 10.1 ms for demodulation and 1 ms for FEC decoding. For applications operating in noise-prone environments, a FIR LPF is recommended to improve SNR. Adding the 24-stage FIR LPF filter doubles the CPU loading.

Table 2. Runtime of Each Operation in Demodulator

Operation	Runtime (ms)
Receiving 210-byte data with FEC encoded	21.84
Demodulating without 24-stage LPF	10.1
24-stage LPF filtering	44.9
FEC decoding	1
Total	78

Table 3 lists the resources that are required for demodulation.

Table 3. Test Results for Demodulator

Parameter	Value	Unit
Current consumption	7	mA
Flash use	6420	bytes
SRAM use	34500	bytes

To calculate the performance advantage of the hardware FPU, an additional experiment with the FPU module disabled was performed. Because the CMSIS DSP Library takes advantage of the FPU, when deactivating FPU, the implementation must use general operations instead of calling functions in the CMSIS DSP Library. In this experiment, the LPF is disabled because the FIR LPF implementation is complex without the use of CMSIS DSP Library functions. The runtime when using general operations with the FPU enabled is higher than operation using the CMSIS DSP Library. This demonstrates that the CMSIS DSP Library has optimized the calculation operation by taking advantage of FPU. Figure 16 shows the runtimes of both test conditions.

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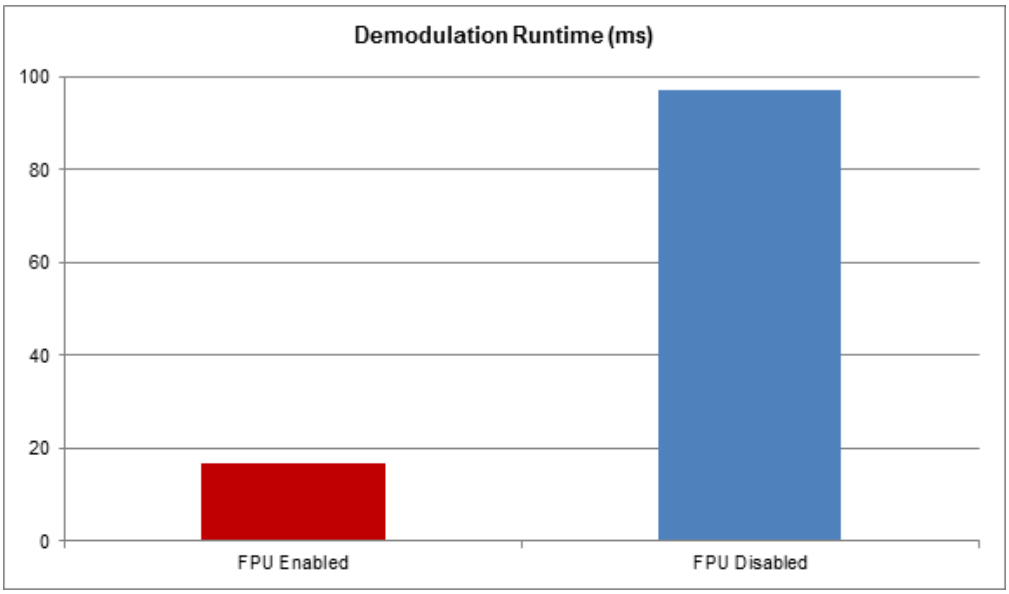

Figure 16. Demodulation Runtime Evaluation for FPU Use

4.4 Optional FEC

A functional test was performed for the FEC implementation. The test added a randomly generated single-bit error in the receive side and determined whether or not the FEC implementation corrected the error. Figure 17 shows the FEC test block diagram. More than one thousand tests were run, and all of them recovered the correct data after FEC decoder. This proves the FEC implementation functionally works well.

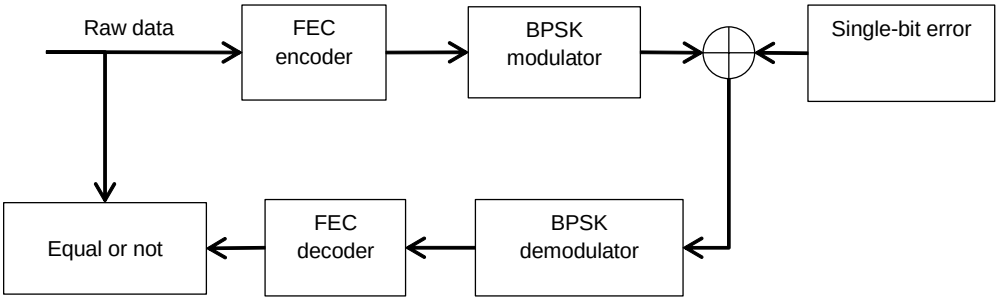

Figure 17. FEC Test Block Diagram

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5 Conclusion

This application report introduces a complete design for a software-based 125-kbps BPSK modem. The test results show that the BPSK modem implemented on MSP432 MCU platform shows significant benefits by taking advantage of the FPU and DSP extensions of the Cortex-M4F CPU. Complete modem functionality can be designed in software using the on-chip timer and ADC peripherals with minimal external components. This can be an effective solution for an application that requires an economic low-power space-limited solution.

6 References

- *MSP432P401x Mixed-Signal Microcontrollers*
- *MSP432P4xx Family Technical Reference Manual*
- *MSP432P401R LaunchPad Development Kit (MSP-EXP432P401R) User's Guide*
- *Using the CMSIS DSP Library in Code Composer Studio™ for TM4C MCUs*
- MSP432 Peripheral Driver Library
- *ARM Optimizing C/C++ Compiler v5.2 User's Guide*

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7 Appendix

7.1 BER

Equation 2 shows the calculation of the BPSK BER.

$$BER = \frac{1}{2}erfc(\sqrt{\frac{SNR(1-\rho)}{4}}) \tag{2}$$

Where erfc(x) is the complementary error function that defined as Equation 3, which is a monotonically decreasing function.

$$erfc(x) = 1 - \frac{2}{\sqrt{\pi}}\int_0^x exp(-z^2)dz \tag{3}$$

Where ρ is the correlation coefficient. For BPSK, ρ reaches its minimum value – 1, which makes the BPSK BER reach its minimum value.

7.2 FEC

Any 8-bit raw data can be encoded into 13-bit codeword by applying Hamming (13, 8) generator matrix G(x) (see Equation 4).

$$G(x) = \begin{bmatrix} 1&0&0&0&0&0&0&0&1&1&1&0&0 \\ 0&1&0&0&0&0&0&0&1&0&0&1&1 \\ 0&0&1&0&0&0&0&0&0&1&0&1&1 \\ 0&0&0&1&0&0&0&0&1&1&0&1&0 \\ 0&0&0&0&1&0&0&0&0&0&1&1&1 \\ 0&0&0&0&0&1&0&0&1&0&1&1&0 \\ 0&0&0&0&0&0&1&0&0&1&1&1&0 \\ 0&0&0&0&0&0&0&1&1&1&1&1&1 \end{bmatrix} \tag{4}$$

The Hamming (13, 8) codeword can be checked by either re-applying G(x), or by using the parity-check matrix H(x) (see Equation 5), where H·G^T = 0, under the binary half-add rule, 1 + 1 = 0.

$$H(x) = \begin{bmatrix} 1&1&0&1&0&1&0&1&1&0&0&0&0 \\ 1&0&1&1&0&0&1&1&0&1&0&0&0 \\ 1&0&0&0&1&1&1&1&0&0&1&0&0 \\ 0&1&1&1&1&1&1&1&0&0&0&1&0 \\ 1&1&1&1&1&1&1&1&1&1&1&1&1 \end{bmatrix} \tag{5}$$

H(x) can be used to calculate if the codeword is broken, or how many bits are broken in the codeword, or which bit is reversed in the single-bit broken codeword. If only a single-bit error occurs in the codeword, the error can be corrected as follows.

Assuming vector *x* represents 8-bit raw data, *y* is the codeword generated using *G* (see Equation 6).

$$y = G^T x \tag{6}$$

When a single-bit error occurs in *y* as *y′*, where *y′* = *y* + *e*, where *e* is the error vector. Use H(x) to check *y′* (see Equation 7).

$$C = Hy' = H(y+e) = H\left(G^T x + e\right) = He \tag{7}$$

If no error occurs, that is, if *e* = *0* , then *C* = *0*; if a 1-bit recoverable error occurs, the elements in *e* are all 0 except for only one 1, and *C* is the one column vector of *H*; if 2 or more bits of unrecoverable error occur, more than one 1 is in *e*, and *C* is the linear combination of column vectors of *H*. The checksum vector *C* can determine if an error occurred and what kind of error occurred. *C* can be used to recover a 1-bit error.

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7.3 CPU Loading

CPU loading is achieved by:

1. Set CPU clock as 48 MHz, in addition to all other system initial settings.
2. Generate the data that to be transmitted.
3. Use interrupt to send the data and, while in the main loop, activate a continuous counter.
4. Record the counter value (as *A*) at the end of transmission.
5. Use a counter to count in a dummy program for the same time, and record the counter value (as *N*).

Calculate the CPU loading as 1 – (A / N).

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