Samsung starts mass roll-out of 3-bit 3D V-NAND flash memory chips

author:itersnews October 9, 2014

(iTers News) - Samsung Electronics Co., Ltd. said today that it has begun mass production of a 3-bit multi-level-cell, or MLC 3D Vertical NAND or V-NAND flash memory for use in solid state drives (SSDs) in what the chip maker said is the world's first of its kind ever.

The 3-bit V-NAND is its third generation of its 3D V-NAND flash memory series, coming complete with 32 vertically stacked cell layers. It has 128 gigabits of memory storage.

Unlike a 2D planar structure NAND flash memory chip that stores data in a conductive floating gate, the 3D V-NAND flash memory chip technology writes and reads data out of a non-conductive layer using charge trap flash (CTF) technology.

Each cell array is vertically stacked on top of one another to form multibillion-cell chips.

The vertical cell stacking structure allows Samsung to get more chip out of silicon wafer. Compared to Samsung's 10 nanometer-class 3-bit planar NAND flash, for example, the new 3-bit V-NAND has more than doubled wafer productivity.

"With the addition of a whole new line of high density SSD that is both performance- and value-driven, we believe the 3-bit V-NAND will accelerate the transition of data storage devices from hard disk drives to SSDs," said Jaesoo Han, Senior Vice President, Memory Sales & Marketing, Samsung Electronics. "The wider variety of SSDs will increase our product competitiveness as we further expand our rapidly growing SSD business."

Samsung started mass-production of its first generation 24 layer-cell V-NAND in August 2013, and in May 2014, the chip maker ramped up to a second generation V-NAND that comes with a single bit 32-laye cell array structure.

With the launch of the 32-layer 3-bit V-NAND, Samsung is leading the 3D memory market by speeding up the evolution of V-NAND production technology.

After having first produced SSDs based on 3-bit planar NAND flash in 2012, Samsung has proven that there is indeed a mass market for high-density 3-bit NAND SSDs.

The industry's first 3-bit 3D V-NAND will considerably expand market adoption of V-NAND memory to SSDs suitable for general PC users, in addition to efficiently addressing the high-endurance storage needs of most servers today.

Samsung opens terabit era with 3D V-NAND flash memory chips

author:JH Bae July 24, 2014

(iTers News) - The semiconductor industry's mantra Moore's Law hits a snag in delivering on its promise that the industry would double the number of transistors every 18 or 24 months, facing the toughest challenge ever in ramping up to a finer chip processing technology.

As the industry is now struggling to go below a 20 nanometer and below chip processing technology, for example, it suffers from slowdowns in the chip performance gain as well as difficulties in containing increases in heat generation and power consumption.

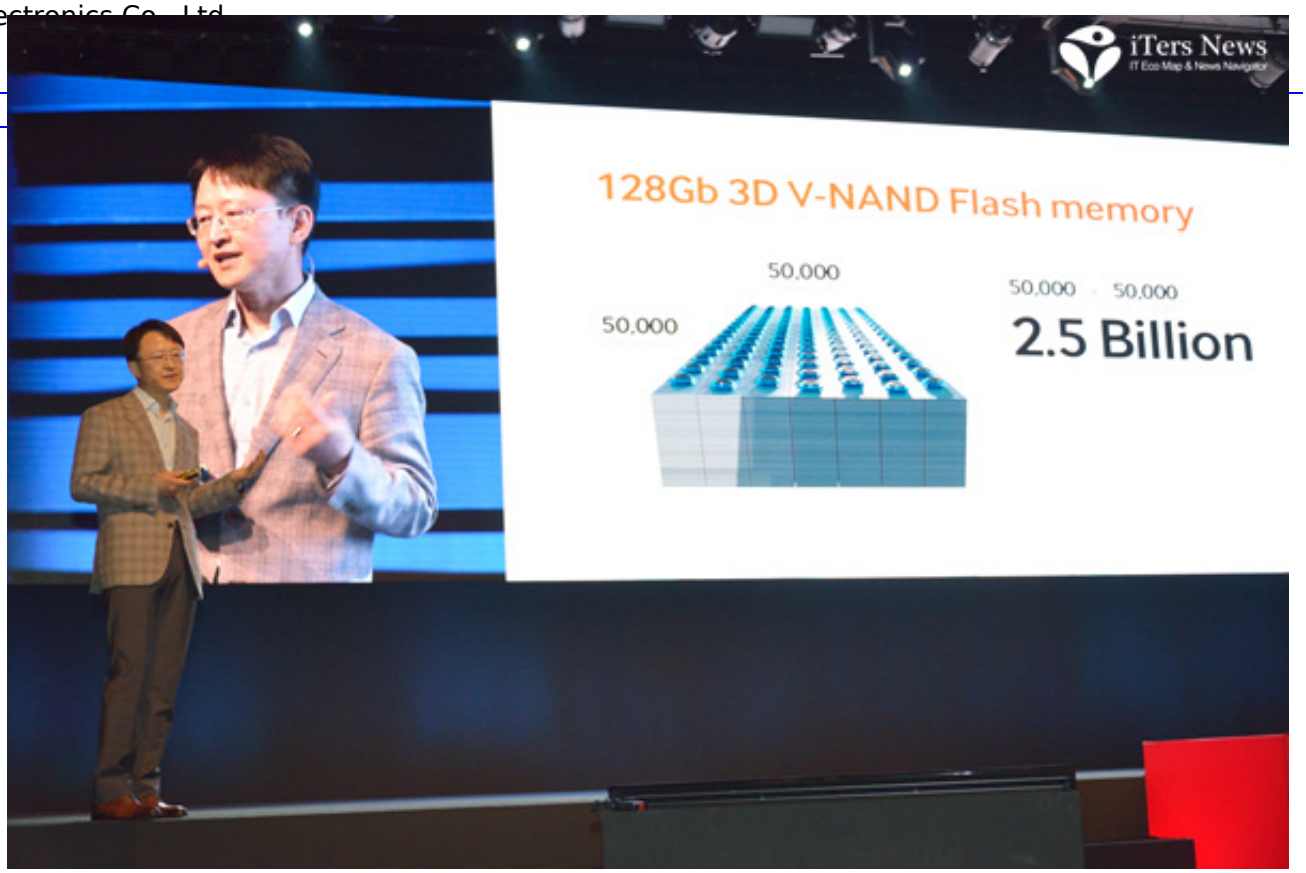
That's because it is increasingly difficult to trace and pattern transistors of which geometry is as thin as 20nm and 10nm without compromising power consumption. So is it to pack two times more transistors into a given silicon footprint every 18 or 24 months.

This technology challenge helps explain why chip giants like Intel Corp. are now turning to a 3D FinFET chip-making technology for future generations of SoCs, as they are scrambling to fabricate chips of as thin geometry as 20nm and 10nm.

NAND flash memory chip makers are no exception. To tackle technology hurdles in reducing costs, doubling chip density, and improving reliability, NIAND flash chip makers are working on a 3D NAND chip technology, too.

Leading their migration to the 3D chip technology is Samsung Electronics that is already mass-producing 3D V-NAND flash memory chips.

"You need another new approach to build the foundation for the future generation of NAND flash memory chips. Disruptive technology is required to satisfy capacity, cost, and reliability requirements," said Dr. Kye-Hyun, Kyung, senior vice president of flash design team with Samsung Electronics Co., Ltd.



Added he, “The benefit of reducing the cell size was vast. In 1999, we only produced 1Gb NAND flash memory chips with a 120nm design rule technology. But, now with the 10nm-class chip processing technology, we can fit 64 times more cells into a same area to put 64Gbs of data (compared with the 120nm technology). Every time, we shrink the cell size, however, we already face technical challenges. We need to develop a design technology to prevent the cell to cell interference. And we should find light source for photolithography process.”

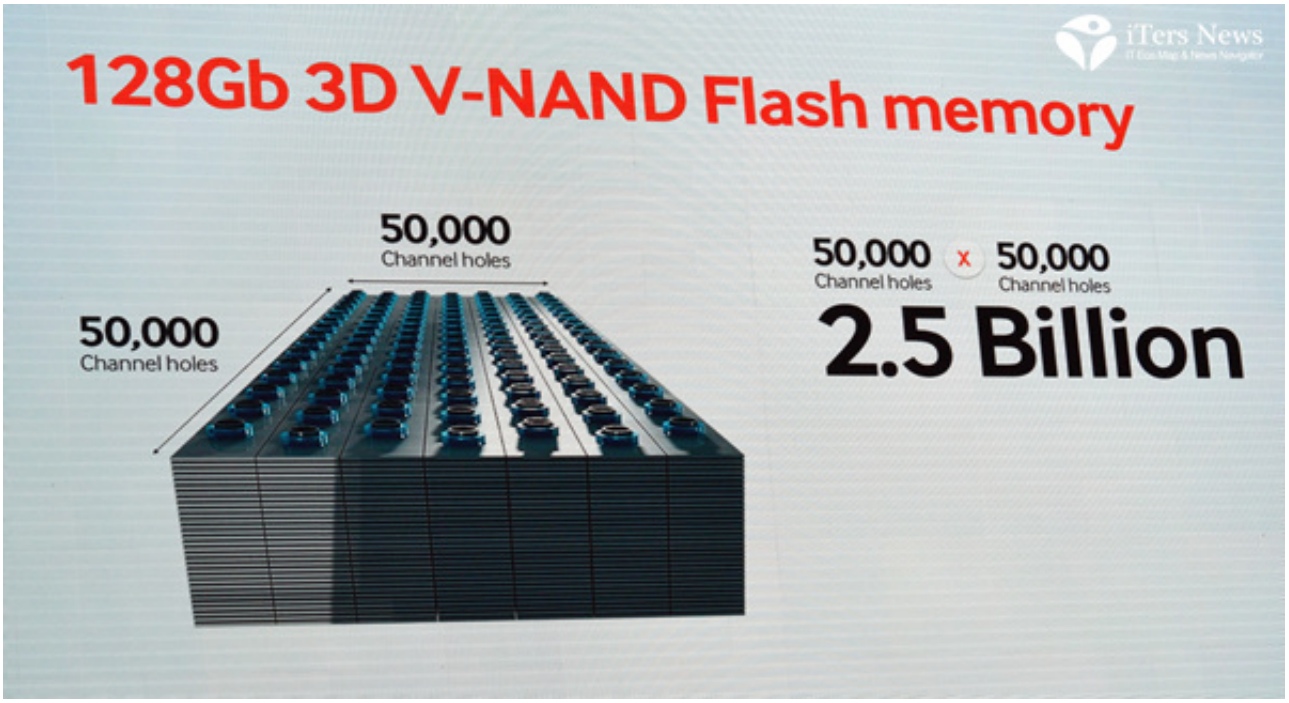
As the geometry of the NAND flash memory chips got below 20nm, according to Dr. Kyung, it started to get increasingly difficult to control the cell-to-cell interference. The ramp-up to the 10nm processing technology also required prohibitively expensive investment costs on new light source equipment for photolithography process like EUV, or extreme ultra violet machine, leading to hefty increases in the chip production costs. It takes still a couple of more years before the EUV equipment gets fully commercialized, too.

The width of the chip circuitry depends on the wavelength of the light source. The EUV is the next generation of light source for patterning the 10nm-class chip circuitry, because its wavelength is far shorter than current ArF immersion light source technology.

The cell-to-cell interference refers to a phenomenon that one cell affects the behavior of another adjacent cell in what’s called as a coupling effect, resulting in data corruption.

The narrower the distance between cells gets, the stronger the interference gets, corrupting more of data.

Bedeviled by these two major technology challenges, NAND flash memory chip makers hit a dead-end in further increasing the density of a chip. For example, the 128Gbs are the maximum chip density that a NAND flash memory chip of a 10nm-class circuitry can implement.



Stack cells in a 3D structure

To break through the technology bottleneck, Samsung broke new grounds in three key areas; material engineering, cell interconnection, and chip structure.

Unlike current NAND flash memory chips that are built with a 2D planar structure. Samsung stacked cells over cells horizontally in a 3 dimensional structure to fabricate a 3D V-NAND flash memory chip.

The 3D chip structure paved the way for Samsung to exponentially increase the density of the NAND flash memory chips, enabling it to break through a current ceiling of 128Gb density with no recourse to a far finer design rule technology..

Using a 20nm-class design rule technology, for example, Samsung packed as many densities in a 3D structure as the chip maker did in 2D planar with a 10nm-class manufacturing process.

Samsung is now fabricating 24-layer and 32-layer 128Gb 3D V-NAND flash memory chips in high volume using a 20nm class-design rule stacking cells on the top of each other up to 24 and 32 layers, respectively.

Innovations in material science also helped Samsung to eliminate the cell-to-cell interferences. Consisting of a floating gate a channel gate, and a control gate, the 2D planar structure NAND flash memory cell stores data in a conductive floating gate, writing and reading it out of the gate.

On the other hand, Samsung’s 3D V-NAND flash memory chip stores data, or electronic charge on a non-conductive insulator using what’s called as a charge trap flash, or CTF technology and then surrounds it with a control gate.

“Our research team had been working on a way to build a cell-to-cell interference-free chip structure, while scrambling to develop a technology to stack more capacity in a given silicon footprint with a larger design rule,” said DR. Kyung of Samsung.

True enough, Samsung’s CTF technology is a new breed of groundbreaking memory chip technology that uses a non-conductive insulator as a data storage circuitry instead of a conductive floating gate.

Etching the insulator circuitry on a silicon wafer required new chemical compound that is different from those used for a conductive floating gate.

Unlike a floating gate where data or electronic charge easily moves in and out, the insulator layer tightly keeps data inside, steering clear of coupling effect and thus cell to cell interference phenomenon.

Write data in an insulator

“As a control gate covers an insulator, there is no cell to cell interference in the 3D V-NAND. In other words, the insulator prevents signal noises, there is no cell to cell interference,” said Dr. Kyung.

To vertically string together cells over cells, Samsung also developed what’s called as channel hole technology, a sort of cell interconnection technology that vertically interconnect layer over layers of cells by punching holes all the way through bottom to top. The vertical interconnection technology allowed Samsung to stack up to 32 layers of cells vertically.

All combined, those technology breakthroughs translate in tremendous gains in chip density performance, reliability, endurance, and power consumption.

For one thing, the 3D NAD flash chip technology laid the foundation for Samsung to exponentially increase the chip density. By 2017, Samsung bets that it will be able to fabricate 1 tera bit 3D V-NAND flash memory chip.

As it comes with no software algorithm to verify and correct cell-to-cell interference, it can also write and read data about two times faster than a 2D planar NAND flash memory chip. It also consumes 46% less power, as it doesn’t need to decode the software algorithm.

Longer endurance is another edge. Endurance is a measure of how many times a NAND flash memory chip can write data into cells. As the 3D V-NAND writes data into an insulator, which is more resistant to data wear-out or corruption, it boasts 2 to 10 times more endurance.

Nearing cross-over price point

These improvements come at a crucial time when NAND flash memory chip-based SSD or solid state drives are increasingly replacing conventional HDDs as a mass-storage device for PCs and data center serve computers.

Samsung bets that mass-production of 3D NAND flash memory chips will likely accelerate the replacements, as it would help greatly reduce costs.

Coming complete with NAND flash memory chips, memory controllers, and a firmware, SSDs far outperform HDDs in data reading and writing speed, but its unit cost per byte is still more expensive than that of HDDs, although there have been dramatic cut-downs in the byte-per-unit price.

For example, the unit price-per-byte of SSDs hovered above US$15 in 2006 when single level cell, or SLC NAND flash memory chip-based SSDs were first released. In 2008, the unit price dropped to US$5.1 per byte, as the industry rolled out world‘s first MLC or multi-level cell NAND flash memory chip-based SSDs.

In 2012 when a 512GB SDD rolled off the production line, it broke a barrier of US$1 per byte, gaining watershed momentums to replace HDDs in PC and other consumer electronics markets.

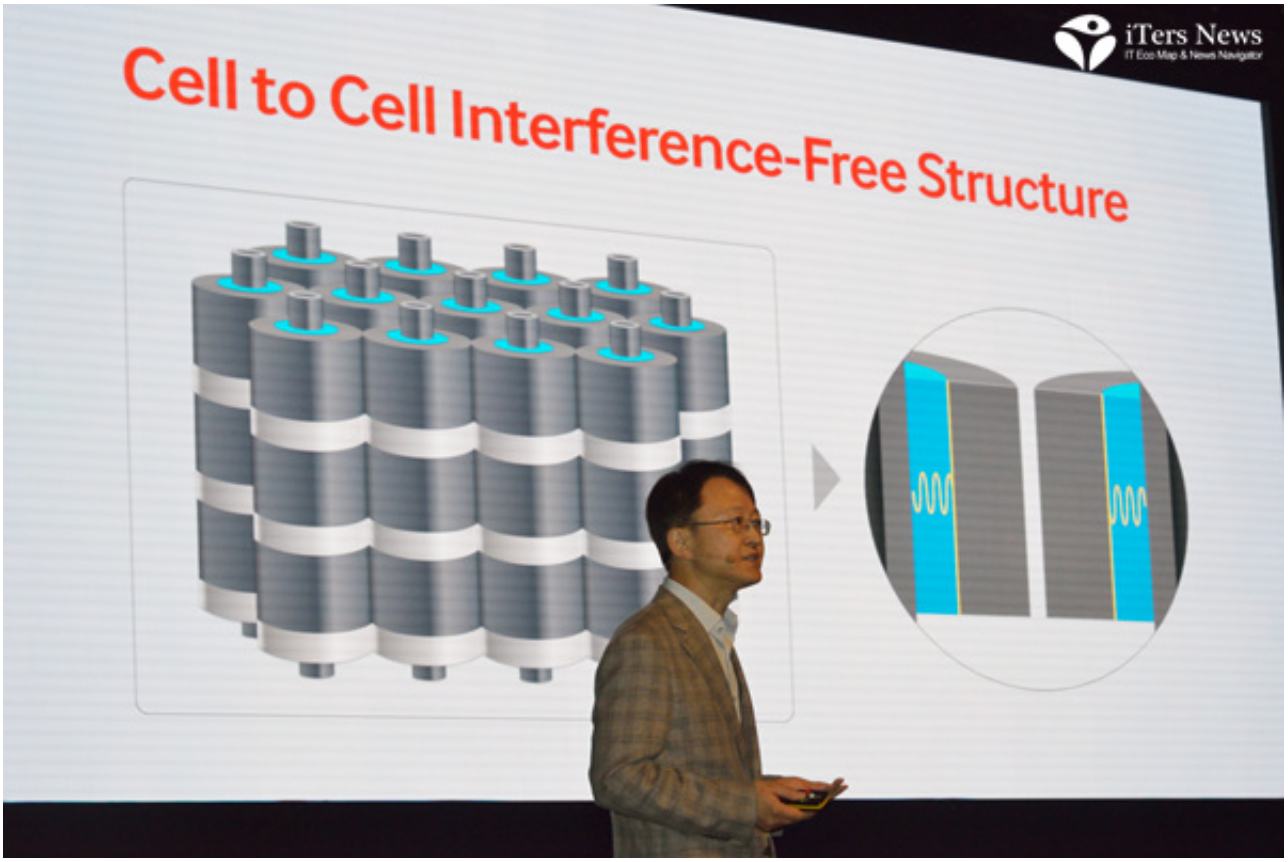
“Think of data center, and stacks of HDDs are replaced by SSDs. NAND flash memory chip is ubiquitous. It is everywhere and is now an integral part of virtually every consumer CE device out

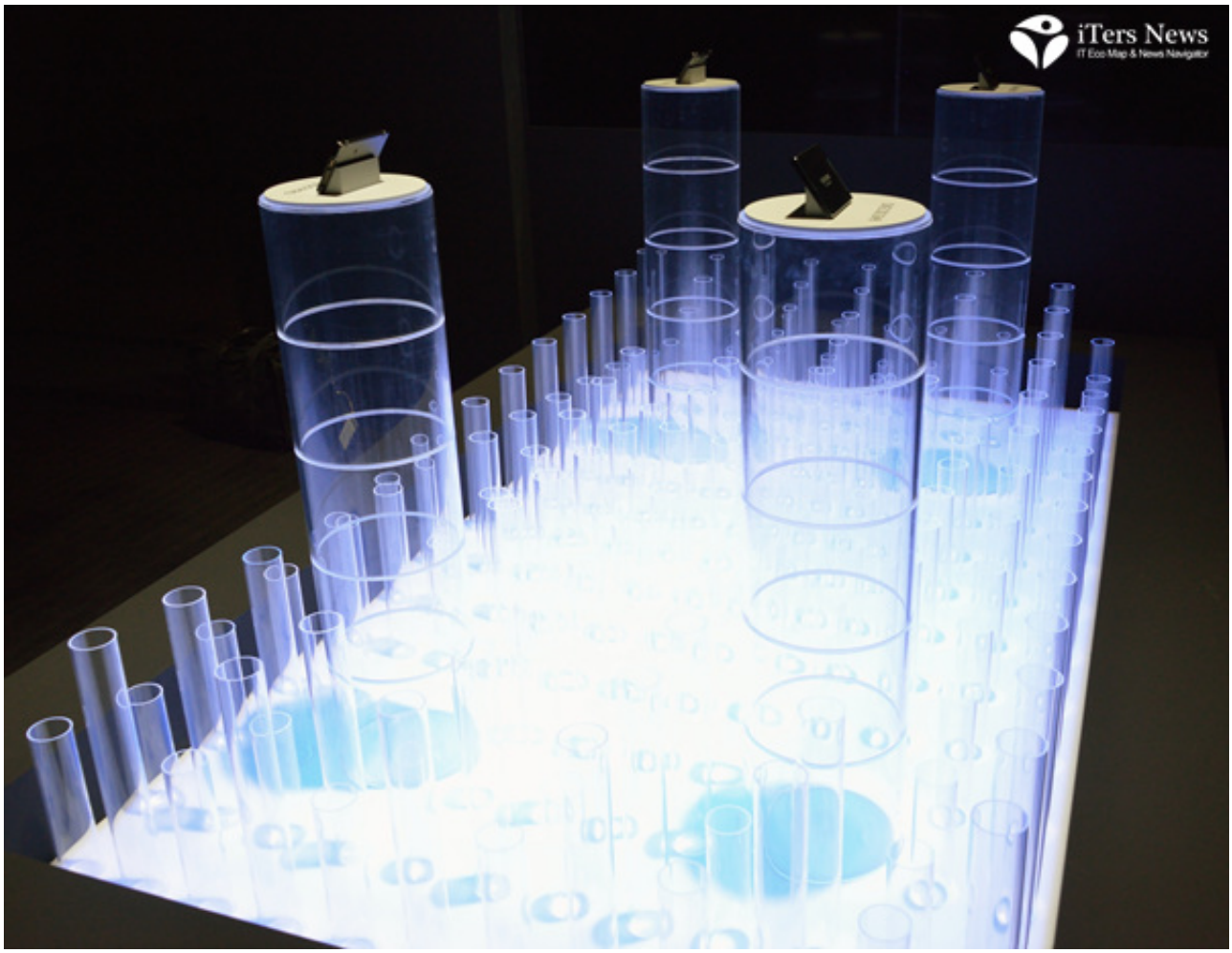
there making a significant inroad into data center and server infrastructure," Jim Elliott, vice president of memory marketing with Samsung Electronics.

According to him, SSD market will grow 30% in 2014 and continue to grow at CAGR 25% to hit US$20 billion in 2017.

As the rapid proliferation of connected devices like smart phones and tablet PCs would drive explosions in the data traffic, he expects data center would become more storage-hungry, fueling explosive demand for SSDs.

"Facebook logs more than 9 billion page views per day, while more than 500 million tweets are being uploaded per day. Think of YouTube. More videos are uploaded to YouTube in one month than major U.S. broadcasting networks created in 60 years. That is the pace of the change the industry is experiencing right now," added Jim Elliott.

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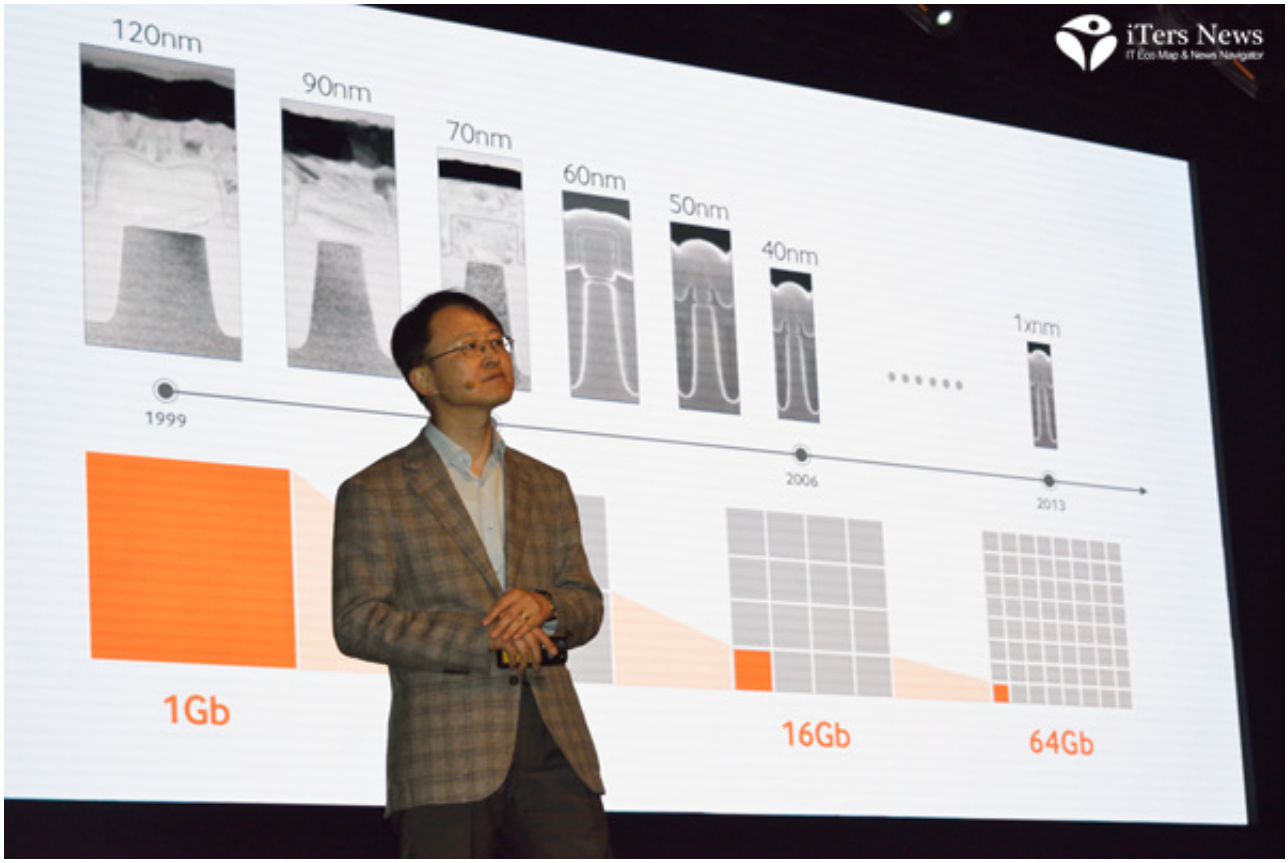
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Samsung starts mass-production of 32 layer V-NAND flash memory chips

author:Jason Jiang May 29, 2014

(iTers News) - Samsung Electronics' push for V-NAND flash memory chip technology is coming closer to fruition, as the 3D structure non-volatile memory chip is laying out the groundwork for the mass-replacement of SSD, or solid state drive markets with traditional HDD, or hard disk drives.

About one year after it started mass-production of 24 layer 3D V-NAND flash memory chips, Samsung Electronics has started volume production of 32 layer 3D V-NAND flash memory chip in what the chip maker said is the world's first mass rollout of the 32 layer-structured NAND flash chip.

The V-NAND flash memory chip is a new breed of NAND flash memory chip that vertically stacks transistor cells in a 3-dimesnion cylindrical structure. The 32 layer NAND flash memory chip refers to a chip that deposit 32 layers of transistor cells atop each other.

Unlike conventional planar 2D structure NAND flash memory chips stores data in a conductive floating gate, the 3D V-NAND NAND flash memory chip writes and reads data out of what's called a non-conductive charge trapping gate.

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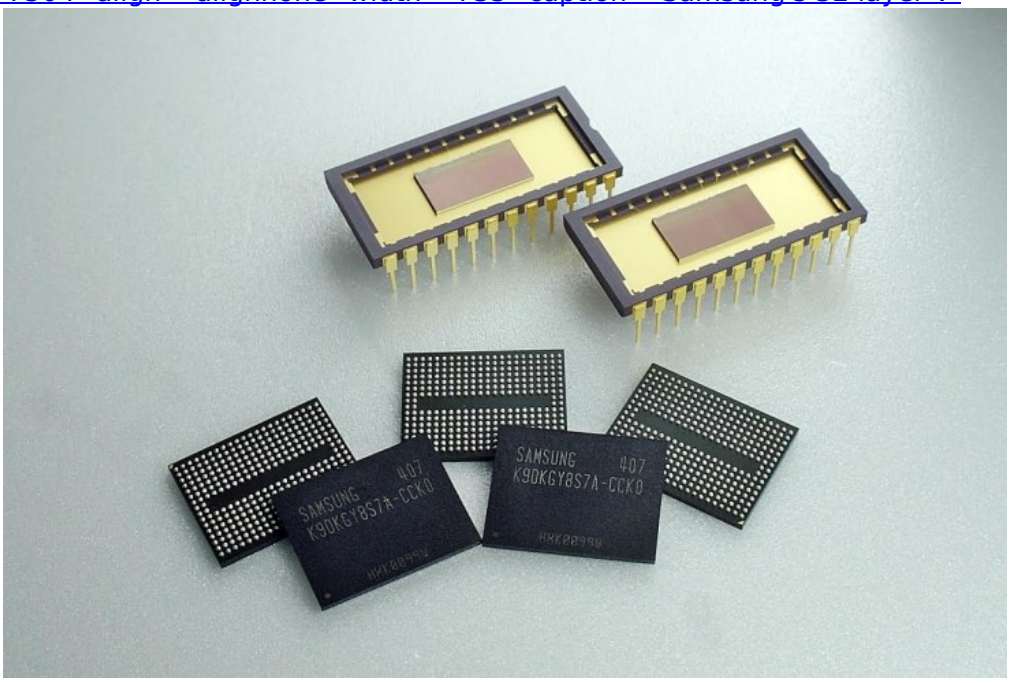


[/caption]The cell of NAND flash memory usually consists of a control gate, a channel gate for data transfer, and a conductive floating gate or a non-conductive charge trapping gate for data storage.

The implementation of the non-conductive charge trapping gate translates into less occurrence of short circuits between the non-conductive gate and the channel gate, more endurance of what's called as flash –out, or data defect rate, thinner gate oxide, and less power consumption. For example, the new 3D V-NAND-based SSDs have approximately twice the endurance for writing data and consume 20% less power, compared to planar 2D MLC NAND-based drives.

Compared with the 2d planar cell structure, the 3D vertical structure also can store more of data in a NAND flash memory chip"]

given silicon footprint, as it cram more of cells in a single silicon die.

All combined, the technology innovations leave Samsung with ample room for cost-cutting, enabling the chip maker to churn out higher density SSD at lower costs.

SSDs are a collection of NAND flash memory chips, a microcontroller, and a firmware on a circuit board. They can read and write data much faster than mechanical ultra-tiny micro-motor-based HDDs. Yet, they are still costlier, which is a major impediment against the rapid replacement of HDDs.

As the 3D V-NAND flash memory chip boasts of lower costs per bit stored in a given space, it has been expected to help speed up the replacement.

For example, Samsung has just launched a line-up of premium SSDs based on the 32 cell-layered V-NAND flash memory, including 128 GB, 256GB, 512GB and 1TB storage options.

“We increased the availability of our 3D V-NAND by introducing an extensive V-NAND SSD line-up that covers the PC market in addition to data centers,” said Young-Hyun Jun, executive vice president, memory sales and marketing, Samsung Electronics. “Look for us to provide a consistent, timely supply of high-performance, high-density V-NAND SSDs as well as core V-NAND chips for IT customers globally, contributing to fast market adoption of 3D NAND technology.”

According to a recent research report by market research firm Gartner, NAND flash memory chips will grow to US$44.6 billion in 2017, or more than 50% of worldwide memory chip market, which will hit approximately US$79.7 billion, as the penetration will speed up.

Samsung's Xian, China 300mm wafer fabrication facility comes on line, churning out 3D V-NAND chip

author:JH Bae May 9, 2014

(iTers News) - Samsung Electronics' Xian, China 300mm wafer fabrication facility comes on line today, starting to roll out 3D V- NAND flash memory chips in high volumes.

The Xian, China fabrication facility marks global memory chip market leader Samsung Electronics' first front-end chip making facility in China,
Spreading on a land lot of 1.14 million square meters, the fabrication facility will operate at a monthly capacity of 100,000 wafers, mainly churning out 3D V-NAND flash memory chips of 10nm-class geometry.
The chip-making operation in China represents Samsung's efforts to address the world's fastest-growing NAND flash memory chip market, which makes up global demand for the non-volatile memory chips.
The company expects the Xian chip-making facility to generate US$4 billion to US$5 billion in annual sales.
The Xian facility is also expected to give Samsung another leg-up in its drive to fuel demand for SSDs, or solid state drives, as the mass-rollout of 3D V NAND flash memory chip would make the still expensive NAND flash-memory chip-based solid state drive more affordable.
Samsung is now mass-producing a NAND flash memory chip at its Hwasung facility in the city of Hwasung, Korea. The Chinese facility will give economies of scale to cut back chip prices.
SSDs is a replacement to HDDs, coming complete with NAND flash memory chips, a controller, and a firmware.

They are still far costlier, compared with HDDs. Yet, the 3D V-NAND flash memory chips would help chip makers not only to cut down prices of NAND flash memory chips, but also expand storage density-per chip, fueling replacement demand for SSDs.
The 3D V-NAND is a chip that stacks cells of transistor vertically.
Keys to the 3D vertical cell-stacking chip processing technology are Samsung‘s two homegrown indigenous technology breakthroughs – 3D CTF, or charge trap flash technology and vertical interconnect technology.
In the conventional planar NAND flash memory chip structure that is composed of a floating gate, a control gate and a channel, bit streams of 1s and 0s are stored in its floating gate – a conductor - when voltage is cut off from a channel, because the cut-off traps electrons in the floating gate. Repeats of write on and off of data out of the floating gate causes a short between a floating gate and a channel, however, compromising the reliability of the NAND flash memory chips.
On the other hand, the CTF technology reorganizes the planar structure into a non-planar cylindrical structure, puting a channel gate at its core, then surrounding it with an insulator, and finally wrapping the insulator with a control gate. Electrons, or electronic charges are stored on the insulator, which is made of silicon nitride film, not on a floating gate.
Then, Samsung stacked this single cylindrical layer of 3D CTF NAND flash cell on top of each other until it reaches 24 layers using special etching technology that connects the layers electronically by punching holes from the top to the bottom.

Taking advantage of the two technology breakthroughs, Samsung developed a 128Gb MLC 3D V-NAND flash memory chip that is built with 24 layers of cells using an older 30nm-class process, and has been mass-producing them starting from early August.
It took 20 months to complete the Xian factory since it broke ground in September 2012.
The chip maker is now even constructing a back-end test and assembly line at the Xian facility to have a fully integrated chip making line. The test and assembly line will start to operate by year-end.

Samsung's Xian, China 300mm wafer facility to come on line in May

author:JH Bae March 27, 2014

(iTers News) - Samsung Electronics said that it is putting finishing touch on its Xian, China 300-mm wafer fabrication facility to have the chip-making facility come on line in May. The wafer fabrication facility, which already started its test operation in early 2014 plans to mainly roll out a next generation of cutting-edge 3D V-NAND flash memory chips. Located in the city of Xian, China the facility is also Samsung's first front-end wafer fabrication facility in China.

The 3D V-NAND is a 3D structured, vertically stacked NAND flash chip that stack transistor layer after layer on a single sliver of wafer. Rather using a traditional floating gate technology, Samsung adopted non-conductive charge trap technology to store in and out electrons.

The construction began in Sept. 2012 with an capital investment of US$ 7 billion

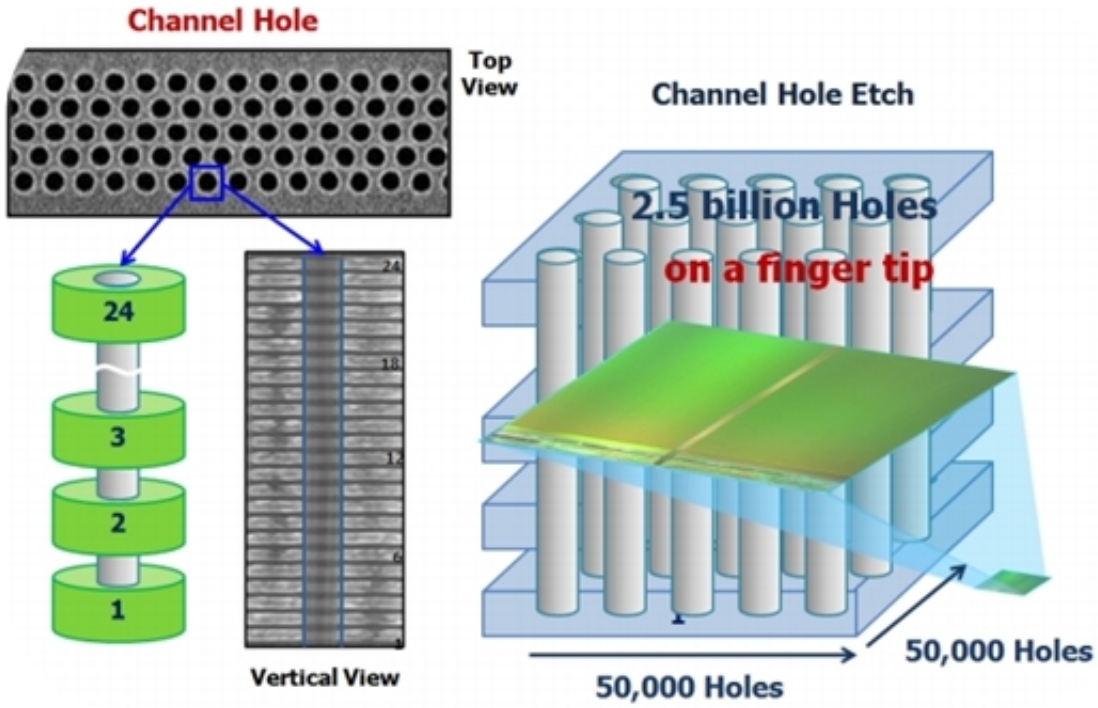
Samsung's 3D V-NAND breaks through chip scaling limits

author:JH Bae February 14, 2014

(iTers News) - As its migration to EUV, or extreme ultra violet lithography technology proves more challenging than expected, global chip-making industry hits a dead-end in scaling down its chip-processing technology below 10nm circuitry.

To break through the limit, chip makers are now struggling with a new groundbreaking way to fabricate transistors in a non-planar 3 dimensional structure. For example, SoC chip makers like Intel Corp. are now tinkering with a FinFET 3D transistor technology to reduce heat dissipation and current leakage that will further deteriorate as the width of the gate circuitry gets as narrow as 10nm and below.
On the other hand, NAND flash memory chip makers like Samsung Electronics and Toshiba Corp. are working on their respective 3D transistor cell structured-NAND flash memory chip technologies.
True enough, the chip-scaling technology is a measurement of how small a chip's gate circuitry, or transistor is. As semiconductor industry's mantra Moore's Law implies, if the size of the transistor is cut in half, the density and the performance of a chip double, opening the way for cuts in half in costs.
Yet, everything has its own trade-off. The downside is that heat dissipation and current leakage increases in proportion to the shrinkage of the transistor size. As electron more often swerve out of the course between a source and a drain.
NAND flash memory chips are no esception to this heat dissipation. As the width of the chip circuitry gets narrower and narrower, the interference between cells gets intensified, aggravating electron leakages.
Especially when the circuitry gets down to 10nm and below, electrons start to bump against each other, making the 10nm circuitry NAND flash memory chip almost commercially unviable.
The commercial unavailability of the 10nm circuitry NAND flash memory chip technology comes as a shock to top-tier NAND flash memory chip makers like Samsung and Toshiba.
That's because the nightmarish scenario suggests that NANAD flash memory chip-based SSDs, or solid state drives won't undercut longtime rival HDDs on price at least for the time being, slowing down the penetration of SSDs into consumer electronics markets.

Stacking transistor cells vertically



That’s where the forte of Samsung Electronics’ 3D V-NAND chip-making technology comes in.

The 3D vertical cell-stacking chip making-technology can step up chip density by a magnitude of two times using current 20nm or 30nm chip circuitry processing technology without ramping up to a 10nm geometry technology.
On top of that, it can keep the cell to cell interference at the minimum and thus minimize electron leakages. .
The 3D vertical cell-stacking technology is a sort of disruptive technology that breaks away from conventional planar transistor technology. Samsung Electronics likens the vertically-stacking structure of the3D V-NAND chip to the world’s tallest towering 160-story Burj Khalifa skyscraper in Dubai.
Keys to the 3d vertical cell-stacking chip processing technology are Samsung‘s two homegrown indigenous technology breakthroughs – 3D CTF, or charge trap flash technology and vertical interconnect technology.
In the conventional planar NAND flash memory chip structure that is composed of a floating gate, a control gate and a channel, bit data of 1s and 0s, the most basic element of digital signals, are stored in its floating gate – a conductor - when voltage is cut off from a channel, as the cut-off traps electrons in the floating gate.
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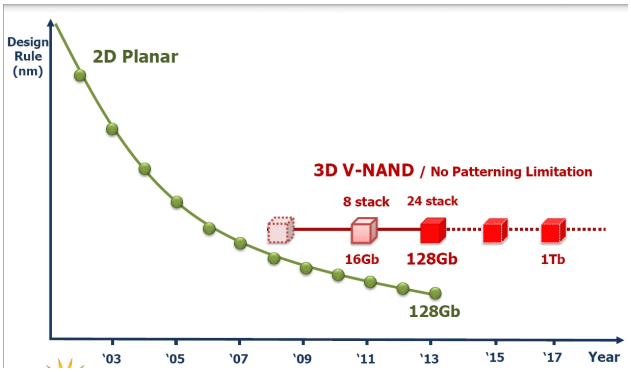
On the other hand, the CTF technology reorganizes the planar structure into a non-planar cylindrical structure, putting a channel gate at its core, then surrounding it with an insulator, and finally surrounding the insulator with a control gate. Electron, or electronic charges are stored on the insulator, which is made of silicon nitride film, not on a floating gate.
Then, Samsung stacked this single cylindrical layer of 3D CTF NAND flash cell on top of each other until it reaches 24 layers using special etching technology that connects the layers electronically by punching holes from the top to the bottom.

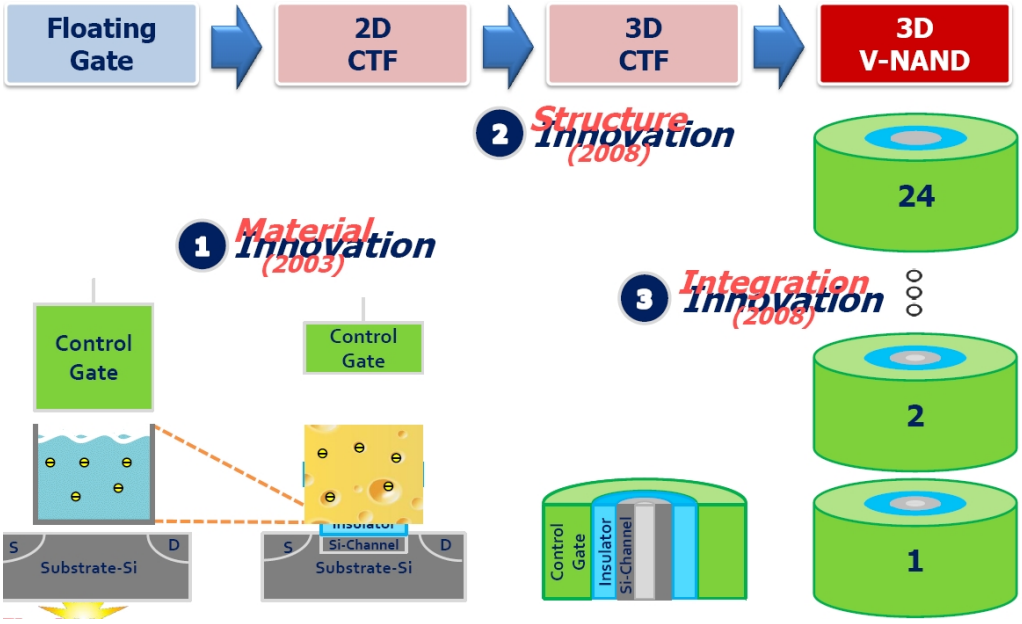


Xian, Chinese wafer- fab reday for mass rollouts

Taking advantage of the two technology breakthroughs, Samsung developed a 128Gb MLC 3D V-NAND flash memory chip that is built with 24 layers of cells using an older 30nm-class process, and has been mass-producing them starting from early August.

The technology benefits are huge. Even though the 128Gb 3D V-NAND chip is processed with a relatively old 30nm-class design rule, the 128 Gb device carries two times more density in the same physical space than the planar structure 64Gb NAND flash chips of 20-nm class geometry. It also boasts better endurance and reliability. For example, the 128Gb 3D V-NAND can withstand 35,000

program per erase cycle, almost 10 times more than 3,000 program per erase cycle of today's 20nm



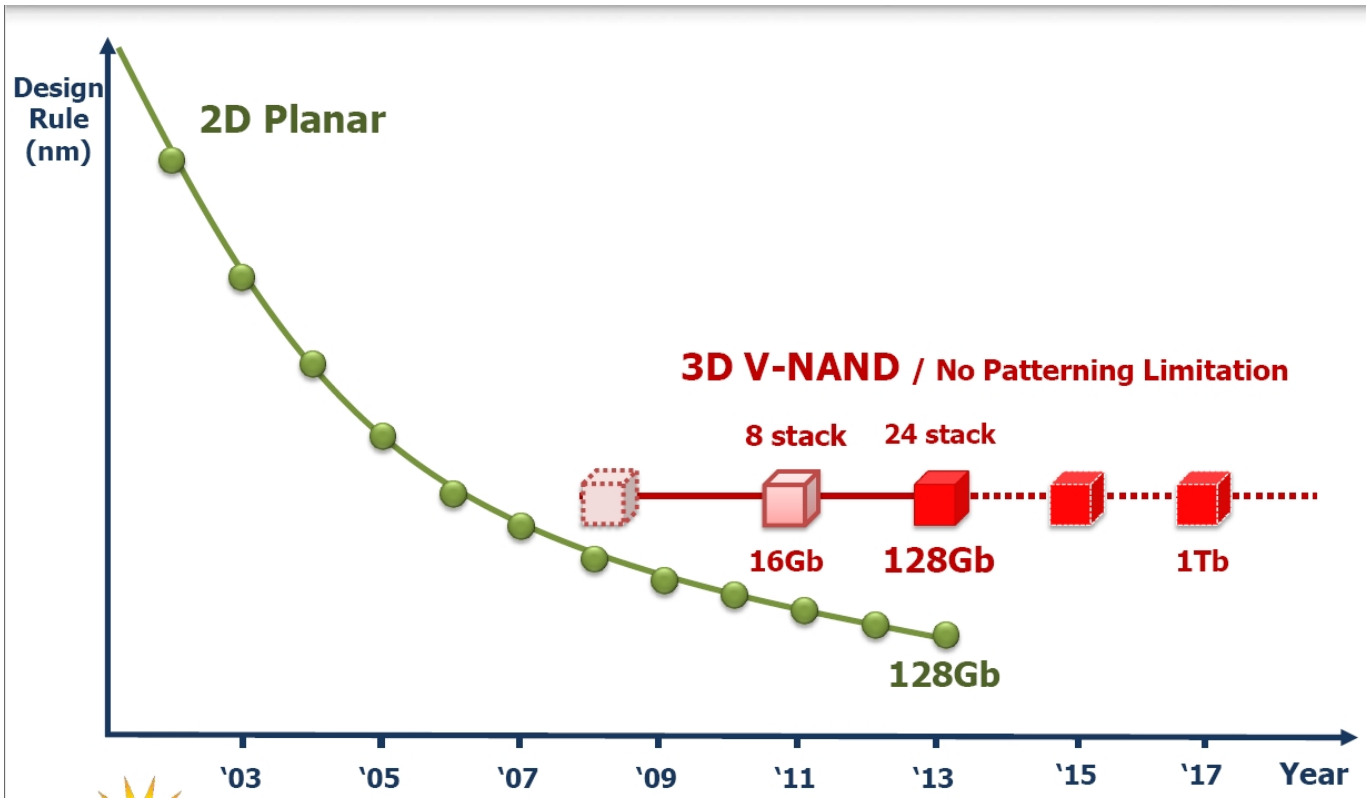
planar NAND flash chips.

The new 3D V-NAND demonstrates two times reliability at the minimum, and a maximum 10 times higher reliability, too, compared with a conventional 20nm-class floating gate NAND flash memory chip. But, it also boasts twice as fast write performance.

"The new 3D V-NAND flash technology is the result of our employees' years of efforts to push beyond conventional ways of thinking and pursue much more innovative approaches in overcoming limitations in the design of memory semiconductor technology," said Jeong-Hyuk Choi, senior vice president, flash product & technology, Samsung Electronics. "Following the world's first mass

production of 3D Vertical NAND, we will continue to introduce 3D V-NAND products with improved performance and higher density, which will contribute to further growth of the global memory industry."

Samsung also has built an enterprise SSD with the 3D V-NAND flash memory chips.
Meanwhile, rival Toshiba announced that it will start volume production of 3D NAND flash memory chips by mid-2014 when the 2nd phase construction projects of its Fab 5 in Yokkaichi facility in Mie, Japan is to be completed. Toshiba will use multilayered BiCS, or Bit-Cost Scalable manufacturing process for 3D NAND flash memory chips.
According to IHS iSuppli, the global NAND flash memory market is expected to growth at a CAGR of


Design Rule (nm)
2D Planar
3D V-NAND / No Patterning Limitation
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24 stack
16Gb
128Gb
1Tb
128Gb
'03
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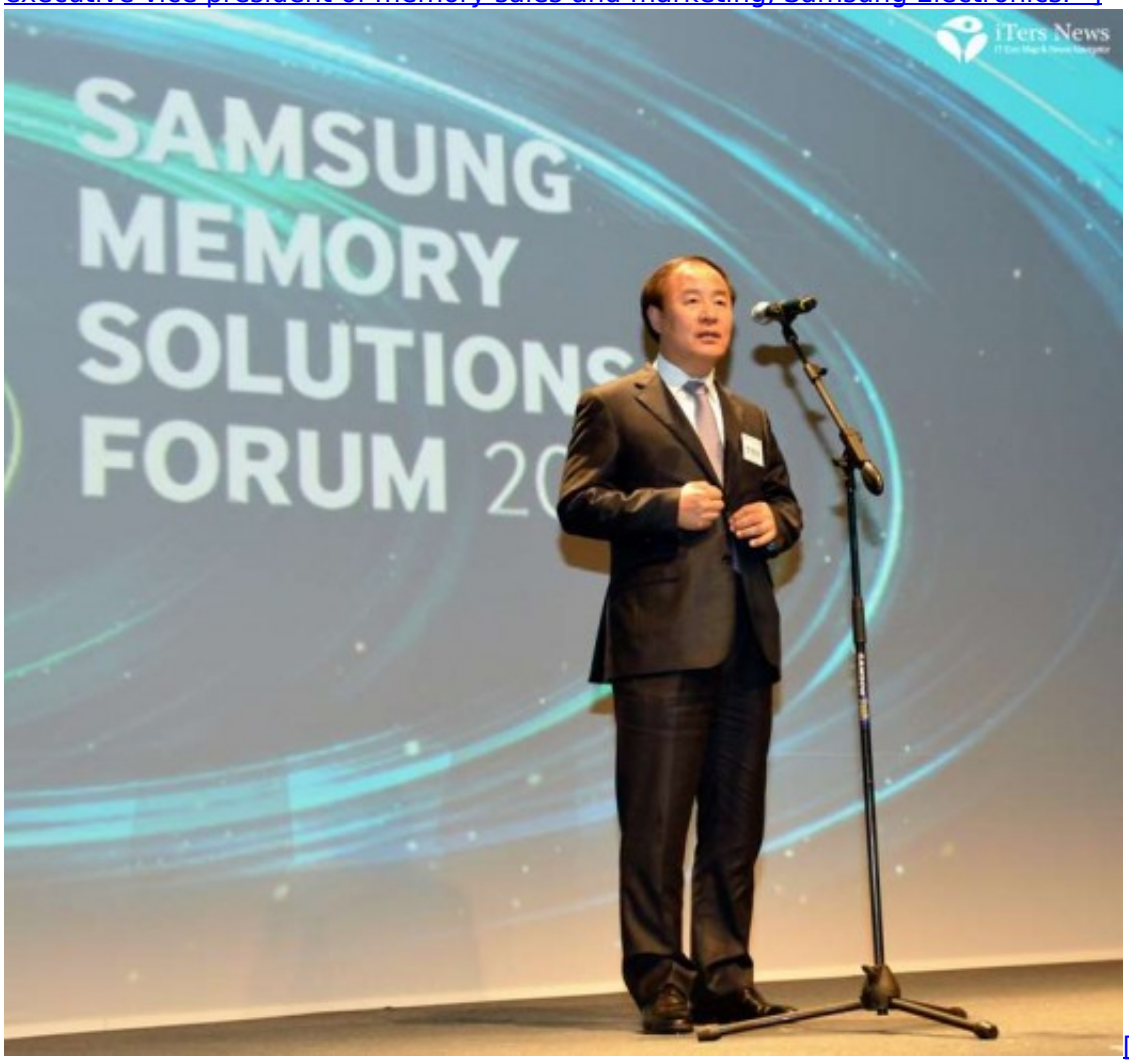
Samsung Electronics opens brave new world for data center server market with roll-out of 3D V-NAND chip

author:JH Bae October 17, 2013

(iTers News) - Samsung Electronics Co., Ltd. unveiled a fifth generation of green memory solutions that include 128gigabit DDR4 DRAM chips, PCIe SSD, and 3D V-NAND flash memory chips.

At the Memory Solution Forum 2013 held in Seoul yesterday, the world's largest memory chip maker demonstrated how these advanced memory chip solutions can combine to help dramatically improve data server computers' performances, while reducing power consumption and heat. .

[caption id="attachment_54262" align="alignnone" width="524" caption="Young-hyun Jun, executive vice president of memory sales and marketing, Samsung Electronics. "]



[/caption]Zeroing in on an enterprise data center server market, these 5th generation memory solutions were deigned to work with Intel's new generation 20nm Haswell CPU to power a next generation of data center server computer that are scheduled to roll off the line in 2014.

"Our new 5th generation memory solutions marks a technology breakaway from the past, shedding new lights on data center server market," said Young-hyun Jun, executive vice president of memory sales and marketing, Samsung Electronics.

3D V-NAND at the core

If the DDR4 and PCIe SSD green memory solutions are embedded together in a server computer, according to Samsung, the combination will dramatically improve the performance of server systems approximately 1.6 times and quadruple system capacity by eliminating unnecessary data duplication in the enterprise storage systems.

In addition, the green memory combo can help save power consumption by a factor of 45 terawatts per hour.

A close look at each of these solutions can help explain how they make it to the big gains in power budget and performance.

For one thing, the new generation of the 20nm-class 128Gb DDR4 DRAM chips boasts a far wider bandwidth of transferring 2,133 megabits of data per second between a CPU and memory system, breaking the industry's long-held ceiling of 1,866 Mbps data transfer speed.

[caption id="attachment_54296" align="alignnone" width="735" caption="Young-hyun Jun,

executive vice president of memory sales and marketing, Samsung Electronics. "]

[/caption]Built with a new breakthrough JEDEC standard Pseudo Open Drain, or POD technology, it also works on an ultralow operating voltage of 1.2 volts, a 23% cut in the operating current, compared with its predecessor DDR3 DRAM chip.

Its technology breakthrough does't stop there. It comes built a error-correction circuitry, which detect errors happened in the data transfer and correct them.

The 5th generation of the green PCIe SSD comes built with new technology innovations, too. At the core of the 2.5-inch 126Gb green PCIe SSD is Samsung's new breed of 3D V-NAND flash memory chip that vertically stacks layer over layer of channels, control gates and floating gates in an up to 24 layered 3D cylindrical form.

Compared with a 20nm-class conventional planar NAND flash memory chip, the 3D V-NAND flash memory chip boast a 2 times faster data write speed, consuming half the power, even if it fabricated with a 30nm-class technology. By stacking layers over layers of silicon gates in a 3D cylinder, the chip maker can pack more of memory cells into a given space that it does it with a conventional planar structure, laying the groundwork for breaking through current technological limits, as the industry faces toughest ever challenge in shrinking below a 20nm geometry.

Works with New generation Haswell

It boasts ten times durability, too, making far less vulnerable to deterioration in the reliability, which is caused by repeated operations of data read and write, compared with a planar-structured NAND flash memory chip.

The green PCIe SSD also comes with an advanced ultra-low power microcontroller and PCIe v.3.0 or Peripheral Component Interconnect Express version 3 interface technology. Today's SATA SSD uses a PCH buffer chip to interface with a CPU, often getting caught in a data transfer bottleneck, as tones of data contend for faster access to a CPU.

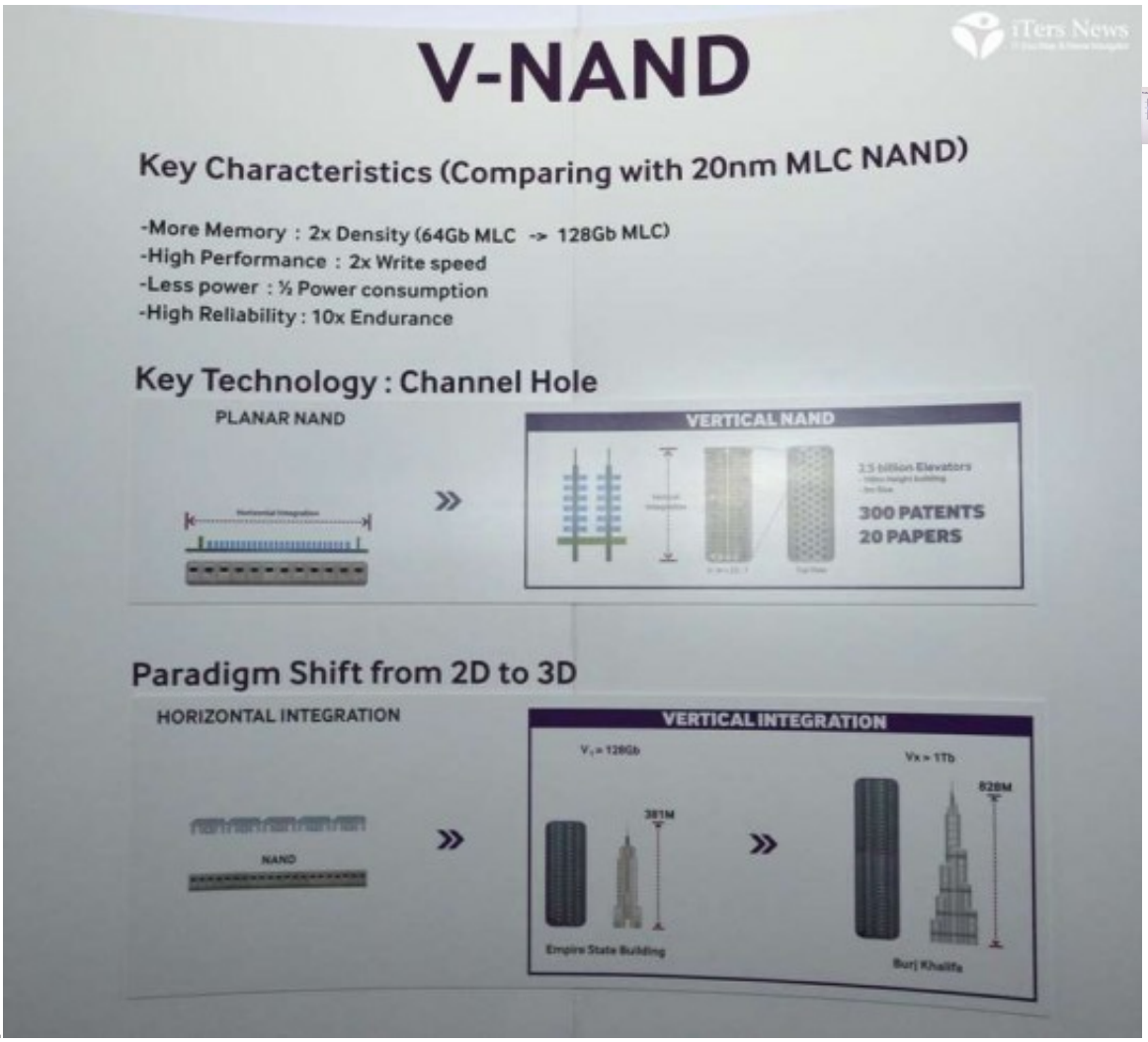
Using the PCIe interface technology, the green SSD comes to make a direct connection with a CPU, reducing data latency by 83%, It also boasts a 4GB/s data transfer bandwidth, a whopping 567% improvement over today's mainstream SATA technology of which data transfer bandwidth hit a wall of 600MB/s.

All combined, the PCIe SSD comes to improve energy efficiency by 145%.

The huge gains combined in the performance of the PCIe SSD and DDR4 DRAM chips translate into massive benefits for data center. Imagine you operate a data center that runs 10,000 server computers with a total investment cost of US$32 million for simultaneous access of up to 4,000 users. If you retool it with a new generation servers incorporating Samsung's PCIe SSD and DDR4 DRAM chips, you can recalibrate it with only 7,880 servers for the same investment costs, seeing big cuts in the power consumption from 2610 kilowatts to 2310 kilowatts. But, its performance would improve so dramatically that it can accommodate simultaneous access of up to 1,000 users.

The 2.5-ich PCIe SSD comes in three versions of 400GB, 800GB and 1,600GB, mainly targeting data center server computer markets.

Mass-production of the green memory solutions has already begun, including DDR4 DRAM chips and PCIe SSD. Samples of the solutions are also being shipped for 2014 rollout of server


V-NAND
Key Characteristics (Comparing with 20nm MLC NAND)
-More Memory : 2x Density (64Gb MLC -> 128Gb MLC)
-High Performance : 2x Write speed
-Less power : ½ Power consumption
-High Reliability : 10x Endurance
Key Technology : Channel Hole
PLANAR NAND
VERTICAL NAND
300 PATENTS
20 PAPERS
Paradigm Shift from 2D to 3D
HORIZONTAL INTEGRATION
NAND
VERTICAL INTEGRATION
381M
828M
Empire State Building
Burj Khalifa

systems.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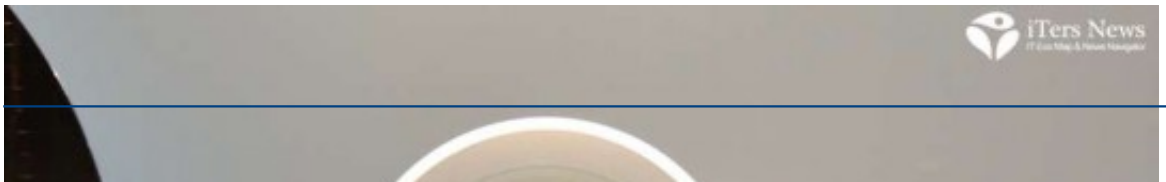
2. Internet access : Type below IP address into your mobile Internet browser
[Server : 192.168.0.2]
[Green Server : 192.168.0.4]


V-NAND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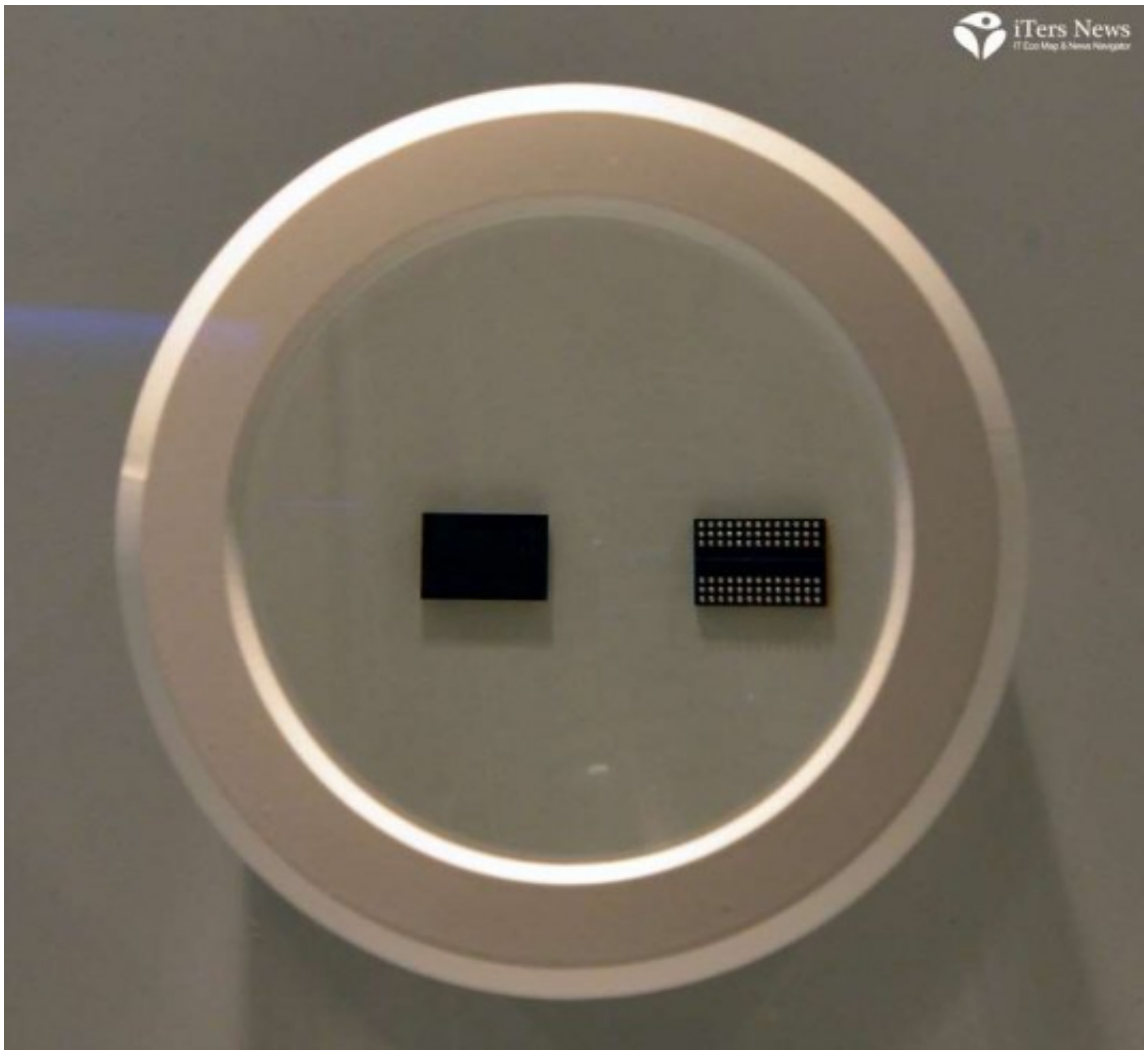
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[caption id="attachment_54303" align="alignnone" width="735" caption="Young-hyun Jun,

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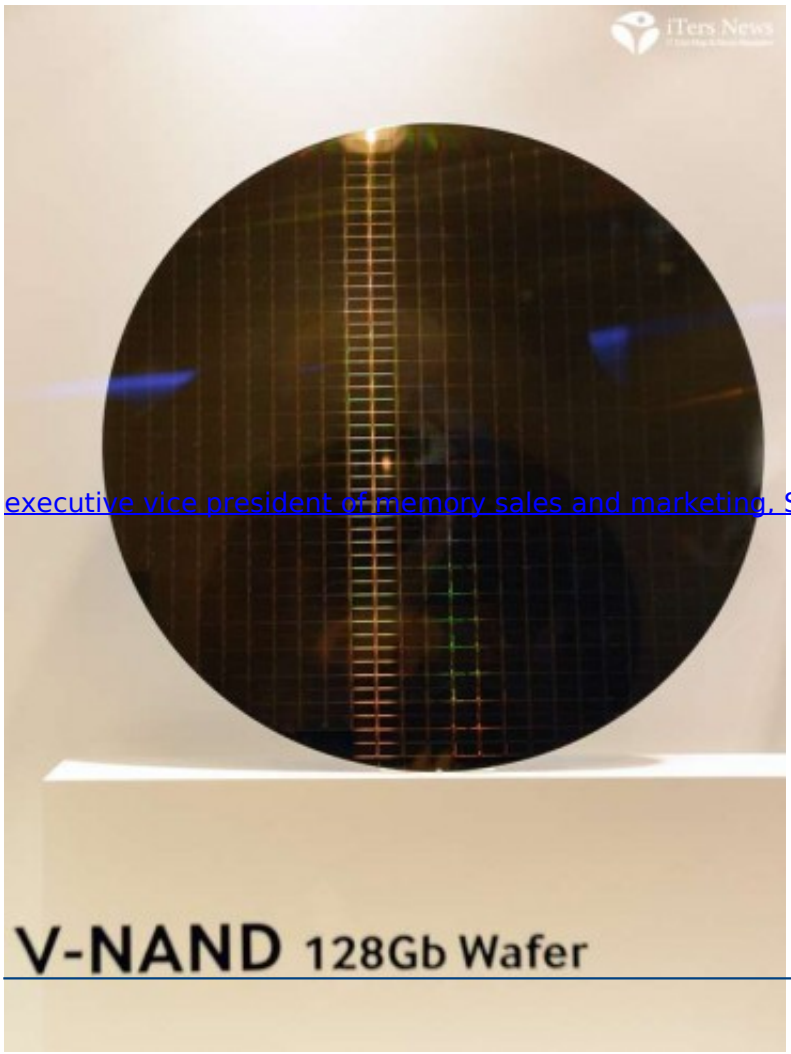


executive vice president of memory sales and marketing, Samsung Electronics. "]

Toshiba broke ground to construct 3D NAND chip-making facility in Yokkaichi

author:JH Bae August 23, 2013

(iTers News) - Toshiba Corporation today broke ground to begin construction of Phase 2 of Fab 5, the company's state-of-the-art fabrication facility at its Yokkaichi chip making cluster for memory chip in Mie Prefecture.

Toshiba will expand Fab 5 to secure manufacturing space for 3D, or 3 dimension NAND flash memories that will be fabricated with a next generation of 3D chip making process technology. Construction will be completed in summer next year. The 3D NAND flash memory chip is a new generation of NAND chips that vertically stack transistors in a 3 dimension to cram more of them in a given silicon space. As the 3D NAND flash memory chip technology is very instrumental in lowering down the price of SSDs, or solid state disk to the level that match those of HDDs, chip makers like Samsung Electronics, Toshiba, and Intel are locking they horns in a battle for 3D NAND flash memory chips markets.

Samsung led the race, as the world's largest memory chip maker started volume production of the 3D V-NAND flash memory chips in early August.

Three fabs at the Yokkaichi Operations are producing NAND flash memories, including Fab 5 phase 1. Fab 5's construction was planned around two phases, the first of which went into operation in July 2011. As demand for NAND flash memory chips are expected to pick up in the years to come, mainly driven by smartphones, tablets, SSD for enterprise servers, Toshiba set out to build the 2nd phase of its Fab. 5 facility.

Outline of Fab 5

Structure of building:	2-story steel frame concrete, five floors	
Ground area:	Approximately 38,000m 2	
Total floor area:	Approximately 187,000m 2	
Start of Construction:	First Phase:	July 2010
	Second Phase:	August 2013
Completion:	First Phase:	March 2011
	Second Phase:	Summer 2014 (target)
Start of Production:	First Phase:	July 2011
	Second Phase:	To be determined later; intended primarily for technology transition of existing wafer capacity

Samsung, Toshiba butt heads for leadership in next generation SSD market

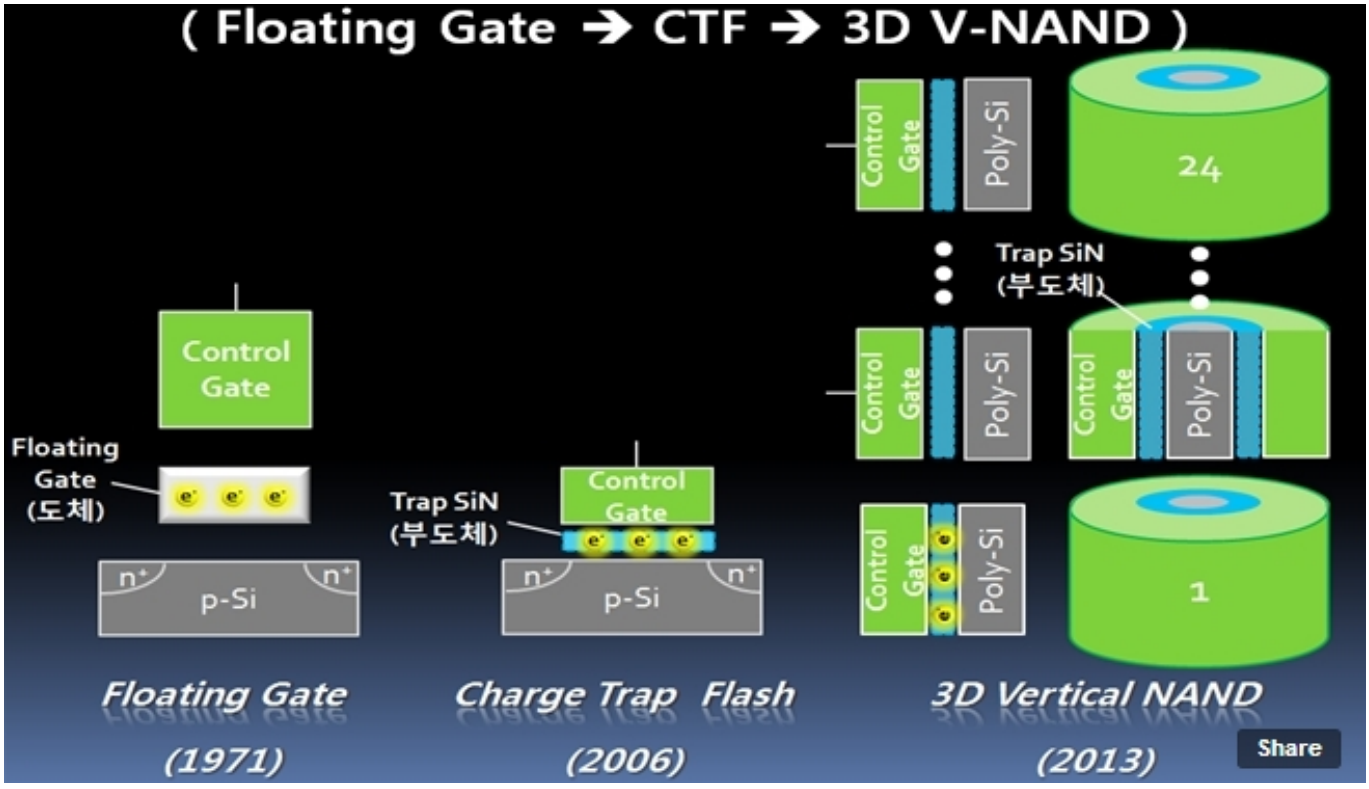
author:itersnews August 13, 2013

(iTers News) - Samsung Electronics and Toshiba Corp. are butting heads in the competition for a next generation of 3D Nand flash memory chips. The victory in the high-stakes game will give the winner a chance to seize control of fast-growing, multi-billion dollar SSD market.

A short of solid state drives, SSDs are a concentration of Nand flash memory chips seated together in a tiny printed circuit board. The silicon-based data storage technology is rapidly emerging as one of the most coveted market segments of global IT industry, as it is now threatening to replace decades-old HDD, or hard disk drive technology as a mainstream data storage technology for an array of computing system from server to desktop PCs to notebook and mobile PCs.

Compared with HDDs, SSDs consume less power, boasts far faster read and write time, and more importantly, can store more of data in a given space. Yet, it is still far costlier to produce, a big impediment against the rapid penetration of SSDs. The 3D, or 3 dimension Nand flash memory chip is rapidly emerging as a key technology-enabler to help cut costs of SDDs so steeply as to match those of HDDS, because it can store two times as much data as current planar structure transistor-based Nand flash memory chips.

Vertically stacked



(Source : Samsung Electronics)

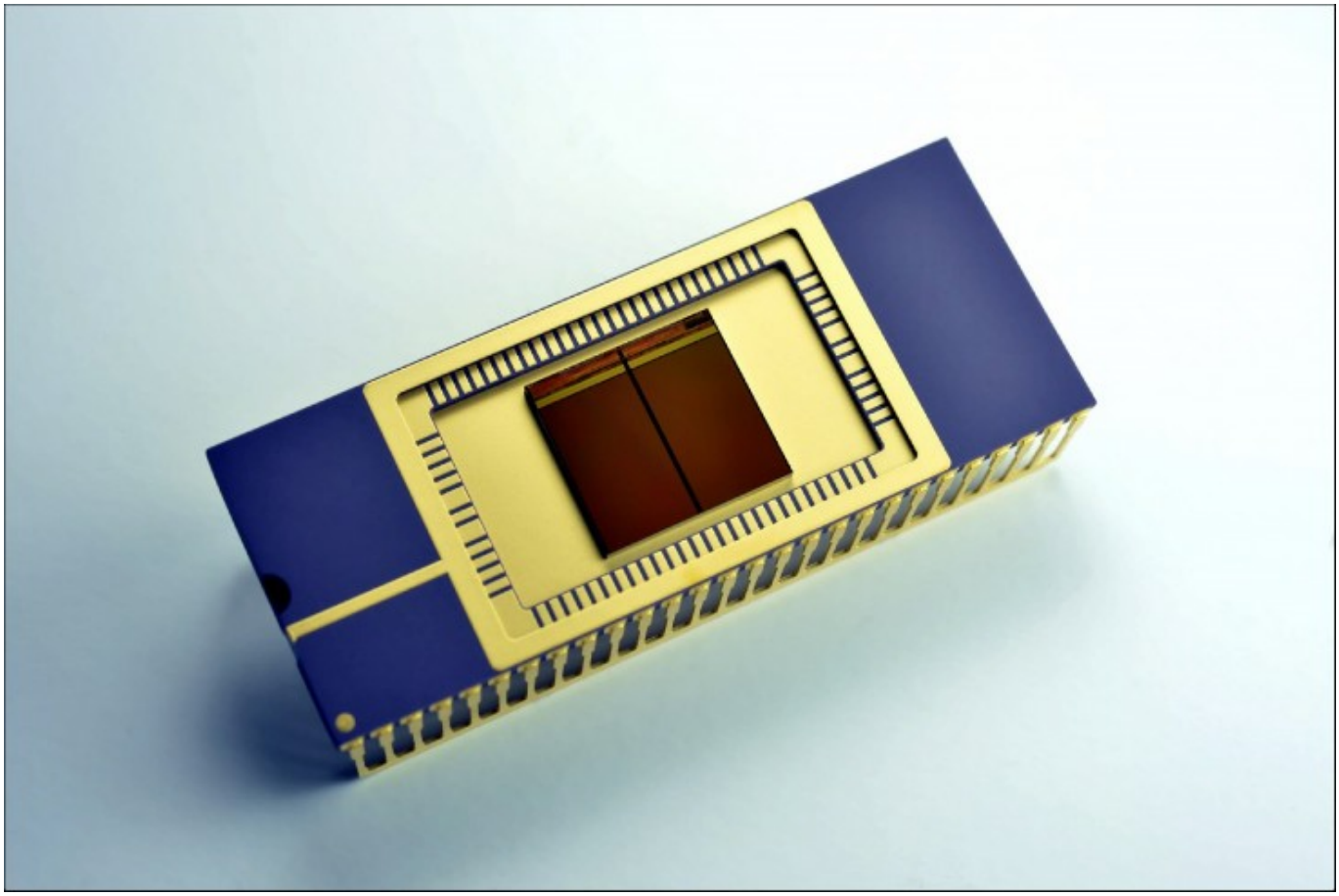
Samsung races one year ahead of Toshiba. The world's largest memory chip maker said on August 6 that it has started mass-production of 128 Gb 3D V, or vertical Nand flash memory chips in what the chip maker said is the world's first commercial roll-out.

Following Samsung's lead, Toshiba said on the same day that it will join hands with SanDisk of the U.S. to build a joint-venture 3D Nand fabrication line as the second phase of its Fab 5 at its Yokkaichi facility in Mie, Japan. The two companies will invest 200 billion yen each to build the 400 billion yen wafer fabrication line to produce 3D Nand flash memory chips. Mass production is scheduled to start in the middle of 2014.

The conventional planar structure Nand flash memory chip transistor usually consists of one control gate and one channel gate as well as a in-between floating gate. Once a voltage is applied to the control gate, electron –the most basic element of digital signal data- gets trapped in a floating gate to keep data. Conversely, electron are relieved to erase, or rewrite data if a voltage is applied the channel.

High-stakes bet

On the other hand, Samsung's 3D V-Nand flash chip transistor cell comes with a 24-layered cylindrical structure that vertically stacks 24 CFT, or charge trap flash cells. Each transistor consists of a control gate, a poly-silicon gate and an in-between insulating trap silicon nitride gate. Once a voltage is applied, the silicon nitride insulating layer traps electrons to store data. Samsung uses its indigenous vertical interconnect technology to vertically stack each cylindrical transistor. Electron moves up and down along the vertical hole to keep, or erase data.



The more transistors it stacks, the more storage capacity it can get. The technology difference translates into huge differences in performance –data read and write time as well as storage density

per space. According to Samsung, the 3D V Nand flash memory chips, which were fabricate with a 20nm class design rule , can store double the density of its planar structure conventional Nand flash chip technology of a 10nm circuit geometry. It also boasts two times as fast read and write time.

The huge gains in the performance open the way for Samsung to cut production costs of SSDs, as the technology innovation allows the chip maker to pack two times as much storage capacity unit production costs. For example, the 3D V-Nand technology enables Samsung to cram 1 terabyte, TB storage capacity in a single piece of the 3D V-Nand flash memory chip 3 Nand in less than 5 years, according to Samsung.

To build one TB SSD Samsung SSD 840 Pro, Samsung crammed together 16 128Gb planar structure Nand flash memory chips, for example. The 1 TB Samsung SSD Pro now sells for about US$670. As is the case, Samsung's 3D V-Nand flash memory chip technology will cut prices of the SSDs to cross over those of HDDs in the foreseeable future, promising to accelerate the replacement.

The 3D chip-making technology also enabled Samsung to break through the limits of the current geometry scaling down technology. True enough, the chip making industry is now confronting tough challenges in shrinking the Nand geometry technology below 10nm. That's because the narrower the transistor cells get together, the more they interfere with each other. Prohibitively expensive EUV, or extreme ultra violet photo lithography equipment is also a hurdle, because the EUV equipment is very instrumental in going down below 10nm technology. Samsung's commercial roll-out of the 3D V-Nand technology has paved way for doubling or tripling the storage capacity without moving beyond 10nm.

Break through the scaling limits

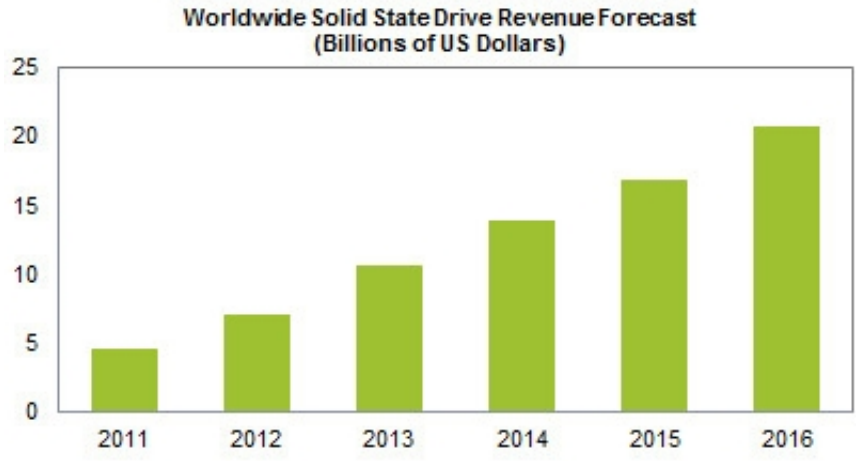
Once its chip-making facility in the city of Xian, China, Samsung also plans to churn out the 3D V-Nand flash memory chips there.

Toshiba Corp. has been working on the multi-layered 3D Nand flash memory chip technology using p-BiCS, or pipe-shaped Bit-Cost Scalable manufacturing process.

Unlike a 2D planar cell array, the 3D V NAND flash chip technology allows the chip maker to vertically stack 2D planar memory cells in a monolithic 3 dimensional structure.

Toshiba's first roll-out of 3D Nand flash memory chip prototype went back to late 2012 when the chip maker unveiled a 16 layer prototype device using a 50nm geometry technology. Samples will be due out sometime in 2013. Toshiba's p-BiCS technology arranges an array of Nand transistor cells in a U-shape.

According to IHS iSuppli, the global NAND flash memory market is expected to growth at a CAGR of 11 % from US$23.6 billion in 2013 to reach approximately US $30.8 billion by 2016. Yet, the prize is far bigger in the SSD market. Worldwide SSD shipments are set to rise to 83 million units this year, up from 39 million in 2012, according to market research firm iSuppli. Shipments are set to continue to rise 239 million units in 2016, about 40% of HDD market size. In terms of value, wolrdwide SSD market would hit US$ 17.2 billion in 2005



Source: IHS iSuppli Research, January 2013

Video & Photos by Bae

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