PRELIMINARY

PSoC® 6 MCU: PSoC 63 with BLE Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with ARM® Cortex™ CPUs (single and multi-core). The PSoC 63 product family, based on an ultra low-power 40-nm platform, is a combination of a dual-core microcontroller with low-power Flash technology and digital programmable logic, high-performance analog-to-digital and digital-to-analog conversion, low-power comparators, and standard communication and timing peripherals. The PSoC 63 family provides wireless connectivity with BLE 5.0 compliance.

Features

32-bit Dual Core CPU Subsystem

- 150-MHz ARM Cortex-M4F CPU with single-cycle multiply (Floating Point and Memory Protection Unit)
- 100-MHz Cortex M0+ CPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Inter-processor communication supported in hardware
- 8 KB 4-way set-associative Instruction Caches for the M4 and M0+ CPUs respectively
- Active CPU power consumption slope with 1.1-V core operation for the Cortex M4 is 40 µA/MHz and 20 µA/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Active CPU power consumption slope with 0.9-V core operation for the Cortex M4 is 26 µA/MHz and 17 µA/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Two DMA controllers with 16 channels each

Flash Memory Sub-system

- 1 MB Application Flash with 32-KB EEPROM area and 32-KB Secure Flash
- 128-bit wide Flash accesses reduce power
- Flash Read-While-Write (RWW) allows updating the Flash while executing from it
- SRAM with Selectable Retention Granularity
- 288-KB integrated SRAM
- 32-KB retention boundaries (can retain 32K to 288K in 32K increments)
- One-Time-Programmable (OTP) E-Fuse memory for validation and security

Bluetooth Low Energy (Bluetooth Smart) BT 4.2 Subsystem

- 2.4-GHz RF transceiver with 50-Ω antenna drive
- Digital PHY
- Link Layer engine supporting master and slave modes
- Programmable output power: up to 4 dBm
- RX sensitivity: –95 dBm
- RSSI: 1-dB resolution
- 4.2 mA TX (0 dBm) and 4.4 mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
- Link Layer engine supports four connections simultaneously
- Supports 2 Mbps LE data rate

Low-Power 1.7-V to 3.6-V Operation

- Active, Low-power Active, Sleep, Low-power Sleep, Deep Sleep, and Hibernate modes for fine-grained power management
- Deep Sleep mode current with 64K SRAM retention is 7 µA with 3.3-V external supply and internal buck
- On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-Time-Clock

Flexible Clocking Options

- On-chip crystal oscillators (High-speed, 4 to 33 MHz, and Watch crystal, 32 kHz)
- Phase Locked Loop (PLL) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with ±1% accuracy
- Ultra low-power 32 kHz Internal Low-speed Oscillator (ILO) with ±10% accuracy
- IMO can be locked to 32 kHz WCO input for better accuracy
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Serial Communication

- Nine independent run-time reconfigurable serial communication blocks (SCBs), each is software configurable as I^2C, SPI, or UART

Timing and Pulse-Width Modulation

- Thirty-two 16-bit Timer/Counter Pulse-Width Modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Up to 78 Programmable GPIOs

- Drive modes, strengths, and slew rates are programmable
- Six overvoltage tolerant (OVT) pins

Packages

- 116-BGA and 104-MCSP packages with PSoC 6 and BLE Radio

Errata: For information on silicon errata, see "Errata" on page 57. Details include trigger conditions, devices affected, and proposed workaround.

Audio Subsystem
- I2S Interface; up to 192 kilosamples (ksps) Word Clock
- Two PDM channels for stereo digital microphones

QSPI Interface
- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4 KB QSPI cache for greater XIP performance with lower power
- Supports 1, 2, 4, and Dual-Quad interfaces

Programmable Analog
- 12-bit 1 Msps SAR ADC with differential and single-ended modes and 16-Channel Sequencer with signal averaging
- One 12-bit voltage mode DAC with < 5-µs settling time
- Two opamps with low-power operation modes
- Two low-power comparators that operate in Deep Sleep and Hibernate modes.
- Built-in temp sensor connected to ADC

Programmable Digital
- 12 programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs to implement functions such as Communication peripherals (for example, LIN, UART, SPI, I^2C, S/PDIF and other protocols), Waveform Generators, Pseudo-Random Sequence (PRS) generation, and many other functions.
- Smart I/O (Programmable I/O) blocks enable Boolean operations on signals coming from, and going to, GPIO pins
- Two ports with Smart_IO blocks, capability are provided; these are available during Deep Sleep

Capacitive Sensing
- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Mutual Capacitance sensing (Cypress CSX) with dynamic usage of both Self and Mutual sensing
- Wake on Touch with very low current
- Cypress-supplied software component makes capacitive sensing design fast and easy
- Automatic hardware tuning (SmartSense™)

Energy Profiler
- Block that provides history of time spent in different power modes
- Allows software energy profiling to observe and optimize energy consumption

PSoC Creator Design Environment
- Integrated Development Environment provides schematic design entry and build (with analog and digital automatic routing) and code development and debugging
- Applications Programming Interface (API Component) for all fixed-function and programmable peripherals
- Bluetooth Smart Component (BLE4.2 compliant protocol stack) with Application level function calls and Profiles

Industry-Standard Tool Compatibility
- After schematic entry, development can be done with ARM-based industry-standard development tools
- Configure in PSoC Creator and export to ARM/Keil or IAR IDEs for code development and debugging
- Supports industry standard ARM Trace Emulation Trace Module

Security Built into Platform Architecture
- Multi-faceted secure architecture based on ROM-based root of trust
- Secure Boot uninterruptible until system protection attributes are established
- Authentication during boot using hardware hashing
- Step-wise authentication of execution images
- Secure execution of code in execute-only mode for protected routines
- All Debug and Test ingress paths can be disabled

Cryptography Accelerators
- Hardware acceleration for Symmetric and Asymmetric cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
- True Random Number Generator (TRNG) function

Contents

Blocks and Functionality

The PSoC 63 block diagram is shown in Figure 1. There are five major subsystems: CPU subsystem, BLE subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 1. Block Diagram

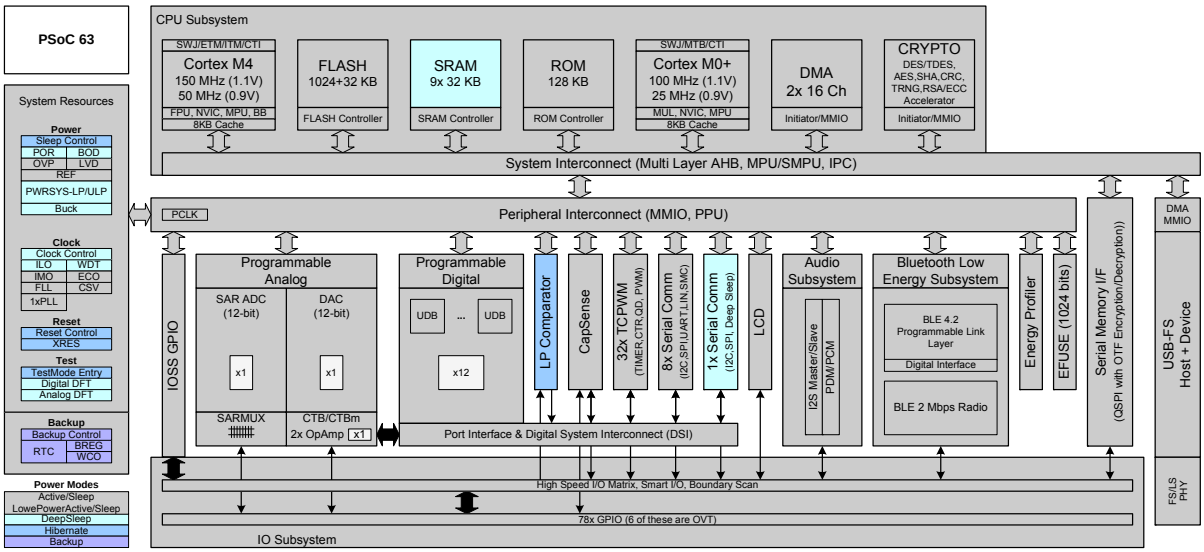


Figure 1 shows the subsystems of the chip and gives a very simplified view of their inter-connections (Multi-layer AHB is used in practice). The color-coding shows the lowest power mode where the particular block is still functional (for example, LP Comparator is functional in Deep Sleep mode).

PSoC 63 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 63 devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 63 family provides a very high level of security.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is a trade-off the customer can make.

Functional Definition

CPU and Memory Subsystem

CPU

The CPU subsystem in the PSoC 63 consists of two ARM Cortex cores and their associated busses and memories: M4 with Floating-point unit and Memory Protection Units (FPU and MPU) and an M0+ with an MPU. The Cortex M4 and M0+ have 8-KB Instruction Caches (I-Cache) with 4-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a Cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM. The Cortex M0+ provides a secure, un-interruptible Boot function. This guarantees that post-Boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal ARM multi-layer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex M4 is 26 µA/MHz and 17 µA/MHz for the Cortex M0+, both at 3.3 V chip supply voltage with the internal buck enabled and at 0.9 V internal supply.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus.

Flash

PSoC 63 has a 1-MB flash module with additional 32K of Flash that can be used for EEPROM emulation for longer retention and a separate 32-KB block of Flash that can be securely locked and is only accessible via a key lock that cannot be changed (One Time Programmable). The Flash block supports Read-While-Write (RWW) operation so that Flash updates may be performed while the CPU is active.

SRAM with 32-KB Retention Granularity

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32-KB blocks.

SROM

There is a supervisory 128-KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of User Flash is required.

One-Time-Programmable (OTP) eFuse

The 1024-bit OTP memory can provide a unique and unalterable Identifier on a per-chip basis. This unalterable key can be used to access Secured Flash.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) when the power supply drops below specified levels. The design will guaranteed safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the Reset occurring. There are no voltage sequencing requirements. The VDD core logic supply (1.7 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of <1 µA. A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the VBACKUP domain and includes the 32-kHz WCO, RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to the resistive pull-up mode by default.

Clock System

The PSoC 63 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 63 consists of the Internal Main Oscillator (IMO) and the Internal Low-speed Oscillator (ILO), crystal oscillators (ECO and WCO), PLL, FLL, and provision for an external clock. The PLL will support spread-spectrum operation. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50 µs). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver ±20-ppm accuracy and will use an external crystal.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 63. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is ±1% and its current consumption is less than 10 µA. The IMO may be locked to a more accurate clock source to obtain higher accuracy. Locking to a 32-kHz WCO can deliver 0.25% accuracy.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. The clock dividers are 16 and 24 bits in length to allow very fine clock control.

Reset

The PSoC 63 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

BLE Radio and Subsystem

PSoC 63 incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
  - Broadcaster, Observer, Peripheral, and Central roles
  - Security mode 1: Level 1, 2, and 3
  - User-defined advertising data
  - Multiple bond support
- GATT features
  - GATT client and server
  - Supports GATT sub-procedures
  - 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)
- Security Manager (SM)
  - Pairing methods: Just works, Passkey Entry, and Out of Band
  - LE Secure Connection Pairing model
  - Authenticated man-in-the-middle (MITM) protection and data signing
- Link Layer (LL)
  - Master and Slave roles
  - 128-bit AES engine
  - Low-duty cycle advertising
  - LE Ping
- Supports all SIG-adopted BLE profiles
- Power levels for Adv (1.28s, 31 bytes, 0 dBm) and Con (300 ms, 0 byte, 0 dBm) are 21 µW and 33 µW respectively

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 3.6 V.

Temperature Sensor

PSoC 63 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

12-bit Digital-Analog Converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

Continuous Time Block (CTBm) with Two Opamps

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

Low-Power Comparators

PSoC 63 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Smart I/O

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate.This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wake-ups.

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC6 A-BLE has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of 32 counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and 24 16-bit counters.

Serial Communication Blocks (SCB)

PSoC 63 has nine SCBs, which can each implement an I^2C, UART, or SPI interface. One SCB will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports an 8-deep FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface will operate with a 48-MHz SPI Clock.

USB Full-Speed Dual Role Host and Device Interface

The PSoC6A-BLE-2 incorporates a dual-role USB Host and Device interface. The device can have up to eight endpoints. A 512-byte SRAM buffer is provided and DMA is supported.

QSPI Interface

A Quad SPI (QSPI) interface (selectable 1, 2, or 4 bits width) is provided running at 80 MHz. This block also supports on-the-fly encryption and decryption to support Execute-In-Place operation at reasonable speeds.

GPIO

PSoC 63 has up to 104 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Six GPIO pins are capable of overvoltage tolerant (OVT) operation where the input voltage may be higher than VDD (these may be used for I^2C functionality to allow powering the chip off while maintaining physical connection to an operating I^2C bus without affecting its functionality).

GPIO pins can be ganged to sink 16 mA or higher values of sink current. GPIO pins may not be pulled up higher than 3.6 V.

Special-Function Peripherals

CapSense

CapSense is supported on all pins in the PSoC 63 through a CapSense Sigma-Delta (CSD) block that can be connected to an analog multiplexed bus. Any GPIO pin can be connected to this AMUX bus through an analog switch. CapSense function can thus be provided on any pin or a group of pins in a system under software control. Cypress provides a software component for the CapSense block for ease-of-use.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

The CapSense block has two 7-bit IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). A (slow) 10-bit Slope ADC may be realized by using one of the IDACs.

The block can implement Swipe, Tap, Wake-up on Touch (< 3 µA at 1.8 V), mutual capacitance, and other types of sensing functions.

Audio Subsystem

This subsystem consists of an I2S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output. The PDM processing channel provides droop correction and can operate with clock speeds ranging from 384 kHz to 3.072 MHz and produce word lengths of 16 to 24 bits at audio sample rates of up to 48 ksps.

The I2S interface supports both Master and Slave modes with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

Pinouts

Table 1. Pinouts for 116-BGA and 104-MCSP Packages

104-MCSP-BLE		116-BGA-BLE	
Pin	Name	Pin	Name
C7	VCCD	A2	VCCD
C6	VDDD	B1	VDDD
C9	VBACKUP	C1	VBACKUP
D8	P0.0	C2	P0.0
E6	P0.1	D3	P0.1
D9	P0.2	E4	P0.2
E7	P0.3	E3	P0.3
E8	P0.4	F3	P0.4
E9	P0.5	D2	P0.5
E5	XRES	E2	XRES
F5	P1.0	G3	P1.0
F6	P1.1	F2	P1.1
		J5	P1.2
F9	P1.3	J4	P1.3
F8	P1.4	J3	P1.4
F7	P1.5	J2	P1.5
G9	VDD_NS	H3	VDD_NS
G8	VIND1	F1	VIND1
H8	VIND2	G1	VIND2
J8	VBUCK1	G2	VBUCK1
H9	VRF	H1	VRF
L9	VDDR1	L2	VDDR1
N9	VSSR	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
M9	ANT	K1	ANT
M9	ANT	K1	ANT
K2	P6.1	J8	P6.1
M2	P6.2	L9	P6.2
L1	P6.3	K9	P6.3
J2	P6.4	J9	P6.4
K1	P6.5	M10	P6.5
N2	P6.6	L10	P6.6
M1	P6.7	K10	P6.7
N1	P7.0	J10	P7.0
G6	P7.1	H10	P7.1
H4	P7.2	H8	P7.2

104-MCSP-BLE		116-BGA-BLE	
Pin	Name	Pin	Name
N9	VSSR	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
P9	VDDR2	M1	VDDR2
P6,P7	VSSR	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
P8	VDDR3	M2	VDDR3
P1	VSS	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
M5	XI	M4	XI
P5	XO	M5	XO
M3	VSSR	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
M4	DVDD	M6	DVDD
P1	VSS	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
P4	VDCDC	M7	VDCDC
P2	NC		
P3	VSSR	J1,K2,K3,K4,K5,L1,L3,L4,L5,M3,M8	VSSR
L2	VDDR_HVL	L7	VDDR_HVL
J7	P5.0	L6	P5.0
J5	P5.1	K6	P5.1
J6	P5.2	J6	P5.2
H7	P5.3	K7	P5.3
H6	P5.4	J7	P5.4
J4	P5.5	L8	P5.5
K3	P5.6	M9	P5.6
K4	P5.7		
L2	VDDR_HVL	L7	VDDR_HVL
L2	VDDR_HVL	L7	VDDR_HVL
J3	P6.0	K8	P6.0
B2	P10.1	A8	P10.1
C3	P10.2	F6	P10.2
E4	P10.3	E6	P10.3
A2	P10.4	D6	P10.4
A3	P10.5	B7	P10.5
D5	P10.6	A7	P10.6
B3	P10.7		
C4	P11.0	F5	P11.0
C5	P11.1	E5	P11.1
D6	P11.2	D5	P11.2

Table 1. Pinouts for 116-BGA and 104-MCSP Packages *(continued)*

104-MCSP-BLE		116-BGA-BLE	
Pin	**Name**	**Pin**	**Name**
G5	P7.3	H7	P7.3
H3	P7.4	H6	P7.4
H2	P7.5	G9	P7.5
G3	P7.6	G8	P7.6
G2	P7.7	G7	P7.7
D1	VDDIO1	G10	VDDIO1
G4	P8.0	F10	P8.0
G1	P8.1	F9	P8.1
F3	P8.2	F8	P8.2
F2	P8.3	F7	P8.3
F1	P8.4	G6	P8.4
E3	P8.5	E9	P8.5
E1	P8.6	E8	P8.6
E2	P8.7	E7	P8.7
A1	VDDA	A9	VDDA
D2	P9.0	D10	P9.0
C1	P9.1	D9	P9.1
D3	P9.2	D8	P9.2
B1	P9.3	D7	P9.3
		C10	P9.4
		C9	P9.5
		C8	P9.6
		C7	P9.7
		B10	VREF
A1	VDDA	A9	VDDA
A1	VDDA	A9	VDDA
C2	P10.0	B8	P10.0
B4	P11.3	C6	P11.3
A4	P11.4	B6	P11.4
B5	P11.5	A6	P11.5
A5	P11.6	B5	P11.6
A6	P11.7	A5	P11.7
B6	VDDIO0	B3	VDDIO0
D7,D4,F4,G7	VSS	B2,B9,H2,H9, D1	VSS
B7	P12.0	A4	P12.0
A7	P12.1	B4	P12.1
B8	P12.2	C4	P12.2
A8	P12.3	A3	P12.3
C8	P12.4	C5	P12.4
		D4	P12.5
		G5	P12.6
		H5	P12.7
A9	P13.0	H4	P13.0
B9	P13.1	G4	P13.1
		F4	P13.6
		C3	P13.7

The correspondence of power supplies to ports by package type is as follows:

- P0: VBACKUP
- P1: VDDD. Port 1 Pins are Over-Voltage Tolerant (OVT).
- P5, P6, P7, P8: VDDIO1
- P9, P10: VDDA
- P11, P12, P13: VDDIO0

Each Port Pin has multiple alternate functions. These are defined in Table 2.

Table 2. Multiple Alternate Functions

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0		srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0						scb[0].spi_select2:0			peri.tr_io_input[1]:0					cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0				scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0				scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0				scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0		srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2					
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0				scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0						
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0				scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0						
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1				scb[7].uart_rts:0		scb[7].spi_clk:0									
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1				scb[7].uart_cts:0		scb[7].spi_select0:0									
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1						scb[7].spi_select1:0									
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1						scb[7].spi_select2:0									
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0				scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss.clk_i2s_if	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0				scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss.tx_sck	peri.tr_io_input[11]:0						
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0				scb[5].uart_rts:0		scb[5].spi_clk:0		audioss.tx_ws							
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0				scb[5].uart_cts:0		scb[5].spi_select0:0		audioss.tx_sdo							
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0						scb[5].spi_select1:0		audioss.rx_sck							
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0						scb[5].spi_select2:0		audioss.rx_ws							

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P5.6	tcpwm[0].line[7]:0	tcpwm[1].line[7]:0						scb[5].spi_select3:0		audioss.rx_sdi							
P5.7	tcpwm[0].line_compl[7]:0	tcpwm[1].line_compl[7]:0						scb[3].spi_select3:0									
P6.0	tcpwm[0].line[0]:1	tcpwm[1].line[8]:0	scb[8].i2c_scl:0			scb[3].uart_rx:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0				cpuss.fault_out[0]					scb[8].spi_mosi:0
P6.1	tcpwm[0].line_compl[0]:1	tcpwm[1].line_compl[8]:0	scb[8].i2c_sda:0			scb[3].uart_tx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0				cpuss.fault_out[1]					scb[8].spi_miso:0
P6.2	tcpwm[0].line[1]:1	tcpwm[1].line[9]:0				scb[3].uart_rts:0		scb[3].spi_clk:0									scb[8].spi_clk:0
P6.3	tcpwm[0].line_compl[1]:1	tcpwm[1].line_compl[9]:0				scb[3].uart_cts:0		scb[3].spi_select0:0									scb[8].spi_select0:0
P6.4	tcpwm[0].line[2]:1	tcpwm[1].line[10]:0	scb[8].i2c_scl:1			scb[6].uart_rx:2	scb[6].i2c_scl:2	scb[6].spi_mosi:2			peri.tr_io_input[12]:0	peri.tr_io_output[0]:1				cpuss.swj_swo_tdo	scb[8].spi_mosi:1
P6.5	tcpwm[0].line_compl[2]:1	tcpwm[1].line_compl[10]:0	scb[8].i2c_sda:1			scb[6].uart_tx:2	scb[6].i2c_sda:2	scb[6].spi_miso:2			peri.tr_io_input[13]:0	peri.tr_io_output[1]:1				cpuss.swj_swdoe_tdi	scb[8].spi_miso:1
P6.6	tcpwm[0].line[3]:1	tcpwm[1].line[11]:0				scb[6].uart_rts:2		scb[6].spi_clk:2								cpuss.swj_swdio_tms	scb[8].spi_clk:1
P6.7	tcpwm[0].line_compl[3]:1	tcpwm[1].line_compl[11]:0				scb[6].uart_cts:2		scb[6].spi_select0:2								cpuss.swj_swclk_tclk	scb[8].spi_select0:1
P7.0	tcpwm[0].line[4]:1	tcpwm[1].line[12]:0				scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[14]:0		cpuss.trace_clock				
P7.1	tcpwm[0].line_compl[4]:1	tcpwm[1].line_compl[12]:0				scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[15]:0						
P7.2	tcpwm[0].line[5]:1	tcpwm[1].line[13]:0				scb[4].uart_rts:1		scb[4].spi_clk:1									
P7.3	tcpwm[0].line_compl[5]:1	tcpwm[1].line_compl[13]:0				scb[4].uart_cts:1		scb[4].spi_select0:1									
P7.4	tcpwm[0].line[6]:1	tcpwm[1].line[14]:0						scb[4].spi_select1:1					bless.ext_lna_rx_ctl_out	cpuss.trace_data[3]:2			
P7.5	tcpwm[0].line_compl[6]:1	tcpwm[1].line_compl[14]:0						scb[4].spi_select2:1					bless.ext_pa_tx_ctl_out	cpuss.trace_data[2]:2			
P7.6	tcpwm[0].line[7]:1	tcpwm[1].line[15]:0						scb[4].spi_select3:1					bless.ext_pa_lna_chip_en_out	cpuss.trace_data[1]:2			
P7.7	tcpwm[0].line_compl[7]:1	tcpwm[1].line_compl[15]:0						scb[3].spi_select1:0	cpuss.clk_fm_pump					cpuss.trace_data[0]:2			

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P8.0	tcpwm[0].line[0]:2	tcpwm[1].line[16]:0				scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0						
P8.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[16]:0				scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0						
P8.2	tcpwm[0].line[1]:2	tcpwm[1].line[17]:0				scb[4].uart_rts:0		scb[4].spi_clk:0									
P8.3	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[17]:0				scb[4].uart_cts:0		scb[4].spi_select0:0									
P8.4	tcpwm[0].line[2]:2	tcpwm[1].line[18]:0						scb[4].spi_select1:0									
P8.5	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[18]:0						scb[4].spi_select2:0									
P8.6	tcpwm[0].line[3]:2	tcpwm[1].line[19]:0						scb[4].spi_select3:0									
P8.7	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[19]:0						scb[3].spi_select2:0									
P9.0	tcpwm[0].line[4]:2	tcpwm[1].line[20]:0				scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:0			
P9.1	tcpwm[0].line_compl[4]:2	tcpwm[1].line_compl[20]:0				scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:0			
P9.2	tcpwm[0].line[5]:2	tcpwm[1].line[21]:0				scb[2].uart_rts:0		scb[2].spi_clk:0		pass.dsi_ctb_cmp0:1				cpuss.trace_data[1]:0			
P9.3	tcpwm[0].line_compl[5]:2	tcpwm[1].line_compl[21]:0				scb[2].uart_cts:0		scb[2].spi_select0:0		pass.dsi_ctb_cmp1:1				cpuss.trace_data[0]:0			
P9.4	tcpwm[0].line[7]:5	tcpwm[1].line[0]:2						scb[2].spi_select1:0									
P9.5	tcpwm[0].line_compl[7]:5	tcpwm[1].line_compl[0]:2						scb[2].spi_select2:0									
P9.6	tcpwm[0].line[0]:6	tcpwm[1].line[1]:2						scb[2].spi_select3:0									
P9.7	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[1]:2															
P10.0	tcpwm[0].line[6]:2	tcpwm[1].line[22]:0				scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1			
P10.1	tcpwm[0].line_compl[6]:2	tcpwm[1].line_compl[22]:0				scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1			

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P10.2	tcpwm[0].line[7]:2	tcpwm[1].line[23]:0				scb[1].uart_rts:1		scb[1].spi_clk:1						cpuss.trace_data[1]:1			
P10.3	tcpwm[0].line_compl[7]:2	tcpwm[1].line_compl[23]:0				scb[1].uart_cts:1		scb[1].spi_select0:1						cpuss.trace_data[0]:1			
P10.4	tcpwm[0].line[0]:3	tcpwm[1].line[0]:1						scb[1].spi_select1:1	audioss.pdm_clk								
P10.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[0]:1						scb[1].spi_select2:1	audioss.pdm_data								
P10.6	tcpwm[0].line[1]:6	tcpwm[1].line[2]:2						scb[1].spi_select3:1									
P10.7	tcpwm[0].line_compl[1]:6	tcpwm[1].line_compl[2]:2															
P11.0	tcpwm[0].line[1]:3	tcpwm[1].line[1]:1			smif.spi_select2	scb[5].uart_rx:1	scb[5].i2c_scl:1	scb[5].spi_mosi:1			peri.tr_io_input[22]:0						
P11.1	tcpwm[0].line_compl[1]:3	tcpwm[1].line_compl[1]:1			smif.spi_select1	scb[5].uart_tx:1	scb[5].i2c_sda:1	scb[5].spi_miso:1			peri.tr_io_input[23]:0						
P11.2	tcpwm[0].line[2]:3	tcpwm[1].line[2]:1			smif.spi_select0	scb[5].uart_rts:1		scb[5].spi_clk:1									
P11.3	tcpwm[0].line_compl[2]:3	tcpwm[1].line_compl[2]:1			smif.spi_data3	scb[5].uart_cts:1		scb[5].spi_select0:1				peri.tr_io_output[0]:0					
P11.4	tcpwm[0].line[3]:3	tcpwm[1].line[3]:1			smif.spi_data2			scb[5].spi_select1:1				peri.tr_io_output[1]:0					
P11.5	tcpwm[0].line_compl[3]:3	tcpwm[1].line_compl[3]:1			smif.spi_data1			scb[5].spi_select2:1									
P11.6					smif.spi_data0			scb[5].spi_select3:1									
P11.7					smif.spi_clk												
P12.0	tcpwm[0].line[4]:3	tcpwm[1].line[4]:1			smif.spi_data4	scb[6].uart_rx:0	scb[6].i2c_scl:0	scb[6].spi_mosi:0			peri.tr_io_input[24]:0						
P12.1	tcpwm[0].line_compl[4]:3	tcpwm[1].line_compl[4]:1			smif.spi_data5	scb[6].uart_tx:0	scb[6].i2c_sda:0	scb[6].spi_miso:0			peri.tr_io_input[25]:0						
P12.2	tcpwm[0].line[5]:3	tcpwm[1].line[5]:1			smif.spi_data6	scb[6].uart_rts:0		scb[6].spi_clk:0									
P12.3	tcpwm[0].line_compl[5]:3	tcpwm[1].line_compl[5]:1			smif.spi_data7	scb[6].uart_cts:0		scb[6].spi_select0:0									
P12.4	tcpwm[0].line[6]:3	tcpwm[1].line[6]:1			smif.spi_select3			scb[6].spi_select1:0	audioss.pdm_clk								

Table 2. Multiple Alternate Functions *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P12.5	tcpwm[0].line_compl[6]:3	tcpwm[1].line_compl[6]:1						scb[6].spi_select2:0	audioss.pdm_data								
P12.6	tcpwm[0].line[7]:3	tcpwm[1].line[7]:1						scb[6].spi_select3:0									
P12.7	tcpwm[0].line_compl[7]:3	tcpwm[1].line_compl[7]:1															
P13.0	tcpwm[0].line[0]:4	tcpwm[1].line[8]:1				scb[6].uart_rx:1	scb[6].i2c_scl:1	scb[6].spi_mosi:1			peri.tr_io_input[26]:0						
P13.1	tcpwm[0].line_compl[0]:4	tcpwm[1].line_compl[8]:1				scb[6].uart_tx:1	scb[6].i2c_sda:1	scb[6].spi_miso:1			peri.tr_io_input[27]:0						
P13.2	tcpwm[0].line[1]:4	tcpwm[1].line[9]:1				scb[6].uart_rts:1		scb[6].spi_clk:1									
P13.3	tcpwm[0].line_compl[1]:4	tcpwm[1].line_compl[9]:1				scb[6].uart_cts:1		scb[6].spi_select0:1									
P13.4	tcpwm[0].line[2]:4	tcpwm[1].line[10]:1						scb[6].spi_select1:1									
P13.5	tcpwm[0].line_compl[2]:4	tcpwm[1].line_compl[10]:1						scb[6].spi_select2:1									
P13.6	tcpwm[0].line[3]:4	tcpwm[1].line[11]:1						scb[6].spi_select3:1									
P13.7	tcpwm[0].line_compl[3]:4	tcpwm[1].line_compl[11]:1															

Analog, Smart I/O, and DSI alternate Port Pin functionality is provided in Table 3.

Table 3. Port Pin Analog, Smart I/O, and DSI Functions

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P0.0	P0.0	wco_in		dsi[0].port_if[0]		
P0.1	P0.1	wco_out		dsi[0].port_if[1]		
P0.2	P0.2			dsi[0].port_if[2]		
P0.3	P0.3			dsi[0].port_if[3]		
P0.4	P0.4		pmic_wakeup_in hibernate_wakeup[1]	dsi[0].port_if[4]		
P0.5	P0.5		pmic_wakeup_out	dsi[0].port_if[5]		
P1.0	P1.0			dsi[1].port_if[0]		
P1.1	P1.1			dsi[1].port_if[1]		
P1.2	P1.2			dsi[1].port_if[2]		
P1.3	P1.3			dsi[1].port_if[3]		
P1.4	P1.4		hibernate_wakeup[0]	dsi[1].port_if[4]		
P1.5	P1.5			dsi[1].port_if[5]		
P14.0	USBDP					usb.usb_dp_pad
P14.1	USBDM					usb.usb_dm_pad
P2.0	P2.0			dsi[2].port_if[0]		
P2.1	P2.1			dsi[2].port_if[1]		
P2.2	P2.2			dsi[2].port_if[2]		
P2.3	P2.3			dsi[2].port_if[3]		
P2.4	P2.4			dsi[2].port_if[4]		
P2.5	P2.5			dsi[2].port_if[5]		
P2.6	P2.6			dsi[2].port_if[6]		
P2.7	P2.7			dsi[2].port_if[7]		
P3.0	P3.0					
P3.1	P3.1					
P3.2	P3.2					
P3.3	P3.3					
P3.4	P3.4					
P3.5	P3.5					
P4.0	P4.0			dsi[0].port_if[6]		
P4.1	P4.1			dsi[0].port_if[7]		
P4.2	P4.2			dsi[1].port_if[6]		
P4.3	P4.3			dsi[1].port_if[7]		
P5.0	P5.0			dsi[3].port_if[0]		
P5.1	P5.1			dsi[3].port_if[1]		
P5.2	P5.2			dsi[3].port_if[2]		
P5.3	P5.3			dsi[3].port_if[3]		
P5.4	P5.4			dsi[3].port_if[4]		
P5.5	P5.5			dsi[3].port_if[5]		
P5.6	P5.6	lpcomp.inp_comp0		dsi[3].port_if[6]		
P5.7	P5.7	lpcomp.inn_comp0		dsi[3].port_if[7]		
P6.0	P6.0			dsi[4].port_if[0]		

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P6.1	P6.1			dsi[4].port_if[1]		
P6.2	P6.2	lpcomp.inp_comp1		dsi[4].port_if[2]		
P6.3	P6.3	lpcomp.inn_comp1		dsi[4].port_if[3]		
P6.4	P6.4			dsi[4].port_if[4]		
P6.5	P6.5			dsi[4].port_if[5]		
P6.6	P6.6		swd_data	dsi[4].port_if[6]		
P6.7	P6.7		swd_clk	dsi[4].port_if[7]		
P7.0	P7.0			dsi[5].port_if[0]		
P7.1	P7.1	csd.cmodpadd csd.cmodpads		dsi[5].port_if[1]		
P7.2	P7.2	csd.csh_tankpadd csd.csh_tankpads		dsi[5].port_if[2]		
P7.3	P7.3	csd.vref_ext		dsi[5].port_if[3]		
P7.4	P7.4			dsi[5].port_if[4]		
P7.5	P7.5			dsi[5].port_if[5]		
P7.6	P7.6			dsi[5].port_if[6]		
P7.7	P7.7	csd.cshieldpads		dsi[5].port_if[7]		
P8.0	P8.0			dsi[11].port_if[0]	smartio[8].io[0]	
P8.1	P8.1			dsi[11].port_if[1]	smartio[8].io[1]	
P8.2	P8.2			dsi[11].port_if[2]	smartio[8].io[2]	
P8.3	P8.3			dsi[11].port_if[3]	smartio[8].io[3]	
P8.4	P8.4			dsi[11].port_if[4]	smartio[8].io[4]	
P8.5	P8.5			dsi[11].port_if[5]	smartio[8].io[5]	
P8.6	P8.6			dsi[11].port_if[6]	smartio[8].io[6]	
P8.7	P8.7			dsi[11].port_if[7]	smartio[8].io[7]	
P9.0	P9.0	ctb_oa0+		dsi[10].port_if[0]	smartio[9].io[0]	
P9.1	P9.1	ctb_oa0-		dsi[10].port_if[1]	smartio[9].io[1]	
P9.2	P9.2	ctb_oa0_out		dsi[10].port_if[2]	smartio[9].io[2]	
P9.3	P9.3	ctb_oa1_out		dsi[10].port_if[3]	smartio[9].io[3]	
P9.4	P9.4	ctb_oa1-		dsi[10].port_if[4]	smartio[9].io[4]	
P9.5	P9.5	ctb_oa1+		dsi[10].port_if[5]	smartio[9].io[5]	
P9.6	P9.6	ctb_oa0+		dsi[10].port_if[6]	smartio[9].io[6]	
P9.7	P9.7	ctb_oa1+ or ext_vref		dsi[10].port_if[7]	smartio[9].io[7]	
P10.0	P10.0	sarmux[0]		dsi[9].port_if[0]		
P10.1	P10.1	sarmux[1]		dsi[9].port_if[1]		
P10.2	P10.2	sarmux[2]		dsi[9].port_if[2]		
P10.3	P10.3	sarmux[3]		dsi[9].port_if[3]		
P10.4	P10.4	sarmux[4]		dsi[9].port_if[4]		
P10.5	P10.5	sarmux[5]		dsi[9].port_if[5]		
P10.6	P10.6	sarmux[6]		dsi[9].port_if[6]		
P10.7	P10.7	sarmux[7]		dsi[9].port_if[7]		

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P11.0	P11.0			dsi[8].port_if[0]		
P11.1	P11.1			dsi[8].port_if[1]		
P11.2	P11.2			dsi[8].port_if[2]		
P11.3	P11.3			dsi[8].port_if[3]		
P11.4	P11.4			dsi[8].port_if[4]		
P11.5	P11.5			dsi[8].port_if[5]		
P11.6	P11.6			dsi[8].port_if[6]		
P11.7	P11.7			dsi[8].port_if[7]		
P12.0	P12.0			dsi[7].port_if[0]		
P12.1	P12.1			dsi[7].port_if[1]		
P12.2	P12.2			dsi[7].port_if[2]		
P12.3	P12.3			dsi[7].port_if[3]		
P12.4	P12.4			dsi[7].port_if[4]		
P12.5	P12.5			dsi[7].port_if[5]		
P12.6	P12.6	srss.eco_in		dsi[7].port_if[6]		
P12.7	P12.7	srss.eco_out		dsi[7].port_if[7]		
P13.0	P13.0			dsi[6].port_if[0]		
P13.1	P13.1			dsi[6].port_if[1]		
P13.2	P13.2			dsi[6].port_if[2]		
P13.3	P13.3			dsi[6].port_if[3]		
P13.4	P13.4			dsi[6].port_if[4]		
P13.5	P13.5			dsi[6].port_if[5]		
P13.6	P13.6			dsi[6].port_if[6]		
P13.7	P13.7			dsi[6].port_if[7]		

Power

The power system diagram (see Figure 2) shows the general requirements for power pins on the PSoC 63. The diagram also shows the radio pins that need to be decoupled. The PSoC 63 power scheme allows different VDDIO and VDDA connections. Since no sequencing requirements need to be analyzed and specified, customers may bring up the power supplies in any order and the power system is responsible for ensuring power is good in all domains before allowing operation. VDDD, VDDA, and VDDIO may be separate nets, which are not ohmically connected on chip. Depending on different package requirements, these may be required to be connected off chip.

The power system will have a buck regulator in addition to an LDO. A Single Input Multiple Output (SIMO) Buck regulator with multiple outputs allows saving an inductor and also providing a high-efficiency supply to the radio.

The preliminary diagram is shown in Figure 2.

Figure 2. SOC Power Connections with Radio (For 104-CSP and 116-BGA Packages)

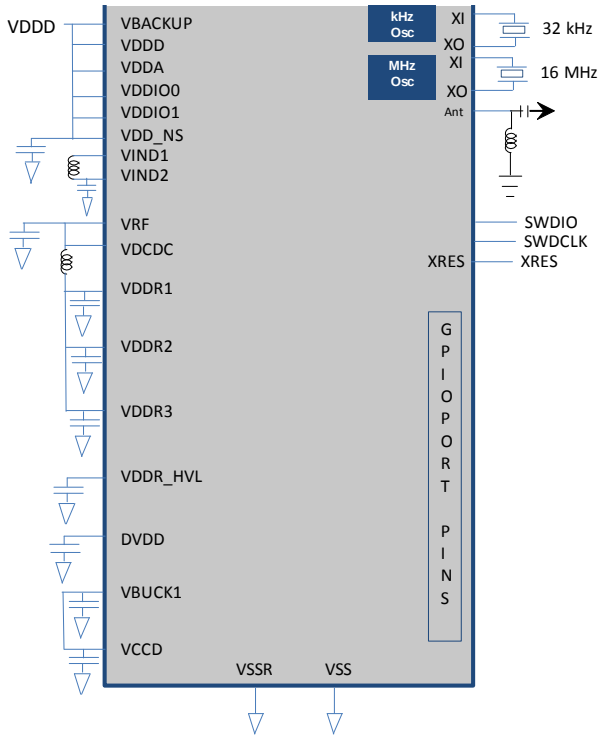


Figure 2 shows the power supply pins to the PSoC and the connections between the PSoC and the radio. It also shows which pins need bypass capacitors.

Description of power pins is as follows:

1. VBACKUP is the supply to the backup domain. The backup domain includes the 32 kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDDD when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0.
2. VDDD is the main digital supply input (1.7 to 3.6V). It provides the inputs for the internal Regulators and for Port 1.
3. VDDA is the supply for analog peripherals (1.7 to 3.6V). It must be connected to VDDIOA on the PCB.
4. VDDIOA is the supply to for Ports 9 and 10. It must be connected to VDDA on the PCB when present. Ports 9 and 10 are supplied by VDDA when VDDIOA is not present.
5. VDD_NS is the supply input to the Buck and should be at the same potential as VDDD. The bypass capacitor between VDD_NS and ground should be 10 µF.
6. VDDIO0 is the Supply for Ports 11 to 13 when present. When not present, these ports are supplied by VDDD.
7. VDDIO1 is the Supply for Ports 5 to 8 when present. When not present, these ports are supplied by VDDA.
8. VDDIOR is the Supply for Ports 2 to 4 on the BGA 124 only.

All the pins above may be shorted to VDDD as shown in Figure 2.

9. VRF is the output of the SIMO buck going to the Radio and should be connected to VDCDC and decoupled.
10. VDCDC is the digital supply input to the Radio and should be connected to VRF.
11. The VDDR1, VDDR2, and VDDR3 pins are for the radio sub-systems and need to be decoupled individually and connected to VDCDC through a bead for filtering high frequency power supply noise.
12. VDDR_HVL is the regulated output to the Radio from the PSoC 63 subsystem and needs to be decoupled.
13. DVDD is a Digital LDO output from the Radio and needs to be decoupled.
14. VBUCK1 is the SIMO buck output to the internal core logic and is to be connected to VCCD.
15. VCCD is the internal core logic and needs to be connected to VBUCK1 and decoupled.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All grounds must be shorted together on the PCB. Bypass capacitors must be used from VDDD and VDDA to ground and wherever indicated in the diagram. Typical practice for systems in this frequency range is to use a capacitor in the 10-µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. Recommended Buck output capacitor values are 10 µF for Vrf and 4.7 µF for Vbuck2. The capacitor connected to Vind2 should be 100 nF.

Development Support

The PSoC 63 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/products/32-bit-arm-cortex-m0-psoc-4 to find out more.

Documentation

A suite of documentation supports the PSoC 63 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/products/32-bit-arm-cortex-m0-psoc-4.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 63 family is part of a development tool ecosystem. Visit us at www.cypress.com/products/psoc-creator-integrated-design-environment-ide for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	4	V	Absolute Maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.2	V	Absolute Maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	Absolute Maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute Maximum
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute Maximum
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	Absolute Maximum
SID3A	ESD_HBM_ ANT	Electrostatic discharge Human Body Model; Antenna Pin	500	–	–	V	Absolute Maximum; RF pin
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	Absolute Maximum
SID4B	ESD_CDM_ ANT	Electrostatic discharge Charged Device Model; Antenna Pin	250	–	–	V	Absolute Maximum; RF pin
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	Absolute Maximum

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
LP RANGE POWER SPECIFICATIONS (V_{CCD} = 1.1 V)							
Cortex M4. Active Mode, V_{DD} = 1.7 V to 3.6 V							
Execute with Cache Disabled (Flash)							
SIDF1	IDD1	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz	–	3.2	–	mA	With IMO & FLL. While (1)
SIDF2	IDD2	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz	–	0.6	–	mA	With IMO. While (1)
Execute with Cache Enabled							
SIDC1	IDD3	Execute from Cache;CM4 Active150 MHz, CM0+ Sleep 75 MHz	–	9.3	–	mA	IMO&FLL; Dhrystone
SIDC2	IDD4	Execute from Cache;CM4 Active100 MHz, CM0+ Sleep 100 MHz	–	6.7	–	mA	IMO&FLL; Dhrystone
SIDC3	IDD5	Execute from Cache;CM4 Active 50 MHz, CM0+ Sleep 25 MHz	–	3.2	–	mA	IMO&FLL; Dhrystone

Note
1. Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDC4	IDD6	Execute from Cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz	–	0.62	–	mA	IMO; Dhrystone
Cortex M0+. Active Mode, VDD = 1.7 to 3.6V							
Execute with Cache Disabled (Flash)							
SIDF3	IDD7	Execute from Flash;CM4 Off, CM0+ Active 50 MHz	–	1.7	–	mA	With IMO & FLL. While (1)
SIDF4	IDD8	Execute from Flash;CM4 Off, CM0+ Active 8 MHz	–	0.5	–	mA	With IMO. While (1)
Execute with Cache Enabled							
SIDC5	IDD9	Execute from Cache;CM4 Off, CM0+ Active 100 MHz	–	3.2	–	mA	With IMO & FLL. Dhrystone.
SIDC6	IDD10	Execute from Cache;CM4 Off, CM0+ Active 8 MHz	–	0.34	–	mA	With IMO. Dhrystone.
Cortex M4. Sleep Mode, V_{DD} = 1.7 V to 3.6 V							
SIDS1	IDD11	CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz	–	1.5	–	mA	With IMO & FLL
SIDS2	IDD12	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz	–	0.90	–	mA	With IMO & FLL
SIDS3	IDD13	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz	–	0.35	–	mA	With IMO
Cortex M0+. Sleep Mode, V_{DD} = 1.7 V to 3.6 V							
SIDS4	IDD14	CM4 Off, CM0+ Sleep 50 MHz	–	0.7	–	mA	With IMO & FLL
SIDS5	IDD15	CM4 Off, CM0+ Sleep 8 MHz	–	0.3	–	mA	With IMO
Cortex M4. Low Power Active (LPA) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPA1	IDD16	Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz	–	0.55	–	mA	LPA mode. With IMO. While (1)
SIDLPA2	IDD17	Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz	–	0.53	–	mA	LPA mode. With IMO. Dhrystone.
Cortex M0+. Low Power Active (LPA) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPA3	IDD18	Execute from Flash; CM4 Off, CM0+ LPA 8 MHz	–	0.4	–	mA	LPA mode. With IMO. While (1)
SIDLPA4	IDD19	Execute from Cache; CM4 Off, CM0+ LPA 8 MHz	–	0.25	–	mA	LPA mode. With IMO. Dhrystone.
Cortex M4. Low Power Sleep (LPS) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPS1	IDD20	CM4 LPS 8 MHz, CM0+ LPS 8 MHz	–	0.3	–	mA	LPS mode. With IMO
Cortex M0+. Low Power Sleep (LPS) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPS3	IDD22	CM4 Off, CM0+ LPS 8 MHz	–	0.25	–	mA	LPA mode. With IMO
ULP RANGE POWER SPECIFICATIONS (V_{CCD} = 0.9 V)							
Cortex M4. Active Mode, V_{DD} = 1.7 V to 3.6 V							
Execute with Cache Disabled (Flash)							
SIDF5	IDD3	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz	–	2.5	–	mA	With IMO & FLL. While (1)
SIDF6	IDD4	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz	–	0.49	–	mA	With IMO. While (1)
Execute with Cache Enabled							
SIDC8	IDD10	Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz	–	2.5	–	mA	With IMO & FLL. Dhrystone.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIDC9	IDD11	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz	–	0.49	–	mA	With IMO. Dhrystone.
Cortex M0+. Active Mode, V_{DD} = 1.7 V to 3.6 V							
Execute with Cache Disabled (Flash)							
SIDF7	IDD16	Execute from Flash; CM4 Off, CM0+ Active 25 MHz	–	0.68	–	mA	With IMO & FLL. While (1)
SIDF8	IDD17	Execute from Flash; CM4 Off, CM0+ Active 8 MHz	–	0.3	–	mA	With IMO. While (1)
Execute with Cache Enabled							
SIDC10	IDD18	Execute from Cache; CM4 Off, CM0+ Active 25 MHz	–	0.675	–	mA	With IMO & FLL. Dhrystone.
SIDC11	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz	–	0.3	–	mA	With IMO. Dhrystone.
Cortex M4. Sleep Mode, V_{DD} = 1.7 V to 3.6 V							
SIDS7	IDD21	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz	–	0.55	–	mA	With IMO & FLL
SIDS8	IDD22	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz	–	0.25	–	mA	With IMO
Cortex M0+. Sleep Mode, V_{DD} = 1.7 V to 3.6 V							
SIDS9	IDD23	CM4 Off, CM0+ Sleep 25 MHz	–	0.3	–	mA	With IMO & FLL
SIDS10	IDD24	CM4 Off, CM0+ Sleep 8 MHz	–	0.2	–	mA	With IMO
Cortex M4. Low Power Active (LPA) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPA5	IDD25	Execute from Flash. CM4 LPA 8 MHz, CM0+ LPS 8 MHz	–	0.40	–	mA	With IMO; While (1).
SIDLPA6	IDD26	Execute from Cache. CM4 LPA 8 MHz, CM0+ LPS 8 MHz	–	0.40	–	mA	With IMO; Dhrystone
Cortex M0+. LPA Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPA7	IDD27	Execute from Flash. CM4 Off, CM0+ LPA 8 MHz	–	0.25	–	mA	With IMO; While (1).
SIDLPA8	IDD28	Execute from Cache. CM4 Off, CM0+ LPA 8 MHz	–	0.25	–	mA	With IMO; Dhrystone
Cortex M4. Low Power Sleep (LPS) Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPS5	IDD29	CM4 LPS 8 MHz, CM0 LPS 8 MHz	–	0.2	–	mA	LPS mode. With IMO
Cortex M0+. LPS Mode, V_{DD} = 1.7 V to 3.6 V							
SIDLPS7	IDD31	CM4 Off, CM0+ LPS 8 MHz	–	0.15	–	mA	LPS mode. With IMO
Deep Sleep Mode							
SIDDS1	IDD33A	With internal Buck enabled and 64K SRAM retention	–	7	–	µA	Max value is at 85 °C
SIDDS1_B	IDD33A_B	With internal Buck enabled and 64K SRAM retention	–	7	–	µA	Max value is at 60 °C
SIDDS2	IDD33B	With internal Buck enabled and 256K SRAM retention	–	9	–	µA	Max value is at 85 °C
SIDDS2_B	IDD33B_B	With internal Buck enabled and 256K SRAM retention	–	9	–	µA	Max value is at 60 °C
Hibernate Mode							
SIDHIB1	IDD34		–	300	–	nA	

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Power Mode Transition Times							
SID12	TLPACT_ACT	Low Power Active to Active transition time	–	100	–	µs	Including PLL lock time
SID13	TDS_LPACT	Deep Sleep to LP Active transition time	–	–	21	µs	Transition to Firmware execution
SID13A	TDS_ACT	Deep Sleep to Active transition time	–	–	21	µs	Transition to Firmware execution
SID14	THIB_ACT	Hibernate to Active transition time	–	500	–	µs	Including PLL lock time

XRES

Table 6. XRES

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
XRES AC Specifications							
SID15	TXRES_ACT	XRES release to Active transition time	–	500	–	µs	–
SID16	TXRES_PW	XRES Pulse width	5	–	–	µs	–
XRES DC Specifications							
SID17	TXRES_IDD	I_{DD} when XRES asserted	–	500	–	nA	–
SID77	V_{IH}	Input Voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input Voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID80	C_{IN}	Input Capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

GPIO

Table 7. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage high threshold	0.7*V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	0.3*V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7*V_{DD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3*V_{DD}	V	
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DD}-0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V

Table 7. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	
SID66	C_{IN}	Input Capacitance	–	–	5	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL $V_{DD} > 2.7$ V	100	0	-	mV	
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05*V_{DD}$	–	-	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, $V_{DD} \leq$ 2.7 V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < $V_{DD} \leq$ 3.6 V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, $V_{DD} \leq$ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < $V_{DD} \leq$ 3.6 V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode	$20*V_{DDIO}/5.5$	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	16.7	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency;1.71 V $\leq V_{DD} \leq$ 5.5 V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Opamp

Table 8. Opamp Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	I_{DD}	Opamp Block current. No load.	–	–	–		–
SID269	I_{DD_HI}	Power = Hi	–	1300	1500	µA	–
SID270	I_{DD_MED}	Power = Med	–	450	600	µA	–
SID271	I_{DD_LOW}	Power = Lo	–	250	350	µA	–
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–		–
SID272	G_{BW_HI}	Power = Hi	6	–	–	MHz	–
SID273	G_{BW_MED}	Power = Med	4	–	–	MHz	–
SID274	G_{BW_LO}	Power = Lo	–	1	–	MHz	–
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–		–
SID275	$I_{OUT\_MAX\_HI}$	Power = Hi	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	Power = Mid	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	Power = Lo	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–		–
SID278	$I_{OUT\_MAX\_HI}$	Power = Hi	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	Power = Mid	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	Power = Lo	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	0	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Input common mode voltage	0	–	V_{DDA}-0.2	V	–
	V_{OUT}	$V_{DDA} \geq 2.7$V	–	–	–		–
SID283	V_{OUT_1}	Power = hi, Iload = 10 mA	0.5	–	V_{DDA}-0.5	V	–
SID284	V_{OUT_2}	Power = hi, Iload = 1 mA	0.2	–	V_{DDA}-0.2	V	–
SID285	V_{OUT_3}	Power = med, Iload = 1 mA	0.2	–	V_{DDA}-0.2	V	–
SID286	V_{OUT_4}	Power = lo, Iload = 0.1 mA	0.2	–	V_{DDA}-0.2	V	–
SID287	VOS_UNTR	Offset voltage, untrimmed	–	–	–	mV	–
SID288	VOS_TR	Offset voltage, trimmed	–1	±0.5	–	mV	High mode, 0.2 to V_{DDA} - 0.2
SID288A	VOS_TR	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	VOS_TR	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID289	VOS_DR_UNTR	Offset voltage drift, untrimmed	–	–	–	µV/°C	–
SID290	VOS_DR_TR	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode, 0.2 to V_{DDA}-0.2
SID290A	VOS_DR_TR	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	VOS_DR_TR	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio	70	80	–	dB	V_{DDD} = 3.3 V
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10-mV ripple	70	85	–	dB	V_{DDD} = 3.3 V
Noise			–	–	–		–
SID293	VN1	Input-referred, 1 Hz - 1 GHz, power = Hi	–	100	–	µVrms	–
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	180	–	nV/rtHz	–

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	70	–	nV/rtHz	–
SID296	VN4	Input-referred, 100kHz, power = Hi	–	38	–	nV/rtHz	–
SID297	CLOAD	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Output slew rate	6	–	–	V/µs	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	25	–	µs	–
	COMP_MODE	Comparator mode; 50-mV overdrive, Trise = Tfall (approx.)	–		–		–
SID300	TPD1	Response time; power = hi	–	150	–	ns	–
SID301	TPD2	Response time; power = med	–	400	–	ns	–
SID302	TPD3	Response time; power = lo	–	2000	–	ns	–
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode operation: $V_{DDA} \geq 2.7$ V. V_{IN} is 0.2 to V_{DDA} -1.5
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	**1300**	1500	µA	Typ at 25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	460	600	µA	Typ at 25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	230	350	µA	Typ at 25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V

Table 8. Opamp Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_23	IOU_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_24	IOU_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

Table 9. Low-Power (LP) Comparator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
LP Comparator DC Specifications							
SID84	$V_{OFFSET1}$	Input offset voltage. Normal power mode.	–10	–	10	mV	–
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1}-0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1}-0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1}-0.1	V	–
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block Current, Normal mode	–	–	150	µA	–
SID248	I_{CMP2}	Block Current, Low power mode	–	–	10	µA	–
SID259	I_{CMP3}	Block Current in Ultra low-power mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC Input impedance of comparator	35	–	–	MΩ	–
LP Comparator AC Specifications							
SID91	T_{RESP1}	Response time, Normal mode, 100 mV overdrive	–	–	100	ns	–
SID258	T_{RESP2}	Response time, Low power mode, 100 mV overdrive	–	–	1000	ns	–

Table 9. Low-Power (LP) Comparator Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID92	T_{RESP3}	Response time, Ultra-low power mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and Low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra low-power mode

Table 10. Temperature Sensor Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 11. Internal Reference Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

SAR ADC

Table 12. 12-bit SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	SAR ADC Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16	–	8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	-	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1	mA	At 1 Msps. External Bypass Cap.
SID100A	A_ISAR_2	Current consumption at 1 Msps. Reference = V_{DD}	–	–	1.25	mA	At 1 Msps. External Bypass Cap.
SID101	A_VINS	Input voltage range - single-ended	Vss	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	Vss	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–

Table 13. 12-bit SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
One Megasample per second mode							
SID108	A_SAMP_1	Sample rate with external reference bypass cap.	–	–	1	Msps	

Table 13. 12-bit SAR ADC AC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID108A	A_SAMP_2	Sample rate with no bypass cap.; Reference = V_{DD}	–	–	250	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference.	–	–	100	ksps	
SID109	A_SINAD	Signal-to-noise and Distortion ratio (SINAD). V_{DDA} = 2.7 V to 3.6 V, 1 Msps	65	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–2	–	2	LSB	V_{REF} = 1.2 to V_{DDA}
SID112A	A_DNL	Differential Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1	LSB	V_{REF} = 1.2 to V_{DDA}
SID113	A_THD	Total harmonic distortion. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–	–	–65	dB	Fin = 10 kHz

Table 14. 12-bit DAC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
12-bit DAC DC Specifications							
SID108D	DAC_RES	DAC resolution	-	-	12	bits	
SID111D	DAC_INL	Integral Non-Linearity	-4	-	4	LSB	
SID112D	DAC_DNL	Differential Non Linearity	-2	-	2	LSB	Monotonic to 11 bits.
SID99D	DAC_OFFSET	Output Voltage zero offset error	-10	-	10	mV	For 000 (hex)
SID103D	DAC_OUT_RES	DAC Output Resistance	-	15	-	kΩ	
SID100D	DAC_IDD	DAC Current			125	µA	
SID101D	DAC_QIDD	DAC Current when DAC stopped			1	µA	
12-bit DAC AC Specifications							
SID109D	DAC_CONV	DAC Settling time			2	µs	Driving through CTBm buffer; 25-pF load
SID110D	DAC_Wakeup	Time from Enabling to ready for conversion			10	µs	

CSD

Table 15. CapSense Sigma-Delta (CSD) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
CSD V2 Specifications							
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDA} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DDA} > 1.75 V (with ripple), 25 ° C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current			4500	µA	
SID.CSD#15	VREF	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.6, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.6, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1900	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1900	µA	
SID308	VCSD	Voltage range of operation	1.7	–	3.6	V	1.71 to 3.6 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} - 0.6, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization							
SID313_1A	SNRC_1	SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity	5	–	–	Ratio	9.5-pF max. capacitance
SID313_1B	SNRC_2	SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity	5	–	–	Ratio	31-pF max. capacitance
SID313_1C	SNRC_3	SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity	5	–	–	Ratio	61-pF max. capacitance
SID313_2A	SNRC_4	PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity	5	–	–	Ratio	12-pF max. capacitance
SID313_2B	SNRC_5	PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity	5	–	–	Ratio	47-pF max. capacitance
SID313_2C	SNRC_6	PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity	5	–	–	Ratio	86-pF max. capacitance
SID313_3A	SNRC_7	PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity	5	–	–	Ratio	27-pF max. capacitance
SID313_3B	SNRC_8	PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity	5	–	–	Ratio	86-pF max. capacitance
SID313_3C	SNRC_9	PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity	5	–	–	Ratio	168-pF Max. capacitance
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5-nA typ

Table 15. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34		46	µA	LSB = 300 nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	270		365	µA	LSB = 2.4 uA typ.
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5nA typ. 2X output stage
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300 nA typ. 2X output stage
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode. V_{DDA} > 2 V	540		730	µA	LSB = 2.4 uA typ.2X output stage
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34		46	µA	LSB = 300 nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	270		365	µA	LSB = 2.4 uA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8		11.4	µA	LSB = 37.5nA typ. 2X output stage
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	67		91	µA	LSB = 300 nA typ. 2X output stage
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode. V_{DDA} > 2V	540		730	µA	LSB = 2.4 uA typ.2X output stage
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8		11.4	µA	LSB = 37.5nA typ.
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	67		91	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540		730	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	IDACGAIN	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 16. CSD ADC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	–
SIDA98	A_GAINERR	Gain error	–	–	TBD	%	–
SIDA99	A_OFFSET	Input offset voltage	–	–	TBD	mV	–
SIDA100	A_ISAR	Current consumption	–	–	TBD	mA	–
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	–
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	–
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio	TBD	–	–	dB	–
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	–
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	TBD	–	–	dB	–
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	kHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps.	–	–	2	LSB	Vref = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps.	–	–	1	LSB	–

Digital Peripherals

Table 17. Timer/Counter/PWM (TCPWM) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	ITCPWM4	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	100	MHz	Fc max = Fcpu Maximum = 100 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar.

Table 18. Serial Communication Block (SCB) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Fixed I2C DC Specifications							
SID149	II2C1	Block current consumption at 100 kHz	–	–	30	µA	
SID150	II2C2	Block current consumption at 400 kHz	–	–	80	µA	
SID151	II2C3	Block current consumption at 1 Mbps	–	–	180	µA	
SID152	II2C4	I2C enabled in Deep Sleep mode	–	–	1.4	µA	
Fixed I2C AC Specifications							
SID153	FI2C1	Bit Rate	–	–	1	Mbps	
Fixed UART DC Specifications							
SID160	IUART1	Block current consumption at 100 Kbps	–	–	30	µA	
SID161	IUART2	Block current consumption at 1000 Kbps	–	–	180	µA	
Fixed UART AC Specifications							
SID162	FUART	Bit Rate	–	–	1	Mbps	
Fixed SPI DC Specifications							
SID163	ISPI1	Block current consumption at 1Mbps	–	–	220	µA	
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	340	µA	
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	360	µA	

Table 18. Serial Communication Block (SCB) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID165A	ISP14	Block current consumption at 25 Mbps	–	–	800	µA	
Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID166	FSPI	SPI Operating frequency Master and Externally Clocked Slave	–	–	25	MHz	14-MHz max for ULP (0.9 V) mode
SID166A	FSPI_IC	SPI Slave Internally Clocked	–	–	15	MHz	5 MHz max for ULP (0.9 V) mode
Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	12	ns	20ns max for ULP (0.9 V) mode
SID168	TDSI	MISO Valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling
SID169	THMO	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	5	–	–	ns	
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	35ns max. for ULP (0.9 V) mode
SID171	TDSO	MISO Valid after Sclock driving edge in Internally Clk. Mode	–	–	TDSO_EXT + 3*Tscb	ns	Tscb is Serial Comm Block clock period.
SID171B	TDSO	MISO Valid after Sclock driving edge in Internally Clk. Mode with Median filter enabled.	–	–	TDSO_EXT + 4*Tscb	ns	Tscb is Serial Comm Block clock period.
SID172	THSO	Previous MISO data hold time	5	–	–	ns	
SID172A	TSSELSCK1	SSEL Valid to first SCK Valid edge	65	–	–	ns	
SID172B	TSSELSCK2	SSEL Hold after Last SCK Valid edge	–	–	65	ns	

LCD Specifications

Table 19. LCD Direct Drive DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low-power mode	–	5	–	µA	16 × 4 small segment display at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 20. LCD Direct Drive AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Memory

Table 21. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	3.6	V	–

Table 22. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[2]	Row (block) write time (erase and program)	–	–	16	ms	Row (block) = 512 bytes
SID175	$T_{ROWERASE}$[2]	Row erase time	–	–	11	ms	–
SID176	$T_{ROWPROGRAM}$[2]	Row program time after erase	–	–	5	ms	–
SID178	$T_{BULKERASE}$[2]	Bulk erase time (1024 KB)	–	–	11	ms	–
SID179	TSECTORERASE	Sector erase time (256 KB)	–	–	11	ms	512 rows per sector
SID178S	TSSERIAE	Sub-Sector erase time	–	–	11	ms	8 rows per sub-sector
SID179S	TSSWRITE	Sub-Sector write time; 1 erase plus 8 program times	–	–	51	ms	–
SID180S	TSWRITE	Sector write time; 1 erase plus 512 program times			2.6	seconds	–
SID180	$T_{DEVPROG}$[2]	Total device program time	–	–	15	seconds	For 256 KB
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	–
SID182	FRET	Flash Retention. Ta ≤ 55 °C, 100K P/E cycles	20	–	–	years	–
SID182a		Flash Retention. Ta ≤ 85 °C, 10K P/E cycles	10	–	–	years	–
SID256	TWS100	Number of Wait states at 100 MHz	3	–	–		–
SID257	TWS50	Number of Wait states at 50 MHz	2	–	–		–

Note
2. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Table 23. PSoC 6 System Resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Power-On-Reset with Brown-out DC Specifications							
Precise POR(PPOR)							
SID190	VFALLPPOR	BOD trip voltage in Active and Sleep modes. V_{DDD}.	1.59	–	–	V	BOD Reset guaranteed for levels below 1.59 V of 30 ns or greater duration
SID192	VFALLDPSLP	BOD trip voltage in Deep Sleep. V_{DDD}	1.54	–	–	V	–
SID192A	VDDRAMP	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active Mode
POR with Brown-out AC Specification							
SID194	TPPOR_TR	PPOR Response time in Active and Sleep modes	–	–	30	ns	BOD Reset guaranteed for levels below 1.59 V of 30 ns or greater duration
SID194A	VDDRAMP_DS	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	10	mV/µs	BOD operation guaranteed
Voltage Monitors DC Specifications							
SID195R	VHVD0		1.18	1.23	1.27	V	–
SID195	VHVDI1		1.38	1.43	1.47	V	–
SID196	VHVDI2		1.57	1.63	1.68	V	–
SID197	VHVDI3		1.76	1.83	1.89	V	–
SID198	VHVDI4		1.95	2.03	2.1	V	–
SID199	VHVDI5		2.05	2.13	2.2	V	–
SID200	VHVDI6		2.15	2.23	2.3	V	–
SID201	VHVDI7		2.24	2.33	2.41	V	–
SID202	VHVDI8		2.34	2.43	2.51	V	–
SID203	VHVDI9		2.44	2.53	2.61	V	–
SID204	VHVDI10		2.53	2.63	2.72	V	–
SID205	VHVDI11		2.63	2.73	2.82	V	–
SID206	VHVDI12		2.73	2.83	2.92	V	–
SID207	VHVDI13		2.82	2.93	3.03	V	–
SID208	VHVDI14		2.92	3.03	3.13	V	–
SID209	VHVDI15		3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–
Voltage Monitors AC Specification							
SID212	TMONTRIP	Voltage monitor trip time	–	–	170	ns	–

SWD Interface

Table 24. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V <= V_{DDD} <= 3.6 V	–	–	25	MHz	LP Mode; V_{CCD} = 1.1 V
SID214L	F_SWDCLK2L	1.7 V <= V_{DDD} <= 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	75	MHz	LP Mode. V_{DD} = 1.1 V
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	70	MHz	LP Mode. V_{DD} = 1.1 V
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	25	MHz	ULP Mode. V_{DD} = 0.9 V

Internal Main Oscillator

Table 25. IMO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 26. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±1	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	6	µs	Startup time to 99% of final frequency
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	250	–	ps	–

Internal Low-Speed Oscillator

Table 27. ILO DC Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 28. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	5	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	28.8	32	35.2	kHz	±10% variation

Crystal Oscillator Specifications

Table 29. ECO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
MHz ECO DC Specifications							
SID316	IDD_MHz	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max = 33 MHz, Type = 16 MHz
MHz ECO AC Specifications							
SID317	F_MHz	Crystal frequency range	4	–	33	MHz	–
kHz ECO DC Specification							
SID318	Idd_kHz	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent Series Resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC Specification							
SID319	F_kHz	32-kHz trimmed frequency	–	32.768	–	KHz	–
SID320	Ton_kHz	Startup time	–	–	500	ms	–
SID320E	FTOL32K	Frequency tolerance	–	50	250	ppm	–

External Clock Specifications

Table 30. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	EXTCLKFREQ	External Clock input Frequency	0	–	100	MHz	–
SID306	EXTCLKDUTY	Duty cycle; Measured at VDD/2	45	–	55	%	–

Table 31. PLL Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305P	PLL_LOCK	Time to achieve PLL Lock	–	16	50	µs	–
SID306P	PLL_OUT	Output frequency from PLL Block	–	–	150	MHz	–
SID307P	PLL_IDD	PLL Current	–	0.55	1.1	mA	Typ. at 100 MHz out.

Table 32. Clock Source Switching Time

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262	TCLKSWITCH	Clock switching from clk1 to clk2 in clock periods	–	–	4 clk1 + 3 clk2	periods	–

Table 33. Frequency Locked Loop (FLL) Specifications[3]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. VCCD = 1.1V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. VCCD = 0.9V	24.00	–	25.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	
SID453	FLL_OUT_UNDIV	Undivided output of FLL. VCCD =1.1V	48.00	–	200.00	MHz	Undivided FLL output
SID453A	FLL_OUT_UNDIV	Undivided output of FLL. VCCD = 0.9V	48.00	–	50.00	MHz	Undivided FLL output
SID454	FLL_STARTUP	Time from stable input clock to 1% of final value	–	–	5.00	µs	With IMO input
SID455	FLL_JITTER	Period jitter (1 sigma)	50.00	–	12.00	pS	50 ps at 48 MHz, 12 pS at 200 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	–

Table 34. UDB AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Data Path Performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	100	MHz	–
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	100	MHz	–
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	100	MHz	–
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	100	MHz	–
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out	–	5	–	ns	–
UDB Port Adaptor Specifications							
Conditions: 10 pF load, 3V VDDIO and VDDD							
SID263	TLCLKDO	LCLK to Output delay	–	–	11	ns	–
SID264	TDINLCLK	Input setup time to LCLCK rising edge	–	–	7	ns	–
SID265	TDINLCLKHLD	Input hold time from LCLK rising edge	5	–	–	ns	–
SID266	TLCLKHIZ	LCLK to Output tristated	–	–	28	ns	–
SID267	TFLCLK	LCLK frequency	–	–	33	MHz	–
SID268	TLCLKDUTY	LCLK duty cycle (percentage high)	40%	–	60%	%	–

Note
3. The undivided output of the FLL must be a minimum of 2.5X the input frequency.

Table 35. USB Specifications (USB requires LP Mode 1.1V internal supply)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
USB Block Specifications							
SID322U	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323U	Vusb_3.3	Device supply for USB operation (functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID325U	Iusb_config	Device supply current in Active mode	–	8	–	mA	VDDD = 3.3 V
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	VDDD = 3.3 V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	VDDD = 3.3 V, Device disconnected
SID330U	USB_Drive_Res	USB driver impedance	28	–	44	Ω	Series resistors are on chip
SID331U	USB_Pulldown	USB pull-down resistors in Host mode	14.25	–	24.8	kΩ	–
SID332U	USB_Pullup_Idle	Idle mode range	900	–	1575	Ω	Bus idle
SID333U	USB_Pullup	Active mode	1425	–	3090	Ω	Upstream device transmitting

Table 36. QSPI Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SMIF QSPI Specifications							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	80	–	–	MHz	–
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	–
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	–
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
SID395Q	Tseloutvalid	Output Select valid time with respect to clock falling edge	–	–	7.5	ns	–
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

Table 37. Audio Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Audio Subsystem specifications							
PDM Specifications							
SID400P	PDM_IDD1	PDM Active current, Stereo operation, 1-MHz clock	–	175	–	µA	16-bit audio at 16 ksps
SID401	PDM_IDD2	PDM Active current, Stereo operation, 3-MHz clock	–	600	–	µA	24-bit audio at 48 ksps
SID402	PDM_JITTER	RMS Jitter in PDM clock	–200	–	200	ps	
SID403	PDM_CLK	PDM Clock speed	0.384	–	3.072	MHz	
SID403A	PDM_BLK_CLK	PDM Block input clock	1.024	–	49.152	MHz	
SID403B	PDM_SETUP	Data input set-up time to PDM_CLK edge	10	–	–	ns	
SID403C	PDM_HOLD	Data input hold time to PDM_CLK edge	10	–	–	ns	
SID404	PDM_OUT	Audio sample rate	8	–	48	ksps	
SID405	PDM_WL	Word Length	16	–	24	bits	
SID406	PDM_SNR	Signal-to-Noise Ratio (A-weighted0	–	100	–	dB	PDM input, 20 Hz to 20 kHz BW
SID407	PDM_DR	Dynamic Range (A-weighted)	–	100	–	dB	20 Hz to 20 kHz BW, -60 dB FS
SID408	PDM_FR	Frequency Response	–0.05	–	–	dB	DC to 0.45f
SID409	PDM_SB	Stop Band	–	0.566	–	f	
SID410	PDM_SBA	Stop Band Attenuation	–	60	–	dB	
SID411	PDM_GAIN	Adjustable Gain	–12	–	10.5	dB	PDM to PCM, 1.5 dB/step
SID412	PDM_ST	Startup time	–	48	–		WS (Word Select) cycles
I2S Specifications. The same for LP and ULP modes unless stated otherwise.							
SID413	I2S_WORD	Length of I2S Word	8	–	32	bits	
SID414	I2S_WS	Word Clock frequency in LP mode	–	–	192	kHz	12.288-MHz bit clock with 32-bit word
SID414M	I2S_WS_U	Word Clock frequency in ULP mode	–	–	48	kHz	3.072-MHz bit clock with 32-bit word
SID414A	I2S_WS_TDM	Word Clock frequency in TDM mode for LP	–	–	48	kHz	8 32-bit channels
SID414X	I2S_WS_TDM_U	Word Clock frequency in TDM mode for ULP	–	–	12	kHz	8 32-bit channels
I2S Slave Mode							
SID430	TS_WS	WS Setup Time to the Following Rising Edge of SCK for LP Mode	5	–	–	ns	
SID430U	TS_WS	WS Setup Time to the Following Rising Edge of SCK for ULP Mode	11	–	–	ns	
SID430A	TH_WS	WS Hold Time to the Following Edge of SCK	TMCLK_SOC+5	–	–	ns	

Table 37. Audio Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID432	TD_SDO	Delay Time of TX_SDO Transition from Edge of TX_SCK for LP mode	-(TMCLK_SOC+25)	–	TMCLK_SOC+25	ns	Associated clock edge depends on selected polarity
SID432U	TD_SDO	Delay Time of TX_SDO Transition from Edge of TX_SCK for ULP mode	-(TMCLK_SOC+70)	–	TMCLK_SOC+70	ns	Associated clock edge depends on selected polarity
SID433	TS_SDI	RX_SDI Setup Time to the Following Edge of RX_SCK in Lp Mode	5	–	–	ns	
SID433U	TS_SDI	RX_SDI Setup Time to the Following Edge of RX_SCK in ULP mode	11	–	–	ns	
SID434	TH_SDI	RX_SDI Hold Time to the Rising Edge of RX_SCK	TMCLK_SOC+5	–	–	ns	
SID435	TSCKCY	TX/RX_SCK Bit Clock Duty Cycle	45	–	55	%	
I2S Master Mode							
SID437	TD_WS	WS Transition Delay from Falling Edge of SCK in LP mode	–10	–	20	ns	
SID437U	TD_WS_U	WS Transition Delay from Falling Edge of SCK in ULP mode	–10	–	40	ns	
SID438	TD_SDO	SDO Transition Delay from Falling Edge of SCK in LP mode	–10	–	20	ns	
SID438U	TD_SDO	SDO Transition Delay from Falling Edge of SCK in ULP mode	–10	–	40	ns	
SID439	TS_SDI	SDI Setup Time to the Associated Edge of SCK	5	–	–	ns	Associated clock edge depends on selected polarity
SID440	TH_SDI	SDI Hold Time to the Associated Edge of SCK	TMCLK_SOC+5	–	–	ns	T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity.
SID443	TSCKCY	SCK Bit Clock Duty Cycle	45	–	55	%	
SID445	FMCLK_SOC	MCLK_SOC Frequency in LP mode	1.024	–	98.304	MHz	FMCLK_SOC = 8*Bit-clock
SID445U	FMCLK_SOC_U	MCLK_SOC Frequency in ULP mode	1.024	–	24.576	MHz	FMCLK_SOC_U = 8*Bit-clock
SID446	TMCLKCY	MCLK_SOC Duty Cycle	45	–	55	%	
SID447	TJITTER	MCLK_SOC Input Jitter	–100	–	100	ps	

Table 38. Smart I/O Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID420	SMIO_BYP	Smart I/O Bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay	–	TBD	–	ns	–

Table 39. BLE Subsystem Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
BLE Sub-system Specifications							
RF Receiver Specification (1 Mbps)							
SID317R	RXS, IDLE	RX Sensitivity with Ideal Transmitter	–	–95	–	dBm	Across RF Operating Frequency Range
SID317RR	RXS, IDLE	RX Sensitivity with Ideal Transmitter	–	–93	–	dBm	255-byte Packet Length, Across Frequency Range
SID318R	RXS, DIRTY	RX Sensitivity with Dirty Transmitter	–	–92	–	dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID319R	PRXMAX	Maximum received signal strength at < 0.1% PER	–	0	–	dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID320R	CI1	Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX	–	9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID321R	CI2	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz	–	3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID322R	CI3	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz	–	–29	–17	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID323R	CI4	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz	–	–39	–27	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID324R	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE)	–	–20	–9	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID325R	CI6	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz)	–	–30	–15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
RF Receiver Specification (2 Mbps)							
SID326	RXS,IDLE	RX Sensitivity with Ideal Transmitter		–92		dBm	Across RF Operating Frequency Range
SID326R	RXS,IDLE	RX Sensitivity with Ideal Transmitter		–90		dBm	255-byte packet length, across Frequency Range
SID327	RXS,DIRTY	RX Sensitivity with Dirty Transmitter		–89		dBm	RF-PHY Specification (RCV-LE/CA/01/C)
SID328R	PRXMAX	Maximum received signal strength at < 0.1% PER		0		dBm	RF-PHY Specification (RCV-LE/CA/06/C)
SID329R	CI1	Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX		9	21	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID330	CI2	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz		3	15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID331	CI3	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 4 MHz		–29	–17	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID332	CI4	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 6 MHz		–39	–27	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID333	CI5	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE)		–20	–9	dB	RF-PHY Specification (RCV-LE/CA/03/C)
SID334	CI6	Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 2 MHz)		–30	–15	dB	RF-PHY Specification (RCV-LE/CA/03/C)
RF Receiver Specification (1 and 2 Mbps)							

Table 39. BLE Subsystem Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID338	OBB1	Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F = 30-2000 MHz	–30	–27		dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID339	OBB2	Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F = 2003-2399 MHz	–35	–27		dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID340	OBB3	Out of Band Blocking, Wanted Signal at –67 dBm and Interferer at F= 2484-2997 MHz	–35	–27		dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID341	OBB4	Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F= 3000-12750 MHz	–30	–27		dBm	RF-PHY Specification (RCV-LE/CA/04/C)
SID342	IMD	Intermodulation Performance Wanted Signal at –64 dBm and 1 Mbps BLE, 3rd, 4th and 5th offset channel	–50			dBm	RF-PHY Specification (RCV-LE/CA/05/C)
SID343	RXSE1	Receiver Spurious emission 30 MHz to 1.0 GHz			–57	dBm	100 kHz measurement bandwidth ETSI EN300 328 V1.8.1
SID344	RXSE2	Receiver Spurious emission 1.0 GHz to 12.75 GHz			–54	dBm	1 MHz measurement bandwidth ETSI EN300 328 V1.8.1
RF Transmitter Specifications							
SID345	TXP,ACC	RF Power Accuracy	–1	–	1	dB	–
SID346	TXP,RANGE	Frequency Accuracy		24		dB	–20 dBm to +4 dBm
SID347	TXP,0dBm	Output Power, 0 dB Gain setting		0		dBm	–
SID348	TXP,MAX	Output Power, Maximum Power Setting		4		dBm	–
SID349	TXP,MIN	Output Power, Minimum Power Setting		–20		dBm	–
SID350	F2AVG	Average Frequency deviation for 10101010 pattern	185			kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID350R	F2AVG_2M	Average Frequency deviation for 10101010 pattern for 2 Mbps	370			kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID351	F1AVG	Average Frequency deviation for 11110000 pattern	225	250	275	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID351R	F1AVG_2M	Average Frequency deviation for 11110000 pattern for 2 Mbps	450	500	550	kHz	RF-PHY Specification (TRM-LE/CA/05/C)
SID352	EO	Eye opening = ΔF2AVG/ΔF1AVG	0.8				RF-PHY Specification (TRM-LE/CA/05/C)
SID353	FTX, ACC	Frequency Accuracy	–150		150	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID354	FTX, MAXDR	Maximum Frequency Drift	–50		50	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID355	FTX, INITDR	Initial Frequency drift	–20		20	kHz	RF-PHY Specification (TRM-LE/CA/06/C)
SID356	FTX, DR	Maximum Drift Rate	–20		20	kHz/ 50 µs	RF-PHY Specification (TRM-LE/CA/06/C)
SID357	IBSE1	In Band Spurious Emission at 2 MHz offset (1 Mbps) In Band Spurious Emission at 4 MHz offset (2 Mbps)			–20	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID358	IBSE2	In Band Spurious Emission at ≥ 3 MHz offset (1 Mbps) In Band Spurious Emission at ≥ 6 MHz offset (2 Mbps)			–30	dBm	RF-PHY Specification (TRM-LE/CA/03/C)
SID359	TXSE1	Transmitter Spurious Emissions (Averaging), <1.0 GHz			–55.5	dBm	FCC-15.247

Table 39. BLE Subsystem Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID360	TXSE2	Transmitter Spurious Emissions (Averaging), >1.0 GHz			–41.5	dBm	FCC-15.247
RF Current Specifications							
SID361	IRX1_wb	Receive Current (1 Mbps)		4.4		mA	AVIN/PVIN and VIO current with buck
SID362	ITX1_wb_0dBm	TX Current at 0 dBm setting (1 Mbps)		4.2		mA	AVIN/PVIN and VIO current with buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID363	IRX1_nb	Receive Current (1 Mbps)		9.5		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID364	ITX1_nb_0dBm	TX Current at 0 dBm setting (1 Mbps)		9		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID365	ITX1_nb_4dBm	TX Current at 4 dBm setting (1 Mbps)		13		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID365R	ITX1_wb_4dBm	TX Current at 4 dBm setting (1 Mbps)		6.5		mA	AVIN/PVIN and VIO current with buck (AVIN/PVIN=1.8 V, VIO=1.8 V)
SID366	ITX1_nb_20dBm	TX Current at –20 dBm setting (1 Mbps)		7		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID367	IRX2_wb	Receive Current (2 Mbps)		4.4		mA	AVIN/PVIN and VIO current with buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID368	ITX2_wb_0dBm	TX Current at 0 dBm setting (2 Mbps)		4.2		mA	AVIN/PVIN and VIO current with buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID369	IRX2_nb	Receive Current (2 Mbps)		9.5		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID370	ITX2_nb_0dBm	TX Current at 0 dBm setting (2 Mbps)		9		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID371	ITX2_nb_4dBm	TX Current at 4 dBm setting (2 Mbps)		13		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID371R	ITX2_wb_4dBm	TX Current at 4 dBm setting (2 Mbps)		6.5		mA	AVIN/PVIN and VIO current with buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
SID372	ITX2_nb_20dBm	TX Current at –20 dBm setting (2 Mbps)		7		mA	AVIN/PVIN and VIO current without buck (AVIN/PVIN = 1.8 V, VIO = 1.8 V)
General RF Specifications							
SID373	FREQ	RF operating frequency	2400		2482	MHz	–
SID374	CHBW	Channel spacing		2		MHz	–
SID375	DR1	On-air Data Rate (1 Mbps)		1000		Kbps	–

Table 39. BLE Subsystem Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID376	DR2	On-air Data Rate (2 Mbps)		2000		Kbps	–
SID377	TXSUP	Transmitter Startup time		80	82	µs	–
SID378	RXSUP	Receiver Startup time		80	82	µs	–
RSSI Specifications							
SID379	RSSI,ACC	RSSI Accuracy	–4	–	4	dB	–
SID380	RSSI,RES	RSSI Resolution		1		dB	–
SID381	RSSI,PER	RSSI Sample Period		6		µs	–
System Level BLE Specifications							
SID433R	Adv_Pwr	1.28s, 32 bytes, 0 dBm		21		µW	3.3 V, Buck, w/o Deep Sleep current
SID434R	Conn_Pwr_300	300 ms, 0 byte, 0 dBm		33		µW	3.3 V, Buck, w/o Deep Sleep current
SID435R	Conn_Pwr_1S	1000 ms, 0 byte, 0 dBm		10		µW	3.3 V, Buck, w/o Deep Sleep current
SID436R	Conn_Pwr_4S	4000 ms, 0 byte, 0 dBm		3		µW	3.3 V, Buck, w/o Deep Sleep current

Table 40. ECO Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
16-MHz Crystal Oscillator							
SID382	FXO1	Crystal frequency	–	16	–	MHz	–
SID383	ESR1	Equivalent series resistance	–	100	250	Ω	–
SID384	Txostart1	Startup time	–	400	–	µs	Frequency Stable (16 MHz ±50 ppm)
SID385	IXO1	Operating current	–	200	300	µA	Include crystal current, LDO and BG
32-MHz Crystal Oscillator							
SID386	FXO2	Crystal frequency	–	32		MHz	–
SID387	ESR2	Equivalent series resistance	–	50	100	Ω	–
SID388	Txostart2	Startup time	–	400	–	µs	Frequency Stable (32 MHz ±50 ppm)
SID389	IXO2	Operating current	–	300	400	µA	Include crystal current, LDO and BG
16-MHz and 32-MHz Crystal Oscillator							
SID390	FTOL	Frequency tolerance	–20	–	20	ppm	After trimming, including aging and temp drift
SID391	PD	Drive level	–	–	100	µW	–

Table 41. Precision ILO (PILO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID 430R	IPILO	Operating current	–	1.2	4	µA	–
SID431	F_PILO	PILO nominal frequency	–	32768	–	Hz	T = 25 °C with 20-ppm crystal
SID432R	ACC_PILO	PILO accuracy with periodic calibration	–250	–	250	ppm	–

Ordering Information

Table 43 lists the PSoC 63 part numbers and features. The following table shows Marketing Part Numbers (MPNs) for products including the BLE Radio. The packages are the 104 M CSP, and the 116 BGA.

Table 42. BLE Series Part Numbers

MPN	CPU Speed (M4)	CPU Speed (M0+)	Single core/Dual core	ULP/LP	Flash	SRAM	No of CTBMs	No of UDBs	CapSense	GPIOs	CRYPTO	Package
CY8C6336BZI-BLF03	150	–	Single	LP	512	160	0	0	No	78	No	116-BGA
CY8C6316BZI-BLF03	50	–	Single	ULP	512	160	0	0	No	78	No	116-BGA
CY8C6316BZI-BLF53	50	–	Single	ULP	512	160	1	12	Yes	78	Yes	116-BGA
CY8C6337BZI-BLF13	150	–	Single	LP	1024	288	0	0	Yes	78	No	116-BGA
CY8C6336BZI-BLD13	150	100	Double	LP	512	160	0	0	Yes	78	No	116-BGA
CY8C6347BZI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	78	Yes	116-BGA
CY8C6347BZI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	No	116-BGA
CY8C6347BZI-BLD54	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	78	Yes	116-BGA
CY8C6347FMI-BLD13	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	No	104-MCSP
CY8C6347FMI-BLD43	150/50	100/25	Double	FLEX	1024	288	0	0	Yes	70	Yes	104-MCSP
CY8C6347FMI-BLD33	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	No	104-MCSP
CY8C6347FMI-BLD53	150/50	100/25	Double	FLEX	1024	288	1	12	Yes	70	Yes	104-MCSP

Table 43 lists the field values.

Table 43. MPN Nomenclature

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
6	Architecture	6	PSoC 6
A	Family	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
B	Speed	1	50 MHz
		2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Flash Capacity	4	128 KB
		5	256 KB
		6	512 KB
		7	1024 KB
D	Package Code	AX	TQFP I (0.8 mm pitch)
		AZ	TQFP II (0.5 mm pitch)
		LQ	QFN
		BZ	BGA
		FM	M-CSP
E	Temperature Range	C	Consumer
		I	Industrial
		Q	Extended Industrial (105 °C)
F	Silicon Family	N/A	PSoC 6A
		S	PSoC 6A-S (Example)
		M	PSoC 6A-M (Example)
		L	PSoC 6A-L (Example)
		BL	PSoC 6A-BLE
G	Core	Z	M0+
		F	M4
		D	Dual-Core M4/M0+
XY	Attributes Code	00-99	Code of feature set in the specific family
ES	Engineering sample	ES	Engineering samples or not
T	Tape/Reel Shipment	T	Tape and Reel shipment or not

Packaging

PSoC 63 will be offered in two packages: 116-BGA and 104-MCSP.

Table 44. Package Dimensions

Spec ID	Package	Description	Package Drawing Number
PKG_2	104-MCSP	104-MCSP, 3.8 × 5 × 0.65 mm height with 0.35-mm pitch	002-16508
PKG_4	116-BGA	116-BGA, 5.2 × 6.4 × 0.5 mm height with 0.5-mm pitch	002-16574

Table 45. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25.00	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (116-BGA)	–	–	36	–	°C/watt
T_{JC}	Package θ_{JC} (116-BGA)	–	–	12	–	°C/watt
T_{JA}	Package θ_{JA} (104-CSP)	–	–	34	–	°C/watt

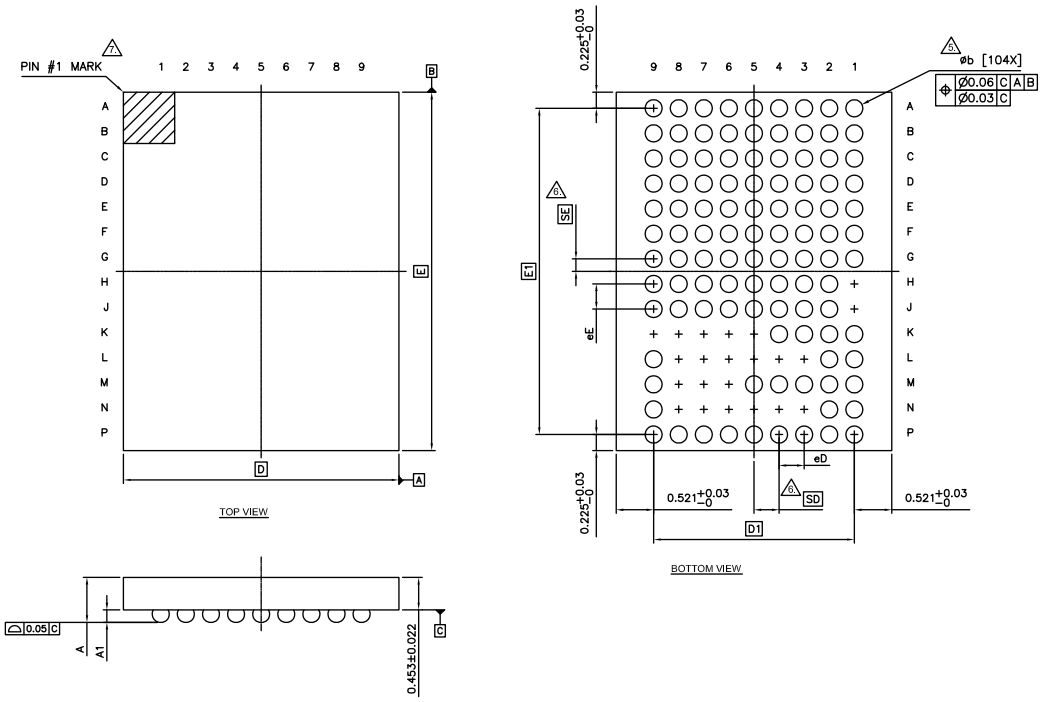
Table 46. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
116-BGA	260 °C	30 seconds
104-MCSP	260 °C	30 seconds

Table 47. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
116-BGA	MSL 3
104-MCSP	MSL 3

Figure 3. 104-WLCSP 3.8 × 5.0 × 0.65 mm

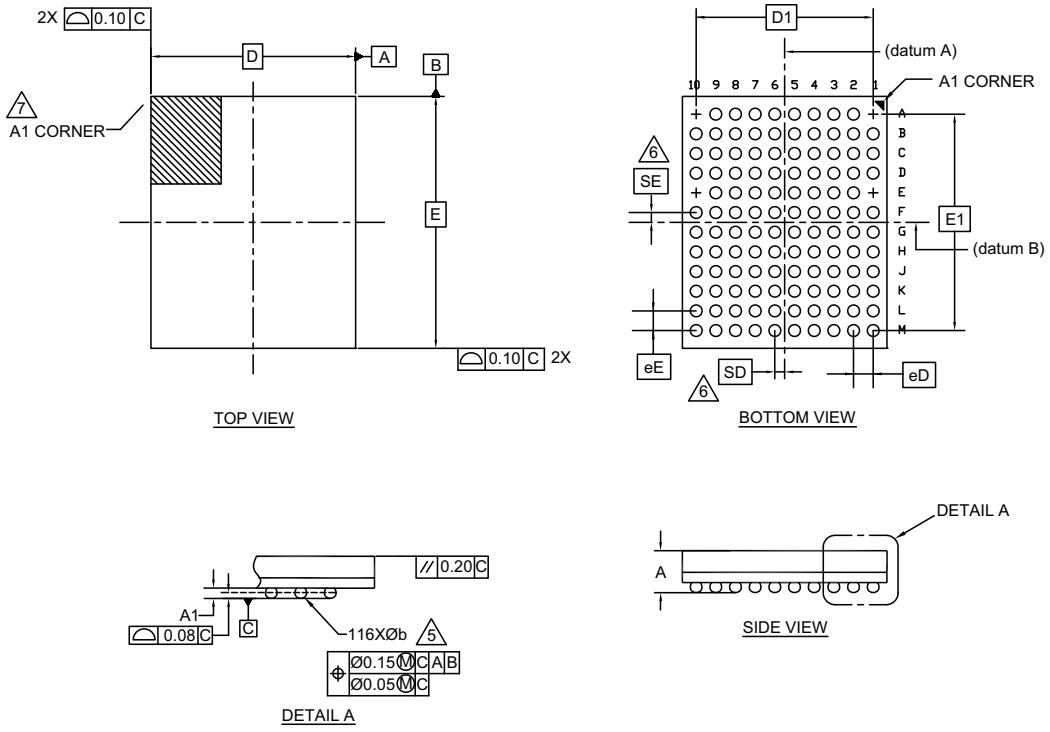


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.650
A1	0.158	0.176	0.194
D	3.791	3.841	3.891
E	4.95	5.00	5.05
D1	2.80 BSC		
E1	4.55 BSC		
MD	9		
ME	14		
N	104		
Ø b	0.208	0.238	0.268
eD	0.335	0.350	0.365
eE	0.335	0.350	0.365
SD	0.35 BSC		
SE	0.175 BSC		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-16508 *B

Figure 4. 116-BGA 5.2 × 6.4 × 0.75 mm



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.70
A1	0.16	0.21	0.26
D		5.20 BSC	
E		6.40 BSC	
D1		4.50 BSC	
E1		5.50 BSC	
MD		10	
ME		12	
N		116	
Ø b	0.25	0.30	0.35
eD		0.50 BSC	
eE		0.50 BSC	
SD		0.25 BSC	
SE		0.25 BSC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF: N/A

002-16574 *A

Acronyms

Table 48. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 48. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter

Table 48. Acronyms Used in this Document *(continued)*

Acronym	Description
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer

Table 48. Acronyms Used in this Document *(continued)*

Acronym	Description
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 49. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Errata

This section describes the errata for the currently sampling PSoC 6 product family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY8C6XX	PSoC 6 MCU

PSoC 6X Qualification Status

Engineering Samples

PSoC 6X Errata Summary

This table defines the errata applicability to available PSoC 6X devices.

Items	CY8C6XX	Silicon Revision	Fix Status
[1]. 124 BGA: SIMO Buck operation at VDDD input voltage >2.7 V	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[2]. Deep Sleep current not meeting spec	All	Rev. *A	No fix planned.
[3]. UDB Deep Sleep retention	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[4].116 BGA: HBM ESD rating	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[5]. Wake-up time from Deep Sleep interrupt to first execution from IMO	All	Rev. *A	No fix planned.
[6]. Frequency-Locked-Loop (FLL) wakeup time from Deep Sleep	All	Rev. *A	No fix planned.
[7]. Flash Read-While-Write (RWW) feature does not work	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[8]. Flash RWW feature requires blocking for 1 ms when Writes to the Emulated EEPROM Sector (32 KB Sector) are done	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[9]. CMAC-based authentication of Boot Flash code in Supervisory Flash can be spoofed	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[10]. Protection Context (PC) is not restored properly in system calls that inherit the Client's PC.	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.
[11]. Hard Fault results if two system calls occur simultaneously and the first system call inherits a non-zero Context.	All	Rev. *A	Silicon fix planned in next silicon. Current sample date is Q4 2017.

1. 124 BGA: SIMO Buck operation at V_{DDD} input voltage >2.7 V

■ **Problem Definition**

SIMO Buck efficiency operates with very low efficiency for V_{DDD} >2.7 V

■ **Parameters Affected**

Power consumption

■ **Trigger Condition(s)**

V_{DDD} > 2.7 V

■ **Scope of Impact**

Power consumption increases above 2.7 V when using the Buck

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

2. Deep Sleep current not meeting spec

■ **Problem Definition**

Deep Sleep current does not meet the spec; it is 7 µA versus spec of 4.5 µA (64-KB SRAM retained) and 9 µA vs spec of 7 µA (256-KB SRAM retained).]

■ **Parameters Affected**

Deep Sleep current

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

Deep Sleep current budget will be higher

■ **Workaround**

None

■ **Fix Status**

No fix is planned

3. UDB Deep Sleep retention

■ **Problem Definition**

GPIOs driven from the UDB circuit may fail to maintain state after wakeup from Deep Sleep.

■ **Parameters Affected**

GPIO states if driven by UDBs

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

Erroneous logic states may occur transiently for outputs controlled by UDB logic after wakeup from Deep Sleep.

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

4. 116 BGA: HBM ESD rating

■ **Problem Definition**

HBM ESD is rated at 1600 V versus spec of 2200 V on the 116 BGA package.

■ **Parameters Affected**

HBM ESD rating on the 116 BGA package

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

HBM spec of 2000 V not met for the 116 BGA package

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error is expected to be removed from the datasheet

5. Wake-up time from Deep Sleep interrupt to first execution from IMO

■ **Problem Definition**

Wakeup time from Deep Sleep interrupt to firmware execution is 21 µs instead of 11 µs.

■ **Parameters Affected**

Time from Deep Sleep wakeup to firmware execution

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

Longer Deep Sleep wakeup time

■ **Workaround**

None

■ **Fix Status**

No fix planned

6. Frequency-Locked-Loop (FLL) wakeup time from Deep Sleep

■ **Problem Definition**

Time from Deep Sleep wakeup to execution from FLL is 26 µs instead of 15 µs.

■ **Parameters Affected**

Time from Deep Sleep wakeup to firmware execution from FLL

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

Longer Deep Sleep wakeup time to firmware execution from FLL

■ **Workaround**

None

■ **Fix Status**

No fix planned

7. Flash Read-While-Write (RWW) feature does not work

■ **Problem Definition**

Reading from one Flash Sector while writing to another is non-functional.

■ **Parameters Affected**

NA

■ **Trigger Condition(s)**

Attempting to read from a Flash address while Flash is being written to.

■ **Scope of Impact**

Attempting to use the RWW feature will cause Hard Faults.

■ **Workaround**

Use Blocking calls for System API functions. DMA/Data-Wire, Crypto, and SMIF (QSPI) blocks are bus masters and must be disabled while the Blocking call is underway if they make any Flash accesses. Basically, there must be no Flash access before the Blocking call is completed. There is a partial workaround for a special case described in the next item.

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

8. Flash RWW feature requires blocking for 1 ms when Writes to the Emulated EEPROM Sector (32 KB Sector) are done

■ **Problem Definition**

Writing to the 32-KB Flash Sector while attempting to read Flash before 1 ms from the beginning of the Write does not work.

■ **Parameters Affected**

NA

■ **Trigger Condition(s)**

Attempting to read from a Flash address less than 1 ms after the beginning of a write to the 32-KB Flash sector.

■ **Scope of Impact**

Attempting to read from Flash less than 1 ms after the beginning of a write to the 32-KB sector will cause Hard Faults.

■ **Workaround**

DMA/Data-Wire, Crypto, and SMIF (QSPI) blocks are bus masters and must be disabled for a period of 1 ms after the call is made if they access Flash. Basically, there must be no Flash access for a period of 1 ms after a write to the 32-KB Sector is initiated. This workaround allows BLE connectivity to be maintained when the 32-KB sector is used for writing pairing information.

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

9. CMAC-based authentication of Boot Flash code in Supervisory Flash can be spoofed

■ **Problem Definition**

CMAC is used to verify authenticity of the Boot Flash but the AES key can be made visible and the integrity of the Message Authentication is compromised.

■ **Parameters Affected**

NA

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

The AES Key is stored in SROM and can be read out in parts, which are in the normal life cycle stage mode. This will be replaced by a Secure Hash Authentication (SHA) method, which does not use a key.

■ **Workaround**

None

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

10.Protection Context (PC) is not restored properly in system calls that inherit the Client's PC.

■ **Problem Definition**

Some System calls can inherit the client's Protection Context (PC); the PC is restored on completion of the call except for the inheritance of PC 0.

■ **Parameters Affected**

NA

■ **Trigger Condition(s)**

NA

■ **Scope of Impact**

Protection context can be changed inadvertently causing access failures.

■ **Workaround**

For System Calls that inherit the Client's Protection Context (PC), PC_SAVED must be Set to 0 if the previous Protection Context was PC0. The CM0+ must be used in Protection Context 0.

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

11.Hard Fault results if two system calls occur simultaneously and the first system call inherits a non-zero Context.

■ **Problem Definition**

If two system calls are made simultaneously, the NMI Handler will try to service the second system call as well before returning. If the first system call inherited a non-zero Protection Context, then the second call will cause a Hard Fault if tries to access a protected region.

■ **Parameters Affected**

NA

■ **Trigger Condition(s)**

Back-to-back system calls with the first call inheriting a non-zero Protection Context.

■ **Scope of Impact**

Protection context can be changed inadvertently causing access failures.

■ **Workaround**

Workaround is to use an IPC channel to make sure that the first system call is completed before making the next call.

■ **Fix Status**

Silicon and/or firmware fix is planned in Q4 2017 when this error will be removed from the datasheet.

Revision History

Description Title: PSoC® 6 MCU: PSoC 63 with BLE Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 002-18787				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5660056	WKA	04/28/2017	New datasheet
*A	5826280	WKA	07/20/2017	Updated Power System and Timer/Counter/PWM Block sections. Updated Table 4, Table 7, Table 18, and Table 24. Updated SID420 max value. Updated Table 39 Conditions. Removed SID335, SID336, and SID337. Updated Ordering Information.
*B	5896512	WKA	09/27/2017	Changed PSoC 63BL references throughout the document to PSoC 63. Updated Deep Sleep mode current. Updated 32-kHz ILO accuracy ratio. Updated Power section. Updated Table 3, Table 4, Table 5, Table 7, Table 13, Table 14, Table 15, Table 18, and Table 37. Updated SID180S, SID237, and SID396Q spec values. Updated Conditions for SID454. Removed WCO Specifications. Updated Ordering Information. Added Errata.

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