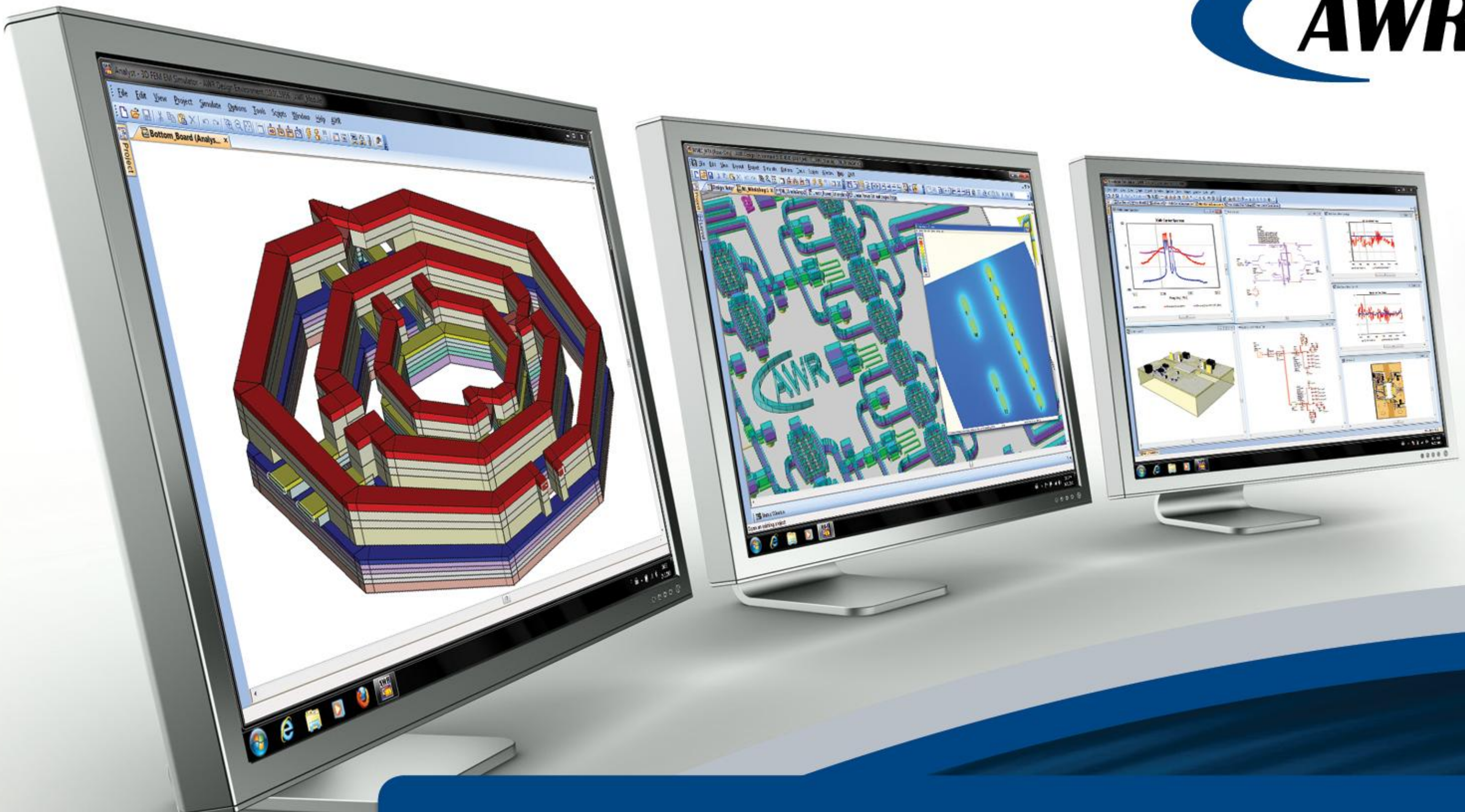
RF and Microwave Amplifier Power Added Efficiency, Fact and Fiction

Dr. Dominic FitzPatrick

Principal Consultant, PoweRFul Microwave

www.powerful-microwave.co.uk

AWR | A National Instruments Company™



AWR Corporation – A National Instruments Company

www.awrcorp.com

AWR - At a Glance

The Innovation Leader in High-Frequency EDA

Product Portfolio:

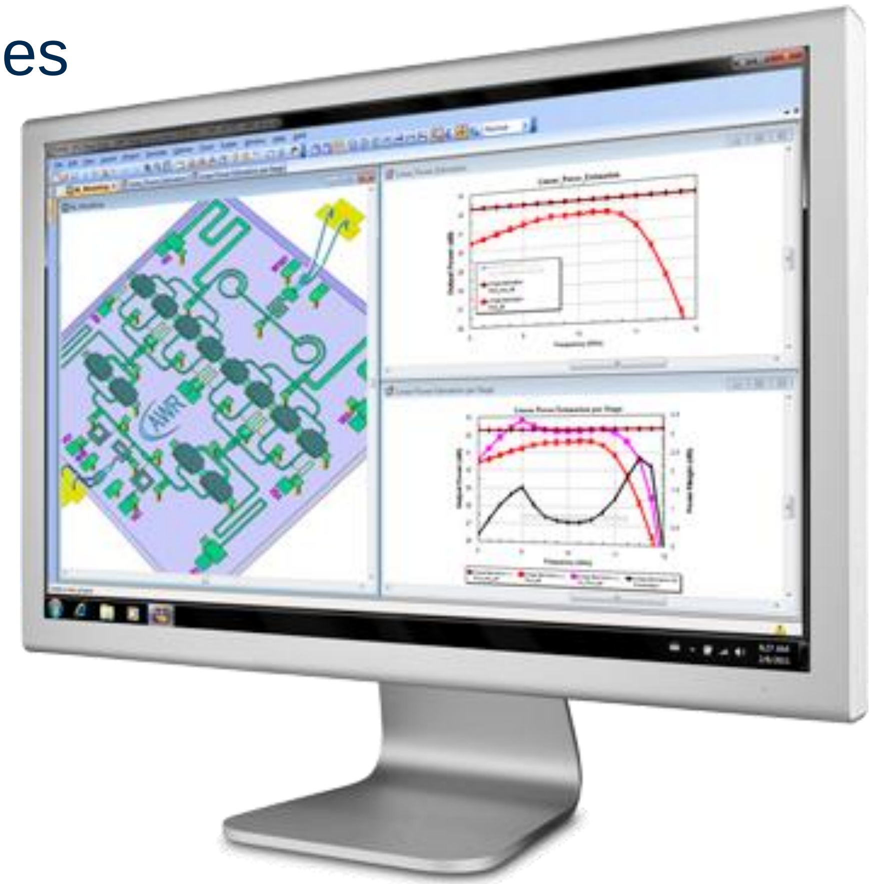
- Microwave Office™ - MMIC, RF PCB and module
- Visual System Simulator™ - Wireless comms/radar
- AXIEM® - 3D planar EM
- Analyst™ - 3D finite element method (FEM) EM
- Analog Office® - RFIC

Global Presence (direct offices)

- Los Angeles, California (headquarters)
- California, Wisconsin, Colorado
- United Kingdom and Finland
- Japan, Korea and China

RF and Microwave Design Software

- MMIC
- RF PCB
- Modules



Amplifier Technology Uses Microwave Office to Design High Performance Amplifiers While Cutting 50% Off Their Design Time

"Microwave Office has helped us characterize appropriate parameters for each prototype design, evaluate possible variants and simulate the device performance straight from the design stage. In my experience Microwave Office is the best design solution available on the market."

Paul Deacon
Senior RF Design Engineer
Amplifier Technology

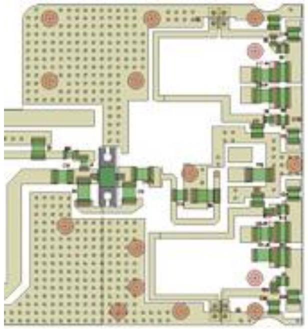
amplifier technology

Microwave Office for PA Design

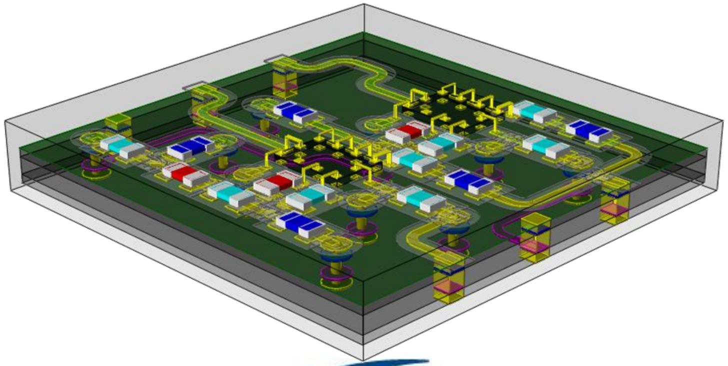
- Innovative Technology:
  - APLAC - Harmonic Balance
  - ACE - Circuit Extraction
  - AXIEM - Electromagnetics
- Flexible & Friendly Environment
  - Microsoft look-n-feel UI
  - Design concurrency
  - Plug-n-play sockets
    - ICED for DRC/LVS
    - EM for many
- Foundry Support: III/V PDKs
    - CREE, GCS, Northrop Grumman
    - OMMIC, RFMD, UMS
    - WIN & TriQuint

Photograph of the NDPA MMIC.

32-port AXIEM layout.



Microwave Office layout of the driver board for the 20MHz – 520MHz, 125W power amplifier.



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Cree: *the World's Largest Pure Play WBG Company*

Overview

- Founded in 1987
- Public since 1993 (Nasdaq: CREE)
- Headquartered in Durham, NC
- Strong patent portfolio

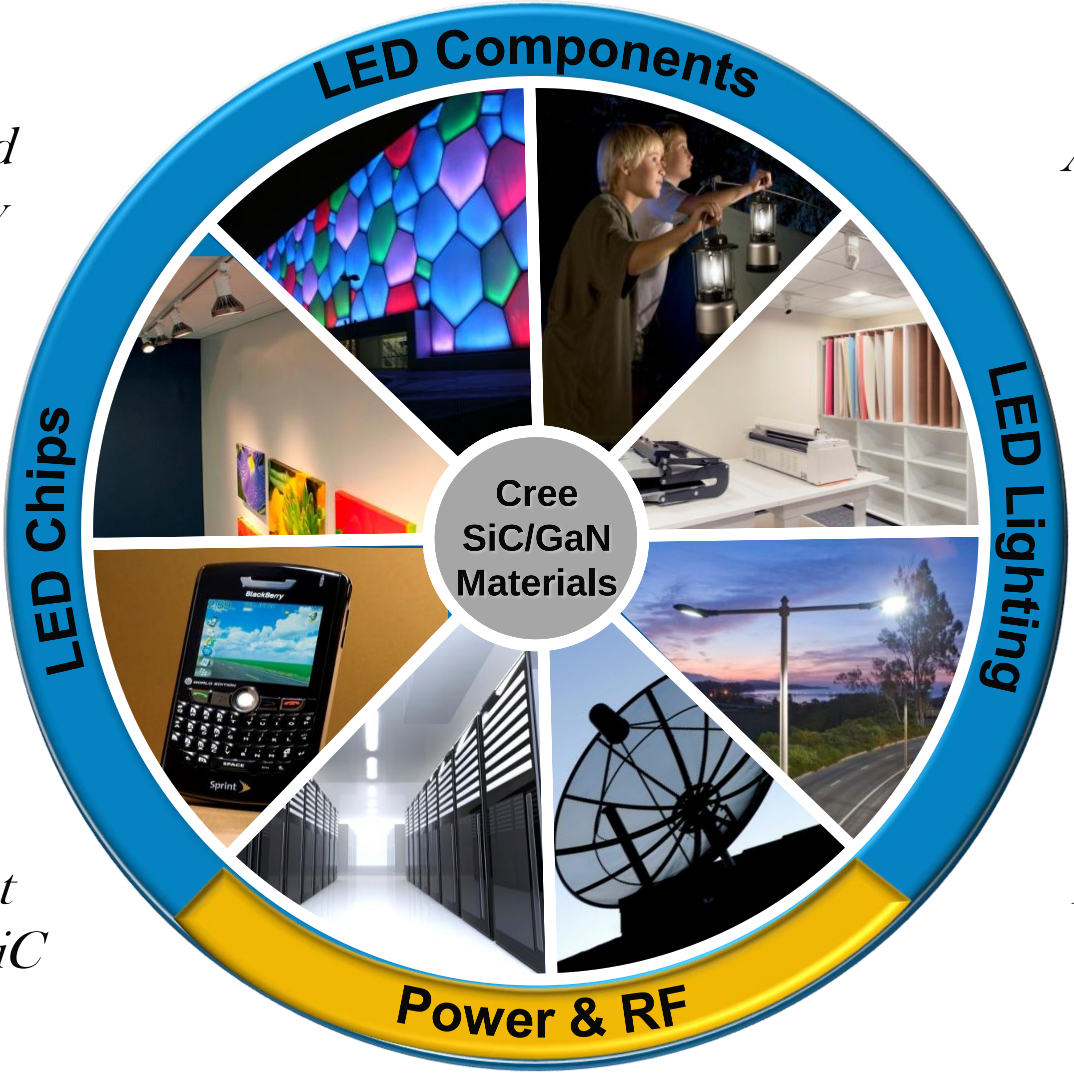
Global Reach

- 12 major locations
- 6000 employees
- Fiscal 2013 Revenues $1.4B

Cree businesses – *a leading player in each sector*

World record LED efficacy (lm/ W)

Award winning commercial lighting

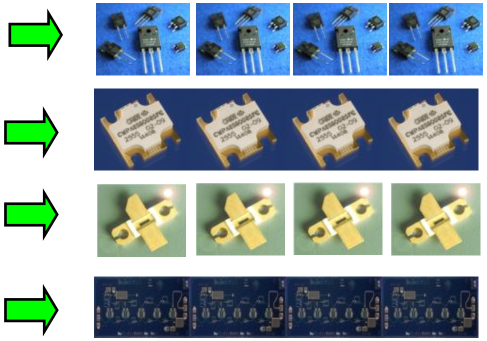


World 's first commercial SiC MOSFET

Leader in GaN RF Sales

Cree WBG Center of Excellence for Power and RF

Cree economies of scale



- Power SiC Products
- RF GaN MMICs
- RF GaN Transistors
- GaN Foundry Services

- Opened August 2006
- SiC and GaN RF and Power products
- World's largest dedicated WBG production device facility
  - Shared high volume Power and RF lines
  - Benefits from LED commercial infrastructure for volume SiC wafer and GaN epi supply
    - Billions of LEDs produced yearly
- Providing rapid cost reduction to industry "**economies of scale**"

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Power Added Efficiency – The Basics

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Specialists in RF and Microwave Amplifier Design

$$PAE = \frac{(RFP_{OUT} - RFP_{IN})}{DCP_{IN}}\%$$

Why is it important?

- ➢ *Smaller power supply, less current drawn*
  - ➢ *Smaller, lighter DC supply cables*
- ➢ *Less heat generated*
  - ➢ *Cooler running, higher reliability*
  - ➢ *Lower weight,*
  - ➢ *The higher the performance.*

But, it doesn't come for free; and it becomes harder to improve the efficiency the higher we go, i.e. 10% increase from 30-40% ✓ from 60-70% 😐 from 70-80% ☹

Power Added Efficiency – The Basics

$$PAE = \frac{(RFP_{OUT} - RFP_{IN})}{DCP_{IN}} \%$$

What does the equation mean?

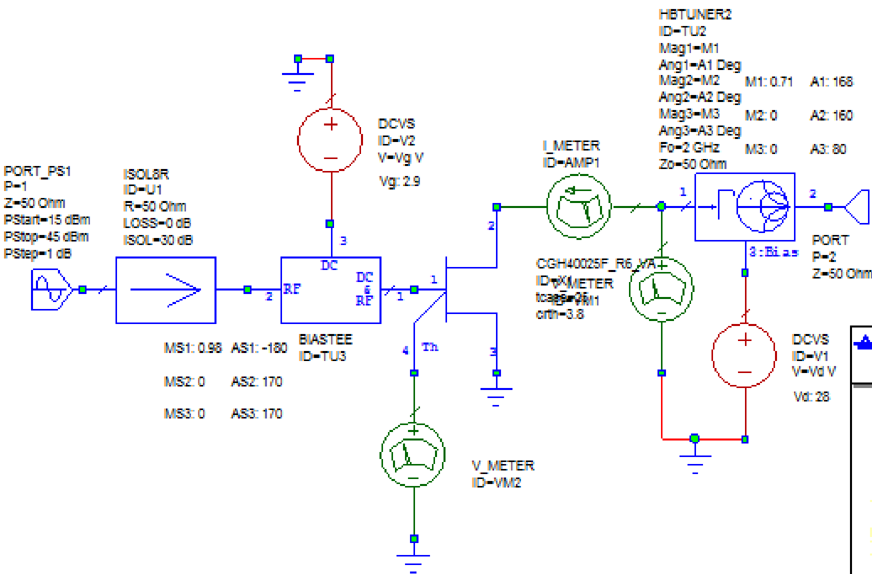
- *Note:- RFP_{IN} means 'IN' to the device, not the source power, i.e. better input match higher PAE?*
- *Higher gain, higher PAE – GaN advantage!*

Don't get confused with Drain Efficiency.

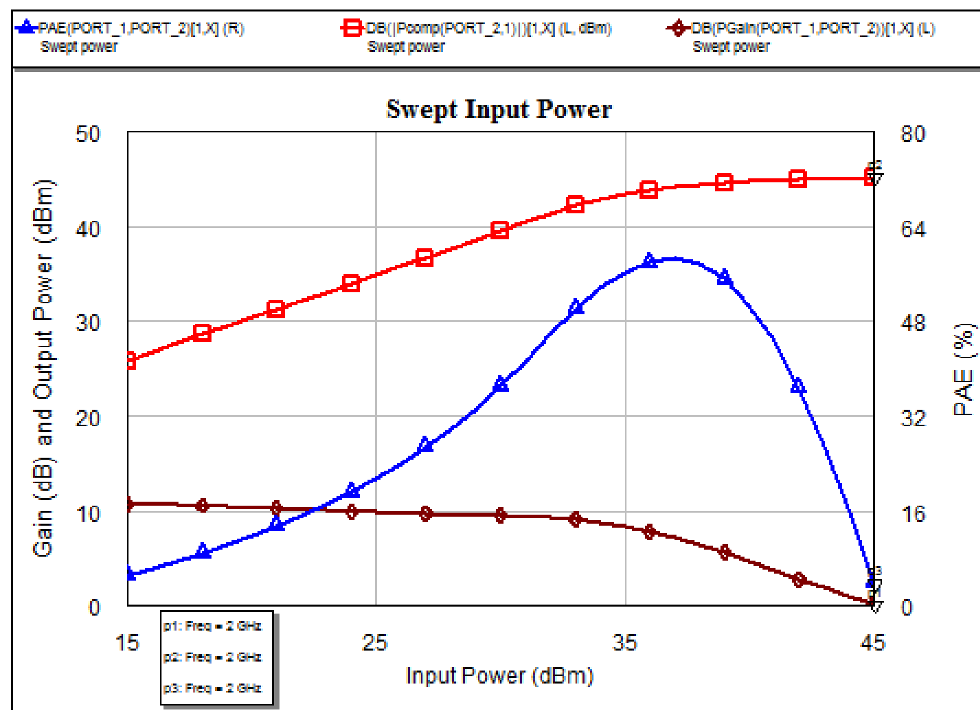
$$DE = \frac{RFP_{OUT}}{DCP_{IN}} \%$$

Is DE actually a useful measure without including the impact of gain?

Input & PAE

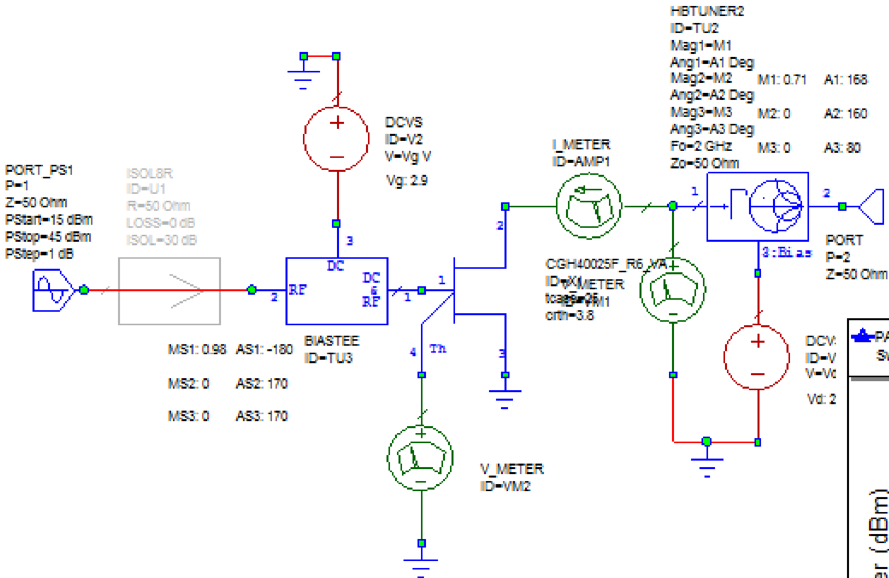


$$PAE = \frac{(RFP_{OUT} - RFP_{IN})}{DCP_{IN}} \%$$

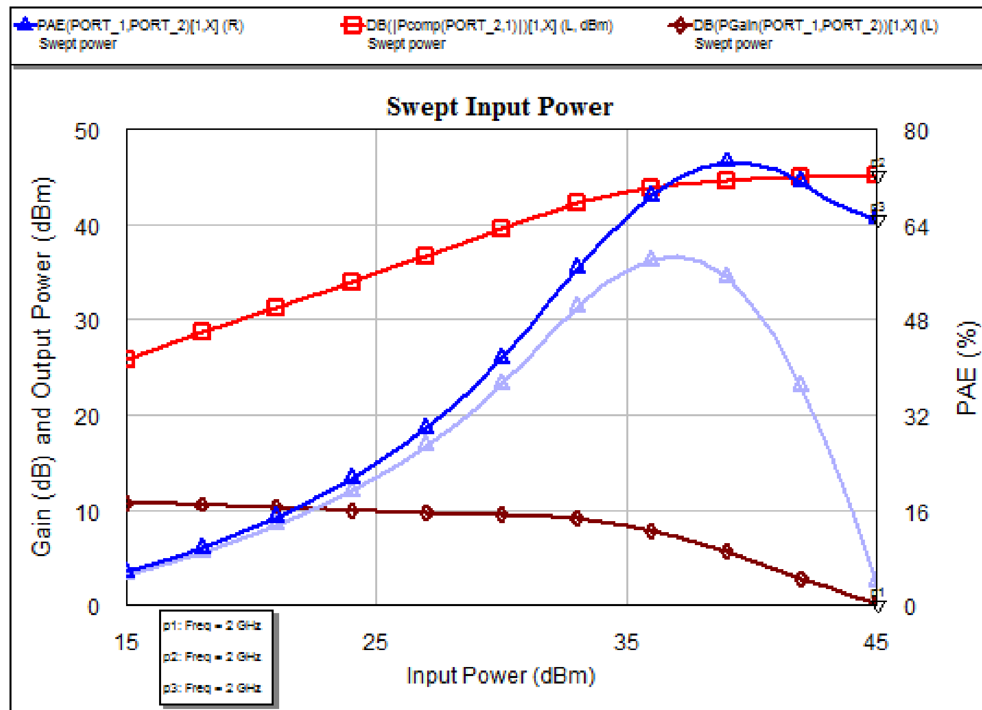


With the isolator no power is reflected back and so RFP_{IN} = source power. Higher RFP_{IN} lower PAE

Input & PAE



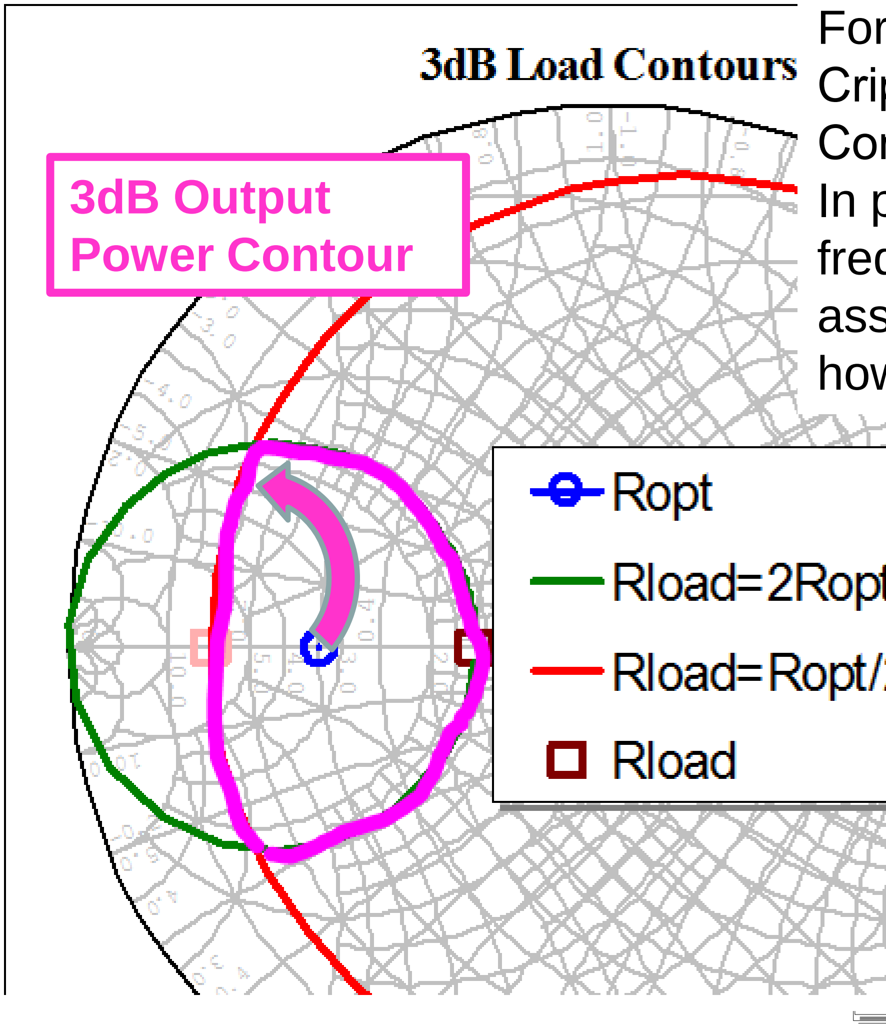
$$PAE = \frac{(RFP_{OUT} - RFP_{IN})}{DCP_{IN}} \, \%$$



Without the isolator the power reflected by the device is subtracted from source power to give RFP_{IN}.

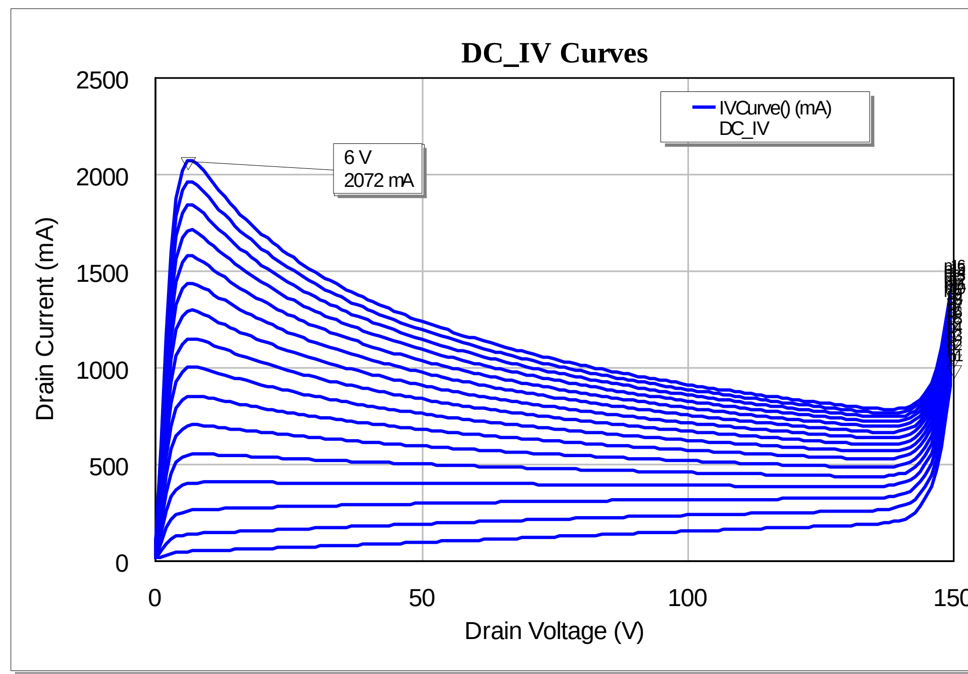
With the isolator no power is reflected back and so RFP_{IN} = source power. Higher RFP_{IN} lower PAE

Power Transfer

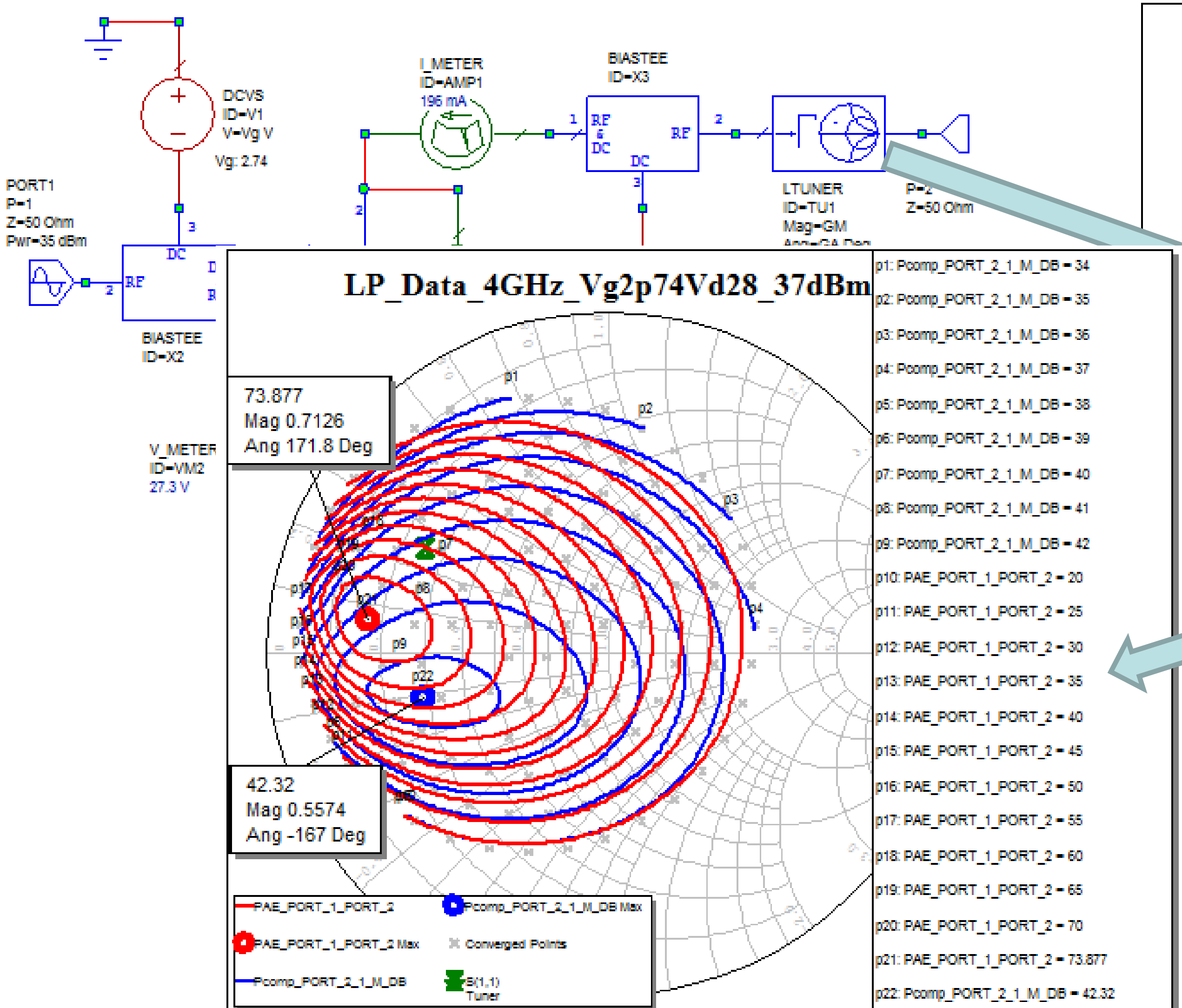


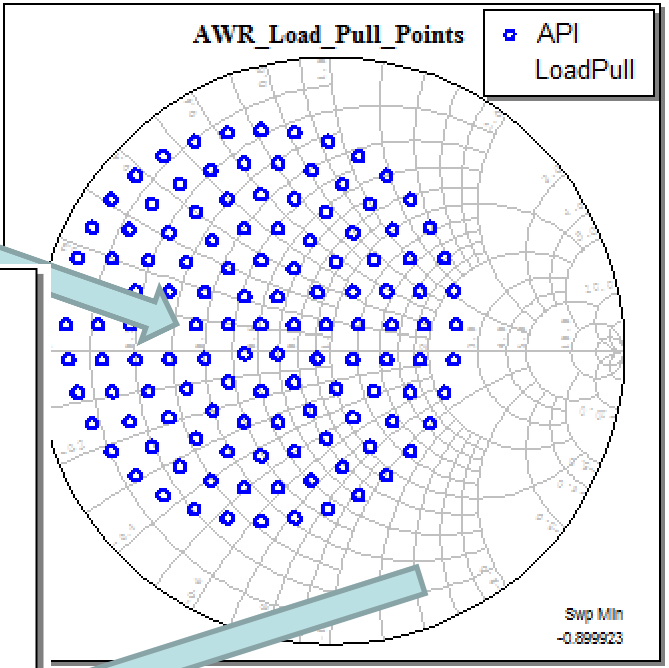
For mathematical proof of the contours see Cripps, “RF Power Amplifiers for Wireless Communications”.

In practice this would be tedious to do for every frequency, bias setting, drive level, etc. Also it assumes ideal DC-IV Curves in practice however:



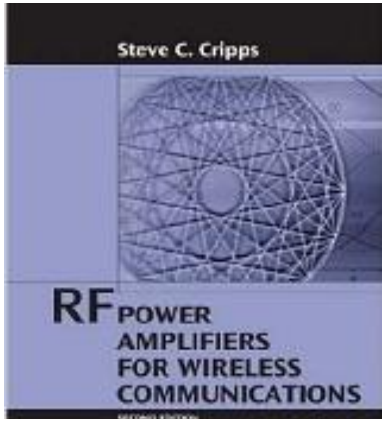
Power Transfer with a Nonlinear Model





Simulation at each load point produces performance contours, in this case of constant PAE (red) and Output Power (blue).

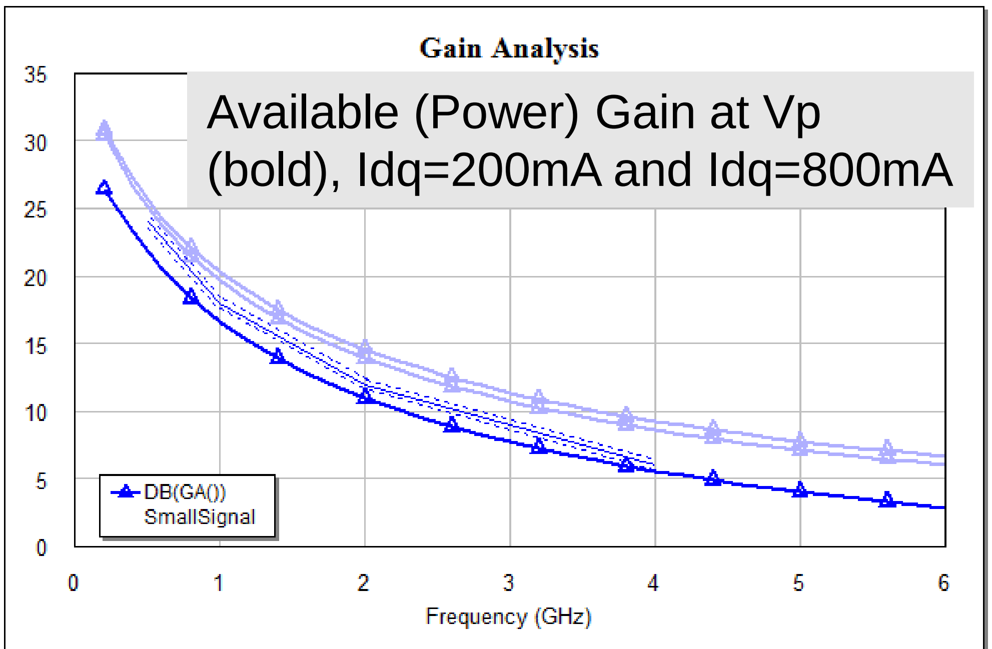
Bias

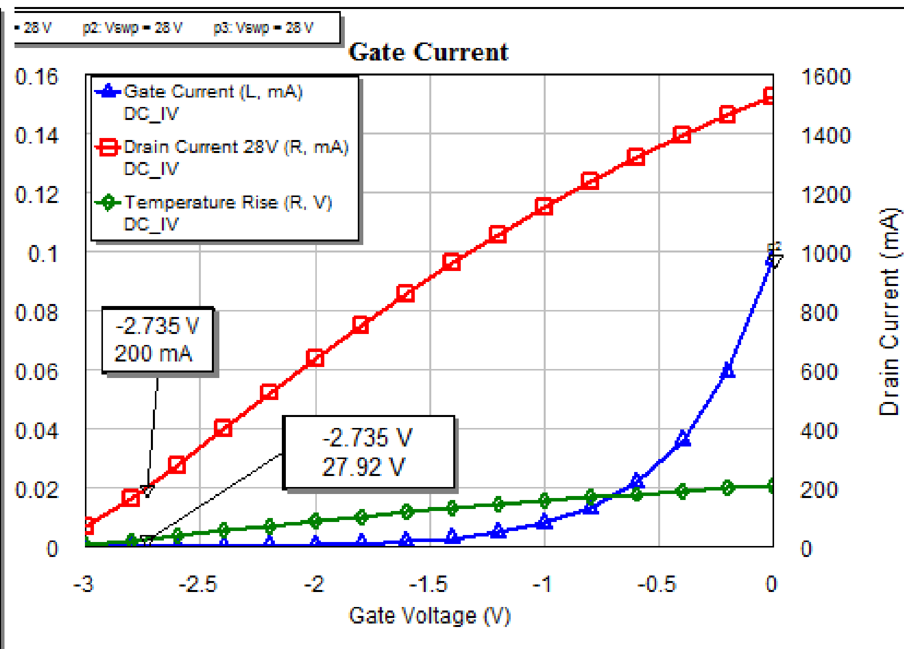


Not going to cover the theory of different classes of operation here

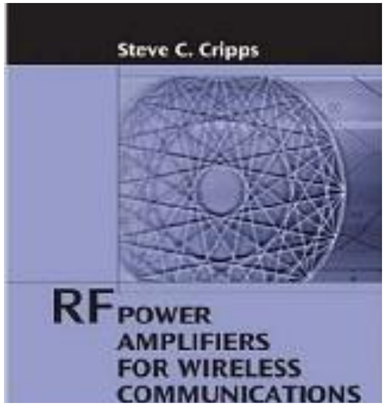
→ Already comprehensively covered such as by Prof. Steve Cripps.

But we will look at the effects of bias and remember that it is another variable open to use.





Bias



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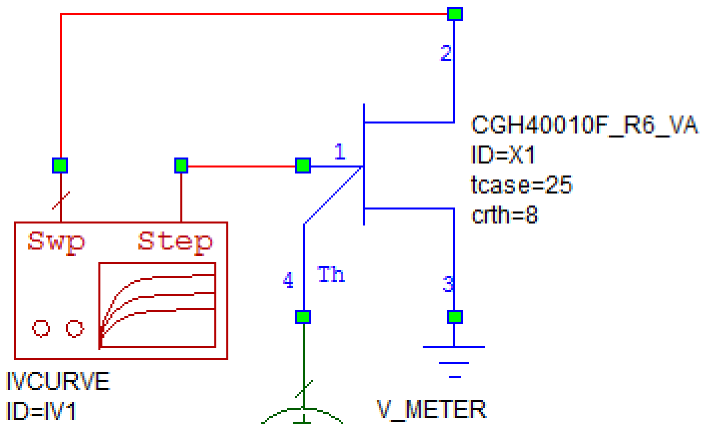
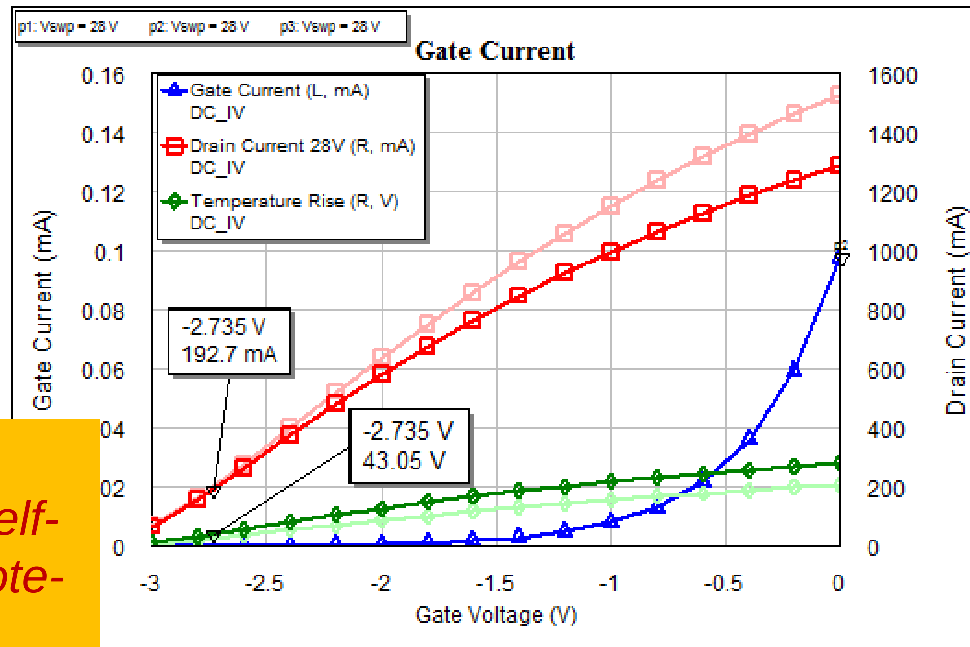


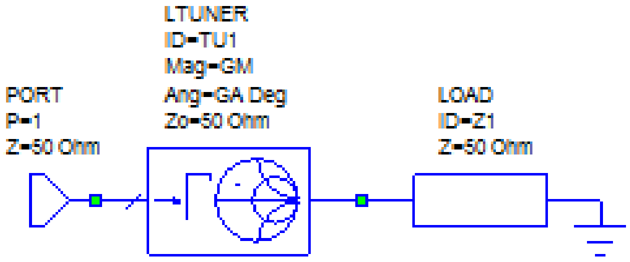


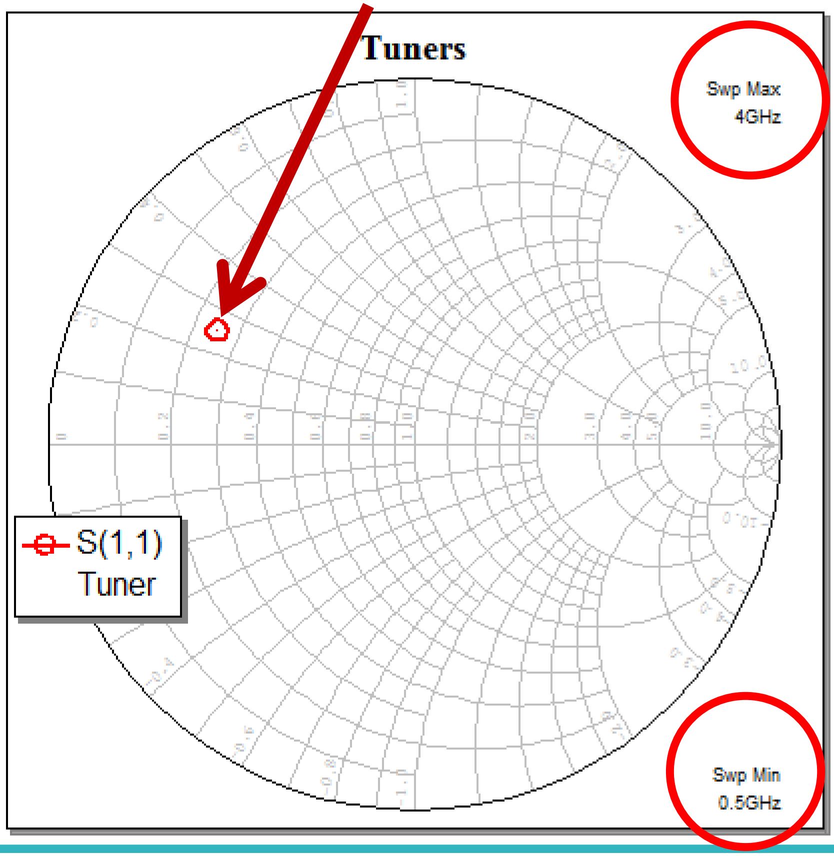
Thermal Optimization of GaN HEMT Transistor Power Amplifiers Using New Self-heating Large Signal Model, Cree-App-Note-006

Tuners – Be Wary

LTUNER – Nice and simple, but what impedance does it present at other frequencies?

LTUNER – All frequencies are terminated with the same load impedance, in this case |GM| /_GA°.





Tuners – Be Wary

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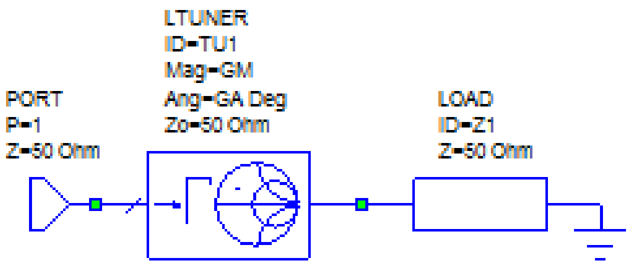
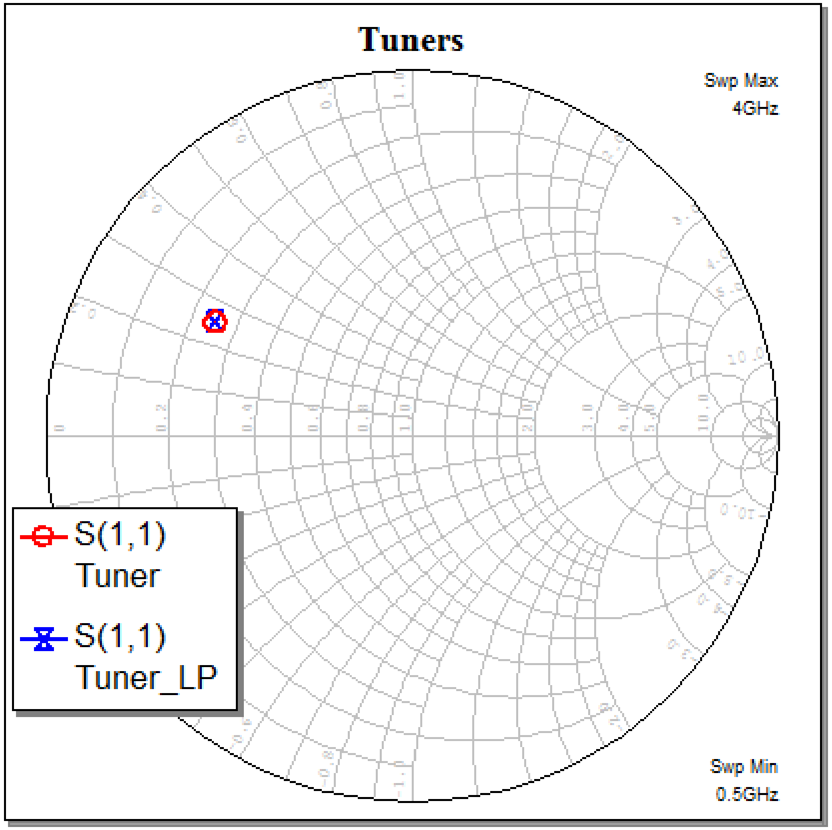
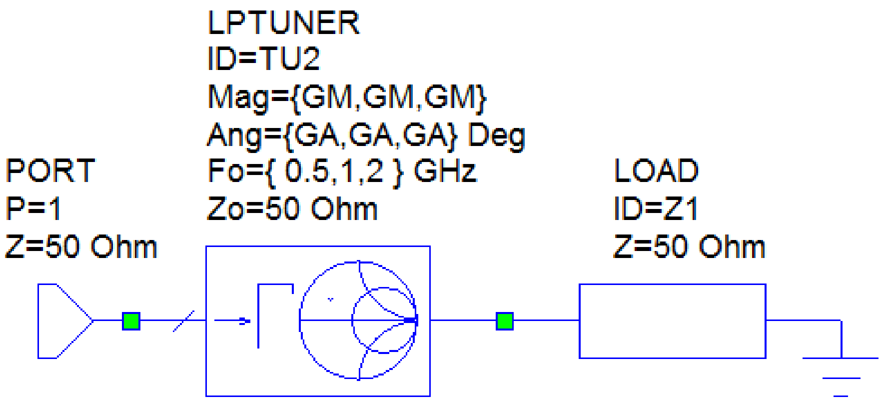
Specialists in RF and Microwave Amplifier Design

LTUNER – Nice and simple, but what impedance does it present at other frequencies?

LPTUNER – Define frequencies and their terminations, but if you don't define them they default.







Here we have defined 0.5, 1 & 2GHz but the other frequencies 2.5, 3, 3.5 and 4GHz also have defaulted to this load.

Tuners – Be Wary

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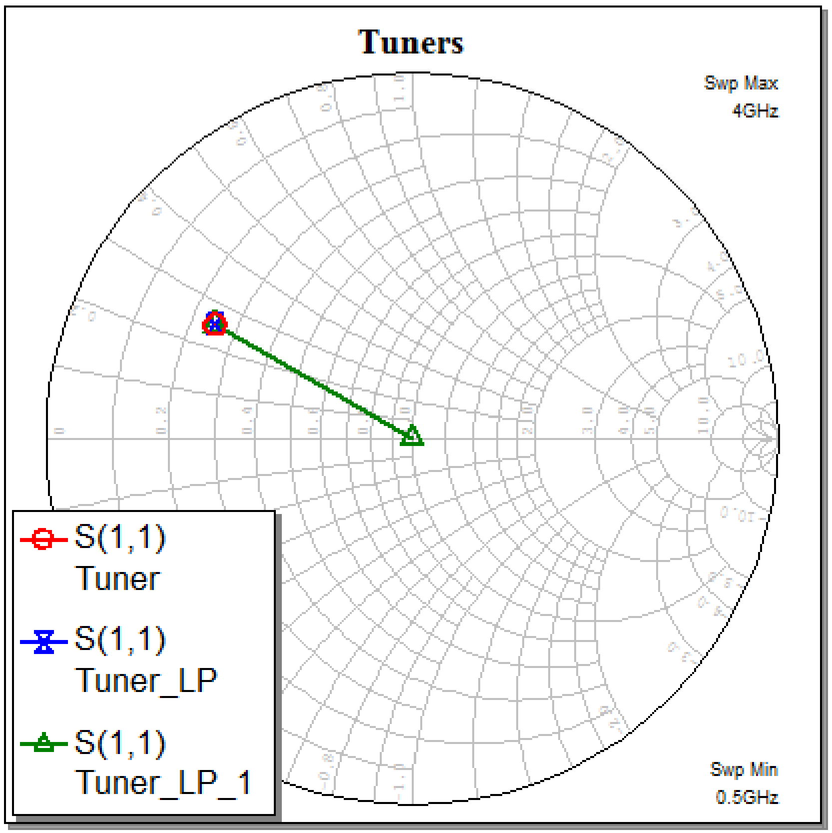
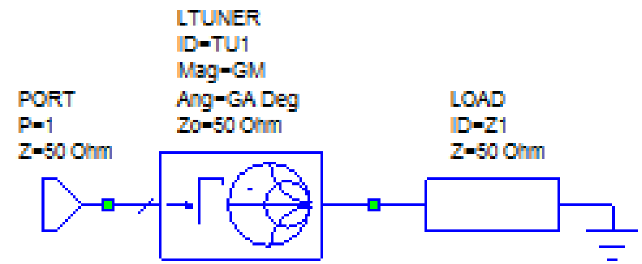
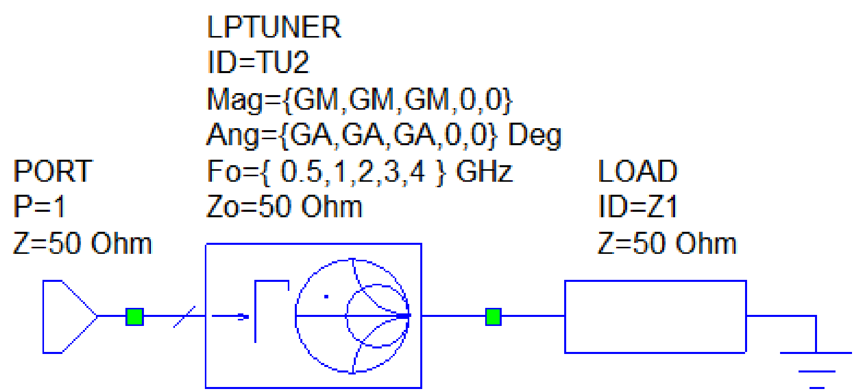




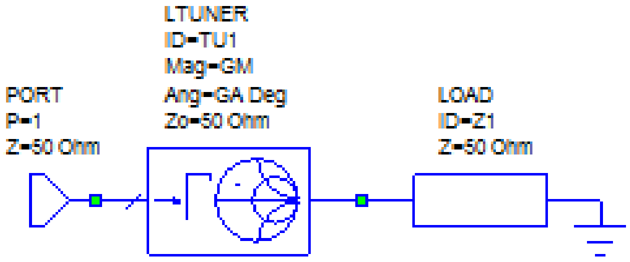


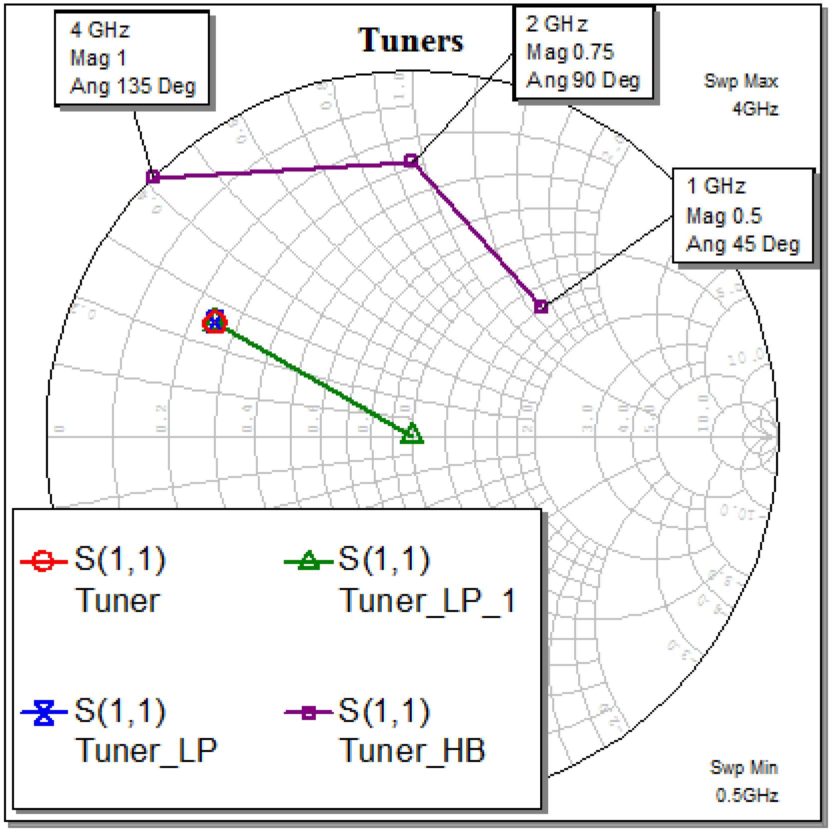
Now we have defined different impedances to some of the frequencies, 3 & 4GHz are terminated in 50Ω

Tuners – Be Wary

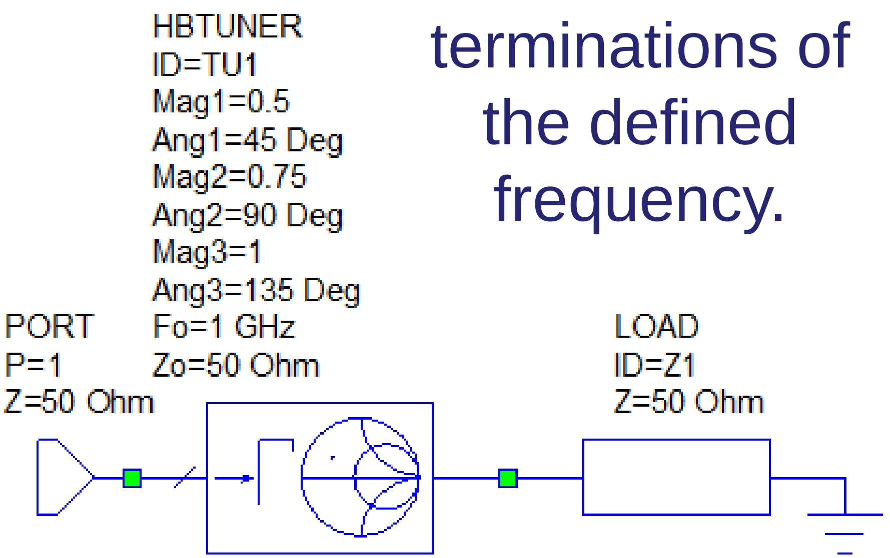
LTUNER – Nice and simple, but what impedance does it present at other frequencies?

HBTUNER – Takes care of the harmonic frequencies for you.





Takes care of the harmonic terminations of the defined frequency.



Tuners – Be Wary

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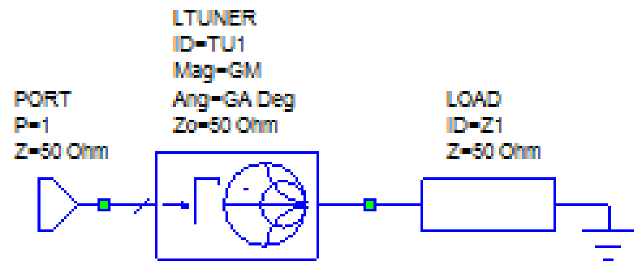
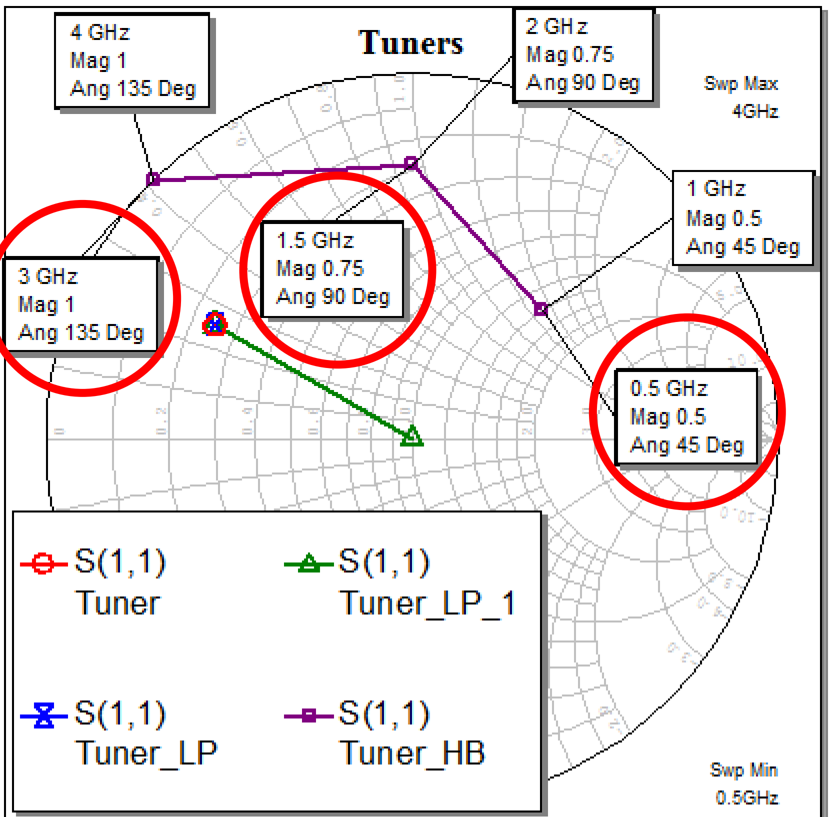
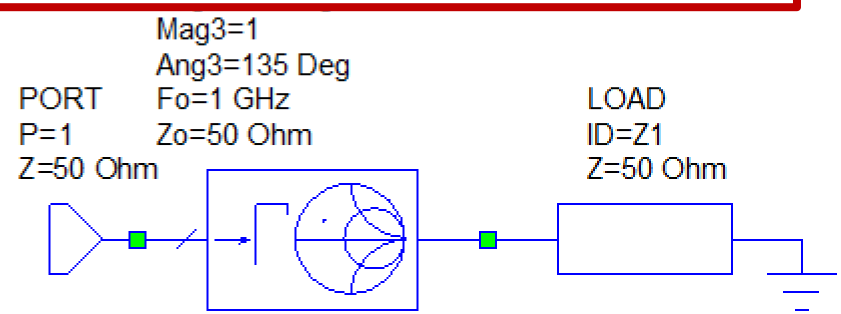
LTUNER – Nice and simple, but what impedance does it present at other frequencies?

HBTUNER – But…. Be aware of what happens at other frequencies and their terminations.





Harmonic impedance has an impact on device performance, so know where you have put yours!



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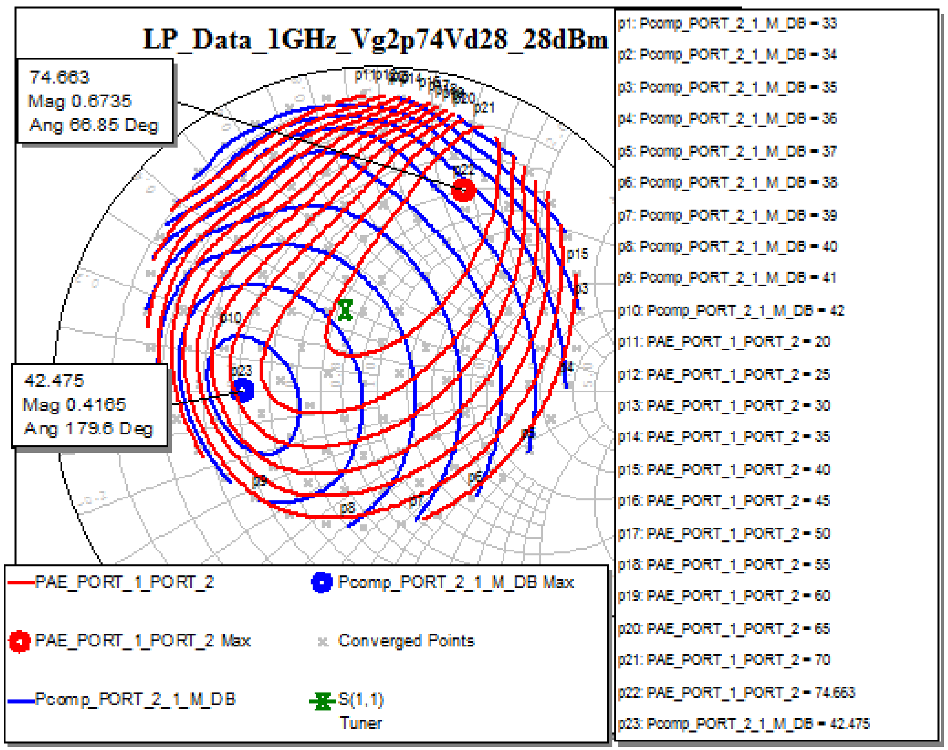
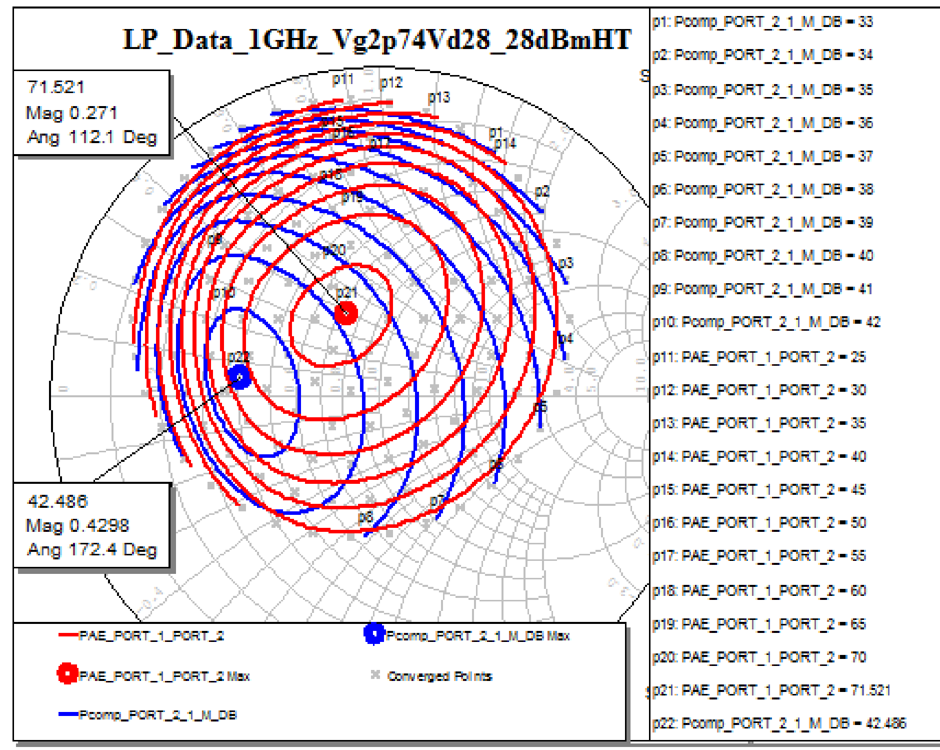
Difference between using LTUNER and HBTUNER with harmonics terminated in 50Ω.



Load Pull with LTUNER



Load Pull with HBTUNER

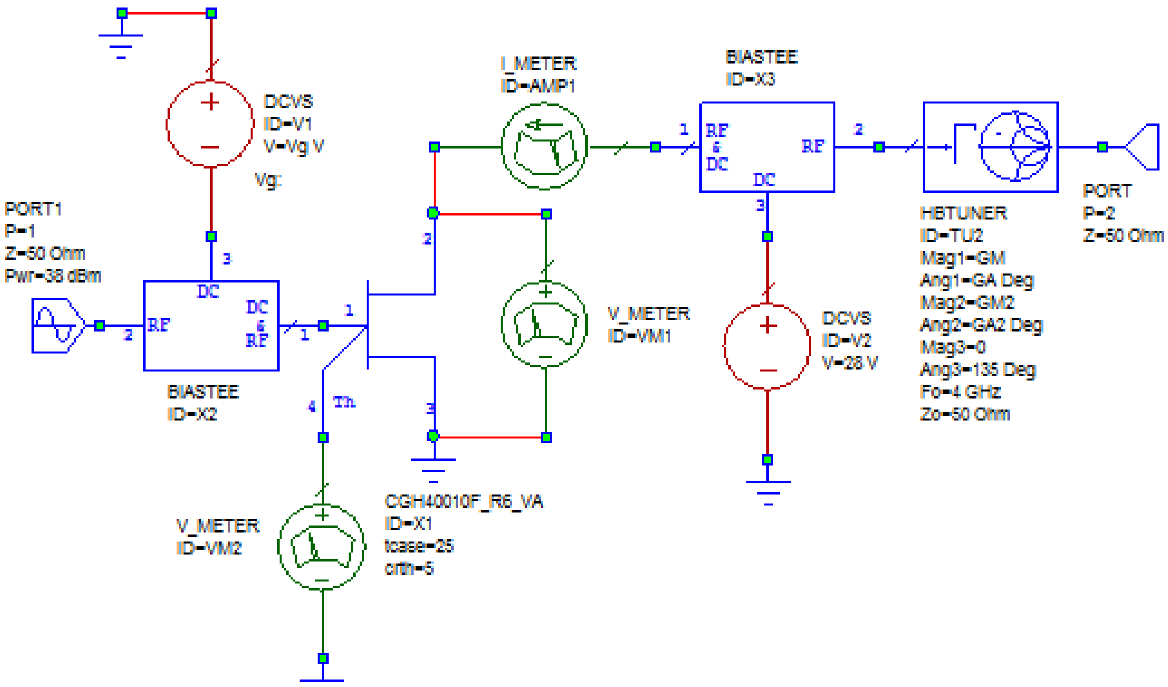
Small impact on Pout – Significant on PAE

Load Pull Set Up

We use Load Pull so that we can visualise the trade-offs between parameters, typically PAE and Pout.

Load Pull Check List

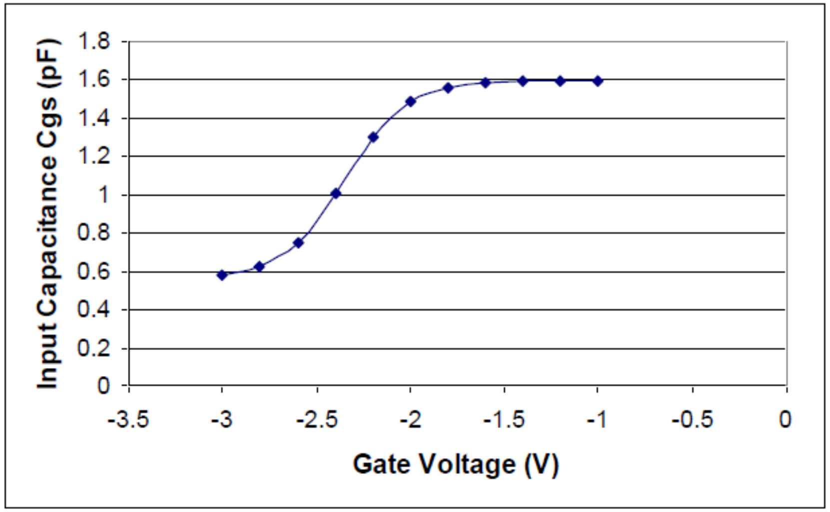
1. Harmonic terminations – use HBTUNER for accurate/consistent results.
2. Input Power level, check that you are using the optimum drive level by conducting a power sweep.
3. Bias/Class of operation.

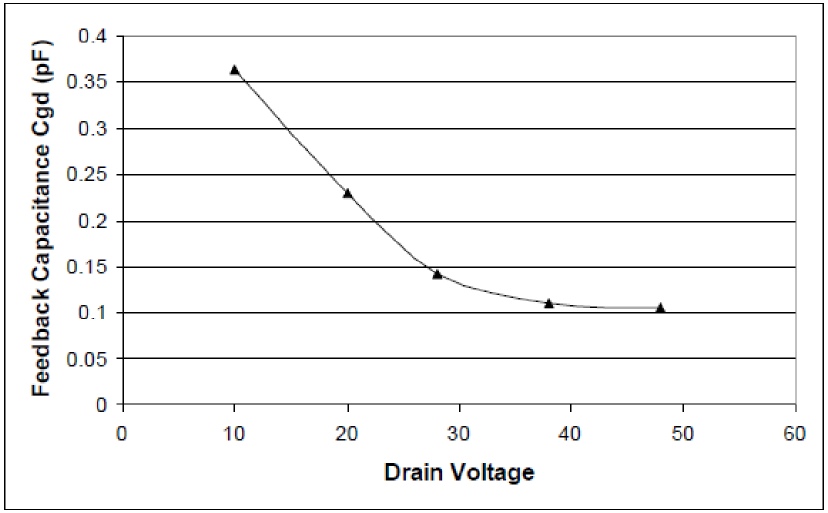


Input Match Effects

Why does the input match change?

1. Intrinsic capacitance
2. Channel resistance
3. Load match

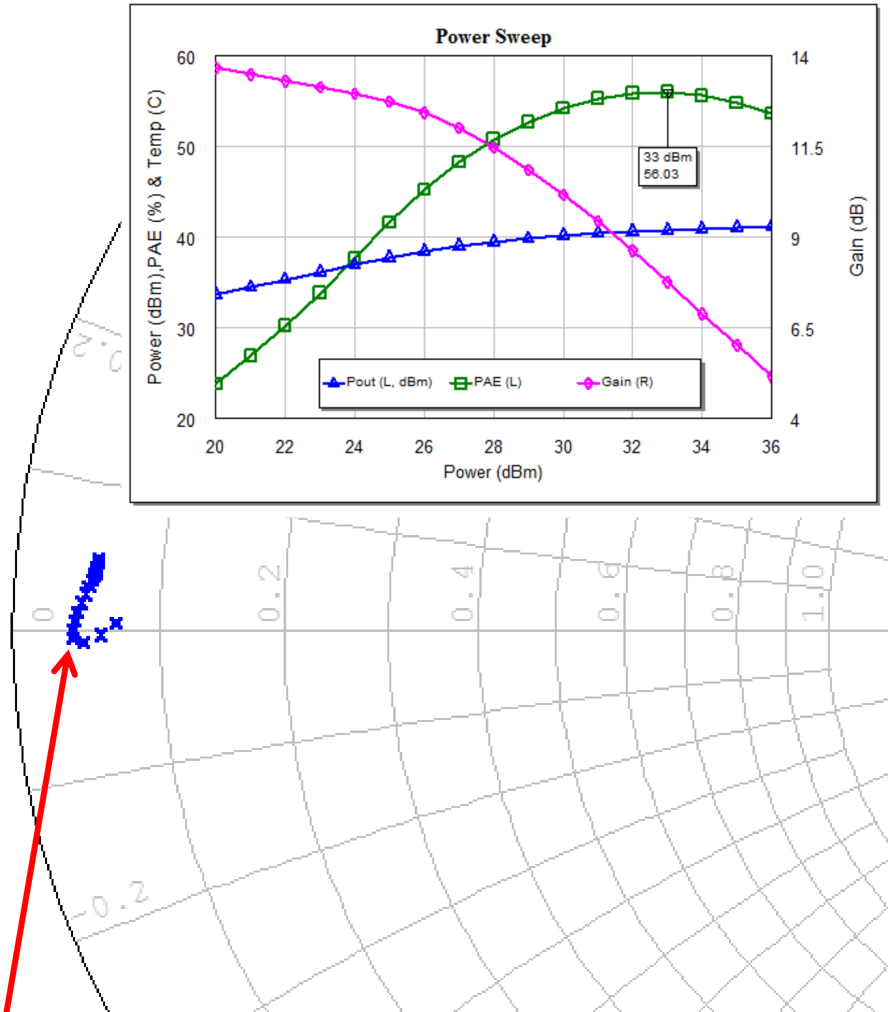




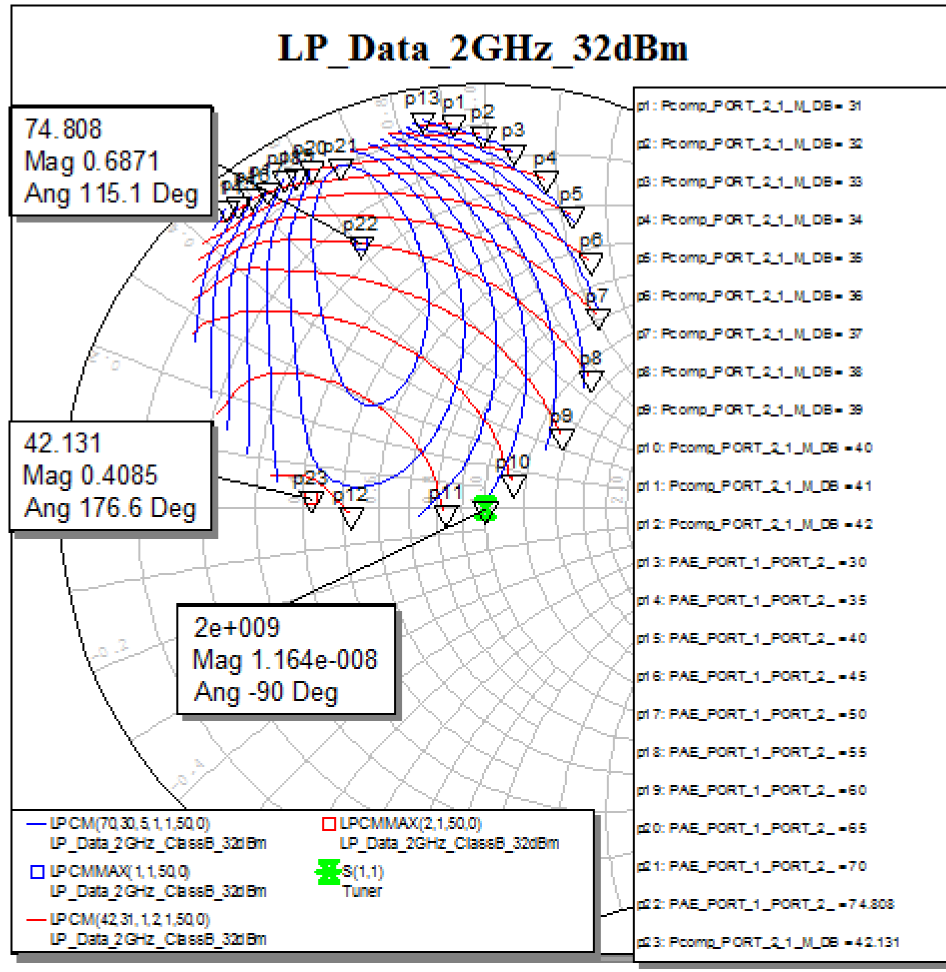
$$\Gamma_{IN} = S_{11} - \frac{S_{12}S_{21}\Gamma_L}{S_{22}\Gamma_L - 1}$$

Intrinsic Cree GaN HEMT Models allow more accurate waveform engineered PA designs
Ray Pengelly and Bill Pribble, Cree RF Products
ARMMS, April, 2013

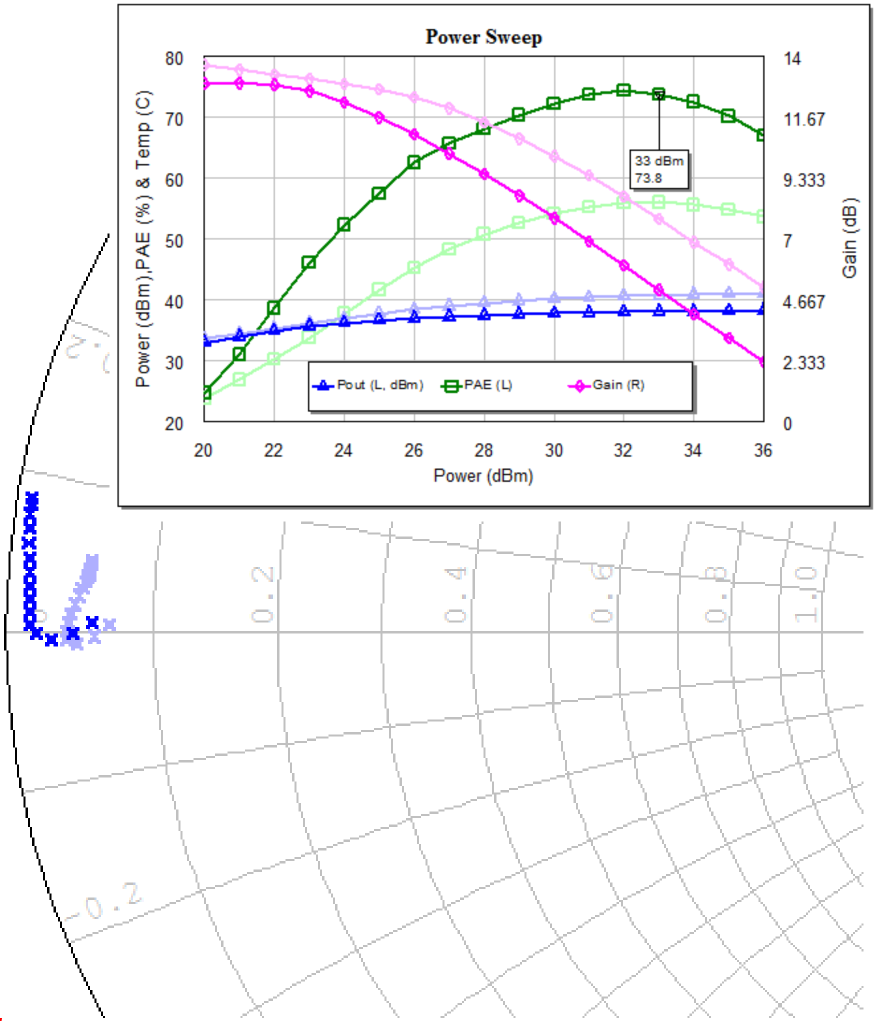
Effect of Load on Input Match

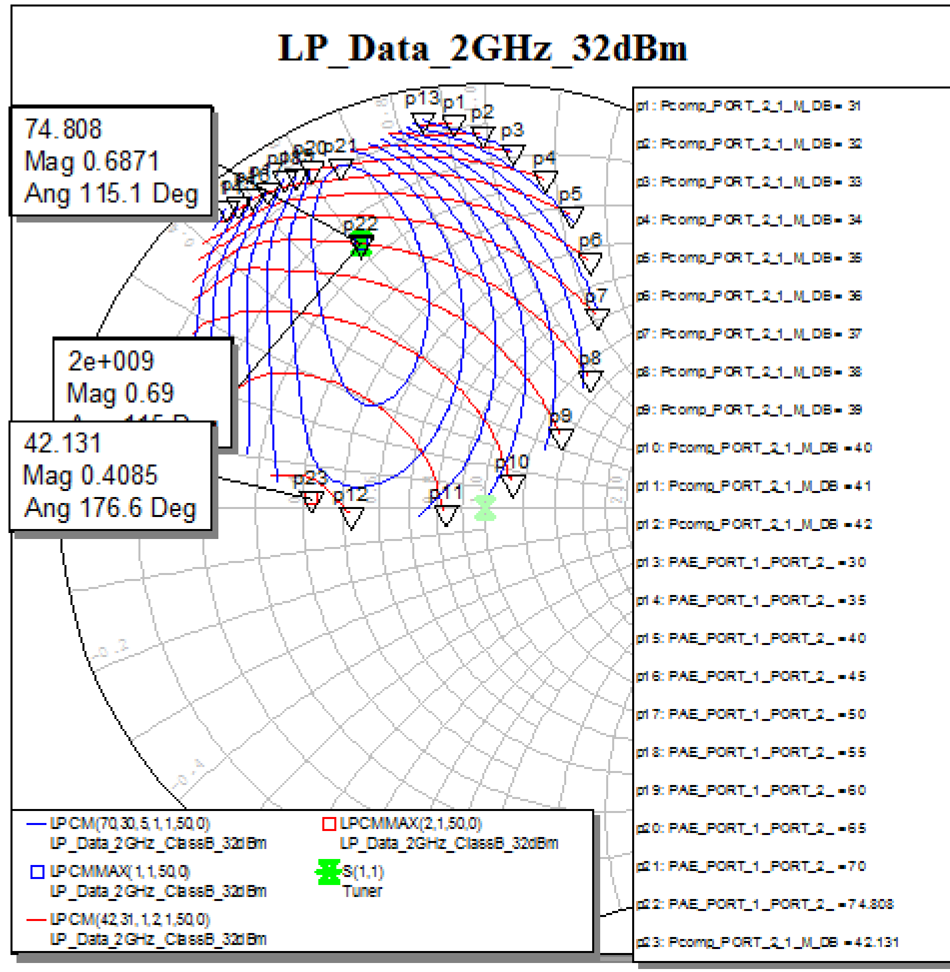


33dBm



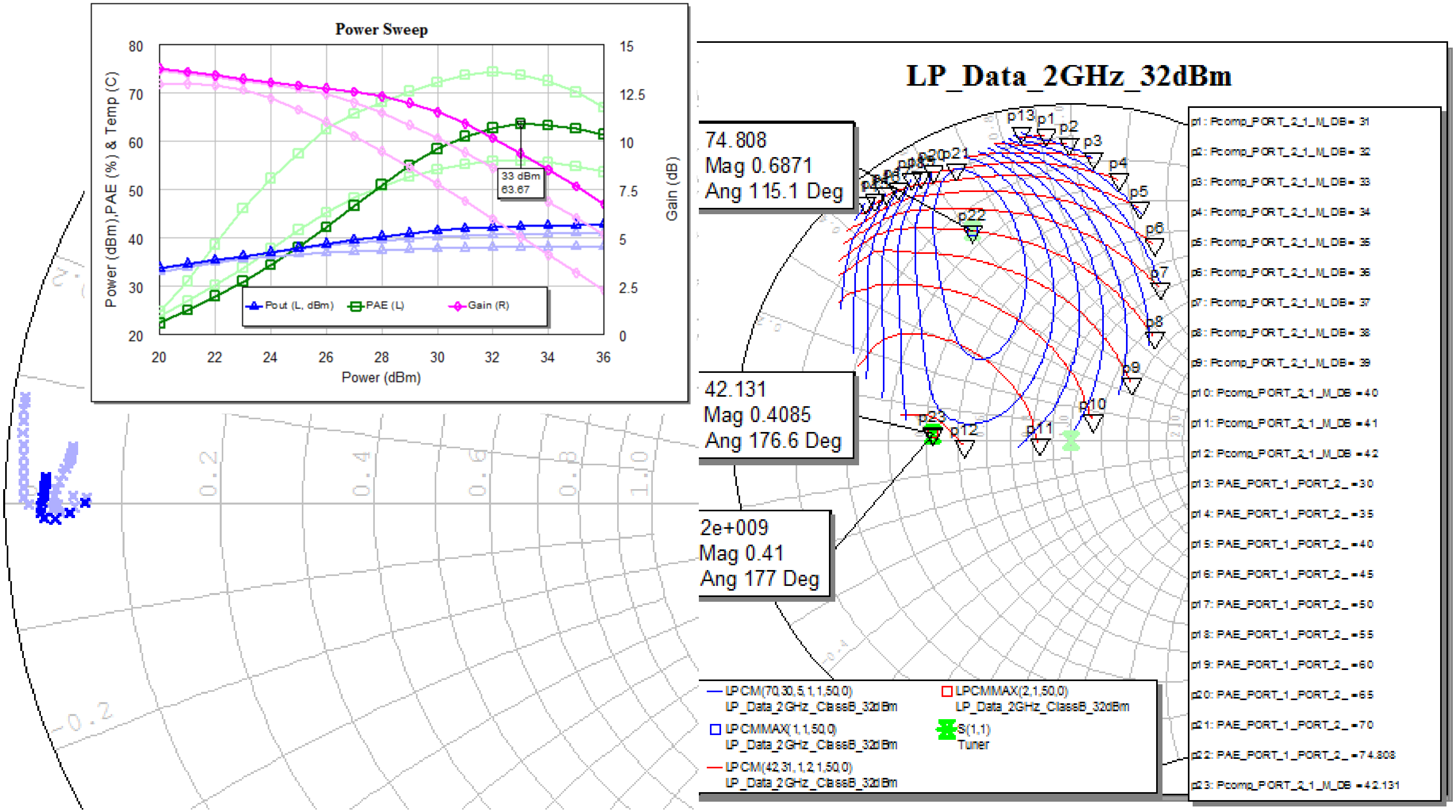
Effect of Load on Input Match





33dBm

Effect of Load on Input Match



33dBm

Input Power with Frequency

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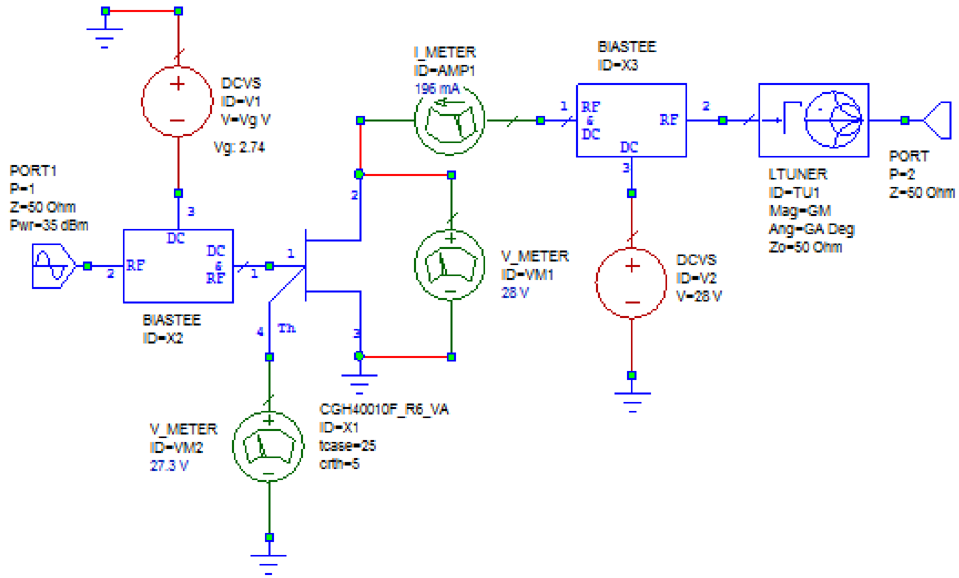
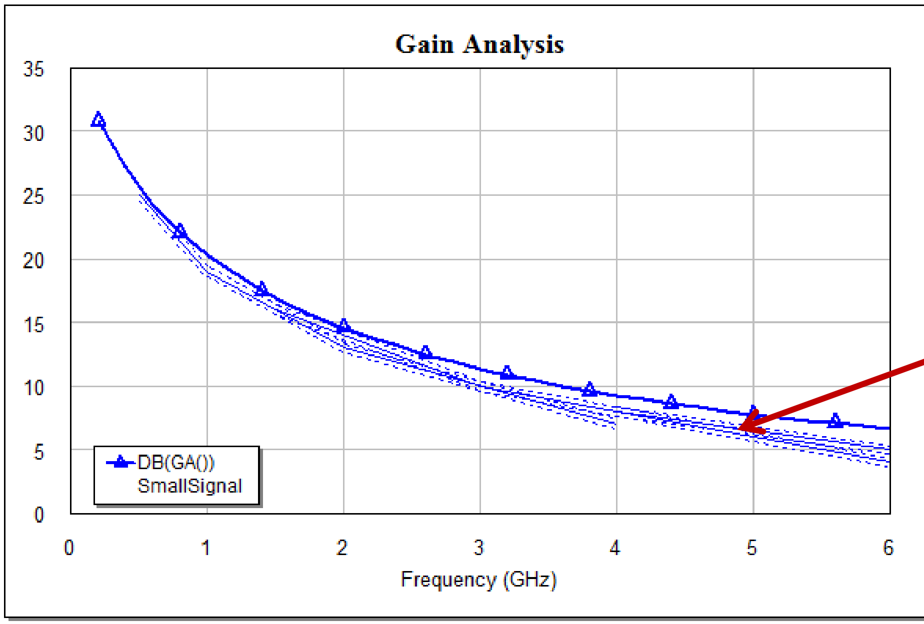
For wideband designs you have to consider input power vs. frequency.

Output power stays ~ constant with frequency.

So, to a first order input power needs to increase at this rate.

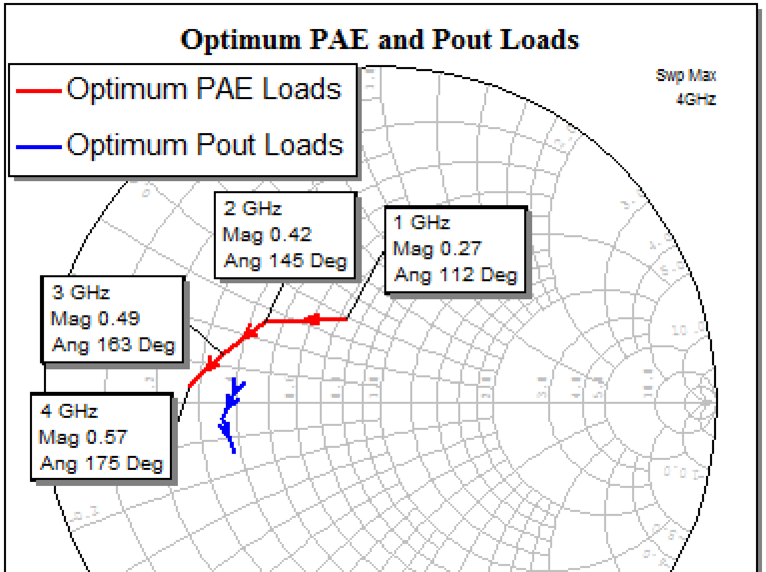
Let's take a look ➔





6dB/octave slope

Input Power with Frequency



Note:

1. Input power variation for optimum PAE.
2. The maximum Output Power is constant.
3. The intrinsic gain rolls off ~5dB/octave. Output matching recovers some but not all.
4. There is no input matching yet, this shows the need for a positive sloped input power match to achieve the maximum PAE across a wide bandwidth.

Freq. (GHz)	Pin (dBm)	Max. PAE (%)	Load	Pout (dBm)	Gain (dB)		Max. Pout (dBm)	Load
1	28	72	0.27/112°	40.5	12.7		42.5	0.43/174°
2	33	70	0.42/145°	41.4	8.4		42.5	0.44/178°
3	36	69	0.49/163°	41.7	5.7		42.5	0.47/-174°
4	38	67	0.57/175°	41.5	3.5		42.5	0.46/-161°

Choosing the Optimum Load

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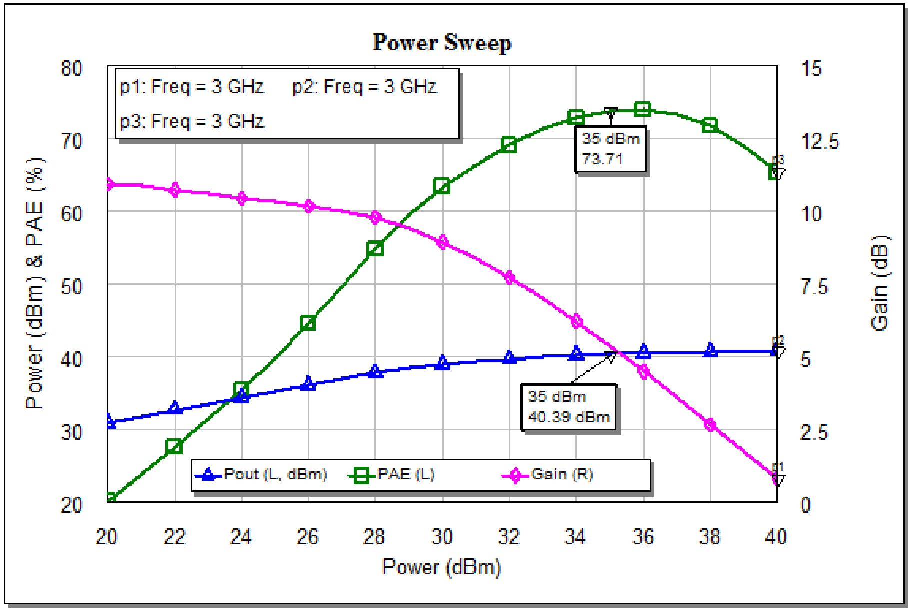
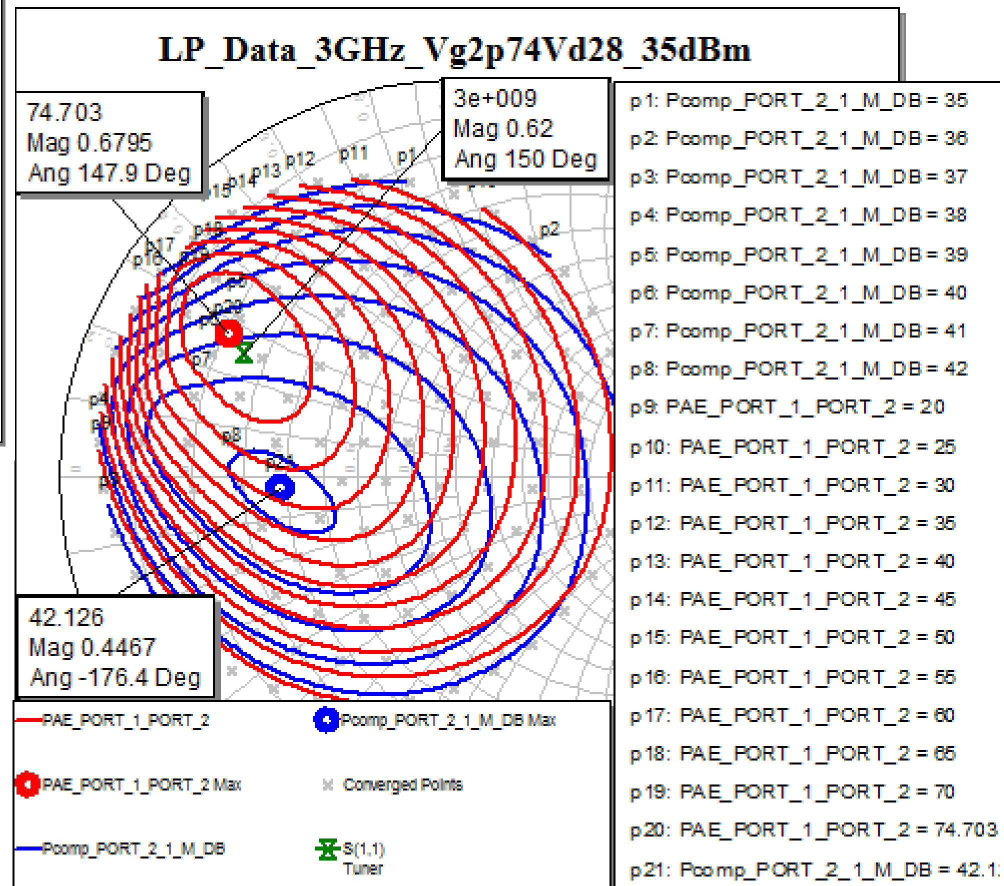
Specialists in RF and Microwave Amplifier Design

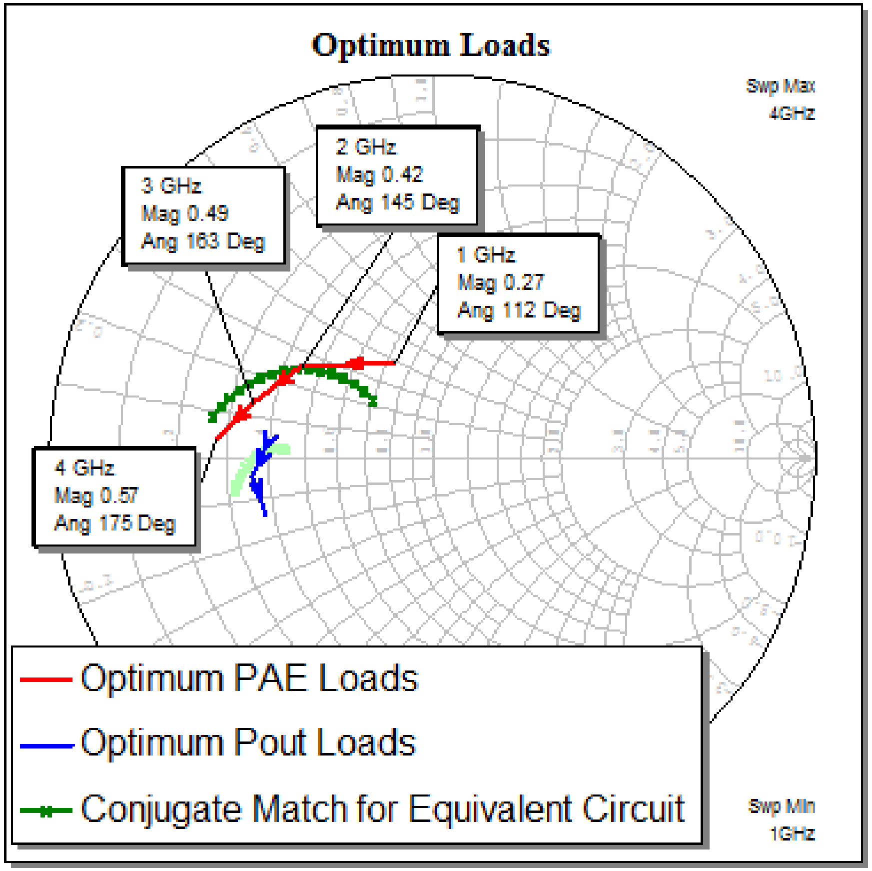


Be aware that the maximum load point may not be the "optimum"



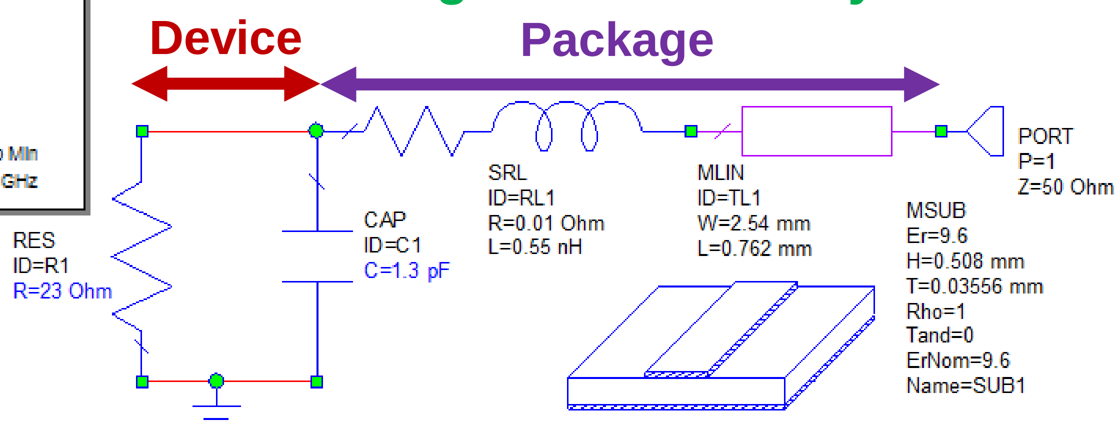
Green 'hour-glass symbol shows load for power sweep.
By observing swept input power performance as you tune the load you can adjust for the best compromise performance between Power and PAE.

Returning to the Optimum Loads



Looking at a simple device output equivalent circuit, including some package de-embedding:

The equivalent load resistance increases from 23Ω for the optimum power loads to 41Ω for the optimum PAE loads – which agrees with theory ☺



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Load Line Theory

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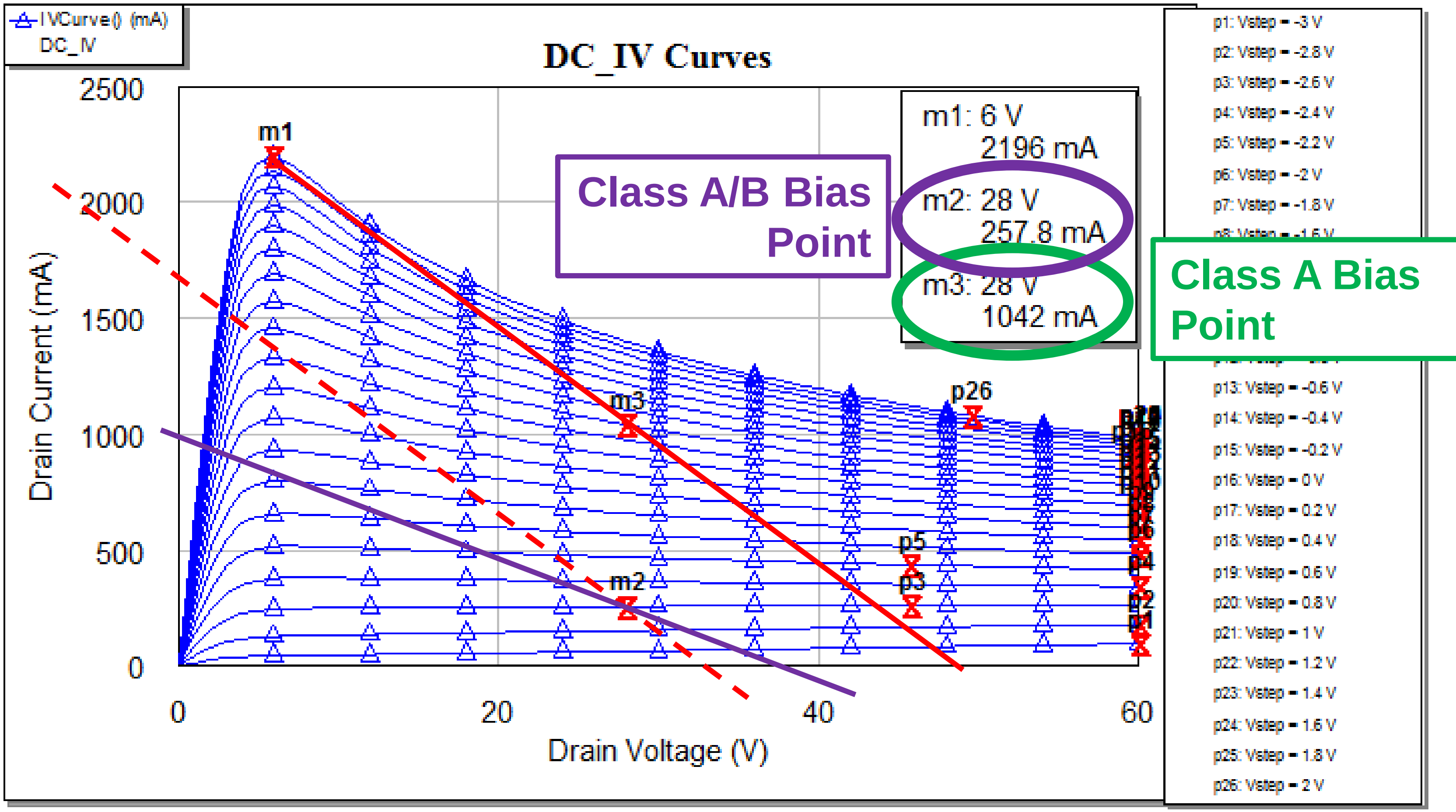

Theory Optimum Power load = $2x(V_D-V_K)/I_{DS}$ = 20Ω

Load Line Simulation

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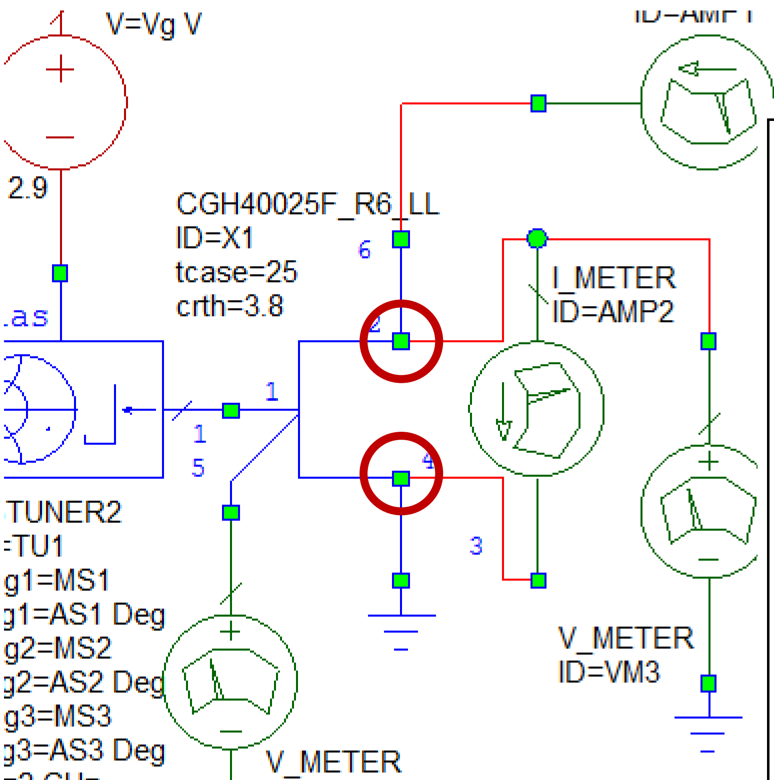
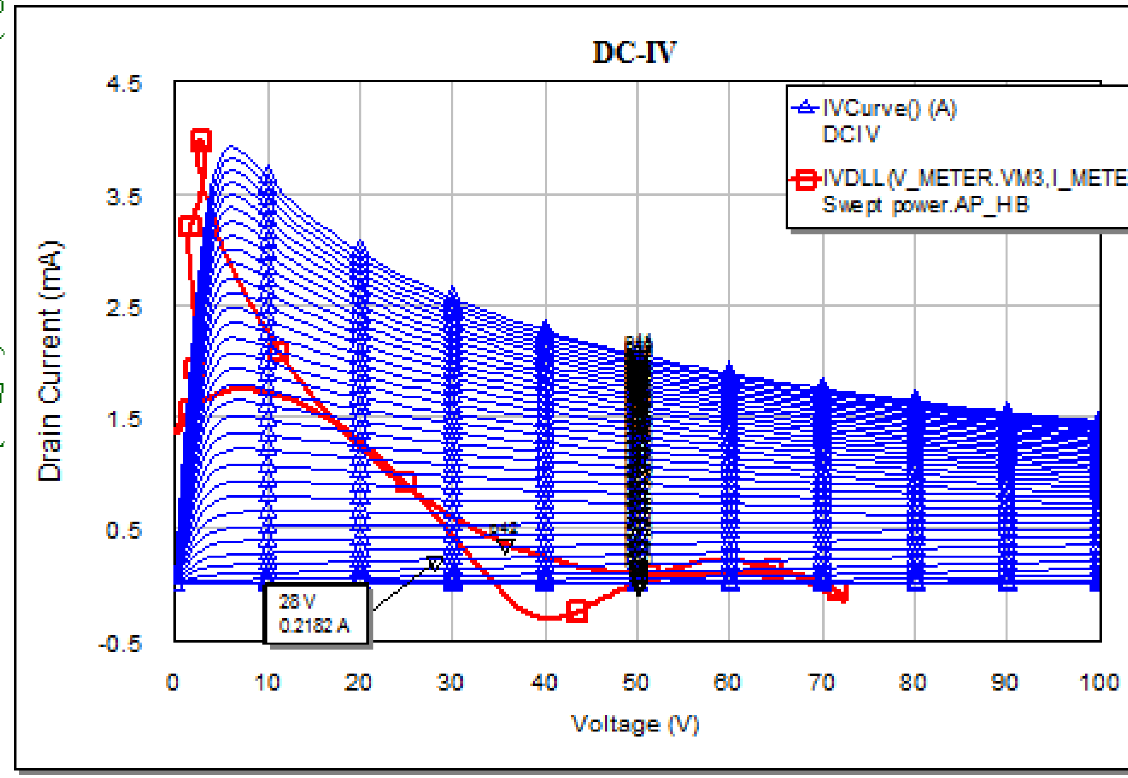
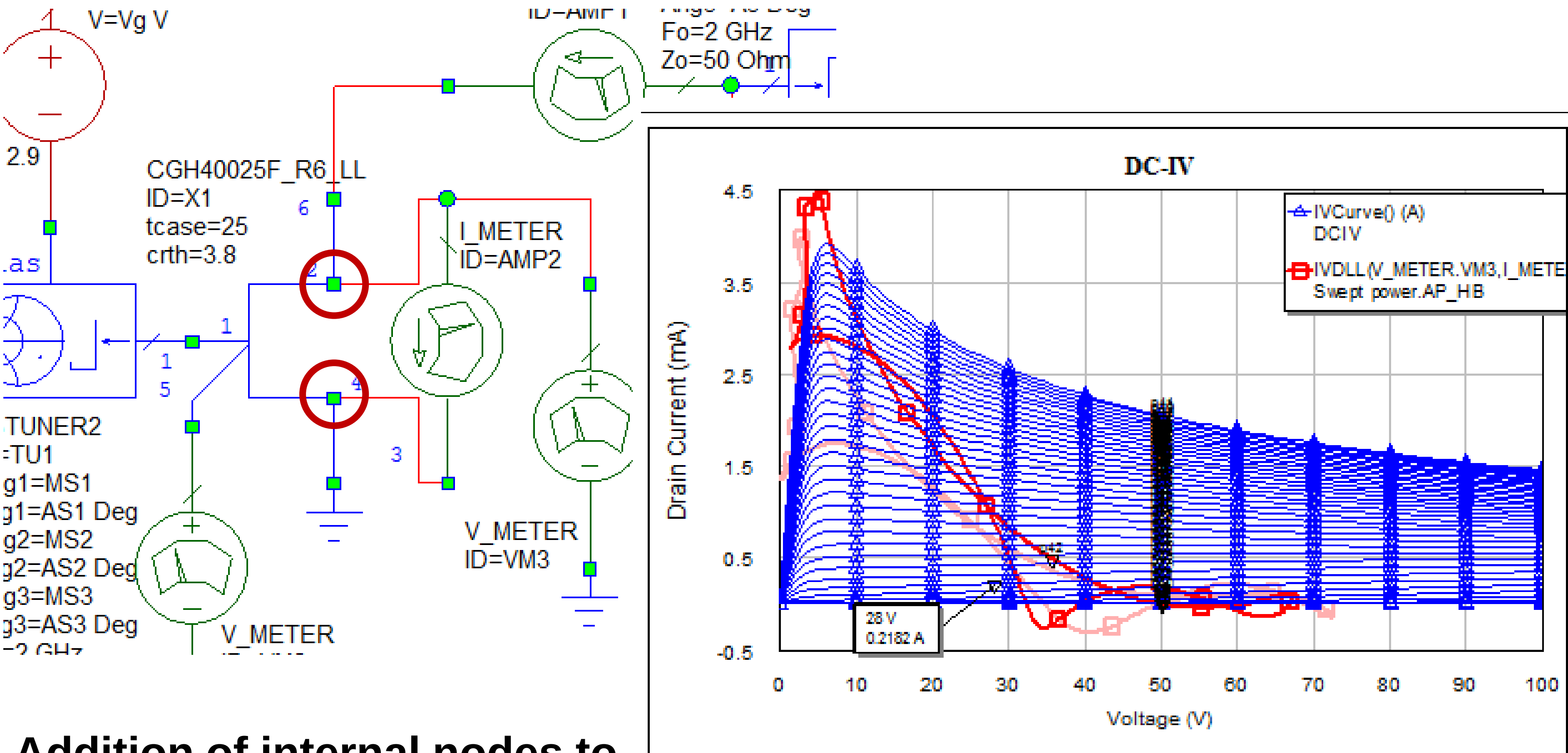




Addition of internal nodes to model allows direct observation of drain waveforms.

As we increase drive Dynamic (RF) load line interacts with limits of the DC-IV envelope.

Load Line Simulation



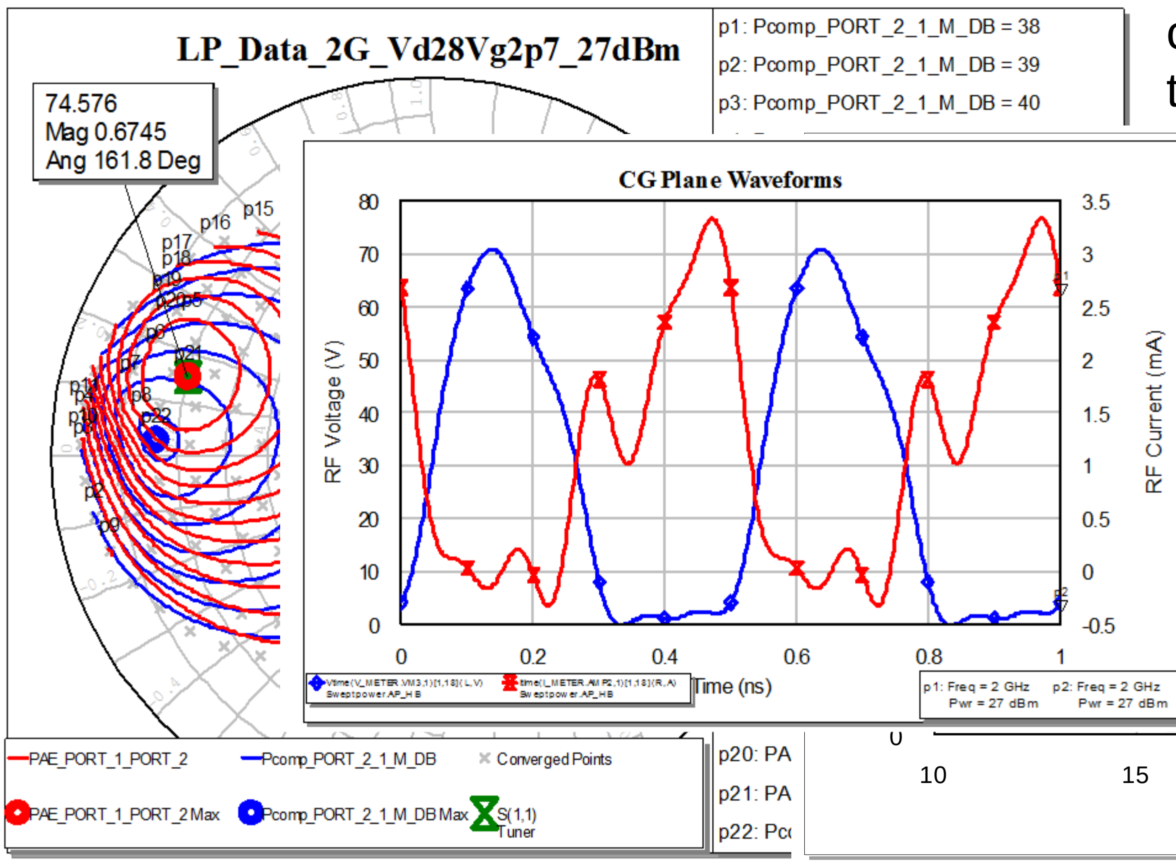
Addition of internal nodes to model allows direct observation of drain waveforms.

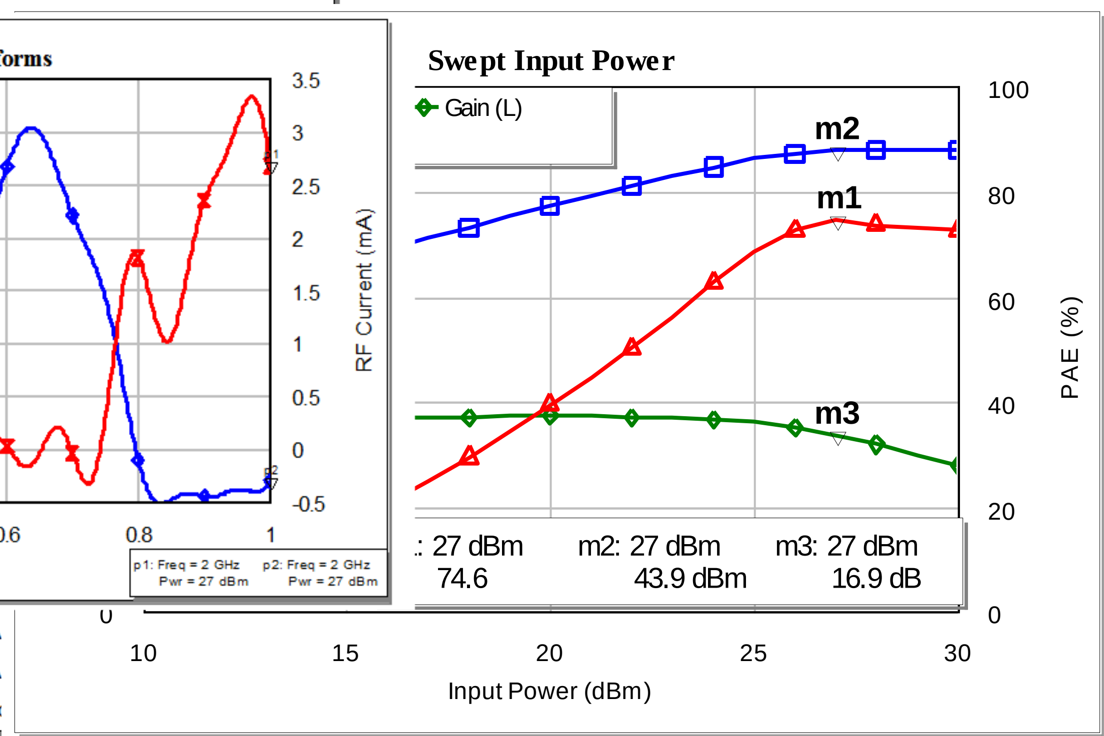
Or change load impedance

Harmonic Terminations

A great deal of research has gone into the design of high PAE modes class E, F & J for example, and the importance of harmonic terminations. Using these tools we can see their impact.

Fundamental Load Pull is conducted with the harmonics terminated in 50Ω.





Harmonic Terminations

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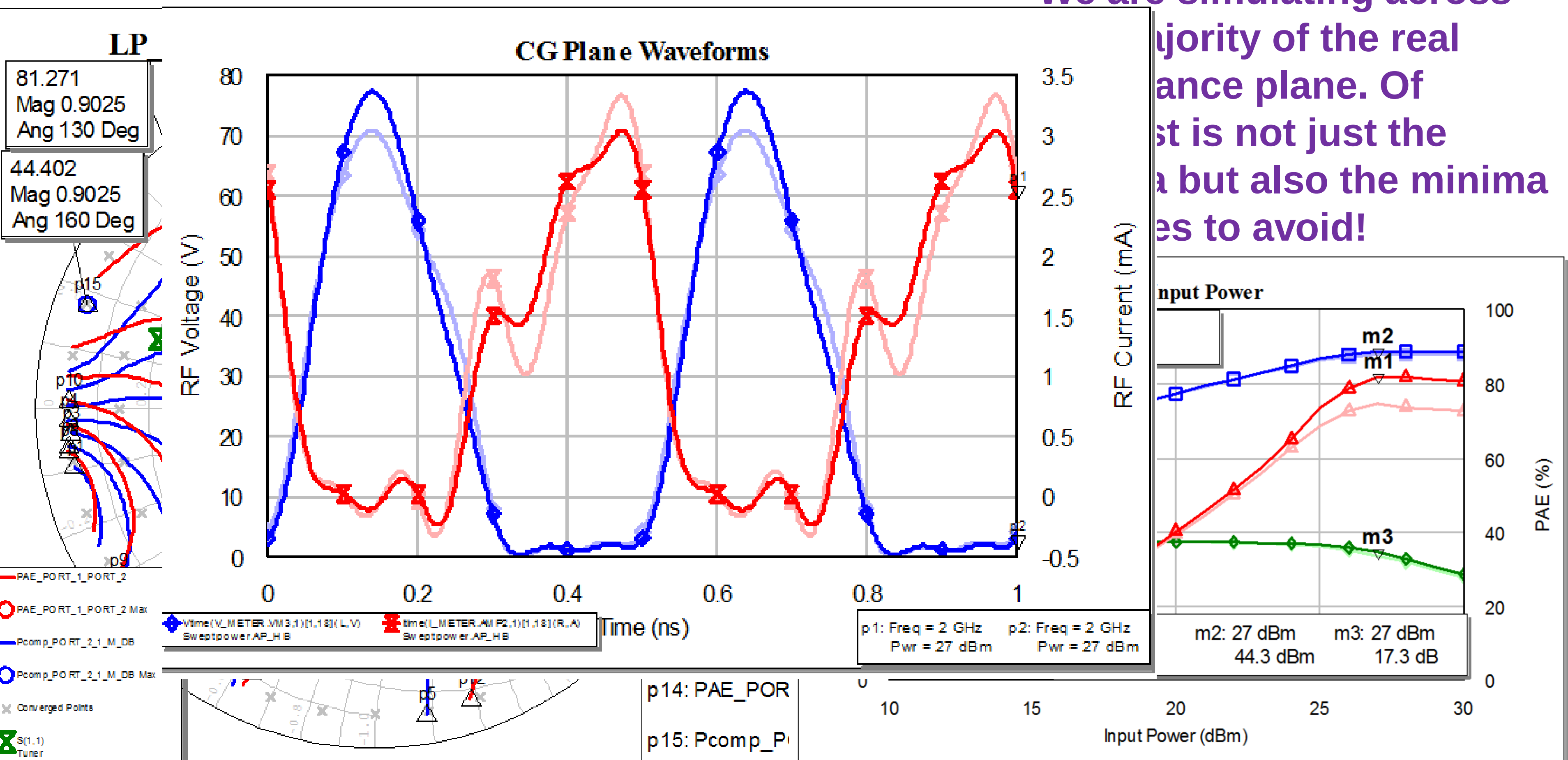
Keeping the Fundamental at the optimum PAE impedance a 2nd Harmonic Load Pull is conducted with the 3r harmonic terminated in 50Ω.

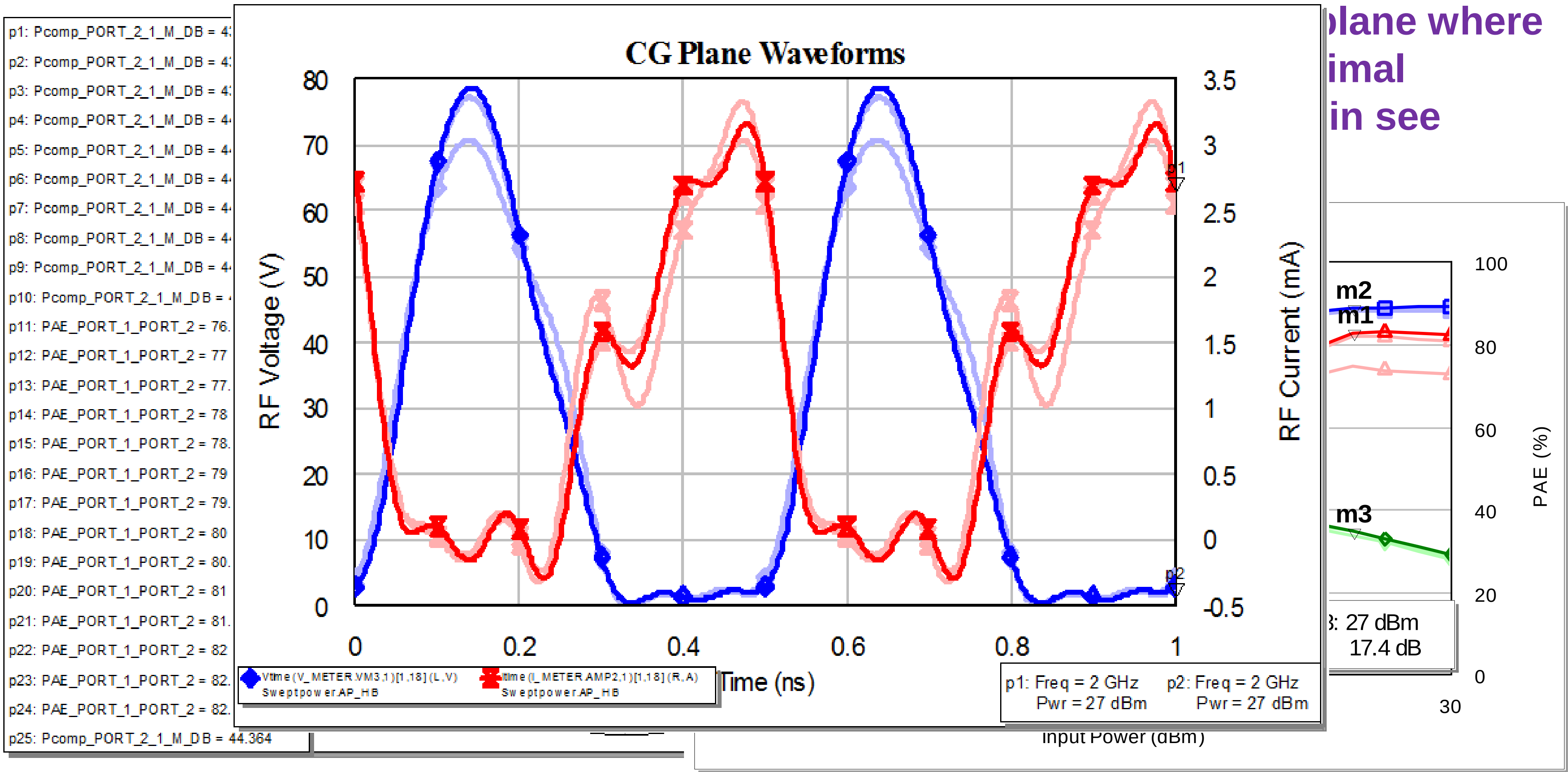
We are simulating across ...jority of the real ...ance plane. Of ...st is not just the ...a but also the minima ...es to avoid!



Harmonic Terminations

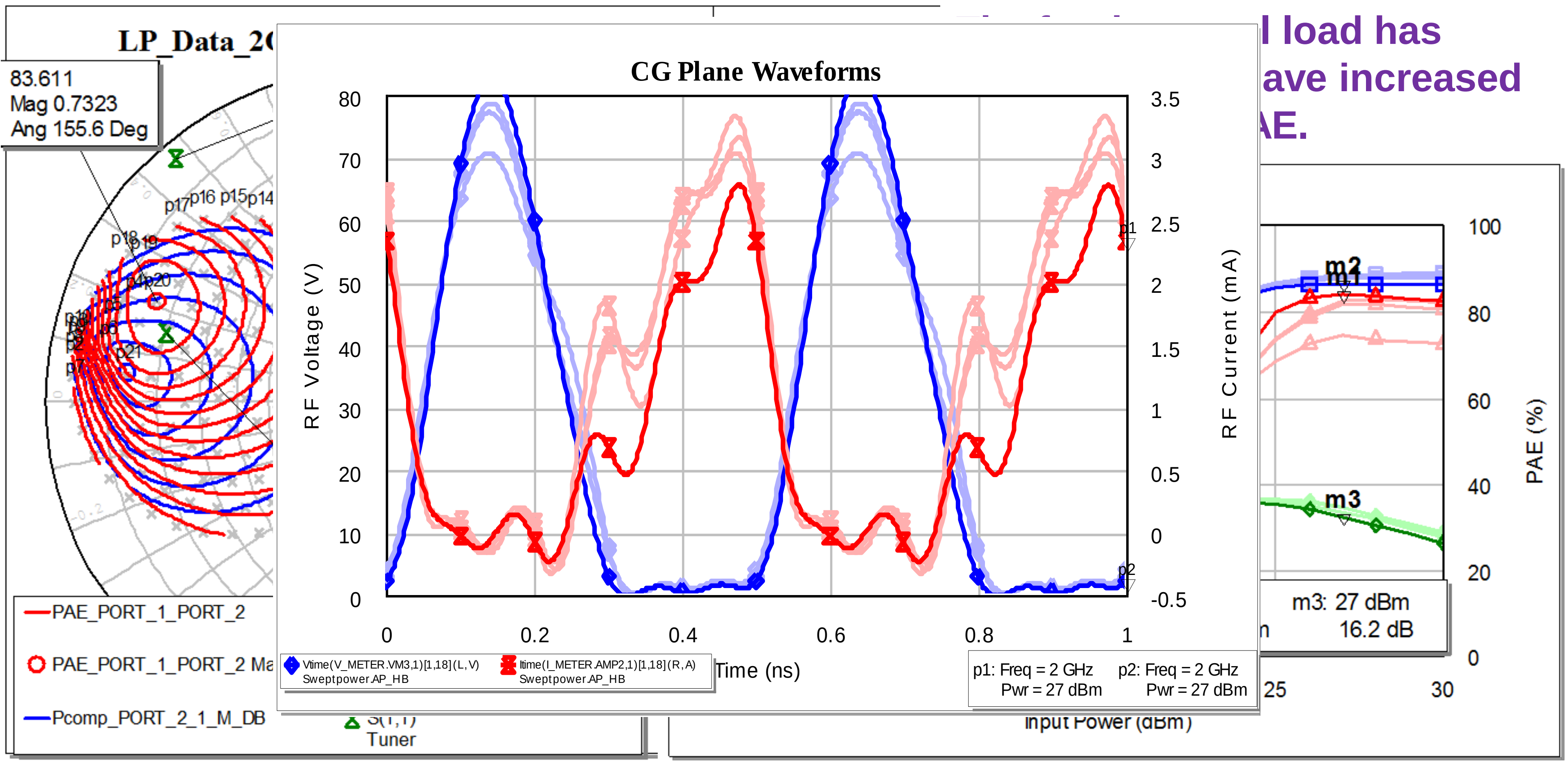
Keeping the Fundamental & now 2nd at their optimum PAE impedances a 3rd Harmonic Load Pull is conducted.

We now have almost half ... plane where ... imal ... in see

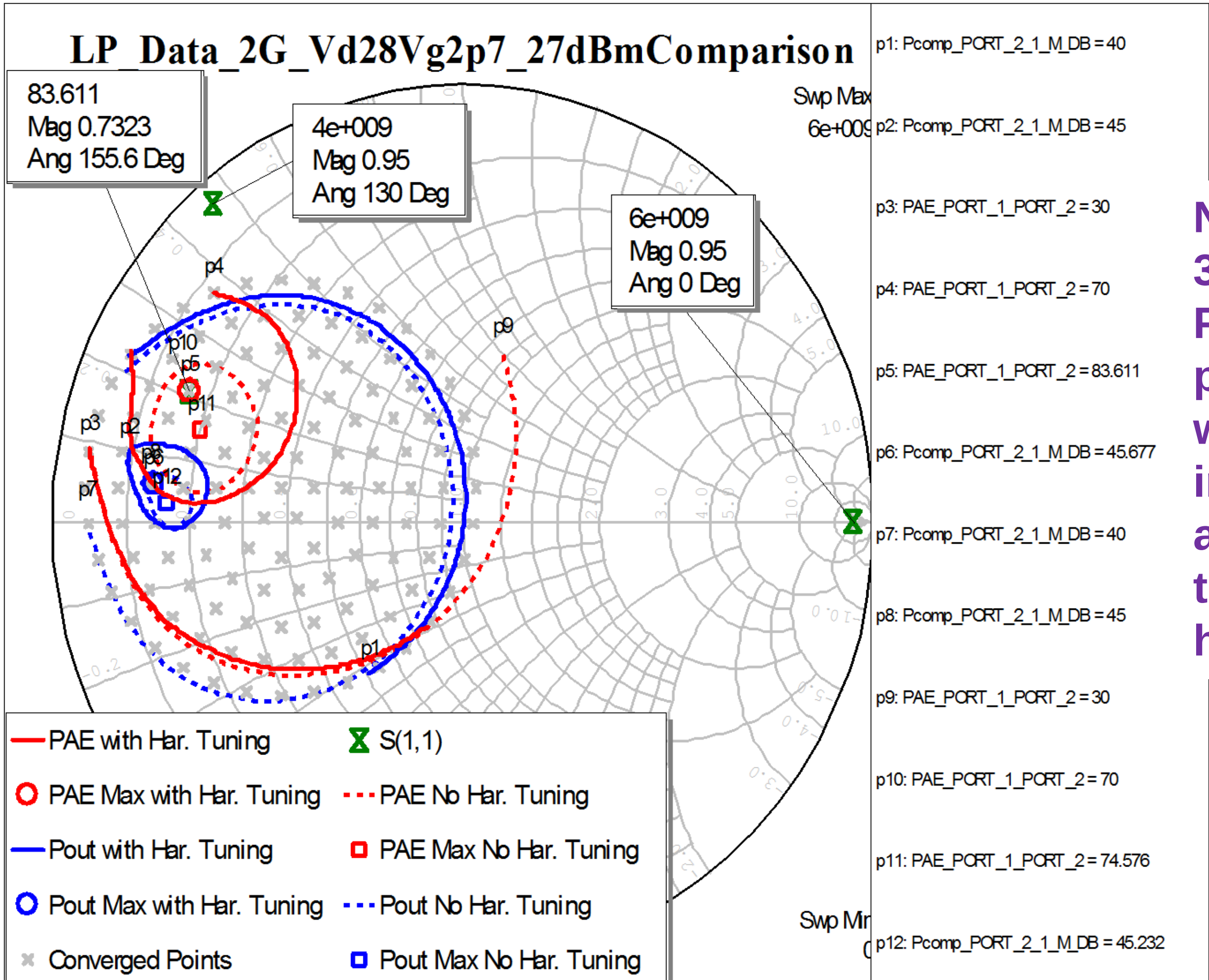


Harmonic Terminations

Now we have all our terminations optimised, or have we? Re-do the fundamental load pull with the optimum PAE harmonic terminations -

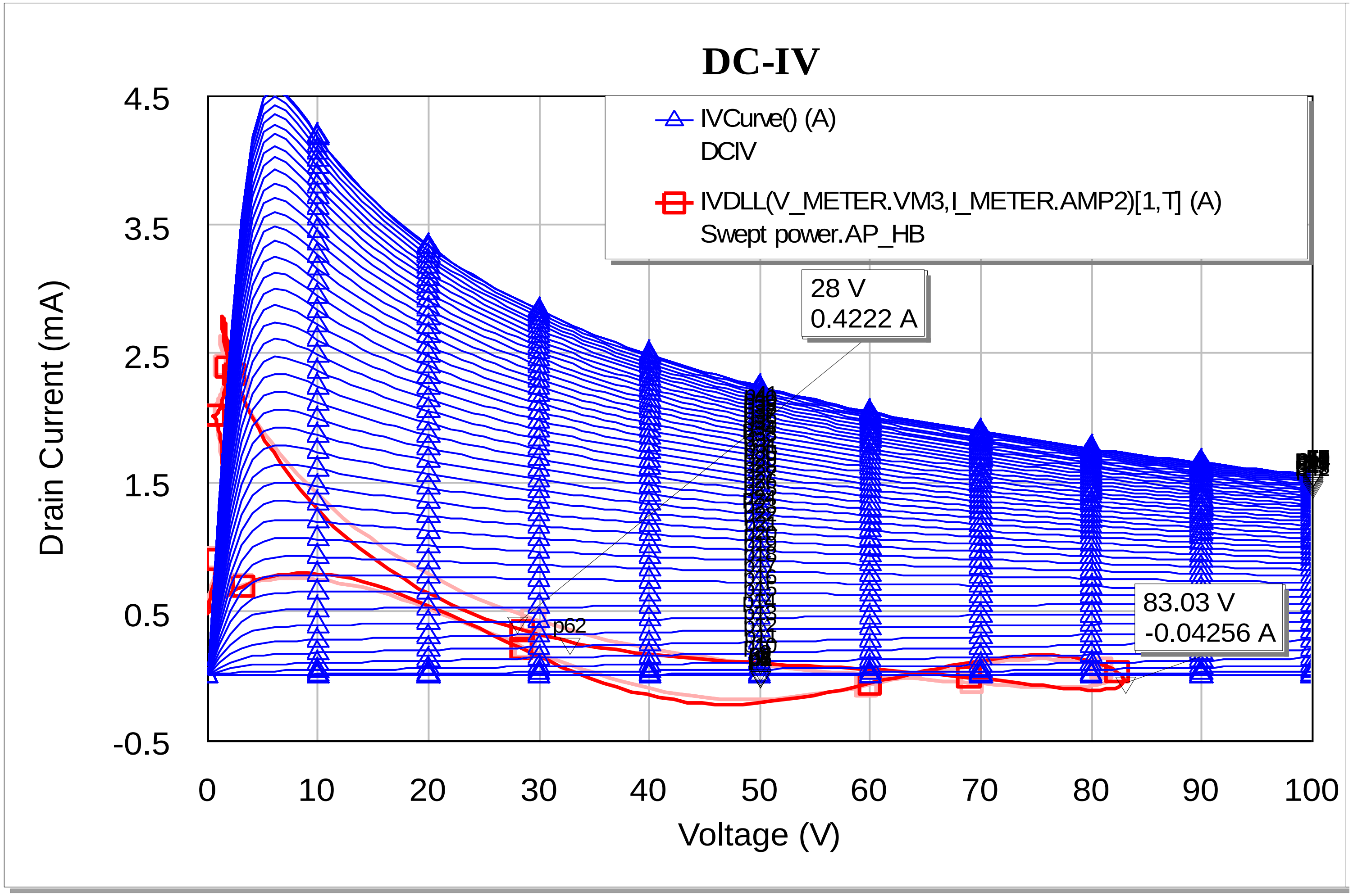


Harmonic Terminations



No significant change at 30% PAE and 40dBm Pout, but increase in the peaks and consequently a wider impedance range included in the 70% PAE and 45dBm Pout, indeed these two regions now have a significant overlap.

Dynamic Load Line & Harmonic Terminations



Notice that we are avoiding high current swings in favour of higher voltage swings.

Fundamental, 2nd, & 3rd Optimum. Note nearly 3x Drain Voltage Swing.

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Optimum Load Design is a Cyclical Process

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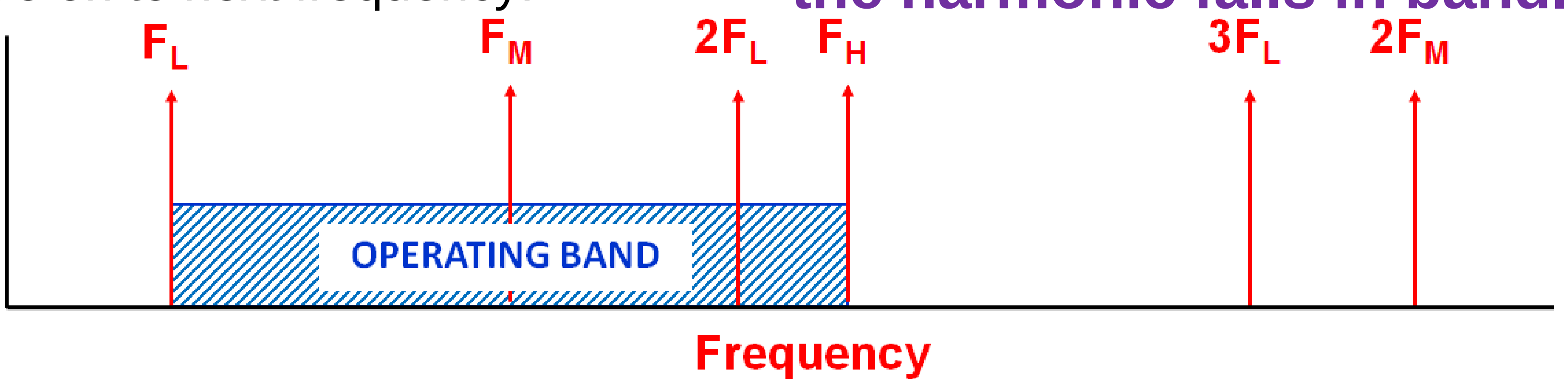
Harmonic Load Pull Steps:

1. Optimum Fundamental Drive Power.
2. Optimum Fundamental Load - Check (1) is still true.
3. 2nd Harmonic LP – Check (1) & (2) are still true.
4. 3rd Harmonic LP –Check (1), (2) and (3) are still true.
5. Go on to next frequency!

Remember it is not only about finding the optimums - you also need to know where to avoid!

We can't always use the optimum harmonic termination. If we are doing wide bandwidth designs the harmonic falls in band.



Broadband Matching:- Insertion Loss and Match

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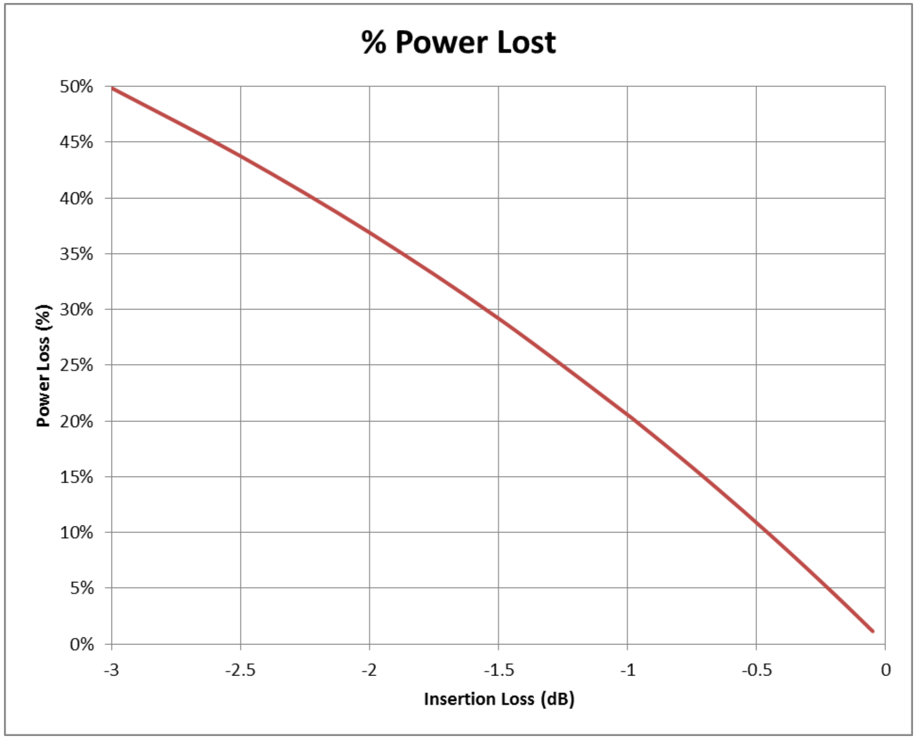
Load Pull gives the performance before any matching circuit -
Broadband Matching circuitry seeks to resolve two key problems:

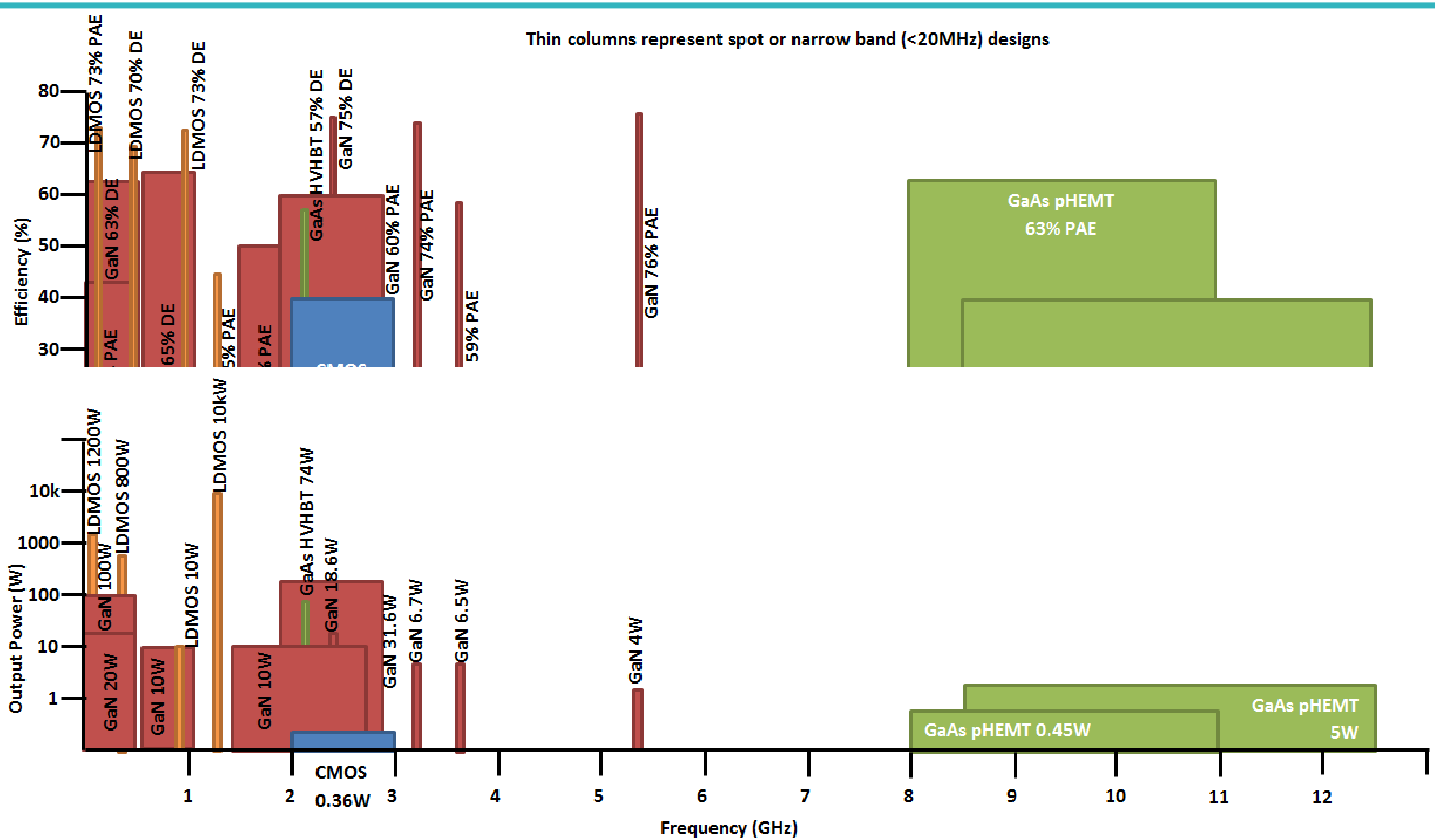
i. How to maximise bandwidth with a minimum Reflection Coefficient, Γ.
ii. How to minimise the number of matching elements, N, for a given bandwidth, (typically loss α N).

Don’t confuse L_T with insertion loss that has got to be included too!

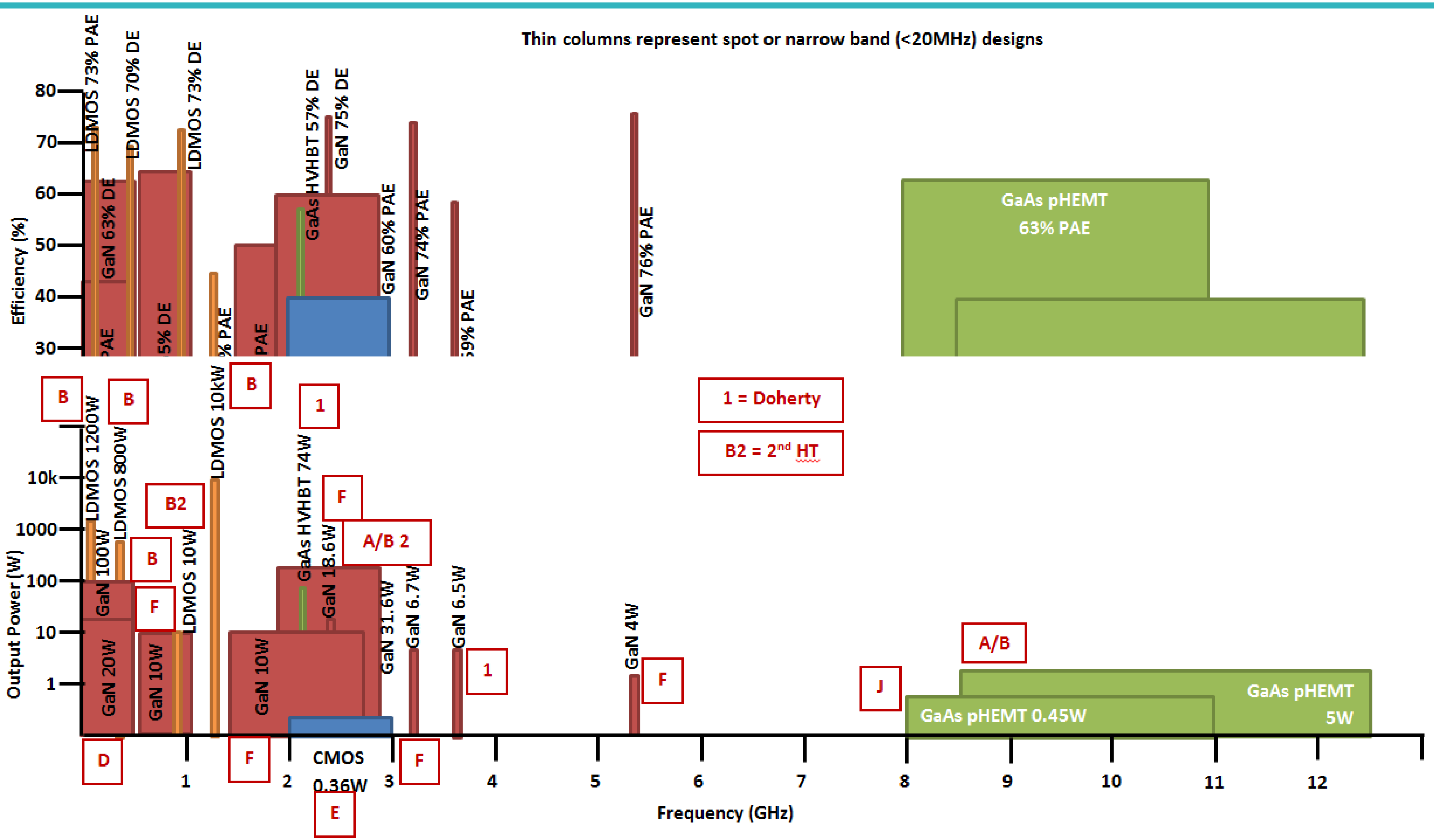


Γ	0.1	0.18	0.2	0.25	0.35	0.4	0.5	0.71	0.8
RL (dB)	20	15	14	12	9	8	6	3	1.9
L_T (dB)	0.04	0.14	0.18	0.28	0.58	0.76	1.25	3.0	4.44
VSWR	1.22	1.43	1.50	1.67	2.1	2.33	3.00	5.85	9.00
Γ, Return Loss, Mismatch (Transmission) Loss and VSWR.									

Current Approaches and Performance



Current Approaches and Performance



Current Approaches and Performance

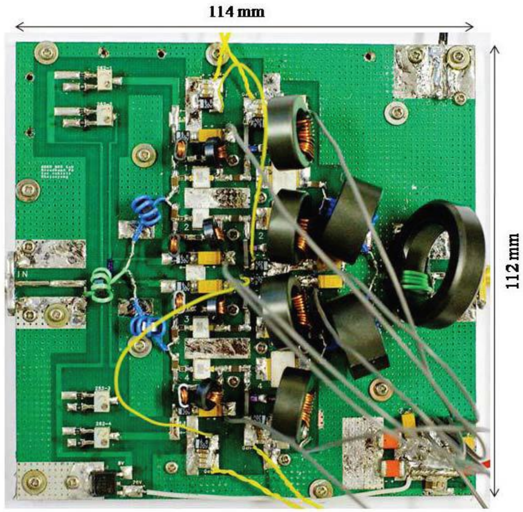
Technology	Class	Fmin GHz	Fmax GHz	Eff. %		Pout	Dev.Power	Year	Reference
cmos	E	2	3	40.2	PAE	0.36	NS	2013	Broadband and High-Efficiency Power Amplifier that Integrates CMOS and IPD Technology
GaAs pHEMT	A/B	8.5	12.5	40	PAE	5	8x 0.8	2013	Design Procedure 4 Hi-Eff and Compact-Size 5–10W MMIC PAs in GaAs pHEMT Tech.
GaN HEMT	F	5.65	5.7	76	PAE	4	0.96mm	2012	Ultra High Efficiency Microwave Power Amplifier for Wireless Power Transmission
GaN HEMT	F^{-1}	3.27	3.3	74	PAE	6.7	10	2010	First-Pass Design of High Efficiency Power Amplifiers using Accurate Large Signal Models
GaN HEMT	F^{-1} PushPull	2.5	2.55	75	DE	18.6	2x 10	2010	First-Pass Design of High Efficiency Power Amplifiers using Accurate Large Signal Models
GaAs pHEMT	J	8	11	63	DE	0.45	0.6	2011	GaAs X-Band Hi Eff (>65%) Broadband (>30%) Amp MMIC based on Class B to J Continuum
GaAs HVHBT	Doherty	2.1	2.15	57	DE	74	2x 120	2010	Doherty Power Amp using 2nd Gen. HVHBT Technology for Hi Eff Basestation Applications
LDMOS	B 2HT	0.9	0.95	73	DE	10	30	2010	Lumped-element Output Networks for High-efficiency Power Amplifiers
GaN HEMT	B?	0.01	0.5	43	PAE	100	4x 45	2009	Design of a 100Watt High-Efficiency Power Amplifier for the 10-500MHz Band
GaN HEMT	VM D	0.05	0.5	63	DE	20	10 x2	2011	Development of a WB Highly Efficient GaN VoltageModeClassD VHFUHF Power Amplifier
GaN HEMT	Doherty	3.5	3.55	59	PAE	6.5	6 x2	2013	A LinearandEfficientDohertyPAat3p5GHz
GaN HEMT	F	0.55	1.1	65	DE	10	10	2011	A Novel Hi Eff BB Continuous ClassF RFPA Delivering 74% Average Eff for an Octave BW
GaN HEMT	A/B 2HT	1.9	2.9	60	DE	31.6	45	2010	Design of a BB Highly Efficient 45W GaN PA via Simplified Real Freq Technique
GaN HEMT	J	1.4	2.7	50	PAE	10	10	2009	Methodology4RealizingHiEffClassJinaLinearBroadbandPA
LDMOS	B	0.5	0.505	66	PAE	680	1000	2012	Developments of High CW RF PowerSSAatSoleil
LDMOS	B	1.3	1.305	45	PAE	10000	160	2012	1st Experience At Elbe with new 1.3GHz CWRF System Based on 10kWSSA
LDMOS	B	0.085	0.115	73	PAE	1200	1200	2012	Own work

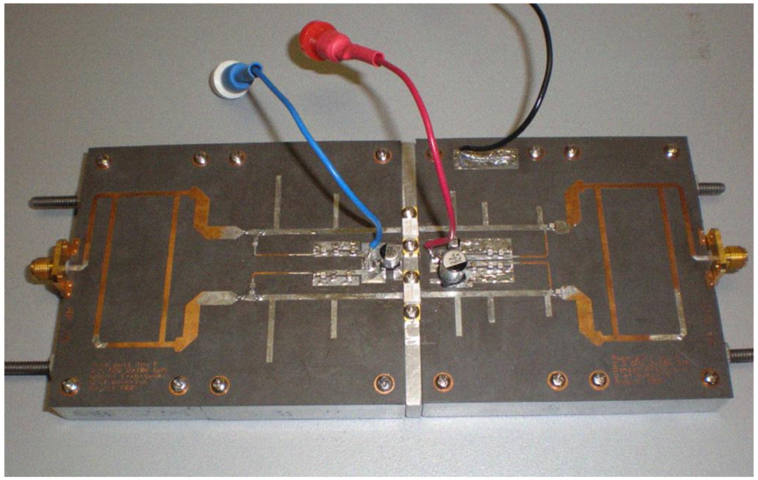
Recommend Cree Website for extensive list of technical papers:
http://www.cree.com/RF/Document-Library

Topology Counts

Balanced Approach:

A number of the papers just referenced used balanced amplifiers to achieve high power and efficiency, particularly the very high power LDMOS. Two GaN exceptions were the broad band “*Design of a 100Watt High-Efficiency Power Amplifier for the 10-500MHz Band”* (left) and the 2.5GHz *“First-Pass Design of High Efficiency Power Amplifiers using Accurate Large Signal Models”* (right). Interesting both use devices capable of 2x the output power they achieve.

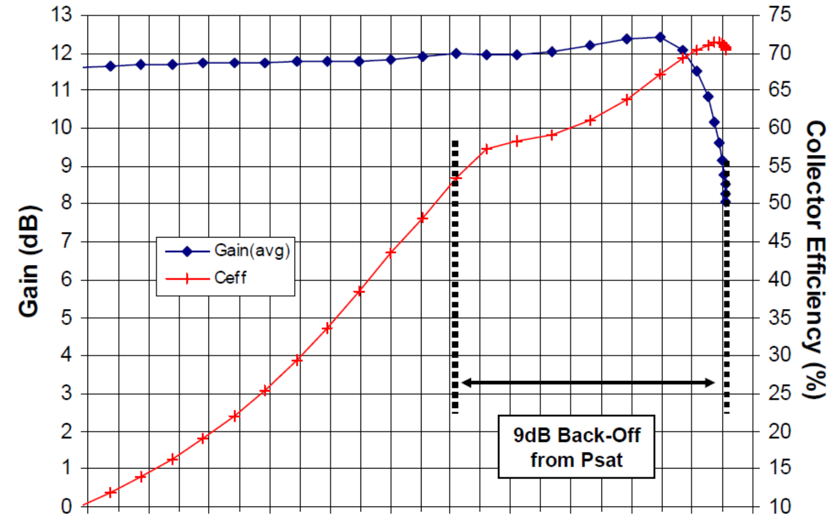




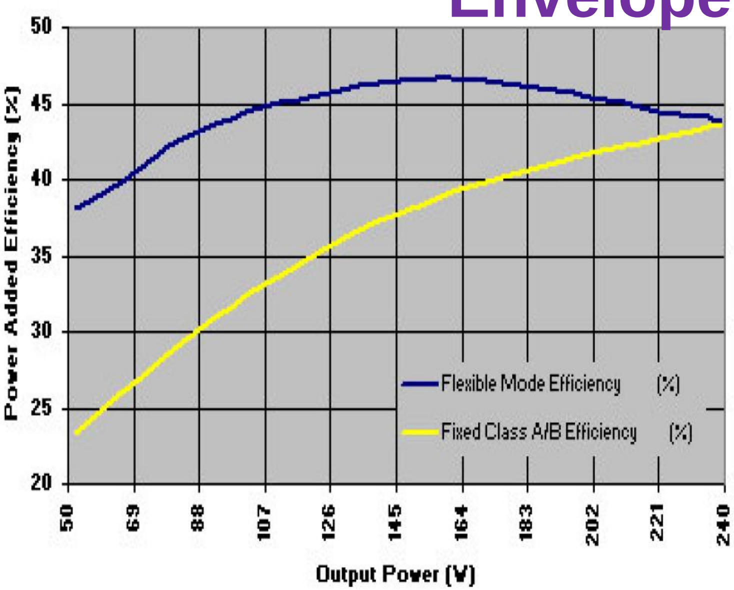
Topology Counts

Doherty Approach:

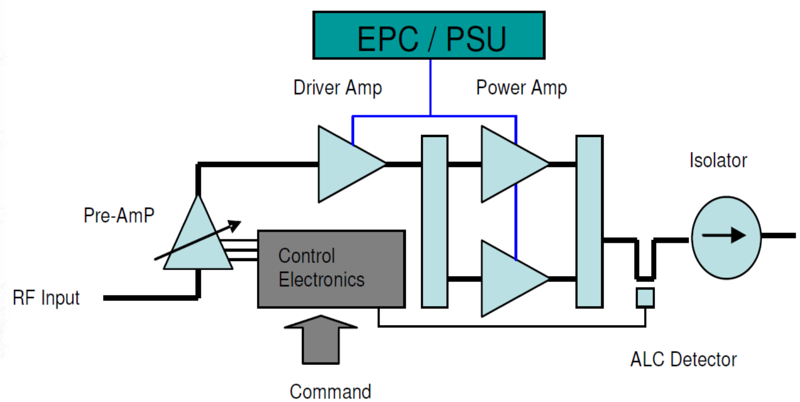
Uses parallel devices to increase efficiency at back off as graph from "*Doherty Power Amplifiers using 2nd Generation HVHBT Technology for High Efficiency Basestation Applications*".



Envelope Tracking



Astrium 200W GaN demonstrator performance using drain bias adjustment for increased PAE.



Summary

a) Device self-heating model.

b) Input match.

c) Wide Band designs ‘tapered’ input drive level.

d) Observe the Current Generator Plane waveforms – 6 port device model.

e) Don’t forget mismatch and insertion losses of output matching circuit.

f) Harmonic terminations - they can both enhance and degrade performance.

g) Models aren’t valid over an infinite range.

Questions?

Thank You!

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