Ingenic® X1000

Hardware Design Guide

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Ingenic Semiconductor Co., Ltd.

Ingenic X1000
Hardware Design Guide

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Release history

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2015.09	1.0	First release
2015.09	2.0	update

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1 Schematics Design

1.1 Power

In order to optimize the power consumption, X1000 has up to 12 power domain, and the recommended design please refer to diagram 1-1,

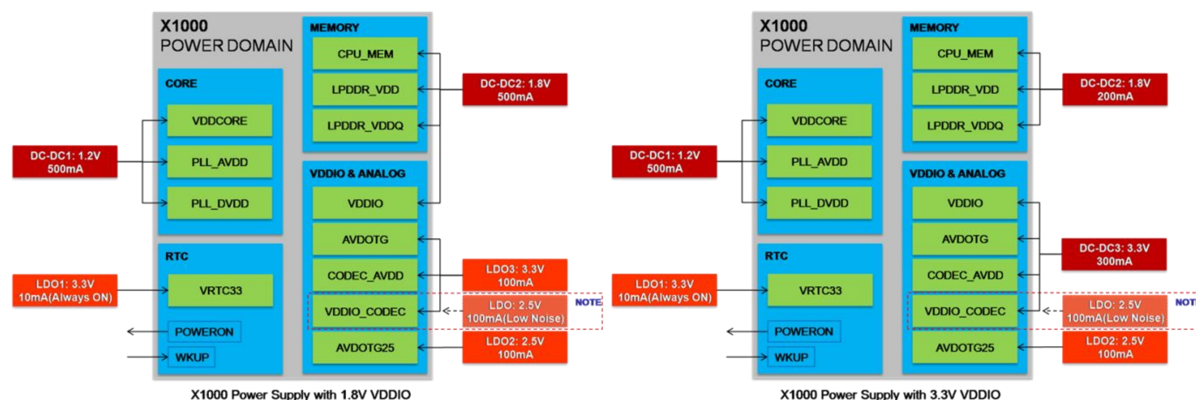

Diagram 1-1 X1000 Power Design

The different between the two design is the voltage of VDDIO(the advantage of 1.8V is low power consumption), please select suitable voltage based on the peripherals.

If need high quality SNR(higher than 85dB) audio output, please add a separate low noise LDO for VDDIO_CODEC.

The POWERON pin is a power enable signal output from CPU， after VDDRTC powered up, the signal will output HIGH, we can use POWERON to enable the power IC. The power ON sequence please refer to diagram 1-2,

Diagram 1-2 X1000 Power ON sequence

Additional notes,

1) The high frequency impedance of the power depends on the inductance of the power, so we need add multistage capacitor filter to VDDCORE and VDDMEM, to increase the filter range of capacitor and decrease the high frequency impedance, such as 22uF, 0.1uF, 0.01uF.
2) When a module is NOT used in product, the power supply of the module can NOT be removed. But the filter capacitor and bead can be saved.
3) For the 5V power adapter, in order to avoid the over voltage damaging the power IC, can add OVP IC or Zener diode.

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1.2 Clock

X1000 needs two clock source, one is 24MHz main clock, another is 32.768KHz RTC clock. the reference design please refer to diagram 1-3,

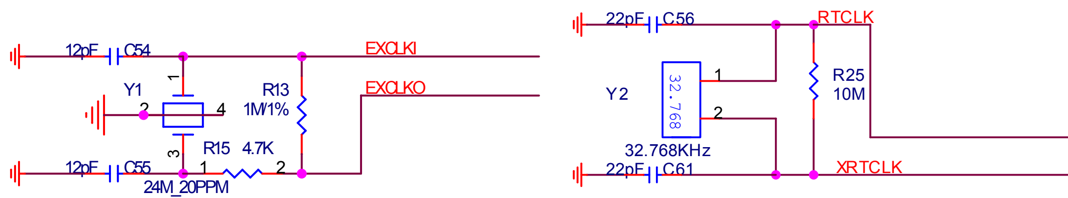

Diagram 1-3 X1000 Clock

When change the crystals, please adjust the C54 and C55, C56 and C61 based on the datasheet of the crystals to guarantee the clock distortionless.

Meanwhile, X1000 can output clock for other devices, please refer to table 1-1,

Table 1-1 X1000 clock output

Num.	Clock range	Output pin	description
1	32KHz	T5	For GPS, Bluetooth and FM radio
2[1]	24MHz~100MHz	L1，K1，K2，J1	The frequency can be configured by software, please refer to the programming guide of TCU module

NOTE: 1. The power domain of the 4 pins is VDDIO.

1.3 VREF

VREF is the reference voltage of LPDDR, should match the specification of SSTL, need add 0.1uF capacitor to each VREF pin.

The default voltage of VREF is half voltage of LPDDR, the reference design please refer to diagram 1-4.

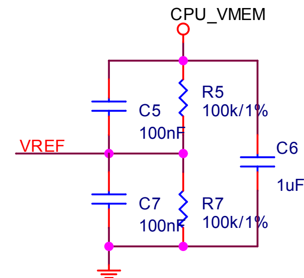

Diagram 1-4 VREF Ref. circuits

1.4 Boot Mode

X1000 has 3 pins for boot mode selected, the supported boot mode please refer to table 1-2.

Table 1-2 X1000 boot mode configuration

Boot_sel2	Boot_sel1	Boot_sel0	Description
H	X	X	EXTCLK is 26MHz
L	X	X	EXTCLK is 24MHz
X	H	H	Boot from SFC0
X	L	H	Boot from MMC(MSC0)
X	H	L	Boot from USB OTG 2.0 device mode

NOTE: X means "DON'T CARE", the 3 pins should NOT be used for output.

The following two sections describes two general boot mode reference design, each mode including two part, boot mode selecting and storage.

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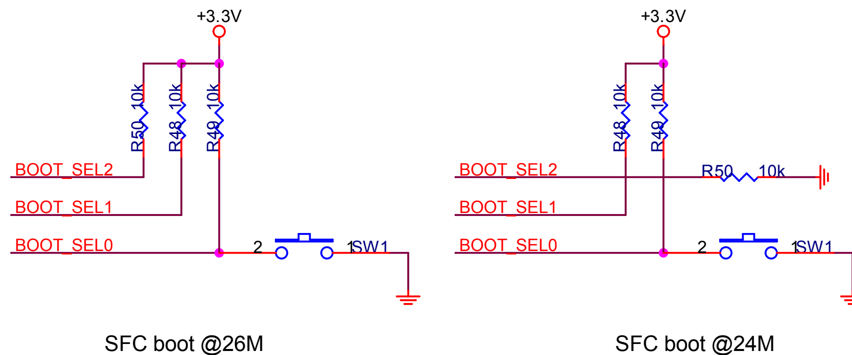
1.4.1 SFC boot with USB updating

Boot mode refer to diagram 1-5, including 24MHz and 26MHz two crystals reference design,



SFC boot @26M SFC boot @24M

Diagram 1-5 SFC boot with USB updating

In order to select SFC boot and USB updating mode, we design a KEY(SW1), SW1 UP is SFC boot mode, and DOWN is USB updating mode. If booting from SFC failed, the system will enter USB updating mode automatically.

The SFC of X1000, DR is data input, and DT is data output, based on the GD25Q128CS1G, refer to diagram 1-6,

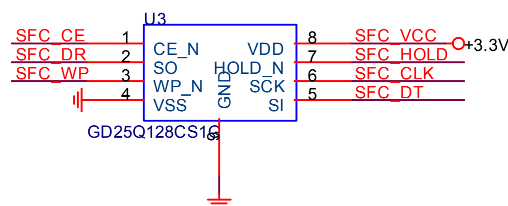
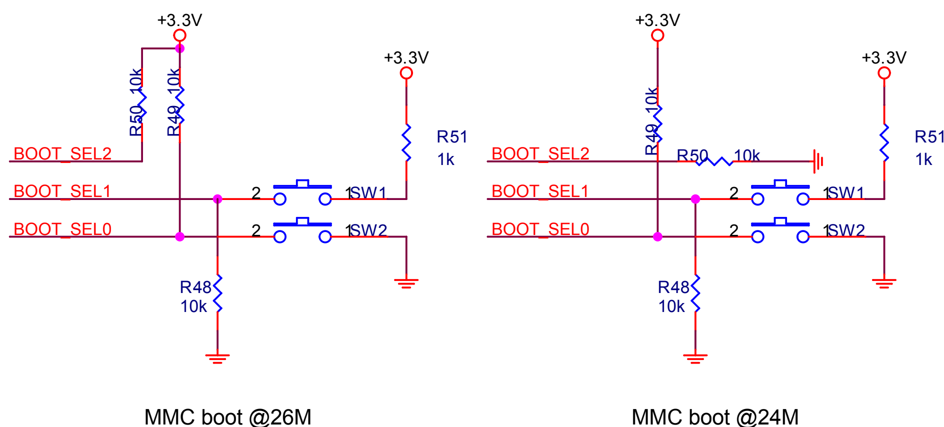


Diagram 1-6 SFC storage reference circuit

1.4.2 MMC boot with USB updating

Boot mode refer to diagram 1-7, including 24MHz and 26MHz two crystals reference design,



MMC boot @26M MMC boot @24M

Diagram 1-5 MMC boot with USB updating

In order to select MMC boot and USB updating mode, we design two KEYs(SW1, SW2), both SW1 and SW2 UP is MMC boot mode, and both DOWN is USB updating mode. If booting from MMC failed, the system will enter USB updating mode automatically, too.

And only the MSC in group A can support boot function, the data line and command line need pull up resistance, the range of the resistant is about 10K~100K OHM for data line and 4.7K~100K OHM for

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command line. If we use MMC socket, we need add the card detect pin(while control the power supply of MMC) and ESD, please refer to diagram 1-8,

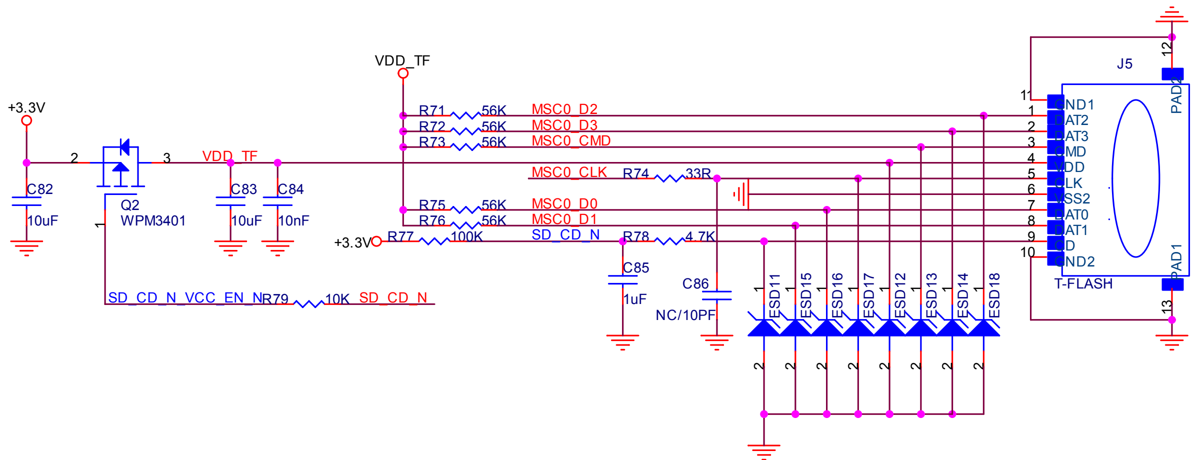

Diagram 1-8 MMC card reference circuit

If we use eMMC or iNand, the circuit will be simplified, please refer to diagram 1-9,

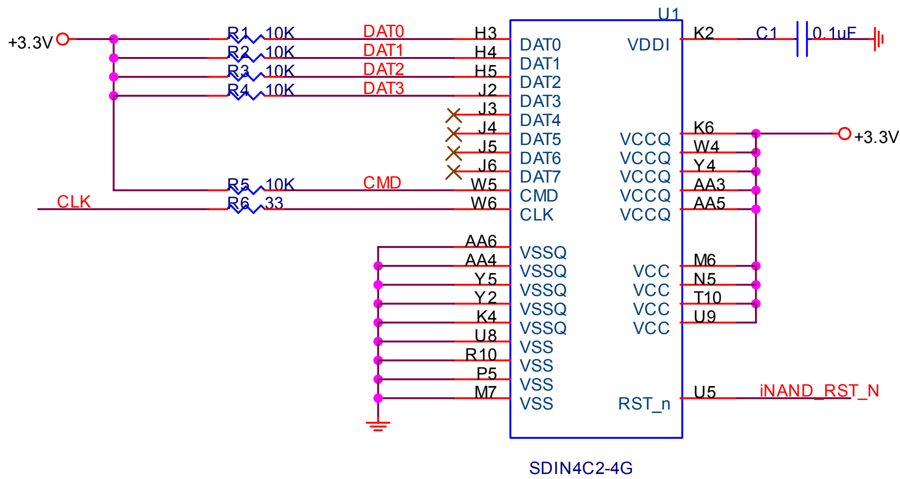

Diagram 1-9 SDIN4C2-4G reference design

If do NOT need camera interface, can use 8 data line for MMC, this will make the performance of MMC double.

1.5 OTG

1) The pin of TXR_RKL needs a 43.2 OHM(1%) pull down resistant.

2) In order to reduce the power consumption, we need connect the ID pin of OTG to a OTG ID pin and a GPIO for interrupt. When the OTG cable is inserted, the pin of ID is LOW, and the GPIO will generate low level interrupt, and then the system will enable OTG PHY and detect the device is HOST or SLAVE inserted. And please refer to the diagram 1-10,

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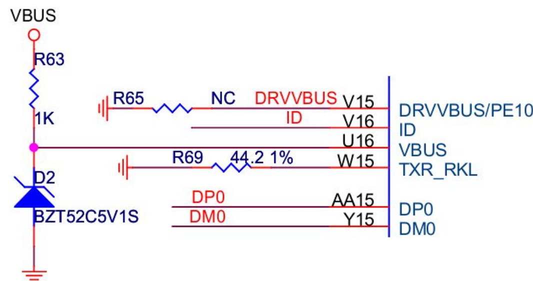

Diagram 1-10 OTG Reference circuits

3) If the OTG acts as device only, the VBUS, DRVVBUS of X1000 can be floating.

1.6 Audio

1.6.1 Digital MIC interface

X1000 can support MIC phone array(4 MIC phone). Please refer to diagram 1-11, is two digital MIC phone reference design, the LR pin of digital MIC, one is HIGH, and another is LOW.

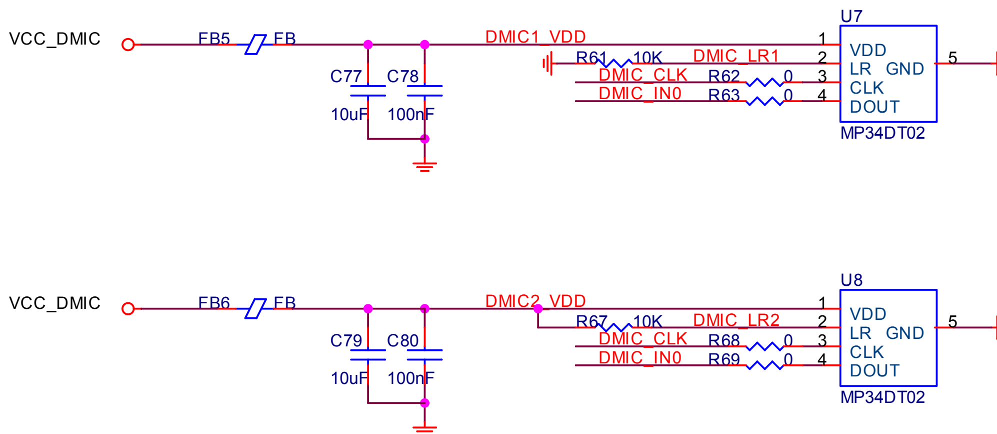

图 **1-11 Digital MIC phone interface**

1.6.2 Internal Codec

X1000 integrates a high quality audio codec, can use the analog MIC phone to recording.

And the output signal is differentia PWM, can drive the digital amplifier directly. If using analog amplifier, need add multistage filter circuits to convert the digital signal to analog, and the reference circuit please refer to diagram 1-12, and for the different amplifier, we need adjust the parameter of the circuits.

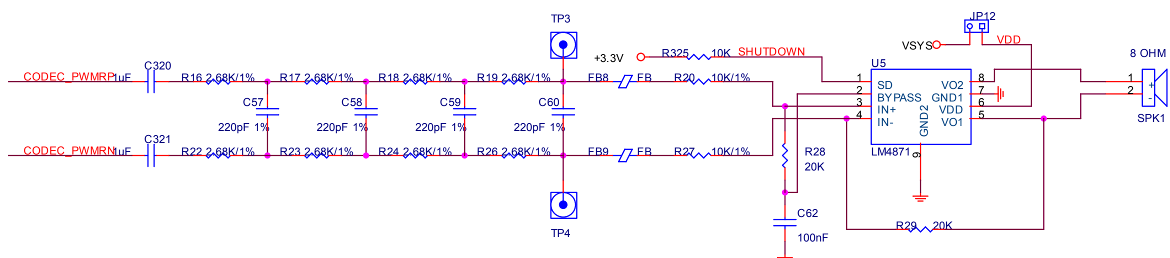

Diagram 1-12 Four stage Butterworth filter

If need high SNR output, recommend the VDDIO_CODEC of X1000 use a separate low noise LDO(the PSRR is more than 70dB).

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1.6.3 External Codec

If the integrated audio codec can NOT match the requirement, can using the I2S to extend a external codec, to get the more better performance of the audio.
And please notice, the external codec and internal codec can NOT work at the same time.

1.7 OTP EFUSE

The OTP has two work mode, one is READ mode, and another is PROGRAM mode.
The different of the two mode is the voltage of AVDEFUSE, if the voltage is 0, and then the OTP is under the READ mode. And if need program the OTP, can control the voltage to 2.5V(±10%) by software, the OTP will enter PROGRAM mode, and please note that the PROGRAM time MUST be less than 1 second. Please refer to the diagram 1-13,

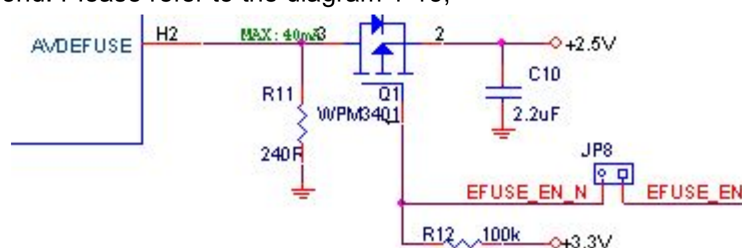

Diagram 1-13 OTP EFUSE

1.8 Other peripherials

X1000 can support 8-bit, 9-bit and 16-bit SLCD, if the PCB has the area, please series resistance(33 OHM) series resistance to reduce the EMI issue.
X1000 integrated RMII MAC controller, can support RMII 10/100M adaptive Ethernet PHY, and X1000 can output 50MHz clock for the PHY.

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2 PCB Design

2.1 PCB Placement

The filter capacitor of VDDCORE, VDDMEM, VDDPLL, VDDIO, should as close as possible to X1000. And the VDDCORE, VDDMEM, VDDIO, need copper at the power layer, NOT using the trace. If change the layer, please make sure there has enough via.

The potentiometer circuit of VREF should be close to X1000, the should be shorter the layout, and the recommended trace width is 20mil, and please make sure the spacing is more than 3W.

The priority of the capacitor of CPU power supply,

1st, PLLAVDD, PLLDVDD, VDDCORE, VDDMEM, VCAP, VREF, VDDIO_CODEC

2nd, CODEC_AVDD, AVDOTG25, AVD_OTG, VDDIO

3rd, VDDRTC, VDDEFUSE

Please make sure the power and ground as solid as possible, do NOT separate by VIA or routing.

2.2 PCB laminates and impedance requirement

2.2.1 PCB laminates

X1000 recommends using 4-layer laminates, and the layer is TOP-GND-POWER-BOTTOM, please refer to diagram 2-1,

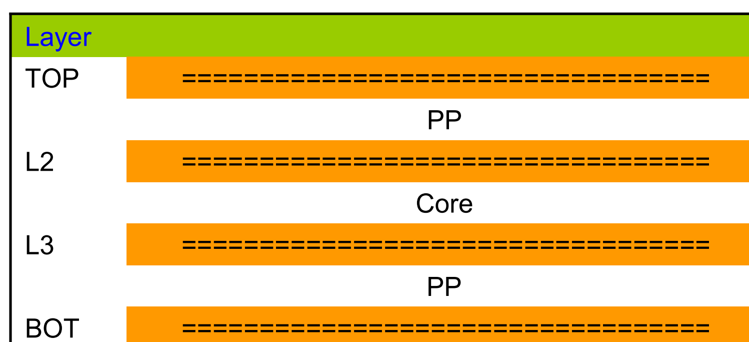

Diagram 2-1 4-Layer laminates

2.2.2 Impedance requirements

The impedance of single end should keep at 50OHM ±10%, reference the layer 2; the impedance of difference should keep at 90OHM ±10%, the mutation of inner and outer wiring impedance should be less than 20 OHM ±10%. And other difference should be keep at 100OHM ±10%.

2.3 PCB Layout

2.3.1 Via

1) 8mil/16mil via is suggested to be used for normal situation.
2) 12mil/24mil via is suggested to be used for power and ground. 12mil/24mil via means the aperture is 12mil and the outer ring is 24mil.

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2.3.2 pour manager

1) The clearance rule of via and copper should NOT be smaller than 6mil.

2.3.3 Thermal Dissipation

1) The thickness of copper is suggested to be 1OZ, which is good for thermal dissipation.
2) The designer should add GND VIAs as many as possible after CPU fans out, on condition that the integrity of power plane is OK.
3) The ground plane must be as integrated as possible. There must be multiple pathways that connect the center of CPU and outside CPU.
4) Shield should be connected to GND as quickly as possible.
5) The board edge should be surrounded with ground via (through-hole), and the copper of ground should be exposed where the metal shell connect the board’s ground. It is good for ESD and thermal dissipation.
6) The heating components should NOT be close to CPU, it should be placed nearby the opening of the shell (such as radiator grille, the opening of big connector, and etc.), and it is better to keep the components with the opening line.

2.3.4 Power

1) The copper under CPU (ground and power) should be integrated and continuous. Then the copper supply a good return line for CPU’s signals. It is better for improving the signal transmission, the stability of the products and thermal dissipation.
2) All the ground pad should be add VIAs to connect the ground layer, and the distance between the VIAs and pad should be as close as possible.
3) Power line should be as short as possible. Copper pour is better than trace and close to GND layer.

2.3.5 USB layout

USB OTG need differential traces and meet 90 Ohm differential impedance .

2.3.6 Audio layout

AIP/AIN and AOLOP/AOLON need differential traces. In order to avoid interface the differential traces should be surrounded by GND traces and GND VIAs.

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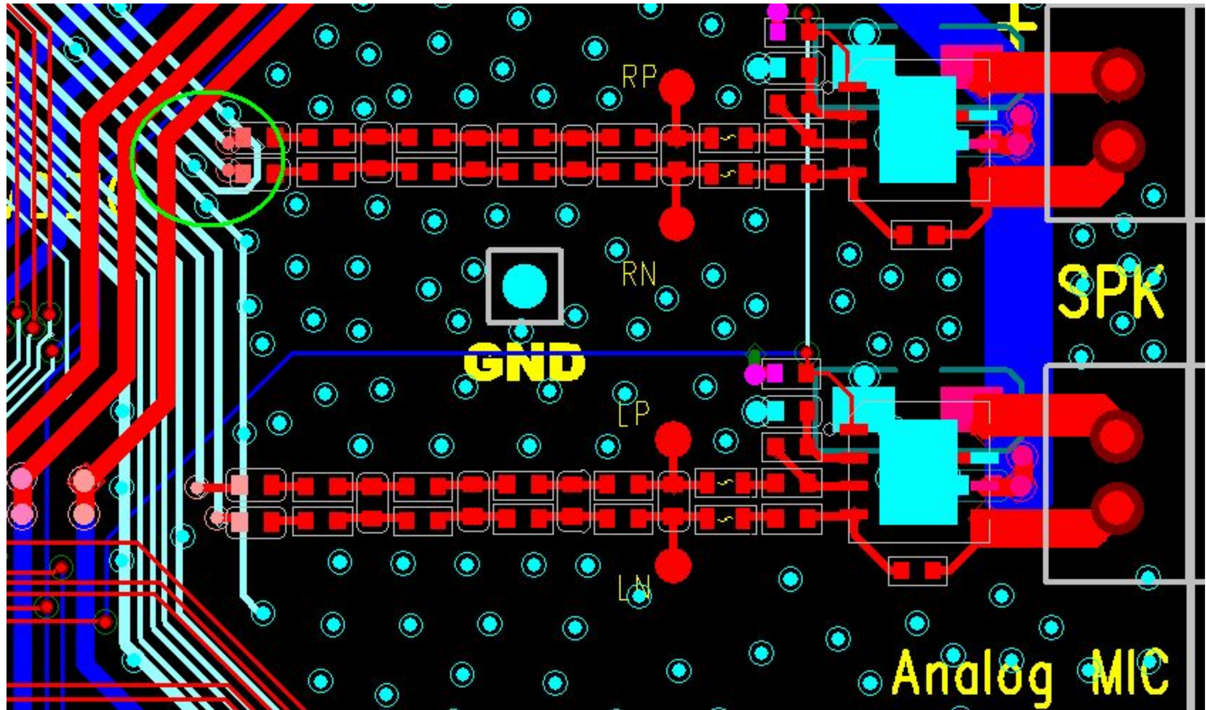

Diagram 2-2 Audio Layout

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