GreenPAK Programmable Mixed Signal Matrix with In System Programmability

PRELIMINARY

General Description

The SLG46824 provides a small, low power component for commonly used mixed-signal functions. The user creates the circuit design by programming the multiple time Non-Volatile Memory (NVM) to configure the interconnect logic, the IOs and the macrocells of the SLG46824. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Two Low Power General Purpose Rail-to-Rail Analog Comparators (ACMPxL)
- One Voltage Reference (Vref)
  - One Vref Output
- Eleven Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Six Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/Latch or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/Latch or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter with Edge Detector
- Three Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Power On Reset (POR)
- In System Programmability
- Multiple Time Programmable Memory
- Wide Range Power Supply
  - 2.5 V (±8 %) to 5 V (±10 %) V_{DD}
  - 1.8 V (±5 %) to 5 V (±10 %) V_{DD2} ($V_{DD2} \leq V_{DD}$)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Two Packages Available
  - 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch
  - 20-pin TSSOP: 6.5 x 6.4 x 1.2 mm, 0.65 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Smartphones and Fitness Bands
- Notebook and Tablet PCs

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1 Block Diagram

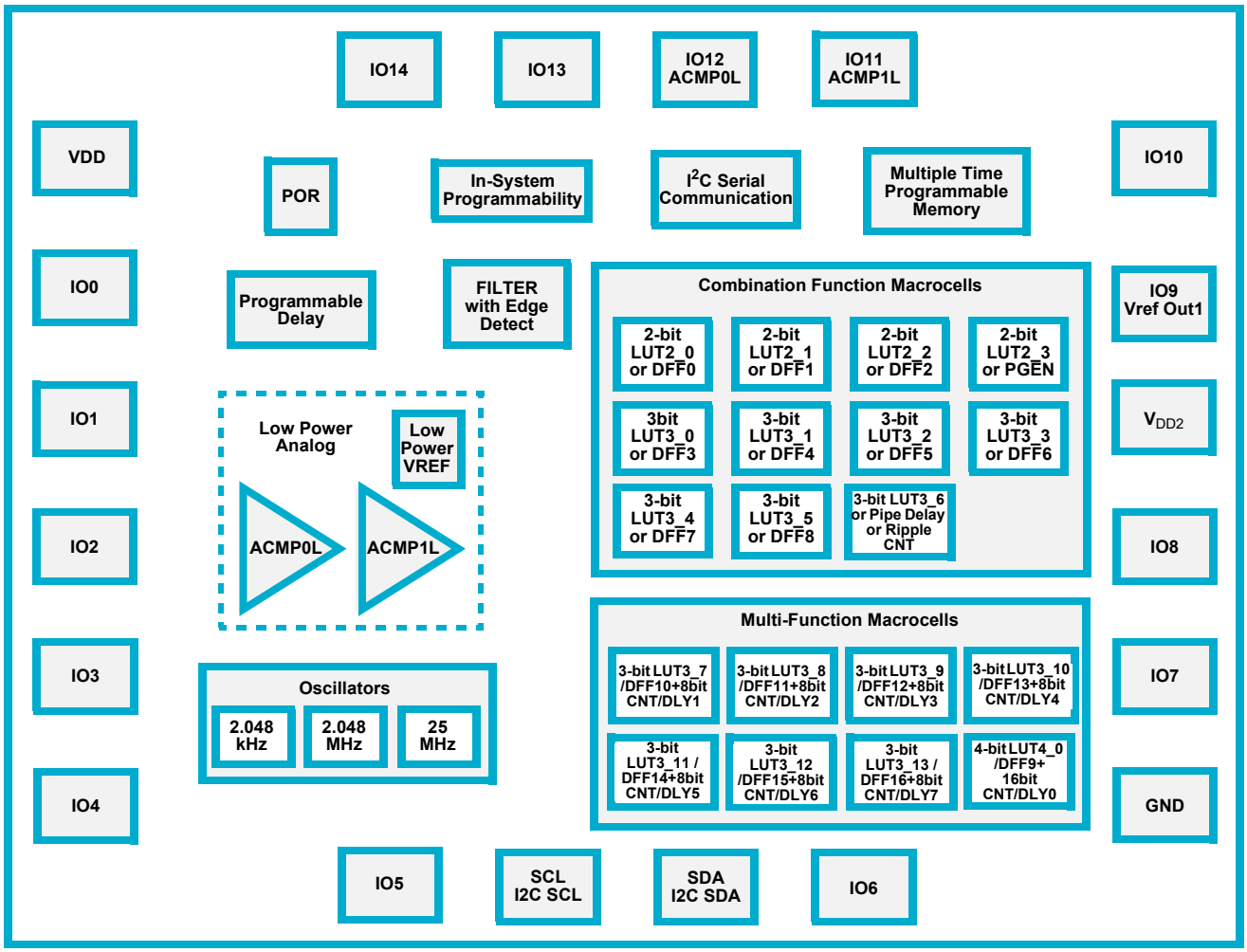
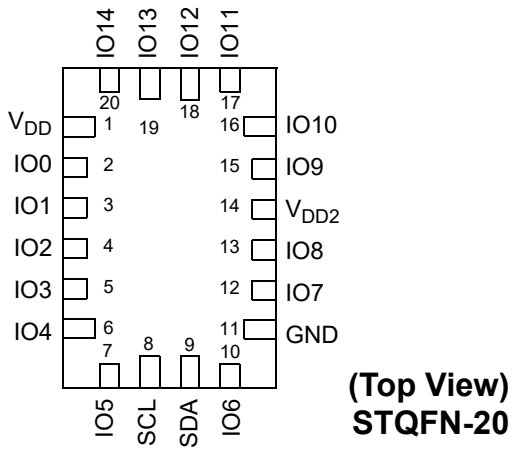


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - STQFN- 20L



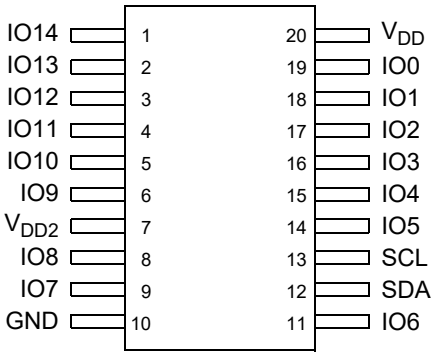
(Top View)
STQFN-20

Pin #	Signal Name	Pin Functions
1	V_{DD}	Power Supply
2	IO0	GPIO
3	IO1	GPIO or VREF IN
4	IO2	GPIO, SLA<3>
5	IO3	GPIO, SLA<2>
6	IO4	GPIO, SLA<1>
7	IO5	GPIO, SLA<0>
8	SCL	I2C_SCL
9	SDA	I2C_SDA
10	IO6	GPIO
11	GND	Ground
12	IO7	GPIO
13	IO8	GPIO
14	V_{DD2}	Power Supply
15	IO9	GPIO or VREF_OUT1
16	IO10	GPIO
17	IO11	GPIO or ACMP1L_IN
18	IO12	GPIO or ACMP0L_IN
19	IO13	GPIO
20	IO14	GPIO

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
VREFx: Voltage Reference Output
EXT_CLKx: External Clock Input
SLA: Slave Address

2.2 PIN CONFIGURATION - TSSOP-20L



TSSOP-20
(Top View)

Pin #	Signal Name	Pin Functions
1	IO14	GPIO
2	IO13	GPIO
3	IO12	GPIO or ACMP0L_IN
4	IO11	GPIO or ACMP1L_IN
5	IO10	GPIO
6	IO9	GPIO or VREF_OUT1
7	V_{DD2}	Power Supply
8	IO8	GPIO
9	IO7	GPIO
10	GND	Ground
11	IO6	GPIO
12	SDA	I2C_SDA
13	SCL	I2C_SCL
14	IO5	GPIO, SLA<0>
15	IO4	GPIO, SLA<1>
16	IO3	GPIO, SLA<2>
17	IO2	GPIO, SLA<3>
18	IO1	GPIO or VREF IN
19	IO0	GPIO
20	V_{DD}	Power Supply

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
VREFx: Voltage Reference Output
EXT_CLKx: External Clock Input
SLA: Slave Address

Table 1: Functional Pin Description

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
1		V_{DD}	VDD	Power Supply	--	--
			ACMP0L+	Analog Comparator 0 Positive Input	Analog	
			ACMP1L+	Analog Comparator 1 Positive Input	Analog	
2		IO0	IO0	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			I2C_EXPAND_0	--	--	--
			EXT_OSC0_IN	External Clock Connection	--	--

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
3		IO1	IO1	General Purpose IO with OE (Note 1)	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_VREF	Analog Comparator Negative Input	Analog	--
				--	--	--
4		IO2	IO2	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
5		IO3	IO3	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
6		IO4	IO4	General Purpose IO with OE (Note 1)	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			CHIP_RESET	--	--	--
7		IO5	IO5	General Purpose IO with OE (Note 1)	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			I2C_EXPAND_1	--	--	--
8		SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
9		SDA	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
10		IO6	IO6	General Purpose Output	--	Push-Pull (1x) (2x)
					--	Open Drain NMOS (1x) (2x)
					--	--
			I2C_EXPAND_2	--	--	--

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
11		GND	GND	Ground	--	--
12		IO7	IO7	General Purpose Output	--	Push-Pull (1x) (2x)
					--	Open Drain NMOS (1x) (2x)
					--	--
13		IO8	IO8	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_OSC2_IN	--	--	--
14		V_{DD2}	V_{DD2}	Power Supply	--	--
15		IO9	IO9	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			VREF1_OUT	Voltage Reference 1 Output	--	Analog
			I2C_EXPAND_3	--	--	--
16		IO10	IO10	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_OSC1_IN	--	--	--
17		IO11	IO11	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Slave Address <0>	--	--	--
			ACMP1L+	Analog Comparator 3 Positive Input	Analog	--
18		IO12	IO12	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Slave Address <1>	--	--	--
			ACMP0L+	Analog Comparator 2 Positive Input	Analog	--

Pin No.		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN 20L	TSSOP 20L					
19		IO13	IO13	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Slave Address <2>	--	--	--
20		IO14	IO14	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Slave Address <3>	--	--	--

Note 1: General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	-0.3	7	V
Current at Input Pin	-1.0	1.0	mA
Input leakage (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

3.2 RECOMMENDED OPERATING CONDITIONS

Table 3: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
Supply Voltage (V_{DD})	During NVM Write command	2.5	5.5	V
Supply Voltage 2 (V_{DD2})	$V_{DD2} \leq V_{DD}$	1.71	5.5	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3 (Note 2)	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.3 ELECTRICAL CHARACTERISTICS

Table 4: Electrical Characteristics at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 3)	0.7x V_{DD} (Note 2)	--	V_{DD}+ 0.3 (Note 2)	V
		Logic Input with Schmitt Trigger	0.8x V_{DD} (Note 2)	--	V_{DD}+ 0.3 (Note 2)	V
		Low-Level Logic Input (Note 3)	1.25	--	V_{DD}+ 0.3 (Note 2)	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 3)**	GND-0.3	--	0.3x V_{DD} **(Note 2)**	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD} **(Note 2)**	V
		Low-Level Logic Input **(Note 3)**	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD2} = 1.8 V +/- 5 %	0.1	0.4	0.7	V
		V_{DD} = 2.5 V +/- 8 % **(Note 2)**	0.4	0.6	0.8	V
		V_{DD} = 3.3 V +/- 10 % **(Note 2)**	0.5	0.7	0.9	V
		V_{DD} = 5 V +/- 10 % **(Note 2)**	0.7	1.0	1.2	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	1.68	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	2.29	2.493	--	V
		Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	2.73	3.12	--	V
		Push-Pull, I_{OH} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	4.19	4.78	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 5 % **(Note 2)**	1.70	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	2.294	2.497	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	2.87	3.21	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	4.32	4.89	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	--	0.010	0.015	V
		Push-Pull, I_{OL}= 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	--	0.06	0.13	V
		Push-Pull, I_{OL} = 3 mA,1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	--	0.13	0.23	V
		Push-Pull, I_{OL}= 5 mA, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	--	0.16	0.27	V
		Push-Pull, I_{OL}= 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 5 %	--	0.007	0.010	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	--	0.03	0.06	V
		Push-Pull, I_{OL}= 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	--	0.06	0.11	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	--	0.08	0.14	V
		NMOS OD, I_{OL}= 100 µA, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	--	0.007	0.010	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	NMOS OD, I_{OL} = 100 µA, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	--	0.03	0.06	V
		NMOS OD, I_{OL} = 3 mA, 1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	--	0.08	0.15	V
		NMOS OD, I_{OL} = 5 mA, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	--	0.10	0.18	V
		NMOS OD, I_{OL}= 100 µA, 2X Drive, V_{DD2} = 1.8 V +/- 5 %	--	0.003	0.010	V
		NMOS OD, I_{OL} = 100 µA, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	--	0.02	0.03	V
		NMOS OD, I_{OL} = 3 mA, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	--	0.04	0.08	V
		NMOS OD, I_{OL} = 5 mA, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	--	0.05	0.11	V
I_{OH}	HIGH-Level Output Current	Push-Pull, V_{OH} = V_{DD2} - 0.2, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	1.03	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	1.07	1.70	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	22.08	34.04	--	mA
		Push-Pull, V_{OH} = V_{DD2} - 0.2, 2X Drive, V_{DD2} = 1.8 V +/- 5 %	2.03	3.41	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	2.22	3.41	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	11.54	24.16	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	41.46	68.08	--	mA
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	0.92	1.66	--	mA
		Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	4.87	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	7.21	11.58	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V +/- 5 %	1.83	3.30	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	1.83	3.38	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	9.75	16.49	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	13.83	23.16	--	mA
		NMOS OD, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V +/- 5 %	1.38	2.53	--	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Current	NMOS OD, V_{OL} = 0.15 V, 1X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	1.37	2.53	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	7.31	12.37	--	mA
		NMOS OD, V_{OL} = 0.4 V, 1X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	10.82	17.38	--	mA
		NMOS OD, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V +/- 5 %	2.75	5.07	--	mA
		NMOS OD, V_{OL} = 0.15 V, 2X Drive, V_{DD} = 2.5 V +/- 8 % **(Note 2)**	2.75	5.07	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 3.3 V +/- 10 % **(Note 2)**	14.54	24.74	--	mA
		NMOS OD, V_{OL} = 0.4 V, 2X Drive, V_{DD} = 5 V +/- 10 % **(Note 2)**	17.34	34.76	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.30	2.15	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.63	1.85	2.04	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.01	1.26	1.49	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD} **(Note 2)**	0.74	1.10	1.50	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD} **(Note 2)**	88	107	132	kΩ
		10 k For Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD} **(Note 2)**	7	10	17	kΩ
C_{IN}	Input Capacitance			4		pF

Note 2: IOs 0 to 6, SCL, SDA are powered from V_{DD} and IOs 7 to 14 are powered from V_{DD2}.

Note 3: No hysteresis.

Table 5: I2C Specifications

Symbol	Parameter	Condition/Note	Fast-Mode			Fast-Mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL	V_{DD} = 2.3 V to 5.5 V	--	--	400	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = 2.3 V to 5.5 V	1300	--	--	500	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = 2.3 V to 5.5 V	600	--	--	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.3 V to 5.5 V	--	--	50	--	--	50	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = 2.3 V to 5.5 V	--	--	900	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = 2.3 V to 5.5 V	1300	--	--	500	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = 2.3 V to 5.5 V	600	--	--	260	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = 2.3 V to 5.5 V	600	--	--	260	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = 2.3 V to 5.5 V	0	--	--	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = 2.3 V to 5.5 V	100	--	--	50	--	--	ns
t_R	Inputs Rise Time	V_{DD} = 2.3 V to 5.5 V	--	--	300	--	--	120	ns
t_F	Inputs Fall Time	V_{DD} = 2.3 V to 5.5 V	--	--	300	--	--	120	ns
t_{SU_STD}	Stop Set-up Time	V_{DD} = 2.3 V to 5.5 V	600	--	--	260	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = 2.3 V to 5.5 V	50	--	--	50	--	--	ns

Table 6: Typical Current Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent (I2C enable)	0.42	0.43	0.54	µA
		Vref	0.42	0.43	0.54	µA
		Vref (ACMPxL, 0.32mV)	4.22	4.29	4.59	µA
		Each additional ACMPL add	1.22	1.24	1.36	µA
		OSC2 25 MHz, predivide = 1	135.81	150.93	244.49	µA
		OSC2 25 MHz, predivide = 4	50.25	54.95	84.51	µA
		OSC2 25 MHz, predivide = 8	35.65	38.58	57.19	µA
		OSC1 2.048 MHz, predivide= 1	17.03	17.53	20.44	µA
		OSC1 2.048 MHz, predivide= 4	14.17	14.38	15.62	µA
		OSC1 2.048 MHz, predivide= 8	13.68	13.84	14.79	µA
		OSC0 2.048 kHz, predivide = 1	0.71	0.72	0.86	µA
		OSC0 2.048 kHz, predivide = 4	0.70	0.72	0.85	µA
		OSC0 2.048 kHz, predivide = 8	0.70	0.72	0.85	µA
		1x push-pull + 4 pF @ 25 kHz	0.4	5	16	µA
		1x push-pull + 4 pF @ 2 MHz	22	47	106	µA

3.4 TIMING CHARACTERISTICS

Table 7: Typical Delay Estimated for Each Macrocell at T = 25°C

Symbol	Parameter	Note	V_{DD} = 2.5 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1X	26	29	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	26	28	16	17	18	12	ns
tpd	Delay	Digital input to PMOS output	29	--	17	-	12	-	ns
tpd	Delay	Digital input to NMOS output	--	44	-	27	-	18	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	29	--	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	--	28	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	19	18	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	19	18	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	21	20	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	23	22	21	17	15	12	ns
tpd	Delay	CNT/DLY Logic	41	43	18	15	13	11	ns
tpd	Delay	P DLY1C	225	225	166	163	123	120	ns
tpd	Delay	P DLY2C	420	420	314	312	233	231	ns
tpd	Delay	P DLY3C	630	630	462	460	343	341	ns
tpd	Delay	P DLY4C	835	835	609	609	451	451	ns
tpd	Delay	Filter	120	120	78	78	53	53	ns
tpd	Delay	ACMP (5 mV overdrive, IN- = 600 mV)	2000	2000	2000	2000	2000	2000	ns
tw	width	IO with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	75	75	55	55	35	35	ns

Table 8: Programmable Delay Expected Delays and Widths (Typical)

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time1	Width, 1 cell	mode:(any) edge detect, edge detect output	325	150	110	ns
time1	Width, 2 cell	mode:(any) edge detect, edge detect output	740	300	225	ns
time1	Width, 3 cell	mode:(any) edge detect, edge detect output	1020	450	340	ns
time1	Width, 4 cell	mode:(any) edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode:(any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode:(any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode:(any) edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode:(any) edge detect, edge detect output	44	18	14	ns
time1	Width, 1 cell	mode: delayed (any)e dge detect, delayed edge detect output	340	150	110	ns
time1	Width, 2 cell	mode: delayed (any) edge detect, delayed edge detect output	670	300	220	ns
time1	Width, 3 cell	mode: delayed (any) edge detect, delayed edge detect output	1000	450	335	ns
time1	Width, 4 cell	mode: delayed (any) edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 2 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any) edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

Table 9: Typical Filter Rejection Pulse Width at T=25°C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 123	< 84	< 52	ns

Table 10: Typical Counter/Delay Offset Measurements

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Power ON time	25 MHz	auto	0.13	0.13	0.13	µs

Table 10: Typical Counter/Delay Offset Measurements

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Power ON time	2.048 MHz	auto	0.3	0.4	0.4	µs
Power ON time	2.048 kHz	auto	660	570	480	µs
frequency settling time	25 MHz	auto	4	4	8	µs
frequency settling time	2.048 MHz	auto	0.3	0.4	0.4	µs
frequency settling time	2.048 kHz	auto	660	570	480	µs
variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2.048 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.5 OSC CHARACTERISTICS

3.5.1 Oscillator0 2.048 kHz

Table 11: Oscillator0 2.048 kHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
2.5 V ±8 %	2.026	2.071	1.907	2.088
3.3 V ±10 %	2.025	2.070	1.906	2.088
5 V ±10 %	2.025	2.071	1.905	2.087
2.5 V to 4.5 V	2.026	2.071	1.906	2.088
2.3 V to 5.5 V	2.025	2.071	1.905	2.088

Table 12: Oscillator0 2.048 kHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.07 %	1.12 %	-6.91 %	1.95 %
3.3 V ±10 %	-1.09 %	1.09 %	-6.94 %	1.94 %
5 V ±10 %	-1.12 %	1.11 %	-6.96 %	1.92 %
2.5 V to 4.5 V	-1.09 %	1.10 %	-6.96 %	1.95 %
2.3 V to 5.5 V	-1.12 %	1.12 %	-6.96 %	1.95 %

3.5.2 Oscillator1 2.048 MHz

Table 13: Oscillator1 2.048 MHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8 %	2.021	2.068	1.987	2.088

Table 13: Oscillator1 2.048 MHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
3.3 V ±10 %	2.024	2.069	1.990	2.089
5 V ±10 %	2.026	2.072	1.994	2.092
2.5 V to 4.5 V	2.022	2.071	1.988	2.090
2.3 V to 5.5 V	2.021	2.072	1.987	2.092

Table 14: Oscillator1 2.048 MHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.32 %	0.96 %	-2.98 %	1.93 %
3.3 V ±10 %	-1.14 %	1.01 %	-2.80 %	2.01 %
5 V ±10 %	-1.03 %	1.18 %	-2.61 %	2.13 %
2.5 V to 4.5 V	-1.27 %	1.09 %	-2.91 %	2.04 %
2.3 V to 5.5 V	-1.32 %	1.18 %	-2.98 %	2.13 %

3.5.3 Oscillator2 25 MHz

Table 15: Oscillator2 25 MHz Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±8 %	24.588	25.238	23.622	25.669
3.3 V ±10 %	24.668	25.261	23.678	25.732
5 V ±10 %	24.736	25.353	23.723	25.803
2.5 V to 4.5 V	24.620	25.288	23.656	25.769
2.3 V to 5.5 V	24.588	25.353	23.622	25.803

Table 16: Oscillator2 25 MHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8 %	-1.65 %	0.96 %	-5.51 %	2.68 %
3.3 V ±10 %	-1.33 %	1.05 %	-5.29 %	2.93 %
5 V ±10 %	-1.06 %	1.42 %	-5.11 %	3.21 %

Table 16: Oscillator2 25 MHz Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range			
	+25 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V to 4.5 V	-1.52 %	1.16 %	-5.38 %	3.08 %
2.3 V to 5.5 V	-1.65 %	1.42 %	-5.51 %	3.21 %

3.5.4 OSC Power On delay

Table 17: Oscillators Power On Delay at Room Temperature, OSC Power Mode: "Auto Power On"

Power Supply Range (V_{DD}), V	Oscillator2 25 MHz		Oscillator2 25 MHz Start with delay		Oscillator1 2.048 MHz		Oscillator0 2.048 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
2.30	0.033	0.044	0.132	0.146	0.319	0.657	706.144	908.371
2.50	0.029	0.038	0.130	0.146	0.332	1.045	668.258	855.197
2.70	0.025	0.034	0.129	0.146	0.336	0.792	638.228	811.718
3.00	0.021	0.028	0.128	0.148	0.345	0.972	602.986	759.657
3.30	0.018	0.025	0.127	0.150	0.366	0.842	575.778	718.414
3.60	0.016	0.022	0.127	0.150	0.368	0.464	553.969	685.120
4.00	0.013	0.018	0.128	0.151	0.357	0.451	530.866	648.916
4.20	0.012	0.015	0.128	0.151	0.355	0.540	521.049	633.638
4.50	0.011	0.015	0.128	0.152	0.355	0.732	507.787	613.429
5.00	0.010	0.015	0.129	0.154	0.382	0.881	486.721	582.113
5.50	0.010	0.012	0.130	0.155	0.386	0.774	462.127	551.579

3.6 ACMP SPECIFICATIONS

Table 18: ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP0L, ACMP1L Input Voltage Range	Positive Input	V_{DD} = 2.3 V to 5.5 V	0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP0L, ACMP1L Input Offset Voltage	Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV, V_{DD} = 2.3 V to 5.5 V	T = 25°C	0	--	5.09	mV
			T = (-40 to 85)°C	0	--	5.55	mV
t_{start}	ACMP0L, ACMP1L Start Time	ACMP Power On delay	T = 25°C V_{DD} = 2.3 V to 5.5 V	--	139.3	233.3	µS
			T = (-40 to 85)°C V_{DD} = 2.3 V to 5.5 V	--	144.6	326.6	µS
V_{HYS}	ACMP0L, ACMP1L Built-in Hysteresis	V_{HYS} = 32 mV	T = 25°C	26.46	--	34.43	mV
		V_{HYS} = 64 mV	T = 25°C	56.58	--	67.38	mV
		V_{HYS} = 196 mV	T = 25°C	185.24	--	197.32	mV
		V_{HYS} = 32 mV	T = -40 °C to +85 °C	22.28	--	36.86	mV
		V_{HYS} = 64 mV	T = -40 °C to +85 °C	54.49	--	68.02	mV
		V_{HYS} = 196 mV	T = -40 °C to +85 °C	183.47	--	197.32	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.25x, 0.33x, 0.5x		--	2.0	--	MΩ

Symbol	Parameter	Description/Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP0L, ACMP1L	Gain = 1, V_{DD} = 2.3 V to 5.5 V, Vref = 32 mV to 2016 mV, Overdrive = 5 mV	Low to High, T = -40 °C to +85 °C	--	74.91	139.75	µS
			High to Low, T = -40 °C to +85 °C	--	72.28	213.26	µS
		Gain = 1, V_{DD} = 2.3 V to 5.5 V, Vref = 32 mV to 2016 mV, Overdrive =10 mV	Low to High, T = -40 °C to +85 °C	--	49.54	70.23	µS
			High to Low, T = -40 °C to +85 °C	--	46.92	68.44	µS
		Gain = 1, V_{DD} = 2.3 V to 5.5 V, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High, T = -40 °C to +85 °C	--	18.41	29.06	µS
			High to Low, T = -40 °C to +85 °C	--	16.54	26.87	µS
G	Gain error (including threshold and internal Vref error), T = -40 °C to +85 °C	G = 1, V_{DD} = 2.3 V to 5.5 V		--	1	--	
		G = 0.5, V_{DD} = 2.3 V to 5.5 V		0.497	--	0.504	
		G = 0.33, V_{DD} = 2.3 V to 5.5 V		0.330	--	0.337	
		G = 0.25, V_{DD} = 2.3 V to 5.5 V		0.247	--	0.253	
Vref	Internal Vref error	V_{DD} = 2.3 V to 5.5 V	Vref = 32 mV to 1504 mV, T = -40 °C to +85 °C, Loading = 1 mA	--	±6	--	mV
	Vref Output Capacitance Loading		Resistance Load = 1 MΩ	--	--	15	pF
			Resistance Load = 560 kΩ	--	--	27	pF
			Resistance Load = 100 kΩ	--	--	64	pF
			Resistance Load = 10 kΩ	--	--	120	pF
			Resistance Load = 2 kΩ	--	--	180	pF
			Resistance Load = 1 kΩ, VRef = 32 mV to 1024 mV	--	--	210	pF

3.7 ANALOG TEMPERATURE SENSOR (TS)

4 User Programmability

The SLG46824 is a user programmable device with Multiple-Time-Programmable (MTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Dialog Semiconductor to integrate into a production process.

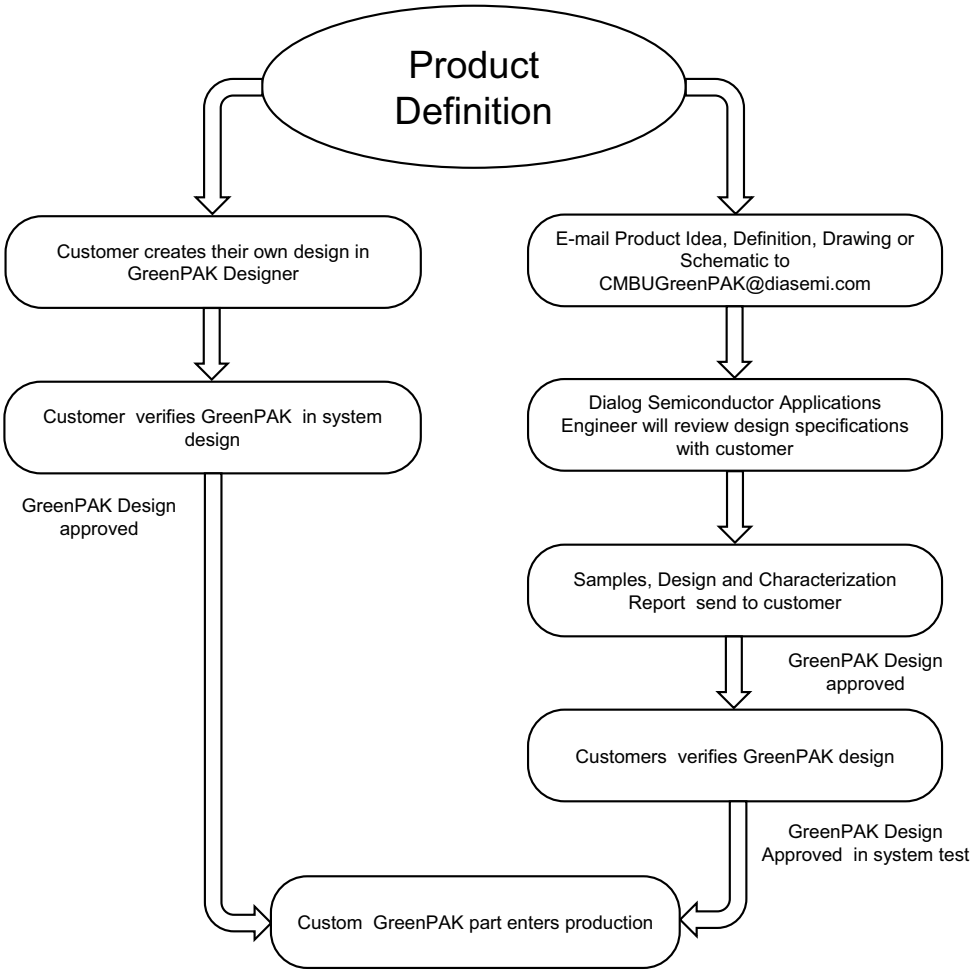


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG46824 has a total of 13 GPIO, 2 GPO and 2 GPI Pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

5.1 GPIO PINS

IO0, IO1, IO2, IO3, IO4, IO5, IO8, IO9, IO10, IO11, IO12, IO13, IO14 serve as General Purpose IO Pins.

5.2 GPO PINS

IO6 and IO7 serve as General Purpose Output Pins

5.3 GPI PINS

SCL and SDA serve as General Purpose Input Pins.

5.4 PULL UP/DOWN RESISTORS

All IO Pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

5.5 FAST PULL-UP/DOWN DURING POWER UP

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by reg <768>.

5.6 I^2C MODE IO STRUCTURE (V_{DD} OR V_{DD2})

5.6.1 I^2C Mode Structure (for SCL and SDA)

5.7 MATRIX OE IO STRUCTURE (VDD OR VDD2)

5.7.1 Matrix OE IO Structure (for IOs 1, 4, 5 with VDD, and IOs 8, 9, 10, 11, 12, 13, 14 with VDD2)

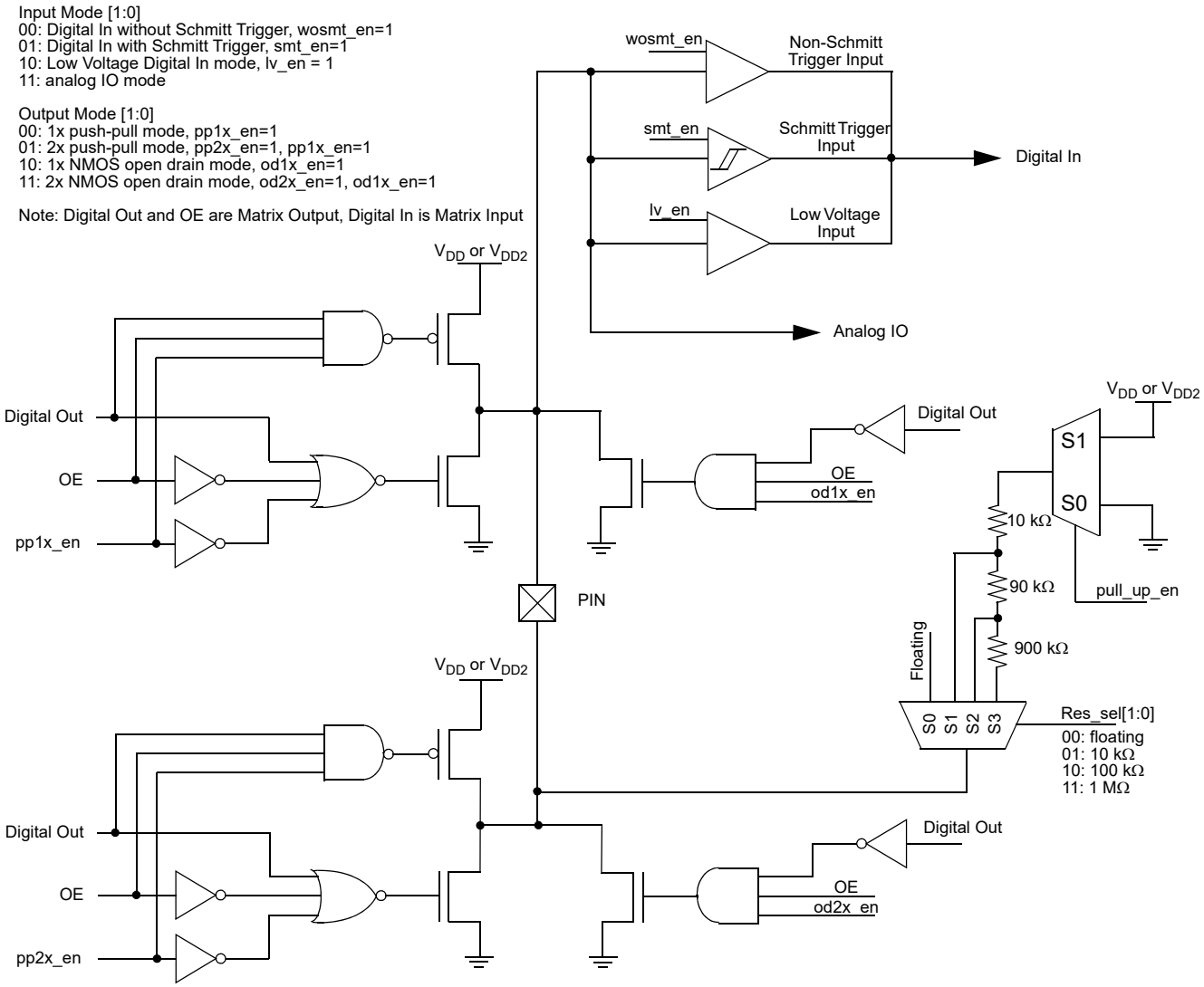


Figure 3: Matrix OE IO Structure Diagram

5.8 REGISTER OE IO STRUCTURE (VDD OR VDD2)

5.9 REGISTER OE IO STRUCTURE (FOR IOS 0, 2, 3 WITH VDD)

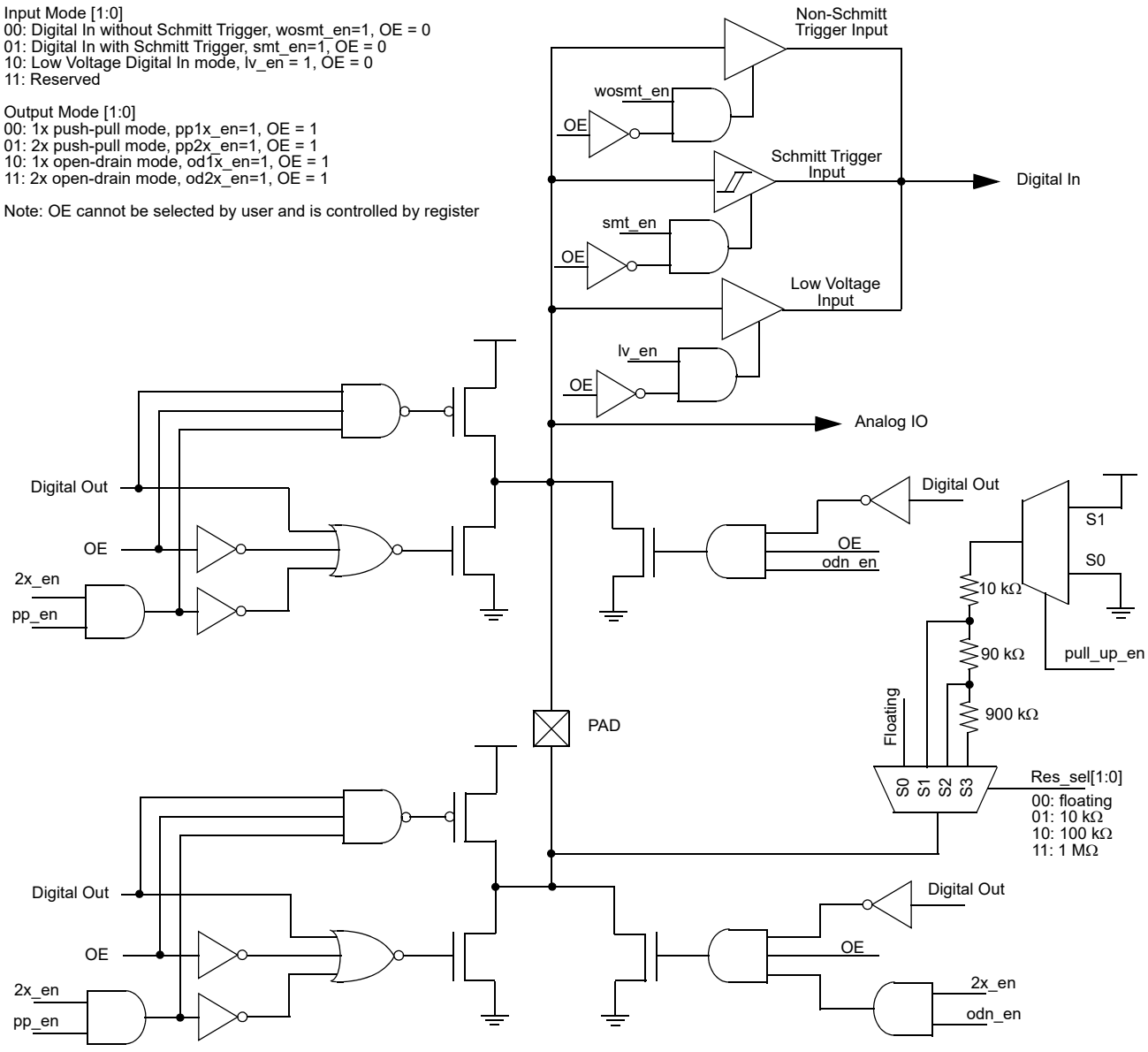


Figure 4: GPIO Register OE IO Structure Diagram

5.10 REGISTER OE IO STRUCTURE (VDD OR VDD2)

5.10.1 Register OE IO Structure (for IO 6 with VDD, and IO 7 with VDD2)

Mode [2:0]
000: Reserved
001: Reserved
010: Reserved
011: Reserved
100: push-pull mode, pp_en=1, OE = 1
101: NMOS open drain mode, odn_en=1, OE = 1
110: PMOS open drain mode, odp_en=1, OE = 1
111: analog IO and NMOS open-drain mode, odn_en=1 and AIO_en=1

Note: OE cannot be selected by user and is controlled by register

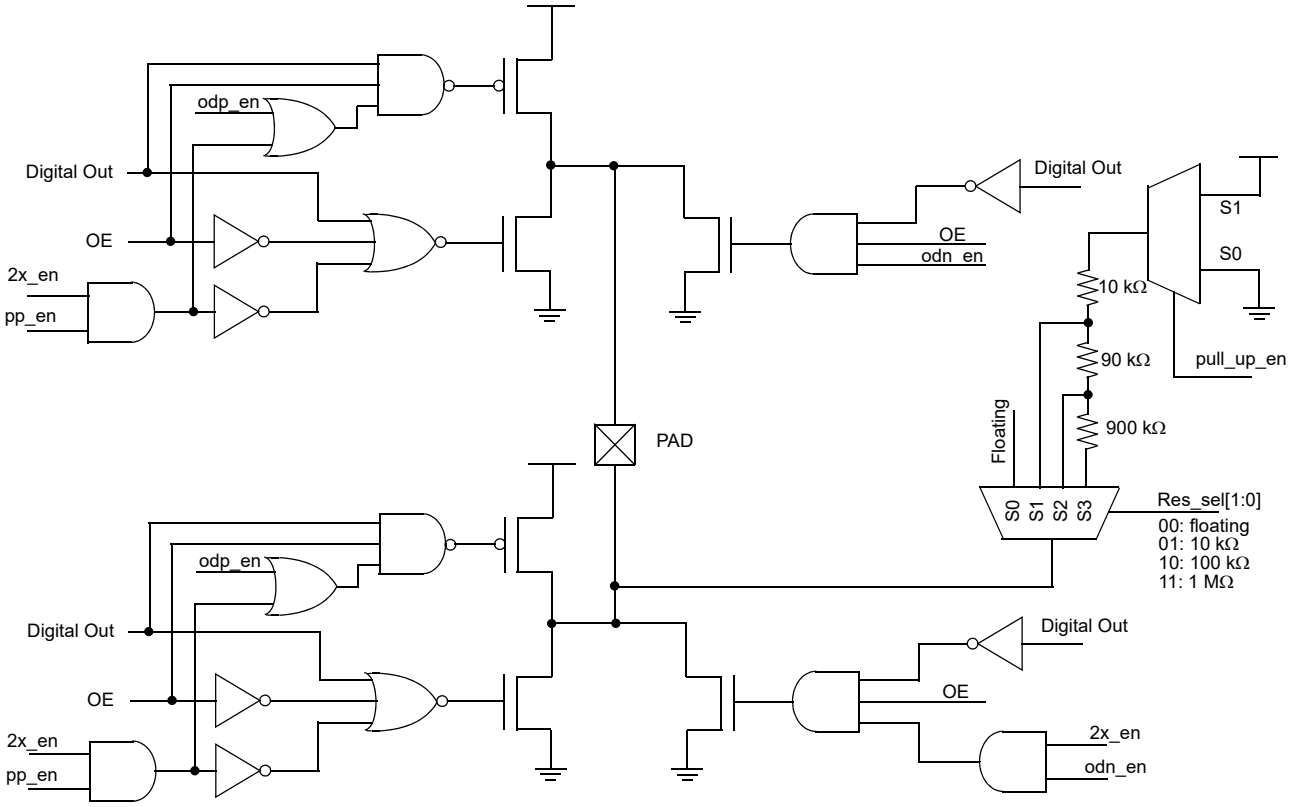


Figure 5: GPIO Register OE IO Structure Diagram

6 Connection Matrix

The Connection Matrix in the SLG46824 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the multiple-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46824 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46824 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IOs, LUTs, analog comparators, other digital resources and VDD and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46824’s register table, see Section 17.

Matrix Input Signal Functions	N
GND	0
IO0 Digital In	1
IO1 Digital In	2
IO2 Digital In	3
⋮	⋮
RB_MAT_D5US	62
VDD	63

Matrix Inputs / Matrix Outputs

N	0	1	2	…	95
Registers	reg<5:0>	reg<11:6>	reg<17:12>	…	reg<575:570>
Function	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0	Matrix Out: IN0 of LUT2_1 or Clock Input of PGEN	…	Matrix Output 95

Figure 6: Connection Matrix

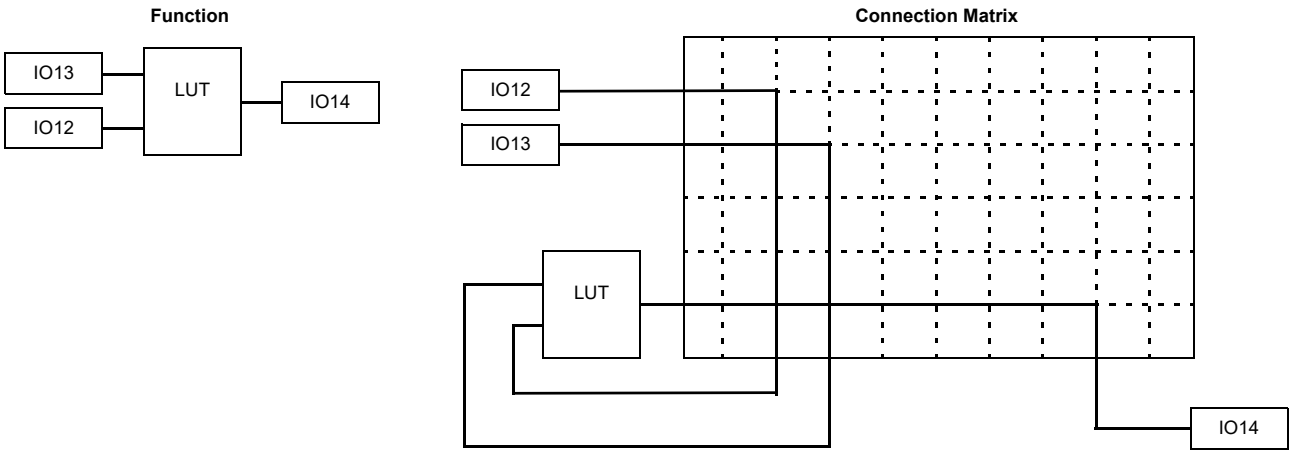


Figure 7: Connection Matrix Example

6.1 MATRIX INPUT TABLE

Table 19: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	IO2 Digital Input	0	0	0	0	1	1
4	IO3 Digital Input	0	0	0	1	0	0
5	IO4 Digital Input	0	0	0	1	0	1
6	IO5 Digital Input	0	0	0	1	1	0
7	IO8 Digital Input	0	0	0	1	1	1
8	IO9 Digital Input	0	0	1	0	0	0
9	IO10 Digital Input	0	0	1	0	0	1
10	IO11 Digital Input	0	0	1	0	1	0
11	IO12 Digital Input	0	0	1	0	1	1
12	IO13 Digital Input	0	0	1	1	0	0
13	IO14 Digital Input	0	0	1	1	0	1
14	LUT2_0_DFF0_OUT	0	0	1	1	1	0
15	LUT2_1_DFF1_OUT	0	0	1	1	1	1
16	LUT2_2_DFF2_OUT	0	1	0	0	0	0
17	LUT2_3_PGEN_OUT	0	1	0	0	0	1
18	LUT3_0_DFF3_OUT	0	1	0	0	1	0
19	LUT3_1_DFF4_OUT	0	1	0	0	1	1
20	LUT3_2_DFF5_OUT	0	1	0	1	0	0
21	LUT3_3_DFF6_OUT	0	1	0	1	0	1
22	LUT3_4_DFF7_OUT	0	1	0	1	1	0
23	LUT3_5_DFF8_OUT	0	1	0	1	1	1
24	LUT3_6_PIPEDLY_RIPP_CNT_OUT0	0	1	1	0	0	0
25	PIPEDLY_RIPP_CNT_OUT1	0	1	1	0	0	1
26	RIPP_CNT_OUT2	0	1	1	0	1	0
27	EDET_FILTER_OUT	0	1	1	0	1	1
28	PROG_DLY_EDET_OUT	0	1	1	1	0	0
29	MULTFUNC_8BIT_1: DLY_CNT_OUT	0	1	1	1	0	1
30	CKRCOSC_MATRIX: OSC1 matrix input	0	1	1	1	1	0
31	CKLFOSC_MATRIX: OSC0 matrix input	0	1	1	1	1	1
32	CKRINGOSC_MATRIX: OSC2 matrix input	1	0	0	0	0	0
33	MULTFUNC_8BIT_2: DLY_CNT_OUT	1	0	0	0	0	1
34	MULTFUNC_8BIT_3: DLY_CNT_OUT	1	0	0	0	1	0
35	MULTFUNC_8BIT_4: DLY_CNT_OUT	1	0	0	0	1	1
36	MULTFUNC_8BIT_5: DLY_CNT_OUT	1	0	0	1	0	0
37	MULTFUNC_8BIT_6: DLY_CNT_OUT	1	0	0	1	0	1

Table 19: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	MULTFUNC_8BIT_7: DLY_CNT_OUT	1	0	0	1	1	0
39	MULTFUNC_16BIT_0: LUT_DFF_OUT	1	0	0	1	1	1
40	MULTFUNC_8BIT_1: LUT_DFF_OUT	1	0	1	0	0	0
41	MULTFUNC_8BIT_2: LUT_DFF_OUT	1	0	1	0	0	1
42	MULTFUNC_8BIT_3: LUT_DFF_OUT	1	0	1	0	1	0
43	MULTFUNC_8BIT_4: LUT_DFF_OUT	1	0	1	0	1	1
44	MULTFUNC_8BIT_5: LUT_DFF_OUT	1	0	1	1	0	0
45	MULTFUNC_8BIT_6: LUT_DFF_OUT	1	0	1	1	0	1
46	MULTFUNC_8BIT_7: LUT_DFF_OUT	1	0	1	1	1	0
47	MULTFUNC_16BIT_0: DLY_CNT_OUT	1	0	1	1	1	1
48	Virtual Input <7>: reg<976>	1	1	0	0	0	0
49	Virtual Input <6>: reg<977>	1	1	0	0	0	1
50	Virtual Input <5>: reg<978>	1	1	0	0	1	0
51	Virtual Input <4>: reg<979>	1	1	0	0	1	1
52	Virtual Input <3>: reg<980>	1	1	0	1	0	0
53	Virtual Input <2>: reg<981>	1	1	0	1	0	1
54	Virtual Input <1>: reg<982>	1	1	0	1	1	0
55	Virtual Input <0>: reg<983>	1	1	0	1	1	1
56	Reserved	1	1	1	0	0	0
57	Reserved	1	1	1	0	0	1
58	ACMP0L_OUT	1	1	1	0	1	0
59	ACMP1L_OUT	1	1	1	0	1	1
60	2nd CKRCOSC_MATRIX	1	1	1	1	0	0
61	2nd CKLFOSC_MATRIX	1	1	1	1	0	1
62	POR OUT	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 20: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <5:0>	IN0 of LUT2_0 or Clock Input of DFF0	0
reg <11:6>	IN1 of LUT2_0 or Data Input of DFF0	1
reg <17:12>	IN0 of LUT2_3 or Clock Input of PGEN	2
reg <23:18>	IN1 of LUT2_3 or nRST of PGEN	3
reg <29:24>	IN0 of LUT2_1 or Clock Input of DFF1	4
reg <35:30>	IN1 of LUT2_1 or Data Input of DFF1	5
reg <41:36>	IN0 of LUT2_2 or Clock Input of DFF2	6
reg <47:42>	IN1 of LUT2_2 or Data Input of DFF2	7
reg <53:48>	IN0 of LUT3_0 or Clock Input of DFF3	8

Table 20: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <59:54>	IN1 of LUT3_0 or Data Input of DFF3	9
reg <65:60>	IN2 of LUT3_0 or nRST(nSET) of DFF3	10
reg <71:66>	IN0 of LUT3_1 or Clock Input of DFF4	11
reg <77:72>	IN1 of LUT3_1 or Data Input of DFF4	12
reg <83:78>	IN2 of LUT3_1 or nRST(nSET) of DFF4	13
reg <89:84>	IN0 of LUT3_2 or Clock Input of DFF5	14
reg <95:90>	IN1 of LUT3_2 or Data Input of DFF5	15
reg <101:96>	IN2 of LUT3_2 or nRST(nSET) of DFF5	16
reg <107:102>	IN0 of LUT3_3 or Clock Input of DFF6	17
reg <113:108>	IN1 of LUT3_3 or Data Input of DFF6	18
reg <119:114>	IN2 of LUT3_3 or nRST(nSET) of DFF6	19
reg <125:120>	IN0 of LUT3_4 or Clock Input of DFF7	20
reg <131:126>	IN1 of LUT3_4 or Data Input of DFF7	21
reg <137:132>	IN2 of LUT3_4 or nRST(nSET) of DFF7	22
reg <143:138>	IN0 of LUT3_5 or Clock Input of DFF8	23
reg <149:144>	IN1 of LUT3_5 or Data Input of DFF8	24
reg <155:150>	IN2 of LUT3_5 or nRST(nSET) of DFF8	25
reg <161:156>	IN0 of LUT3_6 or Input of Pipe Delay or UP Signal of RIPP CNT	26
reg <167:162>	IN1 of LUT3_6 or nRST of Pipe Delay or STB of RIPP CNT	27
reg <173:168>	IN2 of LUT3_6 or Clock of Pipe Delay_RIPP_CNT	28
reg <179:174>	Reserved	29
reg <185:180>	MULTFUNC_16BIT_0: IN0 of LUT4_0 or Clock Input of DFF9; Delay0 Input (or Counter0 RST/SET Input)	30
reg <191:186>	MULTFUNC_16BIT_0: IN1 of LUT4_0 or nRST of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source	31
reg <197:192>	MULTFUNC_16BIT_0: IN2 of LUT4_0 or nSET of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source or KEEP Input of FSM0	32
reg <203:198>	MULTFUNC_16BIT_0: IN3 of LUT4_0 or Data Input of DFF9; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0	33
reg <209:204>	MULTFUNC_8BIT_1: IN0 of LUT3_7 or Clock Input of DFF10; Delay1 Input (or Counter1 nRST Input)	34
reg <215:210>	MULTFUNC_8BIT_1: IN1 of LUT3_7 or nRST (nSET) of DFF10; Delay1 Input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source	35
reg <221:216>	MULTFUNC_8BIT_1: IN2 of LUT3_7 or Data Input of DFF10; Delay1 Input (or Counter1 nRST Input)	36
reg <227:222>	MULTFUNC_8BIT_2: IN0 of LUT3_8 or Clock Input of DFF11; Delay2 Input (or Counter2 nRST Input);	37
reg <233:228>	MULTFUNC_8BIT_2: IN1 of LUT3_8 or nRST (nSET) of DFF11; Delay2 Input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source	38
reg <239:234>	MULTFUNC_8BIT_2: IN2 of LUT3_8 or Data Input of DFF11; Delay2 Input (or Counter2 nRST Input)	39

Table 20: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <245:240>	MULTFUNC_8BIT_3: IN0 of LUT3_9 or Clock Input of DFF12; Delay3 Input (or Counter3 nRST Input)	40
reg <251:246>	MULTFUNC_8BIT_3: IN1 of LUT3_9 or nRST (nSET) of DFF12; Delay3 Input (or Counter3 nRST Input) or Delay/Counter3 External Clock Source	41
reg <257:252>	MULTFUNC_8BIT_3: IN2 of LUT3_9 or Data Input of DFF12; Delay3 Input (or Counter3 nRST Input)	42
reg <263:258>	MULTFUNC_8BIT_4: IN0 of LUT3_10 or Clock Input of DFF13; Delay4 Input (or Counter4 nRST Input)	43
reg <269:264>	MULTFUNC_8BIT_4: IN1 of LUT3_10 or nRST (nSET) of DFF13; Delay4 Input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source	44
reg <275:270>	MULTFUNC_8BIT_4: IN2 of LUT3_10 or Data Input of DFF13; Delay4 Input (or Counter4 nRST Input)	45
reg <281:276>	MULTFUNC_8BIT_5: IN0 of LUT3_11 or Clock Input of DFF14; Delay5 Input (or Counter5 nRST Input)	46
reg <287:282>	MULTFUNC_8BIT_5: IN1 of LUT3_11 or nRST (nSET) of DFF14; Delay5 Input (or Counter5 nRST Input) or Delay/Counter5 External Clock Source	47
reg <293:288>	MULTFUNC_8BIT_5: IN2 of LUT3_11 or Data Input of DFF14; Delay5 Input (or Counter5 nRST Input)	48
reg <299:294>	MULTFUNC_8BIT_6: IN0 of LUT3_12 or Clock Input of DFF15; Delay6 Input (or Counter6 nRST Input)	49
reg <305:300>	MULTFUNC_8BIT_6: IN1 of LUT3_12 or nRST (nSET) of DFF15; Delay6 Input (or Counter6 nRST Input) or Delay/Counter6 External Clock Source	50
reg <311:306>	MULTFUNC_8BIT_6: IN2 of LUT3_12 or Data Input of DFF15; Delay6 Input (or Counter6 nRST Input)	51
reg <317:312>	MULTFUNC_8BIT_7: IN0 of LUT3_13 or Clock Input of DFF16; Delay7 Input (or Counter7 nRST Input)	52
reg <323:318>	MULTFUNC_8BIT_7: IN1 of LUT3_13 or nRST (nSET) of DFF16; Delay7 Input (or Counter7 nRST Input) or Delay/Counter7 External Clock Source	53
reg <329:324>	MULTFUNC_8BIT_7: IN2 of LUT3_13 or Data Input of DFF16; Delay7 Input (or Counter7 nRST Input)	54
reg <335:330>	Filter/Edge detect input	55
reg <341:336>	Programmable delay/edge detect input	56
reg <347:342>	OSC2 ENABLE from matrix	57
reg <353:348>	OSC0 ENABLE from matrix	58
reg <359:354>	OSC1 ENABLE matrix	59
reg <365:360>	Reserved	60
reg <371:366>	BG power down from matrix	61
reg <377:372>	Reserved	62
reg <383:378>	Reserved	63
reg <389:384>	pd of ACMP0L from matrix	64
reg <395:390>	pd of ACMP1L from matrix	65
reg <401:396>	Reserved	66
reg <407:402>	IO0 Digital Output	67
reg <413:408>	IO1 Digital Output	68

Table 20: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg <419:414>	IO1 Digital Output OE	69
reg <425:420>	IO2 Digital Output	70
reg <431:426>	IO3 Digital Output	71
reg <437:432>	IO4 Digital Output	72
reg <443:438>	IO4 Digital Output OE	73
reg <449:444>	IO5 Digital Output	74
reg <455:450>	IO5 Digital Output OE	75
reg <461:456>	IO6 Digital Output	76
reg <467:462>	IO7 Digital Output	77
reg <473:468>	IO8 Digital Output	78
reg <479:474>	IO8 Digital Output OE	79
reg <485:480>	IO9 Digital Output	80
reg <491:486>	IO9 Digital Output OE	81
reg <497:492>	IO10 Digital Output	82
reg <503:498>	IO10 Digital Output OE	83
reg <509:504>	IO11 Digital Output	84
reg <515:510>	IO11 Digital Output OE	85
reg<521:516>	IO12 Digital Output	86
reg<527:522>	IO12 Digital Output OE	87
reg<533:528>	IO13 Digital Output	88
reg<539:534>	IO13 Digital Output OE	89
reg<545:540>	IO14 Digital Output	90
reg<551:546>	IO14 Digital Output OE	91
reg<557:552>	Reserved	92
reg<563:558>	Reserved	93
reg<569:564>	Matrix OUT 94	94
reg<575:570>	Matrix OUT 95	95

Note 4: For each Address, the two most significant bits are unused.

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x7A (0122).

An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). See Table 21.

Table 21: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
55	I2C_virtual_0 Input	reg<983>
54	I2C_virtual_1 Input	reg<982>
53	I2C_virtual_2 Input	reg<981>
52	I2C_virtual_3 Input	reg<980>
51	I2C_virtual_4 Input	reg<979>
50	I2C_virtual_5 Input	reg<978>
49	I2C_virtual_6 Input	reg<977>
48	I2C_virtual_7 Input	reg<976>

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are 0x74 (0116) to 0x7B (0123). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at 0x7A (0122)).

7 Combination Function Macrocells

The SLG46824 has 11 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- Three macrocells that can serve as either 2-bit LUT or as D Flip Flop
- Six macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGEN)

Inputs/Outputs for the 11 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP FLOP MACROCELLS

There are three macrocells that can serve as either 2-bit LUT or as D Flip Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High)

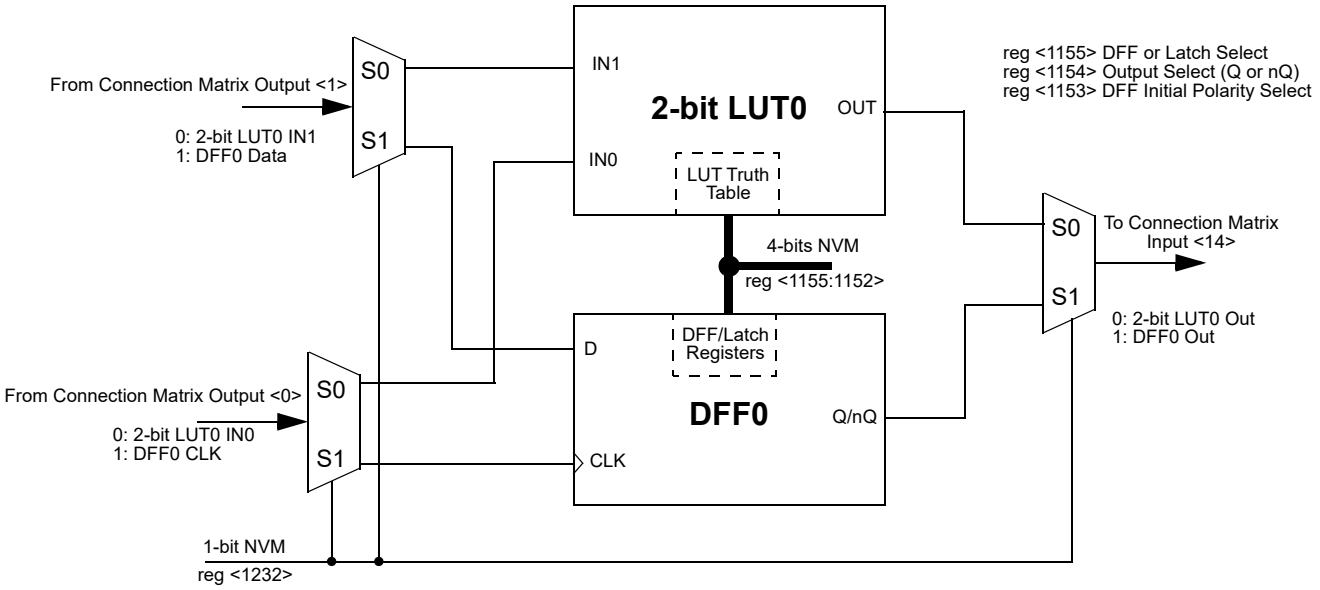


Figure 8: 2-bit LUT0 or DFF0

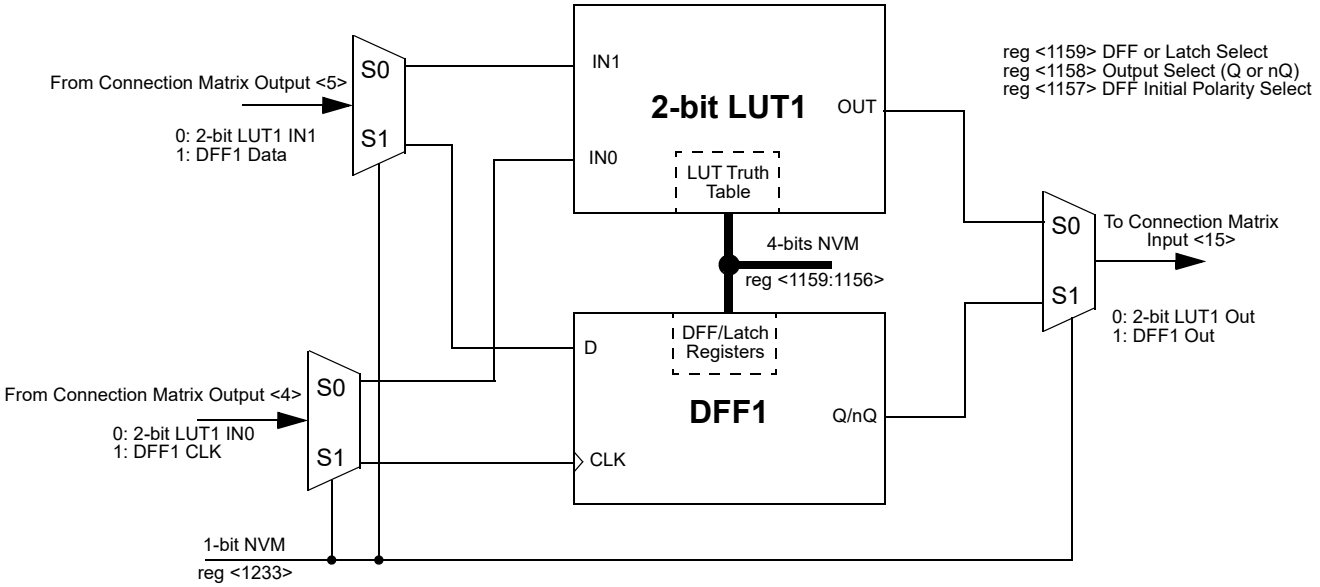


Figure 9: 2-bit LUT1 or DFF1

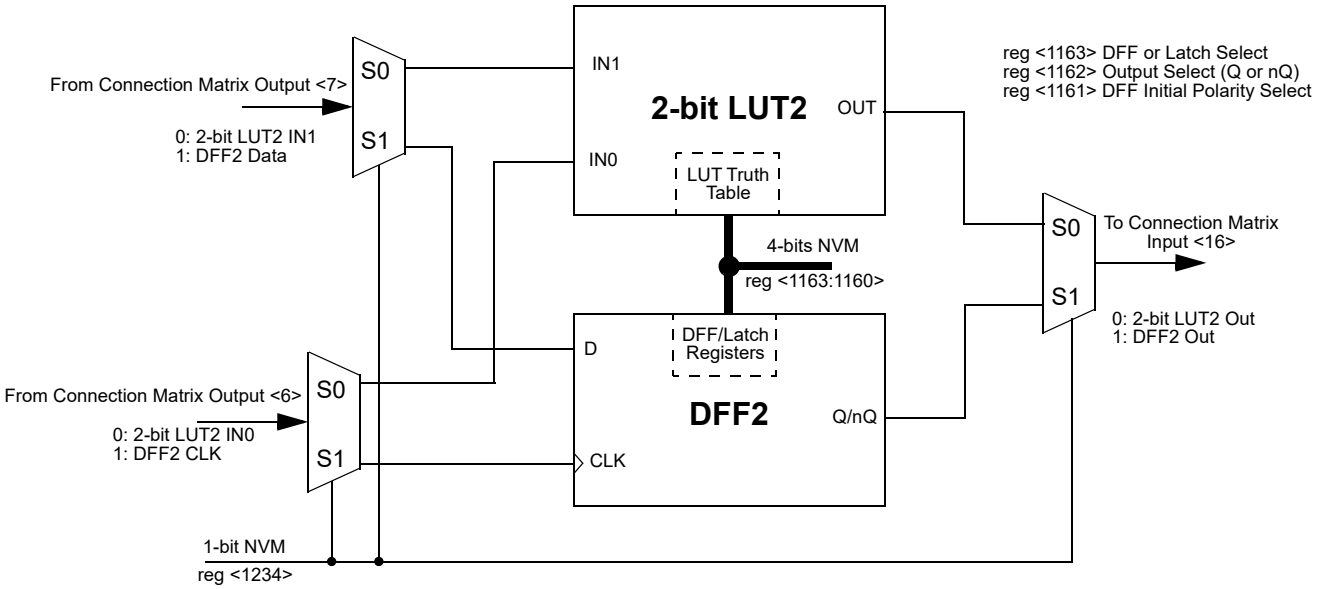


Figure 10: 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip Flop Macrocell Used as 2-Bit LUTT

Table 22: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	reg <1152>	LSB
0	1	reg <1153>	
1	0	reg <1154>	
1	1	reg <1155>	MSB

Table 23: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	reg <1156>	LSB
0	1	reg <1157>	
1	0	reg <1158>	
1	1	reg <1159>	MSB

Table 24: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	reg <1160>	LSB
0	1	reg <1161>	
1	0	reg <1162>	
1	1	reg <1163>	MSB

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg<1155:1152>

2-Bit LUT1 is defined by reg<1159:1156>

2-Bit LUT2 is defined by reg<1163:1160>

The Table 25 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 25: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

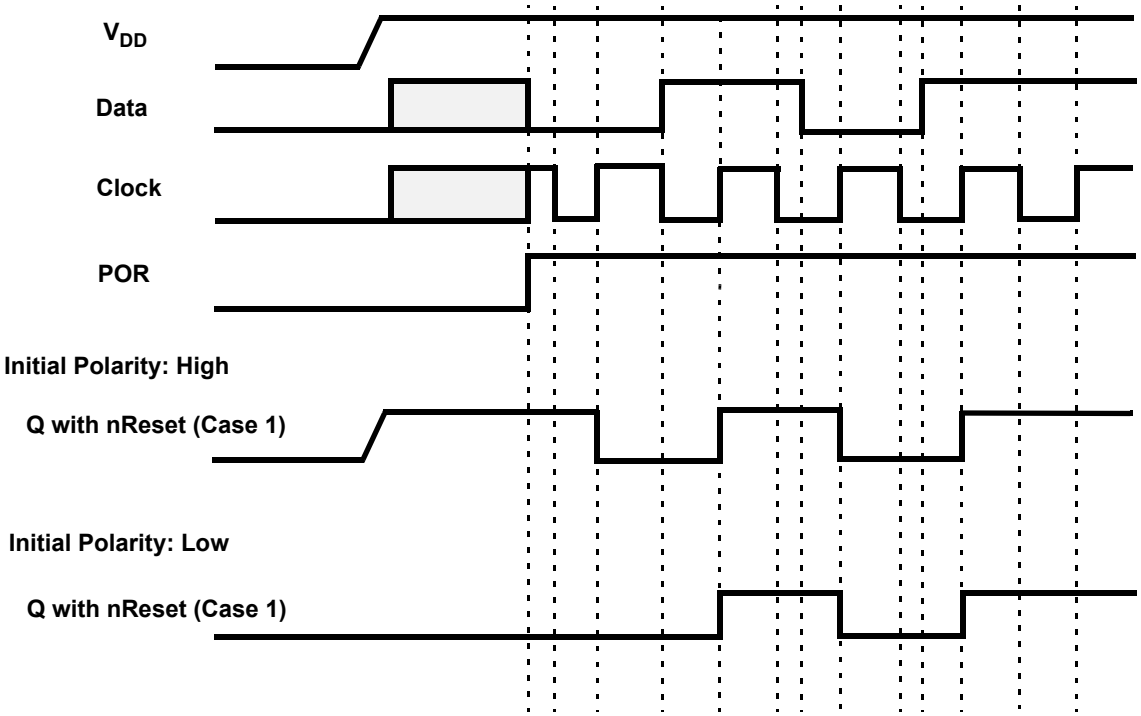


Figure 11: DFF Polarity Operations

7.2 2-bit LUT or Programmable Pattern Generator

The SLG46824 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGEN).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

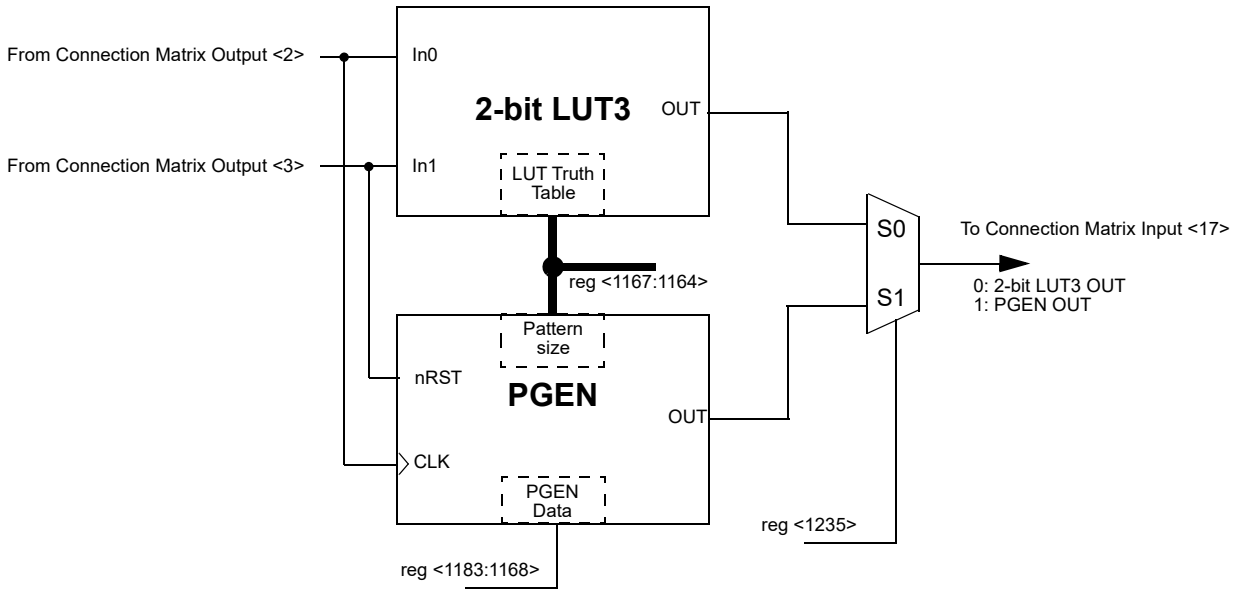


Figure 12: 2-bit LUT3 or PGEN

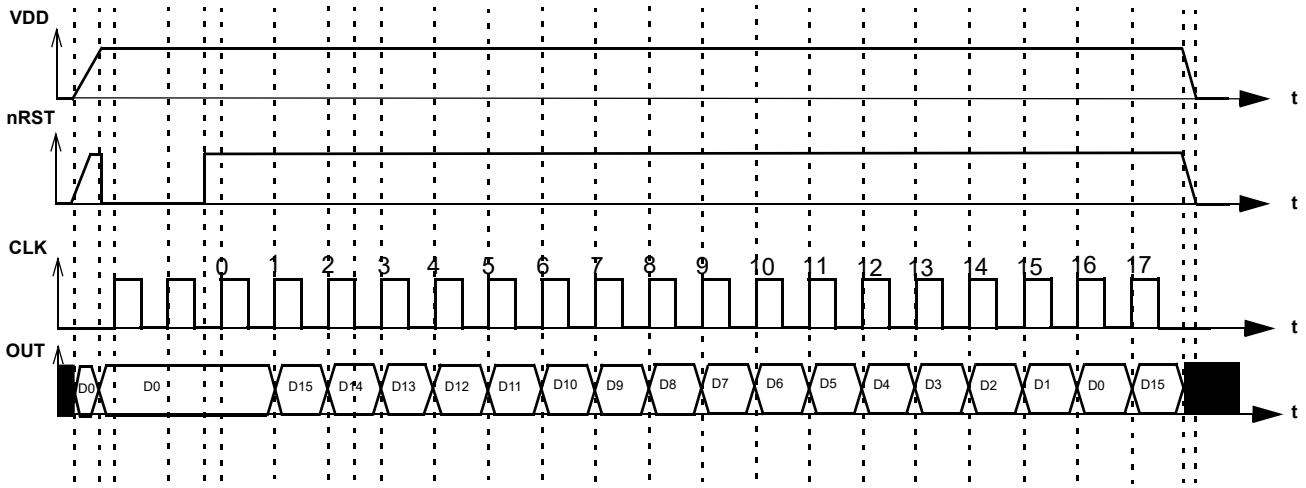


Figure 13: PGEN Timing Diagram

7.2.1 2-Bit LUT or PGEN Macrocell Used as 2-Bit LUT

Table 26: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	reg <1164>	LSB
0	1	reg <1165>	
1	0	reg <1166>	
1	1	reg <1167>	MSB

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT3 is defined by reg<1167:1164>

The Table 27 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 27: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are six macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

DFF3 operation is described below:

- If reg <1237> = 0, and the CLK is rising edge triggered, then Q=D, otherwise Q will not change

If reg <1237> = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

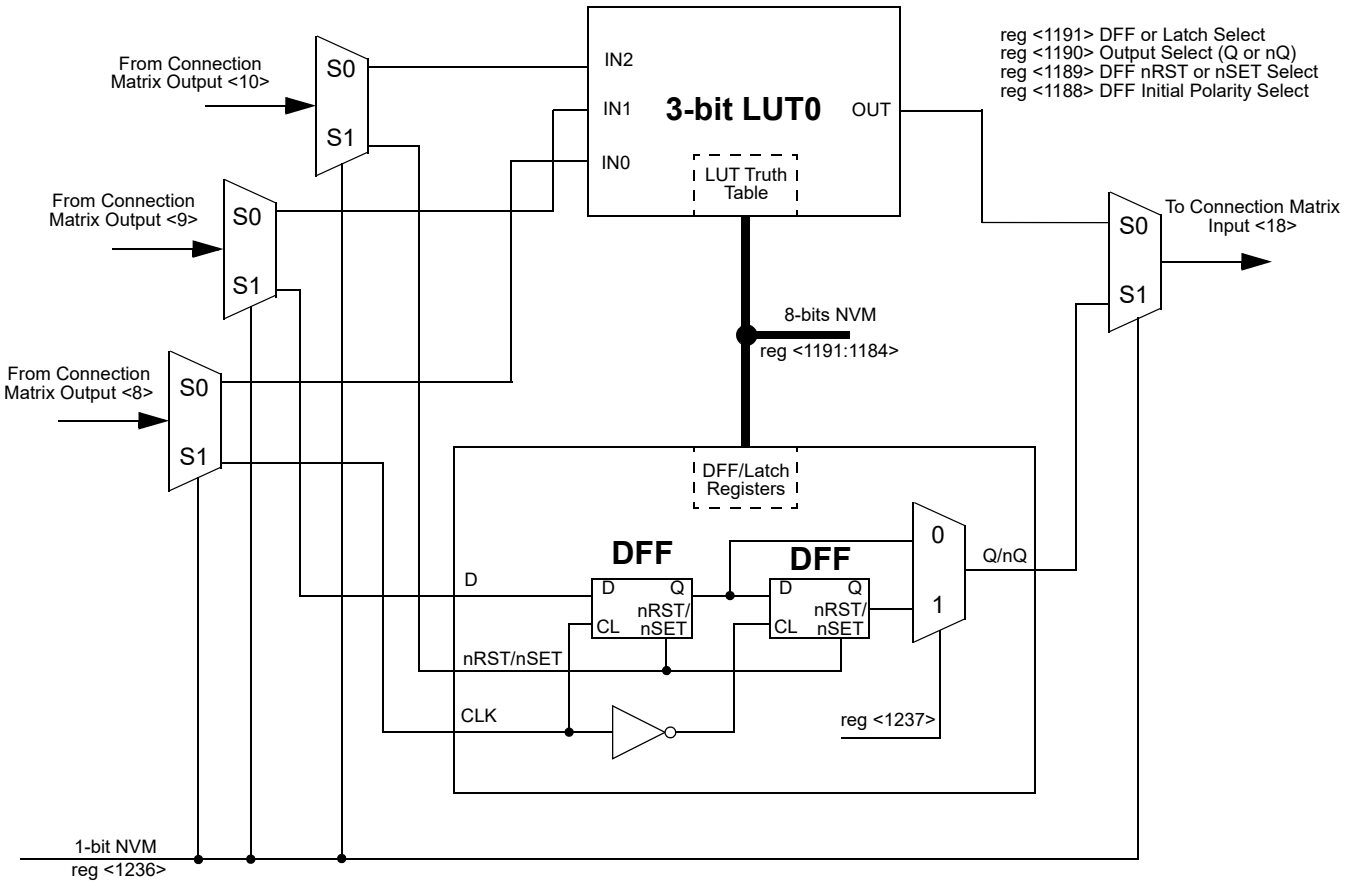


Figure 14: 3-bit LUT0 or DFF3

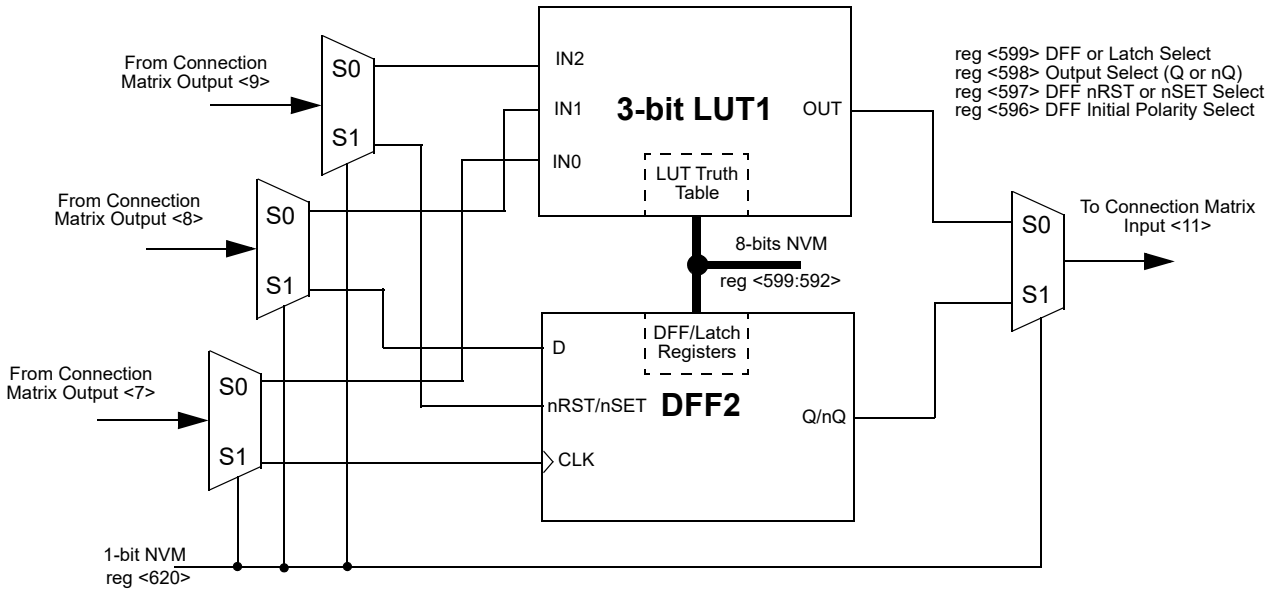


Figure 15: 3-bit LUT1 or DFF2

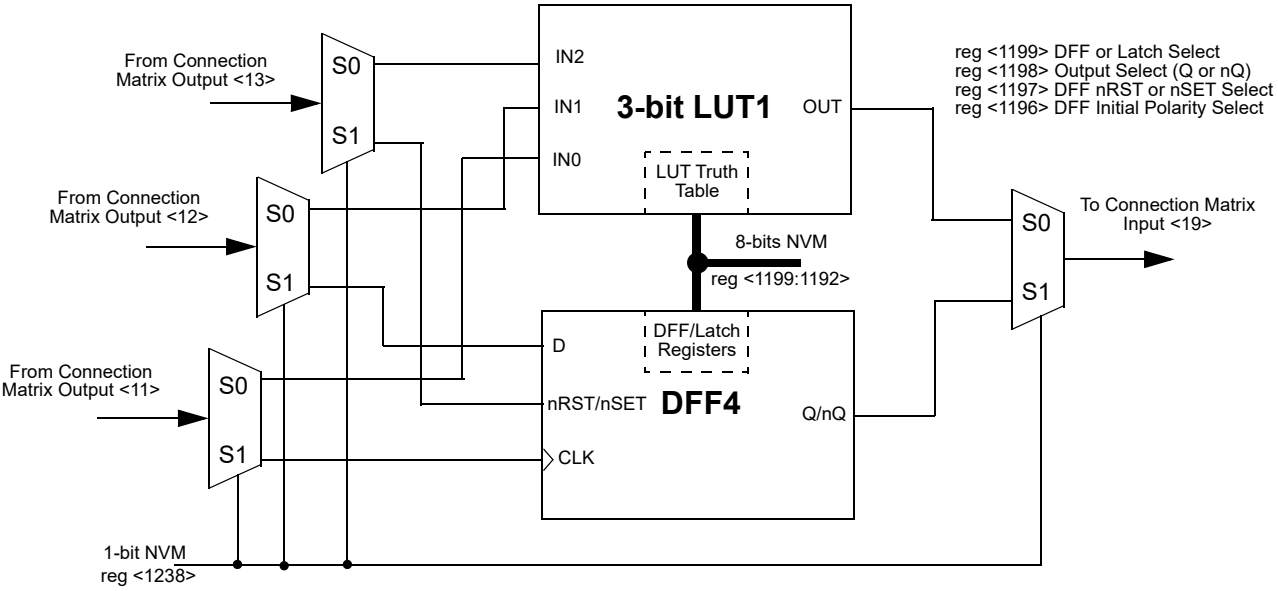


Figure 16: 3-bit LUT1 or DFF4

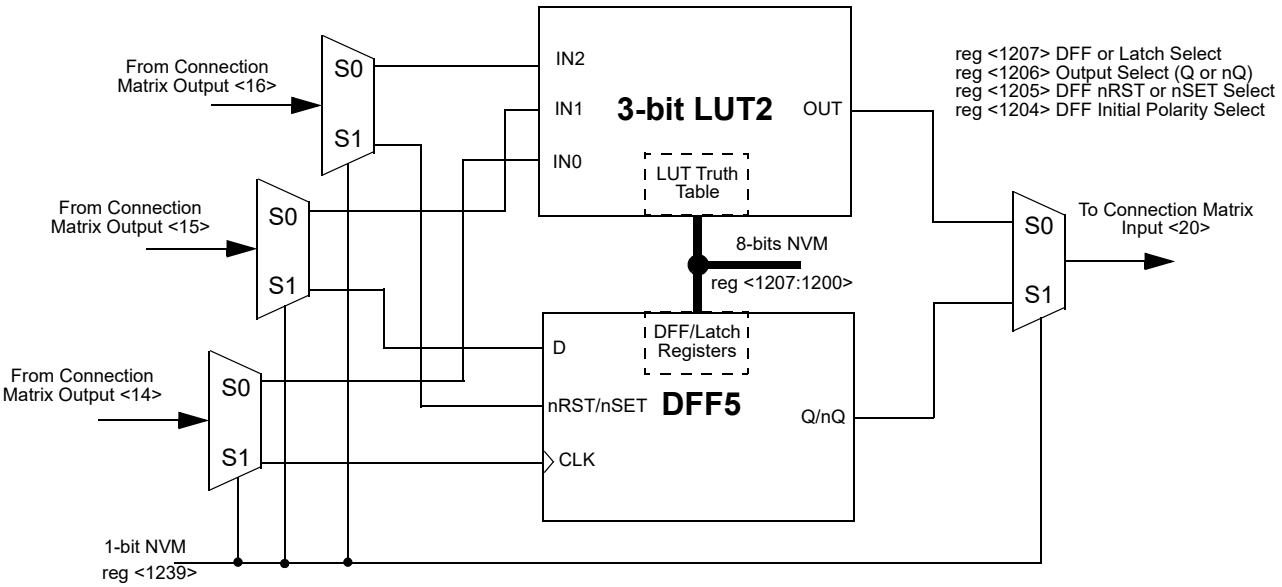


Figure 17: 3-bit LUT2 or DFF5

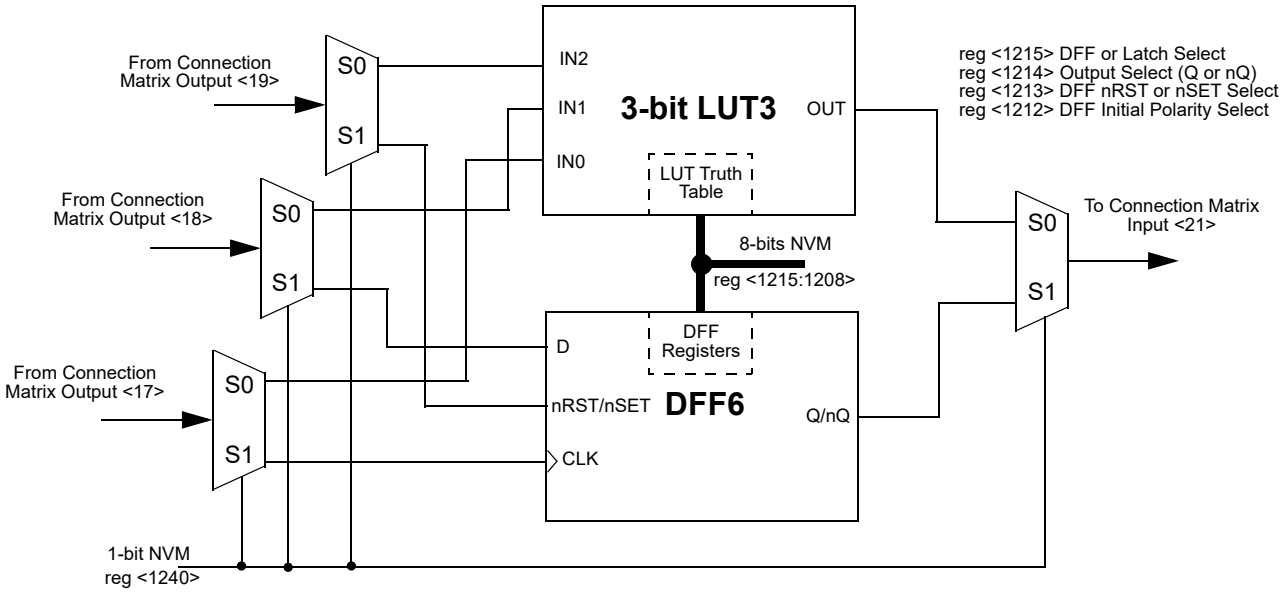


Figure 18: 3-bit LUT3 or DFF6

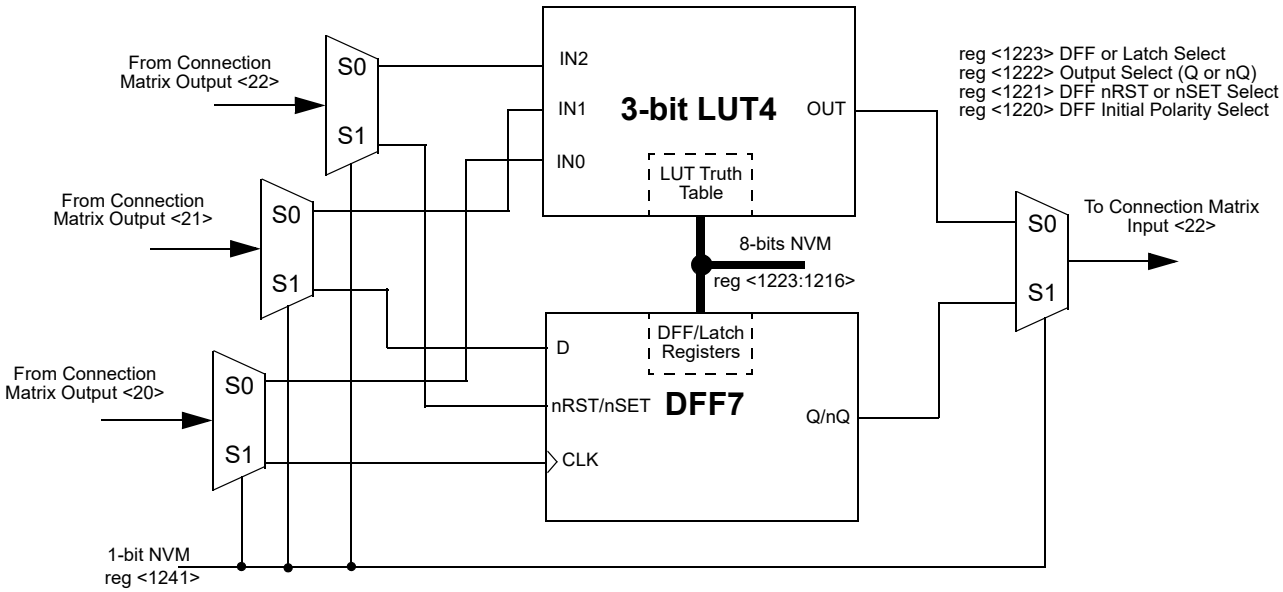


Figure 19: 3-bit LUT4 or DFF7

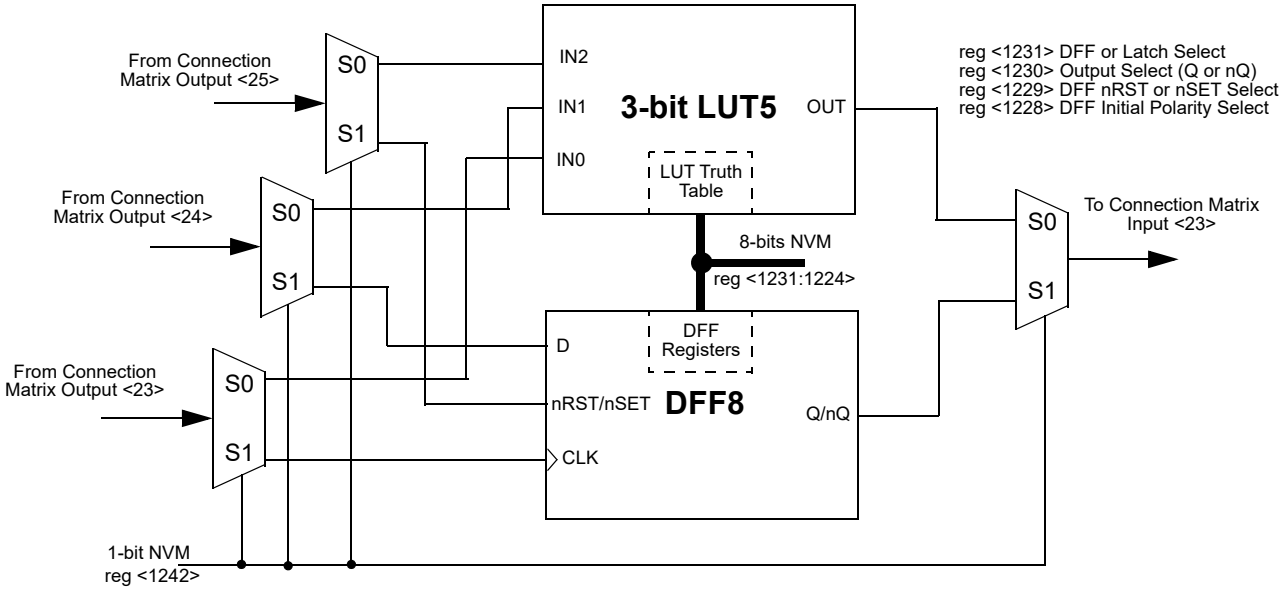


Figure 20: 3-bit LUT5 or DFF8

7.3.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 28: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1184>	LSB
0	0	1	reg <1185>	
0	1	0	reg <1186>	
0	1	1	reg <1187>	
1	0	0	reg <1188>	
1	0	1	reg <1189>	
1	1	0	reg <1190>	
1	1	1	reg <1191>	MSB

Table 29: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1192>	LSB
0	0	1	reg <1193>	
0	1	0	reg <1194>	
0	1	1	reg <1195>	
1	0	0	reg <1196>	
1	0	1	reg <1197>	
1	1	0	reg <1198>	
1	1	1	reg <1199>	MSB

Table 30: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1200>	LSB
0	0	1	reg <1201>	
0	1	0	reg <1202>	
0	1	1	reg <1203>	
1	0	0	reg <1204>	
1	0	1	reg <1205>	
1	1	0	reg <1206>	
1	1	1	reg <1207>	MSB

Table 31: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1208>	LSB
0	0	1	reg <1209>	
0	1	0	reg <1210>	
0	1	1	reg <1211>	
1	0	0	reg <1212>	
1	0	1	reg <1213>	
1	1	0	reg <1214>	
1	1	1	reg <1215>	MSB

Table 32: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1216>	LSB
0	0	1	reg <1217>	
0	1	0	reg <1218>	
0	1	1	reg <1219>	
1	0	0	reg <1220>	
1	0	1	reg <1221>	
1	1	0	reg <1222>	
1	1	1	reg <1223>	MSB

Table 33: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1224>	LSB
0	0	1	reg <1225>	
0	1	0	reg <1226>	
0	1	1	reg <1227>	
1	0	0	reg <1228>	
1	0	1	reg <1229>	
1	1	0	reg <1230>	
1	1	1	reg <1231>	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by reg<1191:1184>

3-Bit LUT1 is defined by reg<1199:1192>

3-Bit LUT2 is defined by reg<1207:1200>

3-Bit LUT3 is defined by reg<1215:1208>

3-Bit LUT4 is defined by reg<1223:1216>

3-Bit LUT5 is defined by reg<1231:1224>

The Table 34 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 34: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

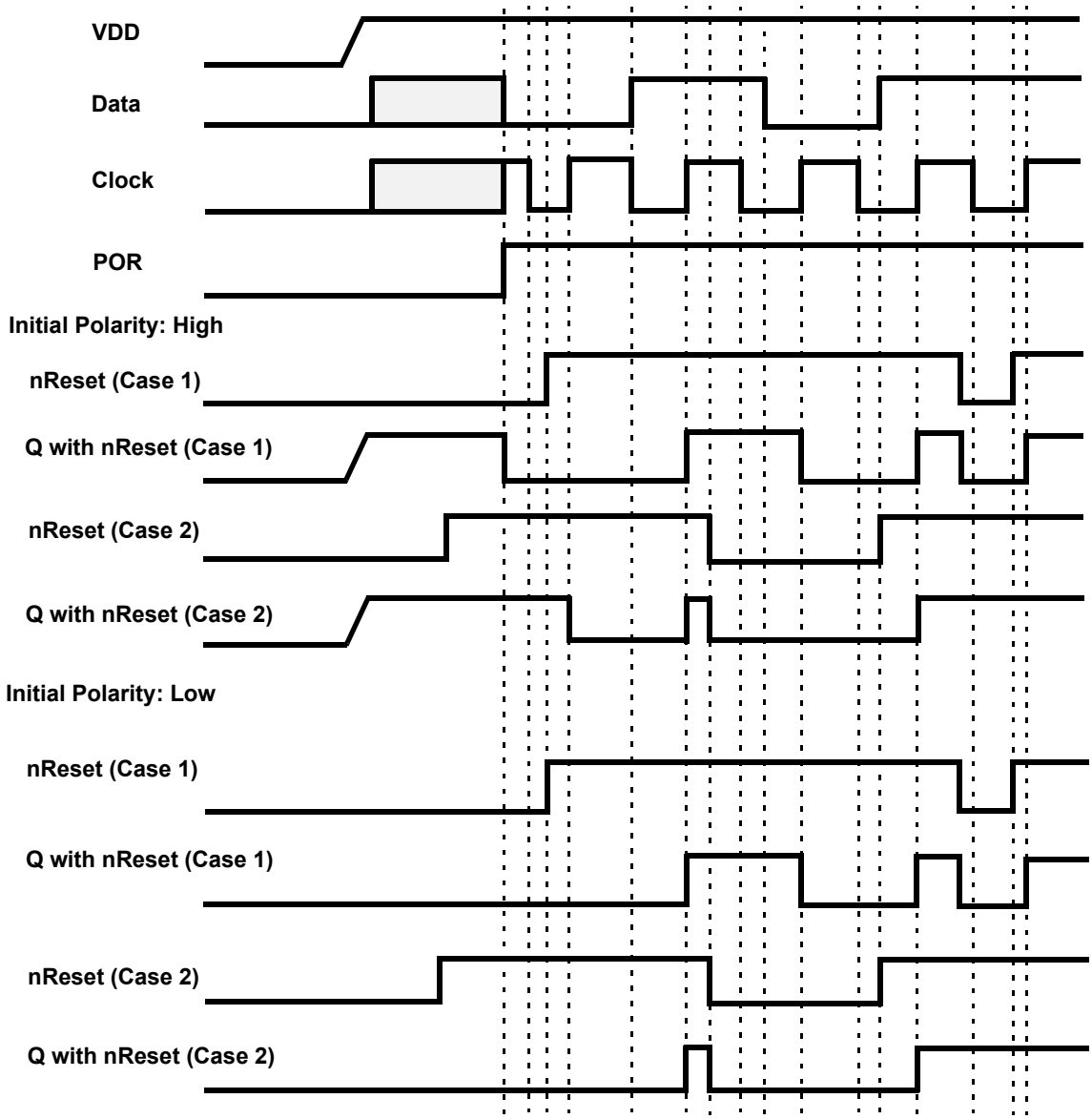


Figure 21: DFF Polarity Operations with nReset

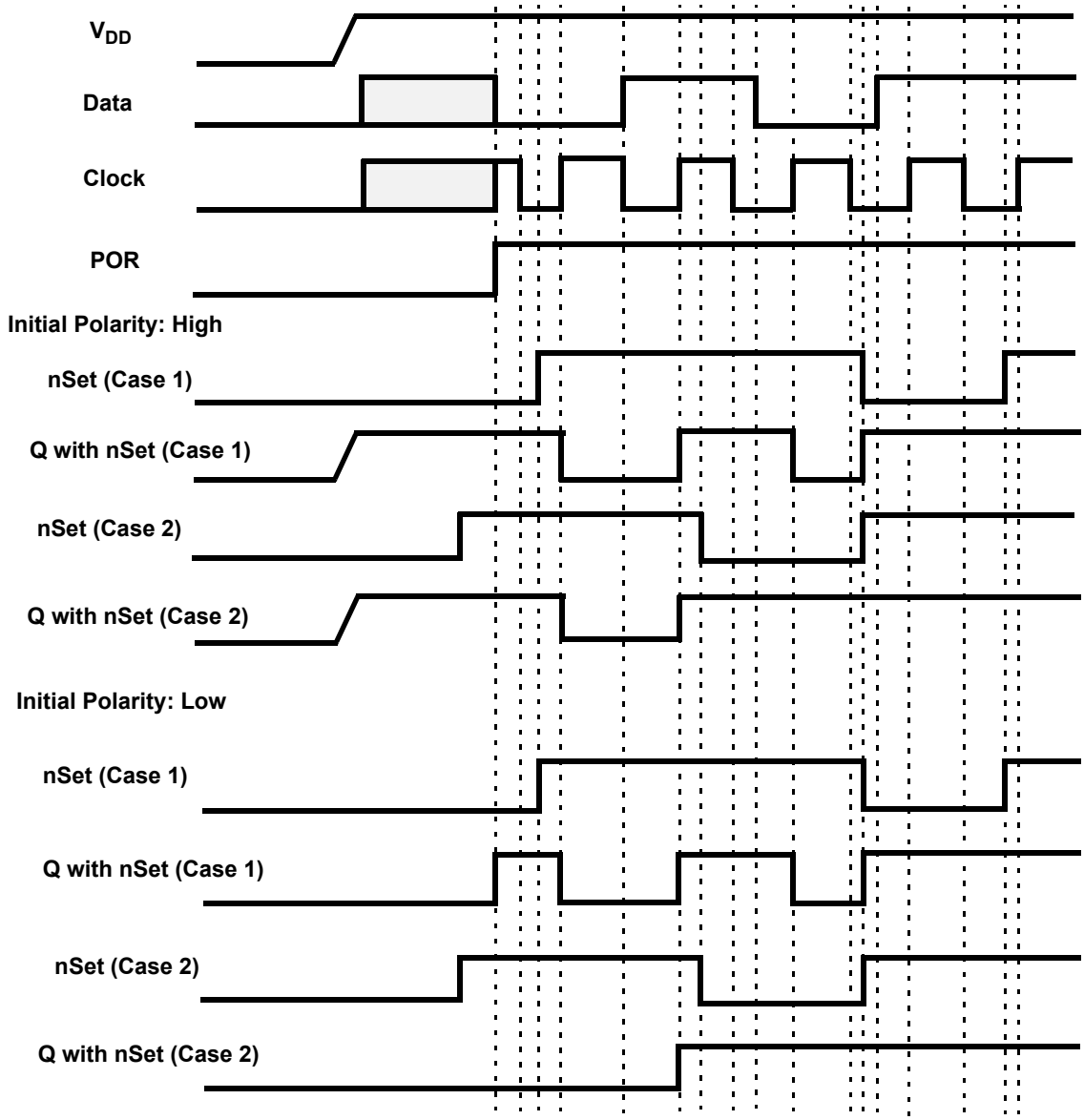


Figure 22: DFF Polarity Operations with nSet

7.4 3-BIT LUT OR PIPE DELAY / RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay / Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (nRST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <1251:1248> for OUT0 and reg <1255:1252> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46824 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG46824). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by reg <1256>).

In the Ripple Counter mode, there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV->EV->EV-1 to SV+1->SV etc (if SV is smaller than EV) or SV->SV-1 to EV+1->EV->SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV etc.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV etc. see Ripple counter functionality example in Figure 24.

Every step is executed by the rising edge on CLK input.

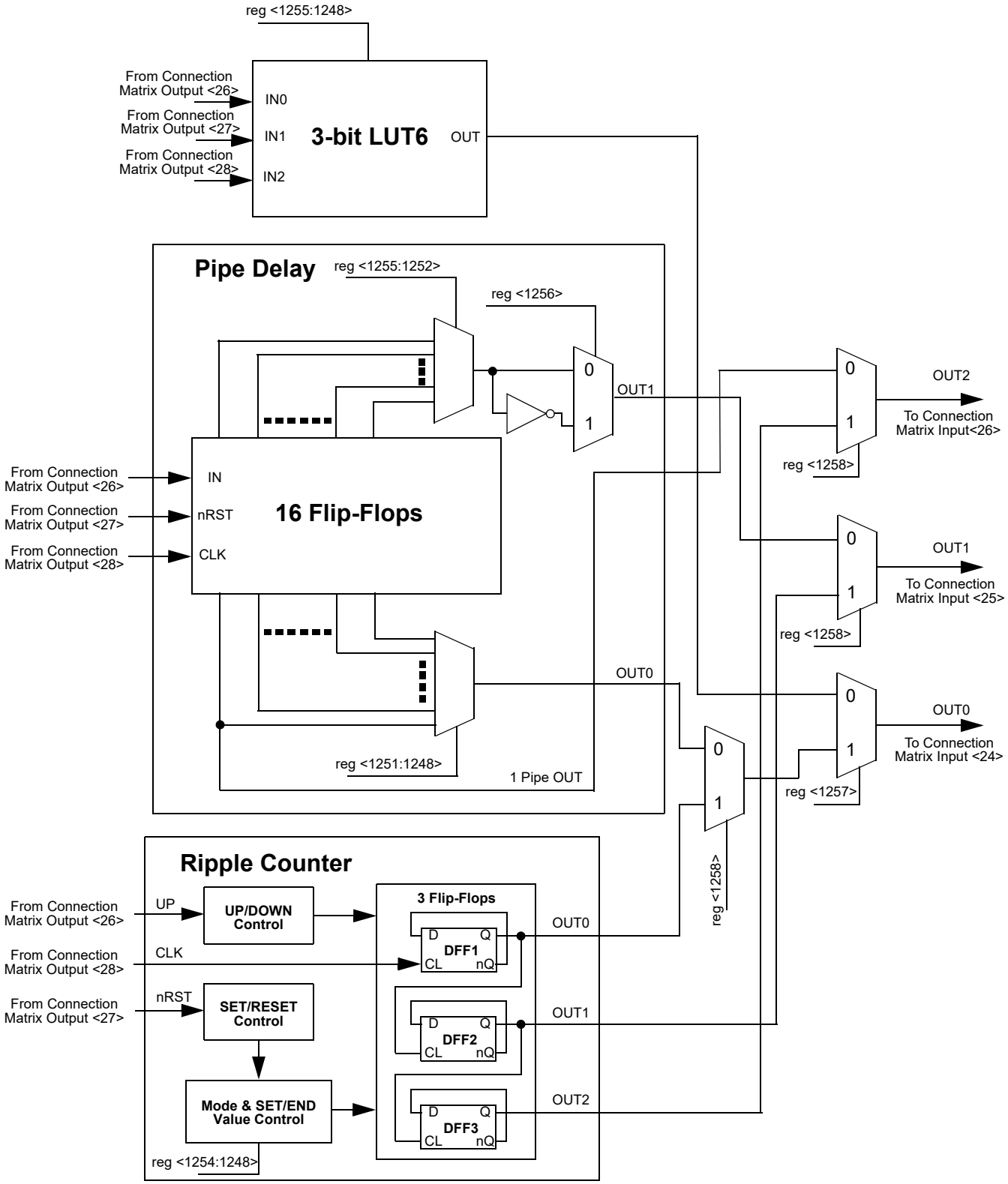


Figure 23: 3-bit LUT6 / Pipe Delay / Ripple Counter

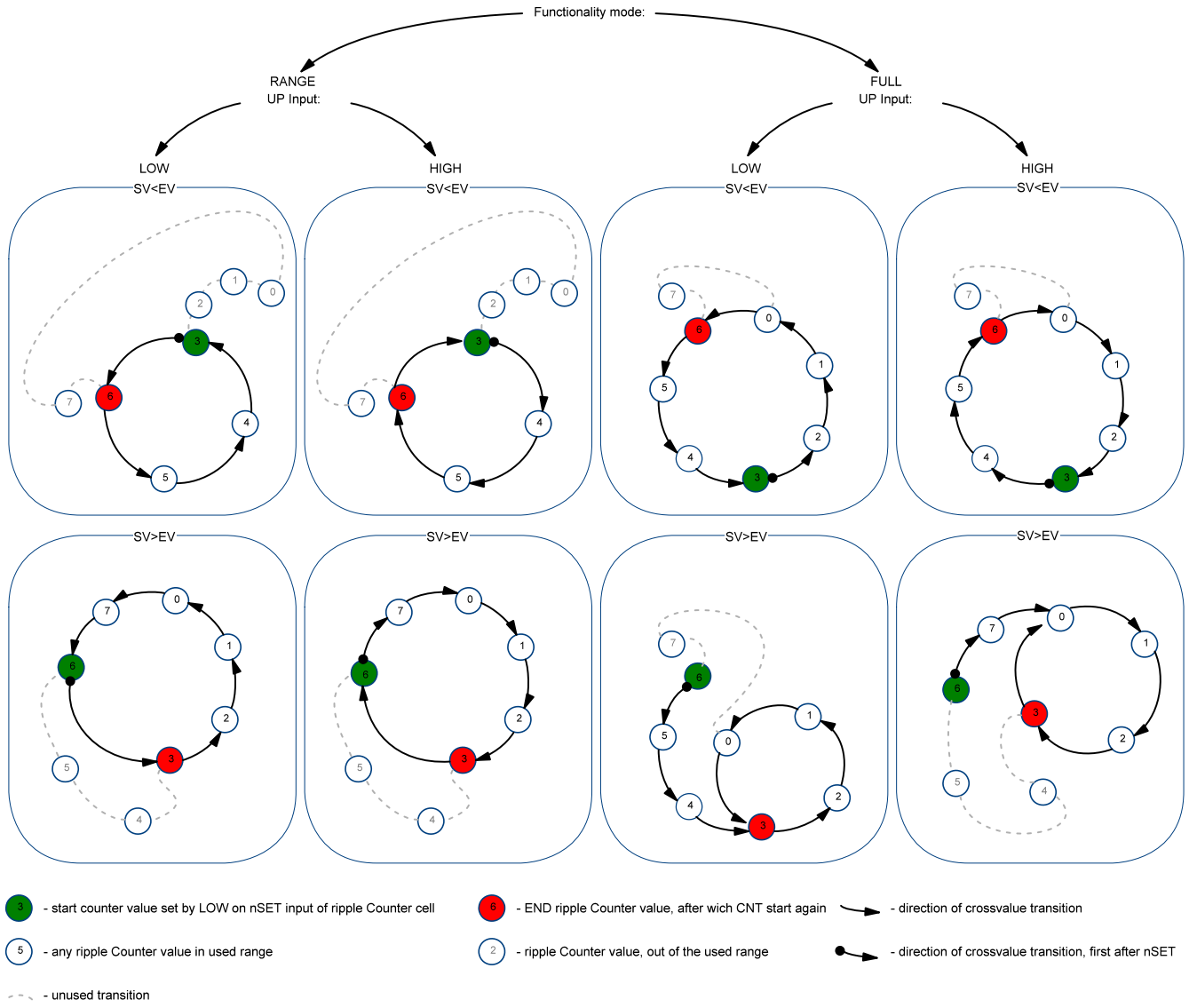


Figure 24: Example: Ripple Counter Functionality

7.4.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 35: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <1248>
0	0	1	reg <1249>
0	1	0	reg <1250>
0	1	1	reg <1251>
1	0	0	reg <1252>
1	0	1	reg <1253>
1	1	0	reg <1254>
1	1	1	reg <1255>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT6 is defined by reg<1255:1248>

8 Multi-Function Macrocells

The SLG46824 has 8 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect etc. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 25.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs / D Flip Flops and as 8-Bit Counter / Delays
- One macrocell that can serve as a 4-bit LUT / D Flip Flop and as 16-Bit Counter / Delay / FSM

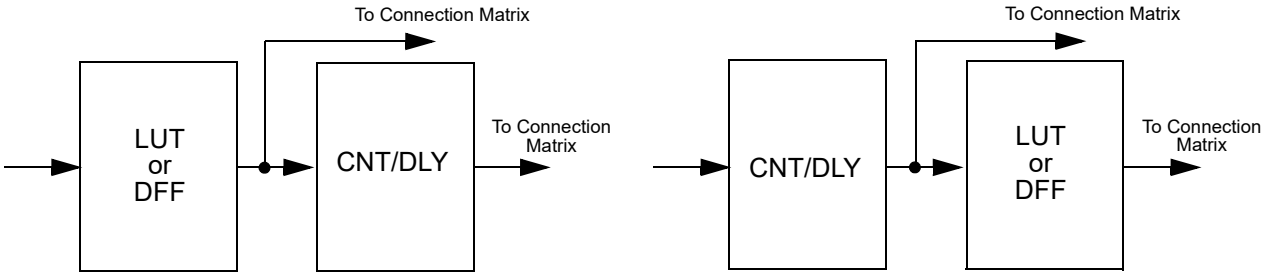


Figure 25: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the 8 Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR 8- BIT COUNTER / DELAY MACROCELLS

There are seven macrocells that can serve as 3-bit LUTs / D Flip Flops and as 8-Bit Counter / Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Set/Reset (nRST/nSET) inputs of the Flip Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter / Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 8.2.

Three of eight macrocells can have their active count value read/write via I2C (CNT0, CNT2 and CNT4). In this mode, it is possible to load count data immediately (plus two clock cycles) or after counter ends counting. See Section 15.5.3 for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

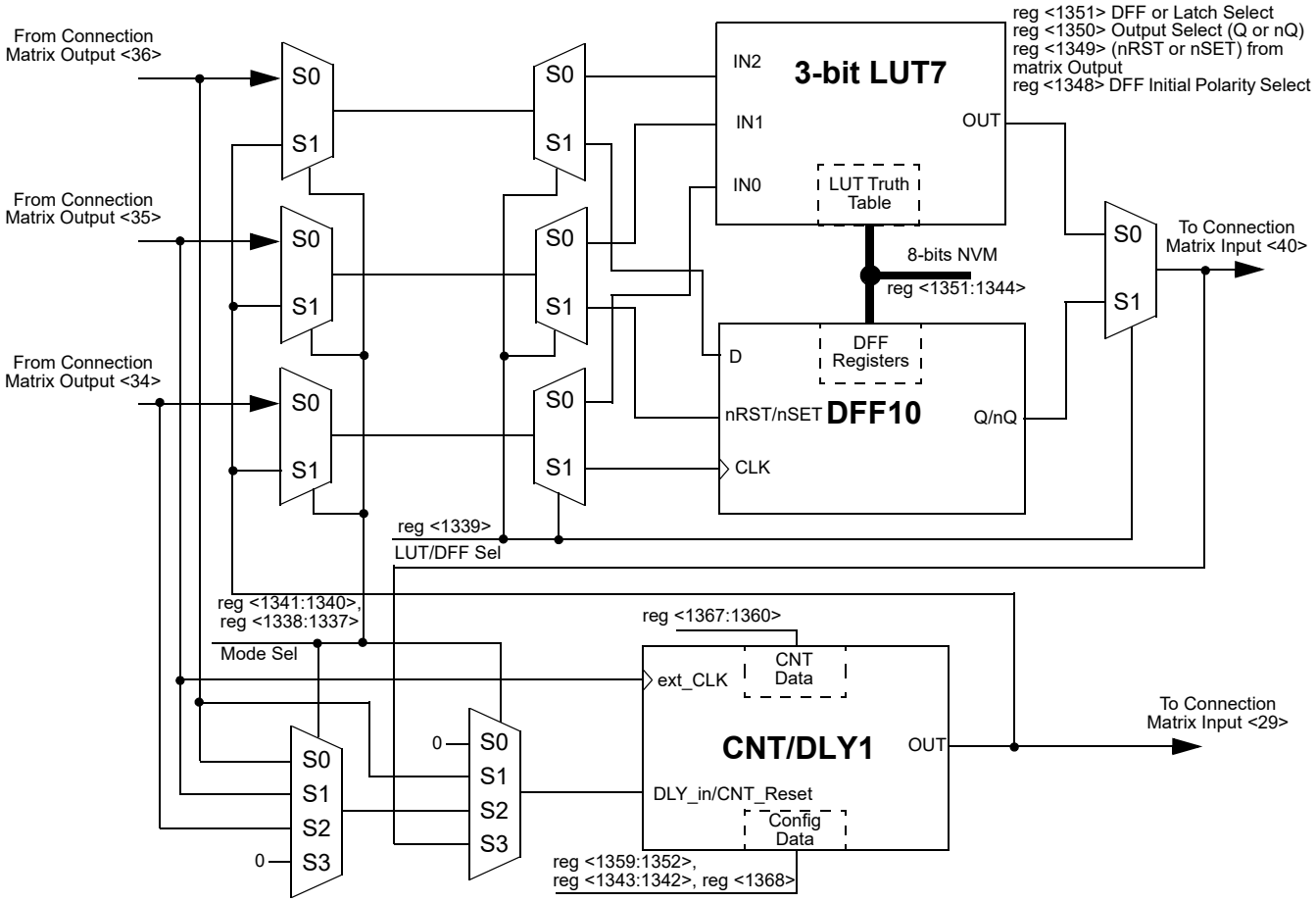


Figure 26: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF10, CNT/DLY1)

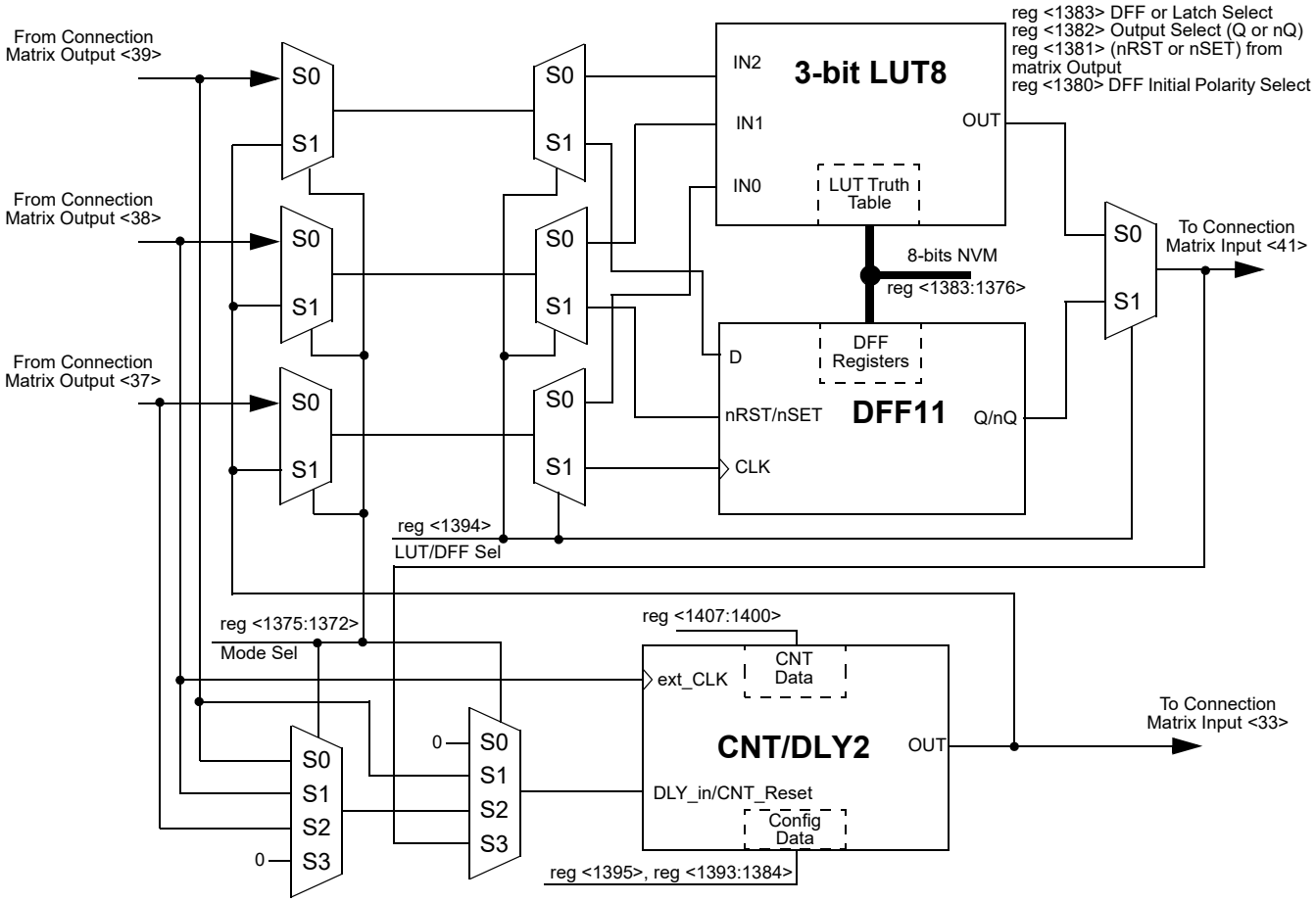


Figure 27: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF11, CNT/DLY2)

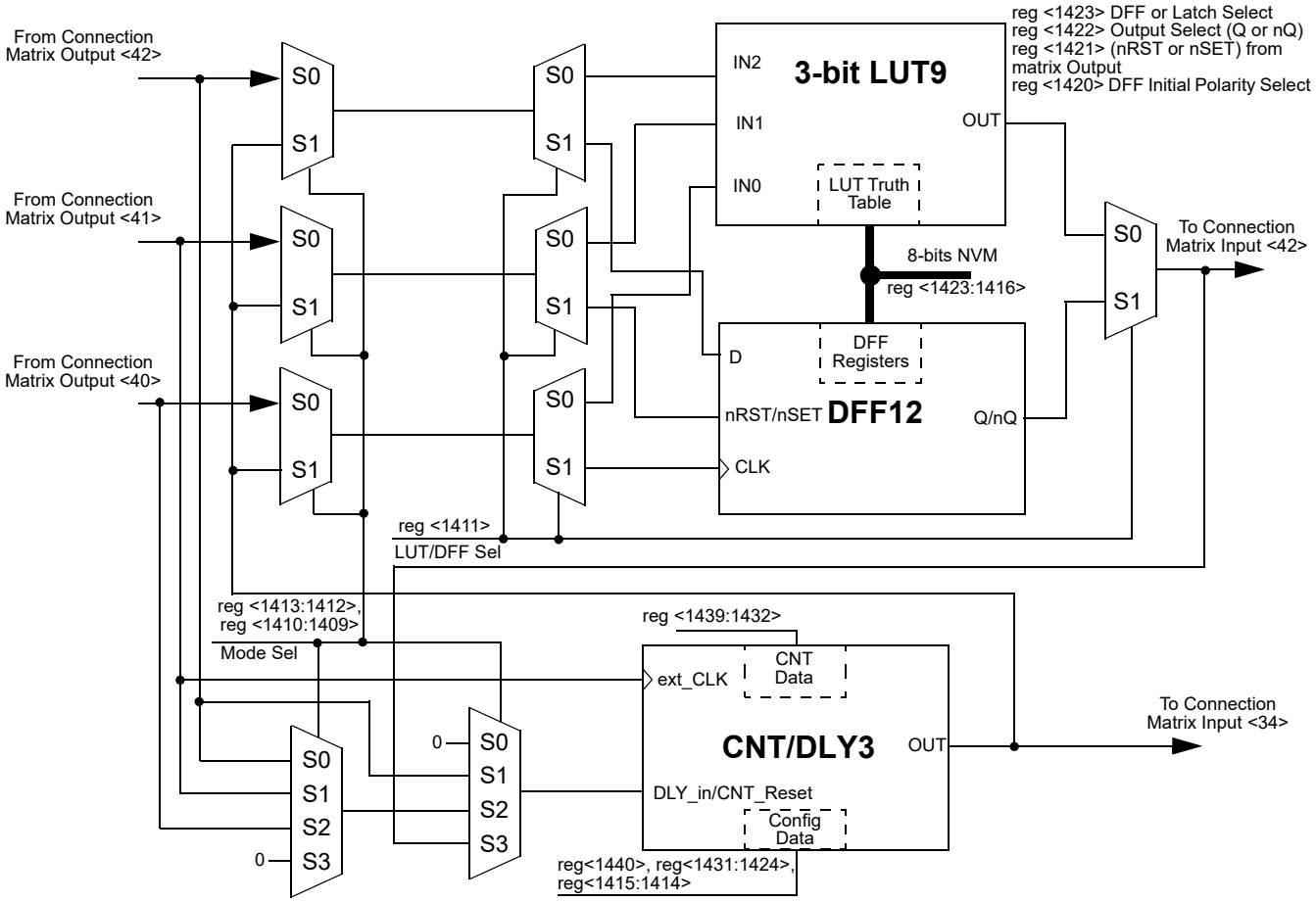


Figure 28: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF12, CNT/DLY3)

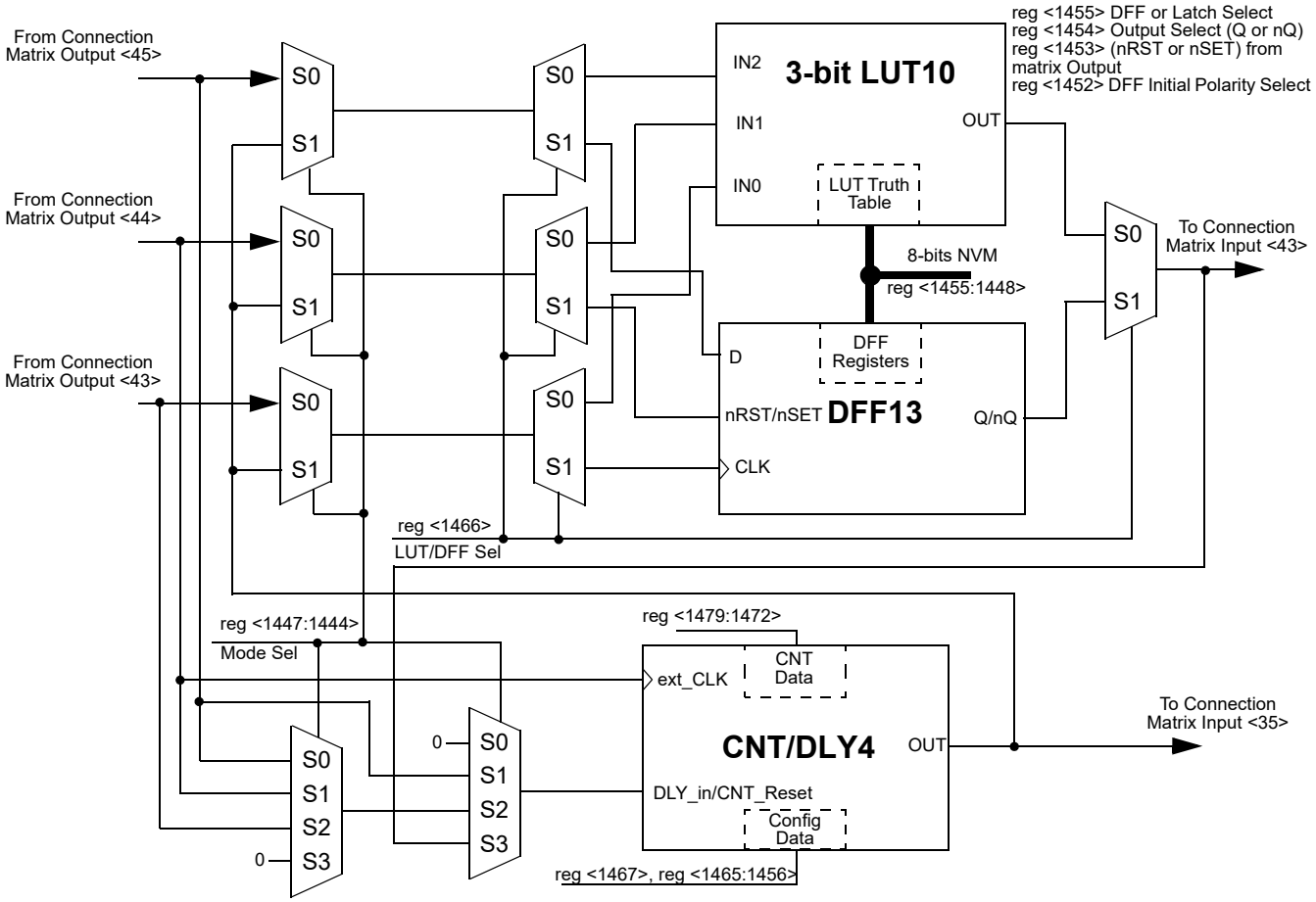


Figure 29: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF13, CNT/DLY4)

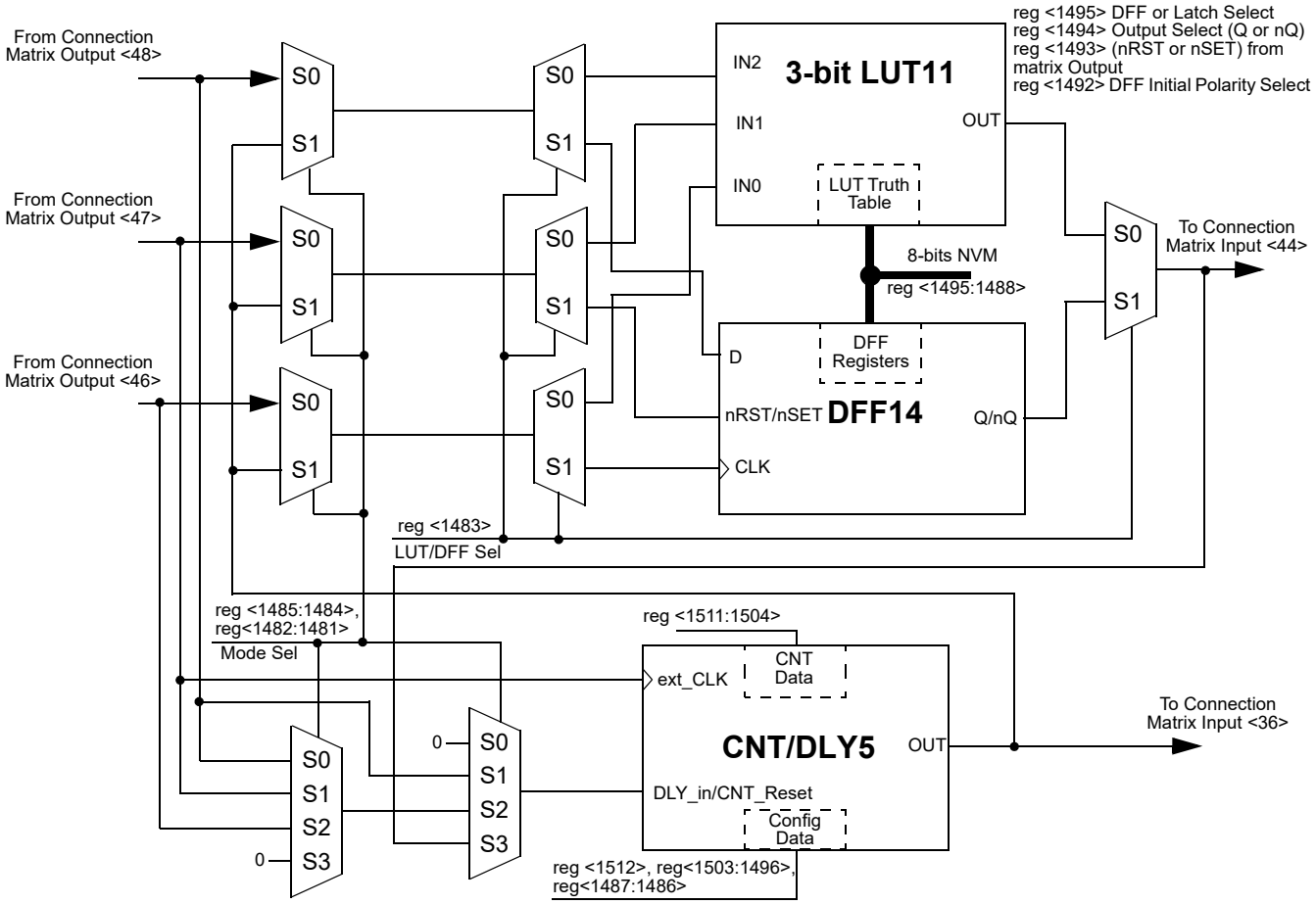


Figure 30: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF14, CNT/DLY5)

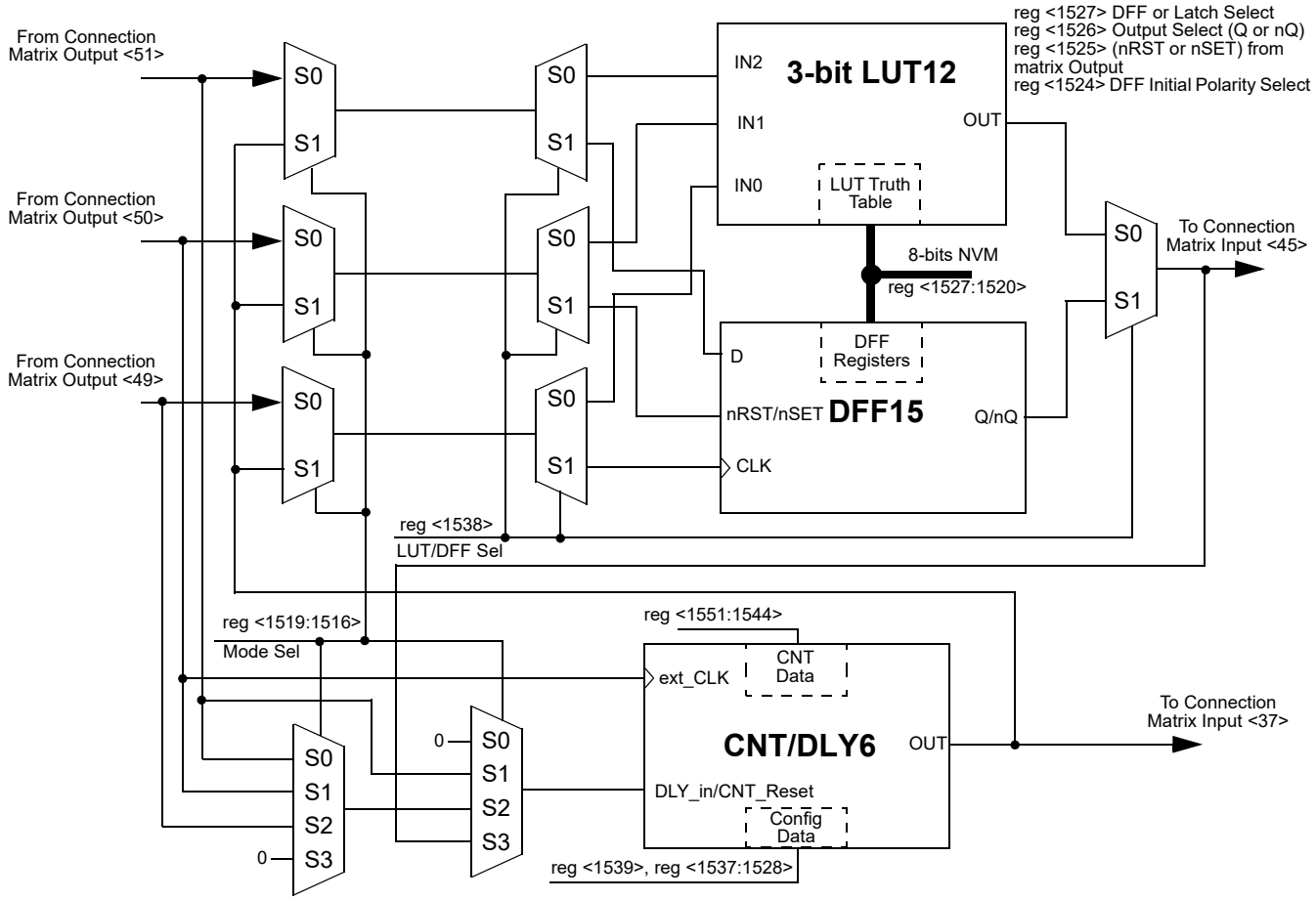


Figure 31: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF15, CNT/DLY6)

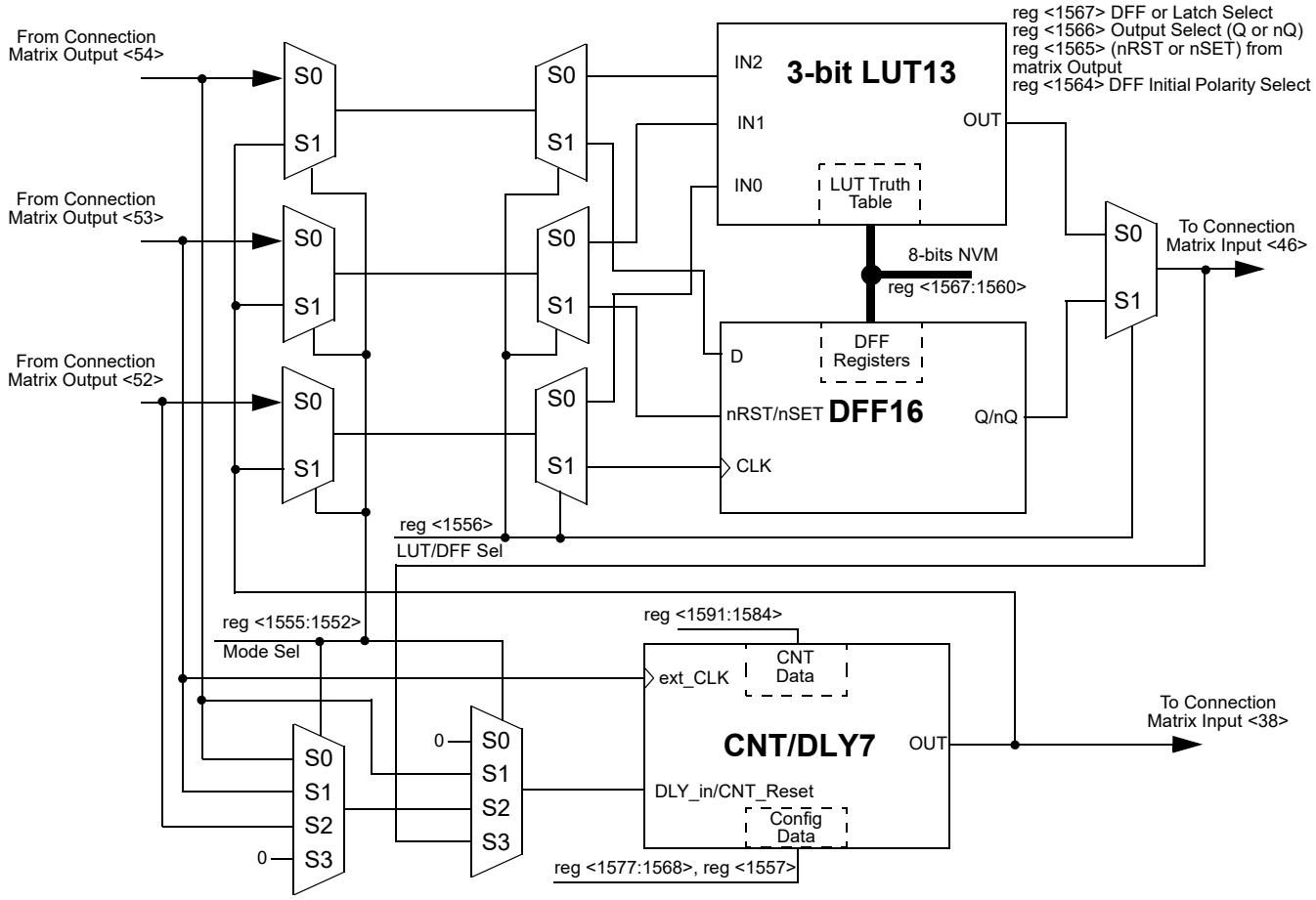


Figure 32: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF16, CNT/DLY7)

As shown in Figures 24-30 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note 5: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter / Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (in and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 36: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1344>	LSB
0	0	1	reg <1345>	
0	1	0	reg <1346>	
0	1	1	reg <1347>	
1	0	0	reg <1348>	
1	0	1	reg <1349>	
1	1	0	reg <1350>	
1	1	1	reg <1351>	MSB

Table 37: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1376>	LSB
0	0	1	reg <1377>	
0	1	0	reg <1378>	
0	1	1	reg <1379>	
1	0	0	reg <1380>	
1	0	1	reg <1381>	
1	1	0	reg <1382>	
1	1	1	reg <1383>	MSB

Table 38: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1416>	LSB
0	0	1	reg <1417>	
0	1	0	reg <1418>	
0	1	1	reg <1419>	
1	0	0	reg <1420>	
1	0	1	reg <1421>	
1	1	0	reg <1422>	
1	1	1	reg <1423>	MSB

Table 39: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1448>	LSB
0	0	1	reg <1449>	
0	1	0	reg <1450>	
0	1	1	reg <1451>	
1	0	0	reg <1452>	
1	0	1	reg <1453>	
1	1	0	reg <1454>	
1	1	1	reg <1455>	MSB

Table 40: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1488>	LSB
0	0	1	reg <1489>	
0	1	0	reg <1490>	
0	1	1	reg <1491>	
1	0	0	reg <1492>	
1	0	1	reg <1493>	
1	1	0	reg <1494>	
1	1	1	reg <1495>	MSB

Table 41: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1520>	LSB
0	0	1	reg <1521>	
0	1	0	reg <1522>	
0	1	1	reg <1523>	
1	0	0	reg <1524>	
1	0	1	reg <1525>	
1	1	0	reg <1526>	
1	1	1	reg <1527>	MSB

Table 42: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	reg <1560>	LSB
0	0	1	reg <1561>	
0	1	0	reg <1562>	
0	1	1	reg <1563>	
1	0	0	reg <1564>	
1	0	1	reg <1565>	
1	1	0	reg <1566>	
1	1	1	reg <1567>	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT7 is defined by reg<1351:1344>

3-Bit LUT8 is defined by reg<1383:1376>

3-Bit LUT9 is defined by reg<1423:1416>

3-Bit LUT10 is defined by reg<1455:1448>

3-Bit LUT11 is defined by reg<1495:1488>

3-Bit LUT12 is defined by reg<1527:1520>

3-Bit LUT13 is defined by reg<1567:1560>

8.2 CNT/DLY/FSM TIMING DIAGRAMS

8.2.1 Delay Mode (edge select: both, counter data: 3) CNT/DLY0 to CNT/DLY7

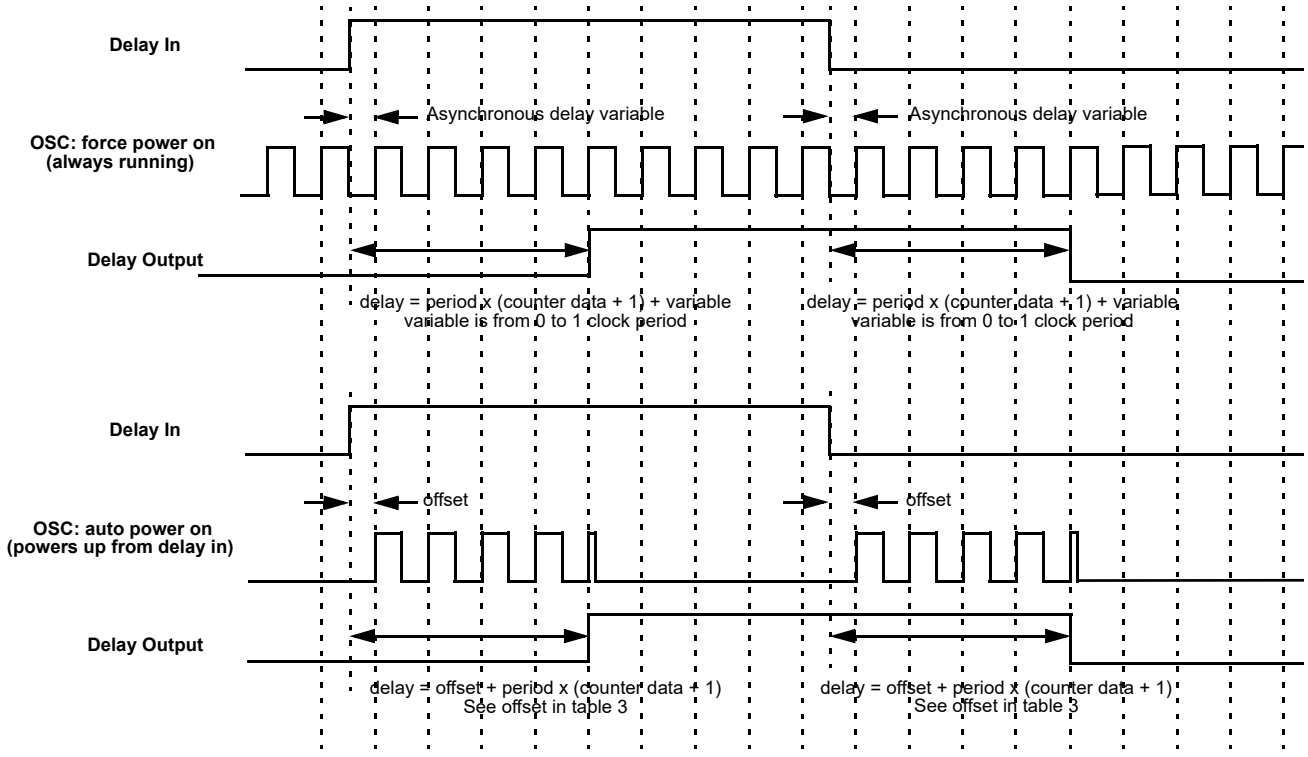


Figure 33: Delay Mode Timing Diagram

8.2.2 Count Mode (count data: 3), Counter Reset (rising edge detect) CNT/DLY0 to CNT/DLY7

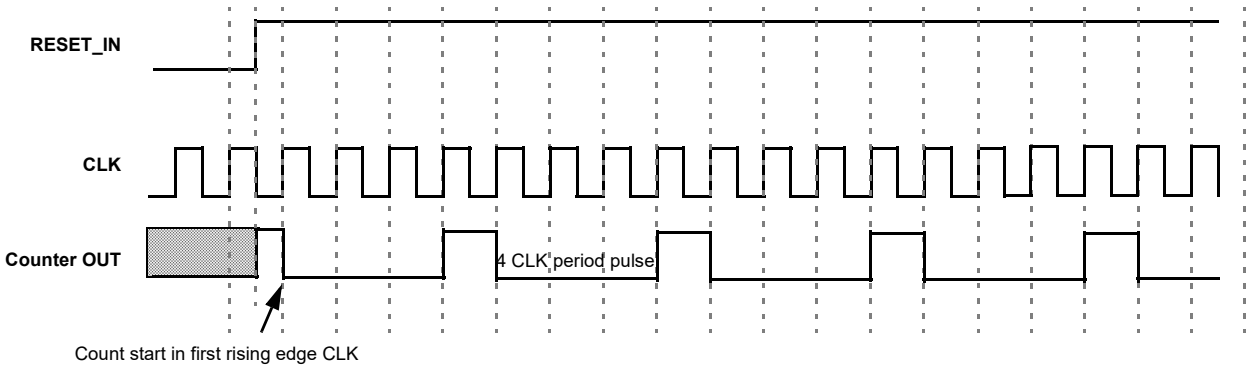


Figure 34: Counter Mode Timing Diagram without two DFFs synced up

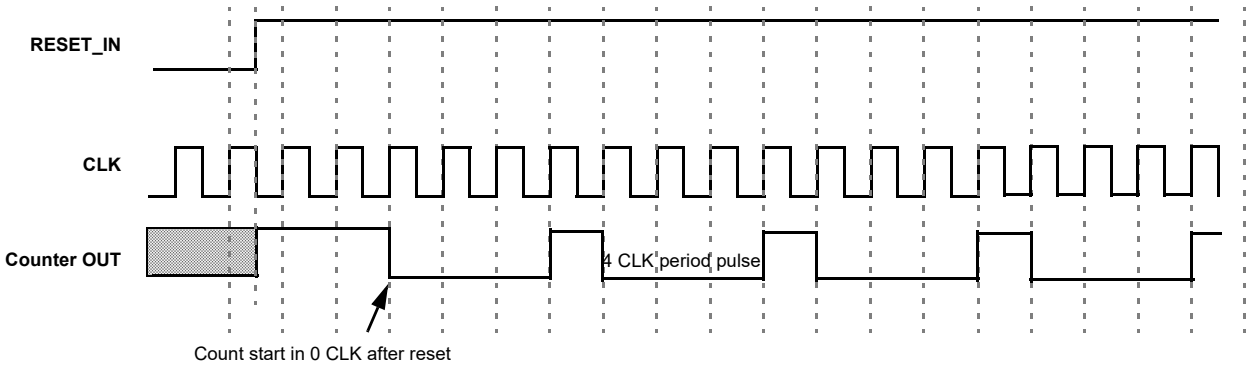


Figure 35: Counter Mode Timing Diagram with two DFFs synced up

8.2.3 One-Shot Mode CNT/DLY0 to CNT/DLY7

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

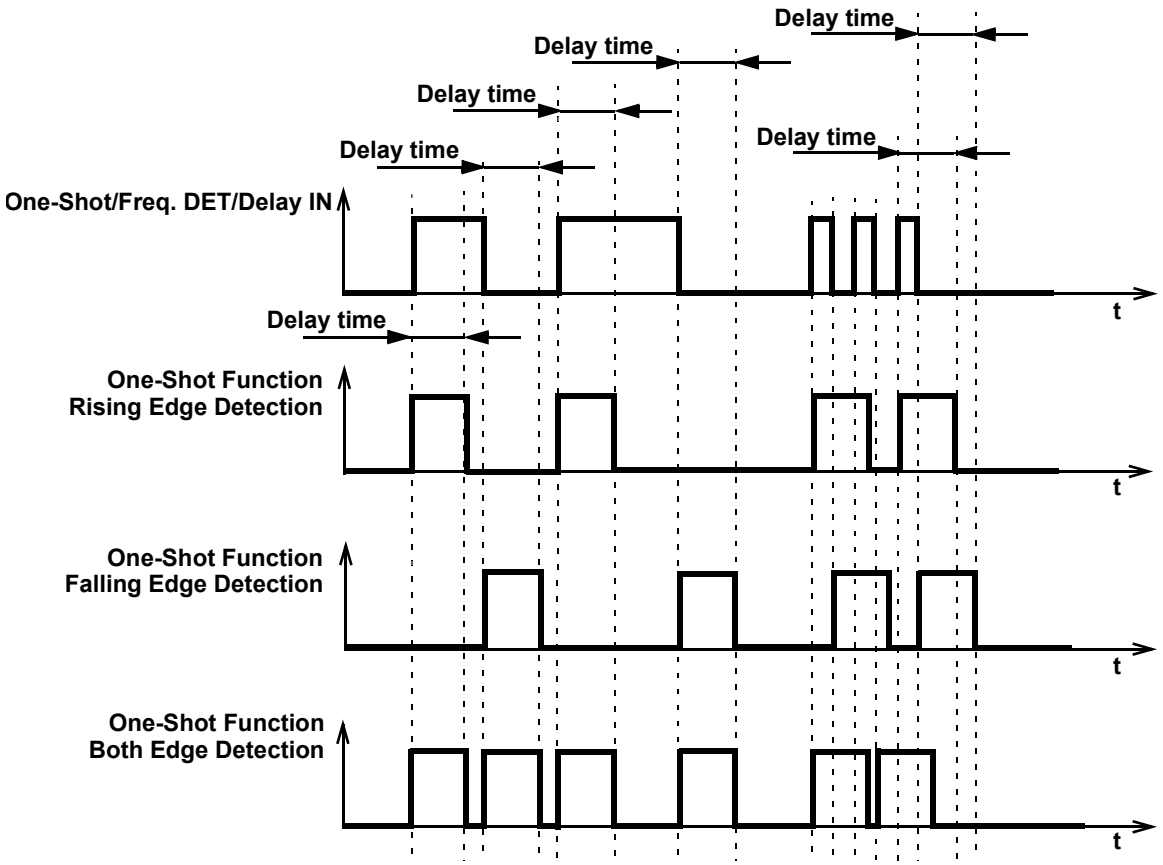


Figure 36: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.2.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY7

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

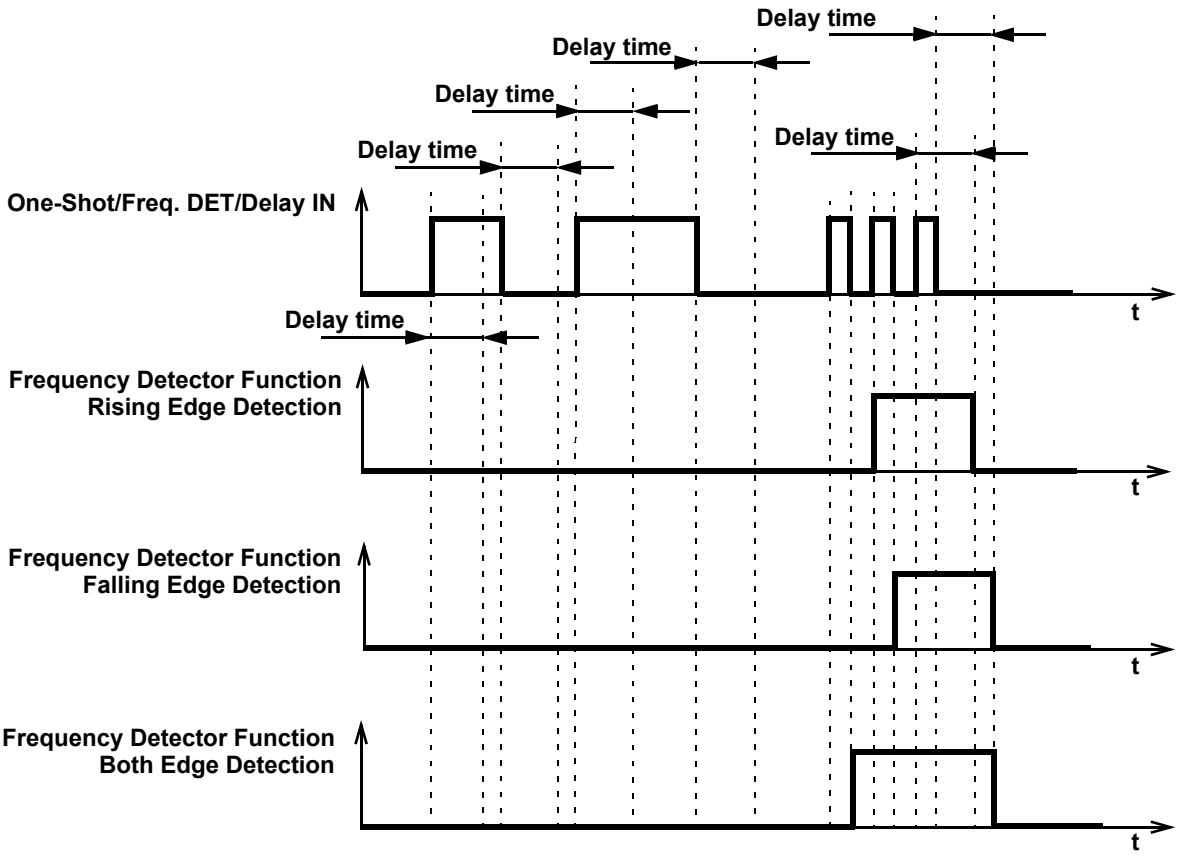


Figure 37: Frequency Detection Mode Timing Diagram

8.2.5 Edge Detection Mode CNT/DLY1 to CNT/DLY7

The macrocell generates high level short pulse when detecting the respective edge. See Table 8.

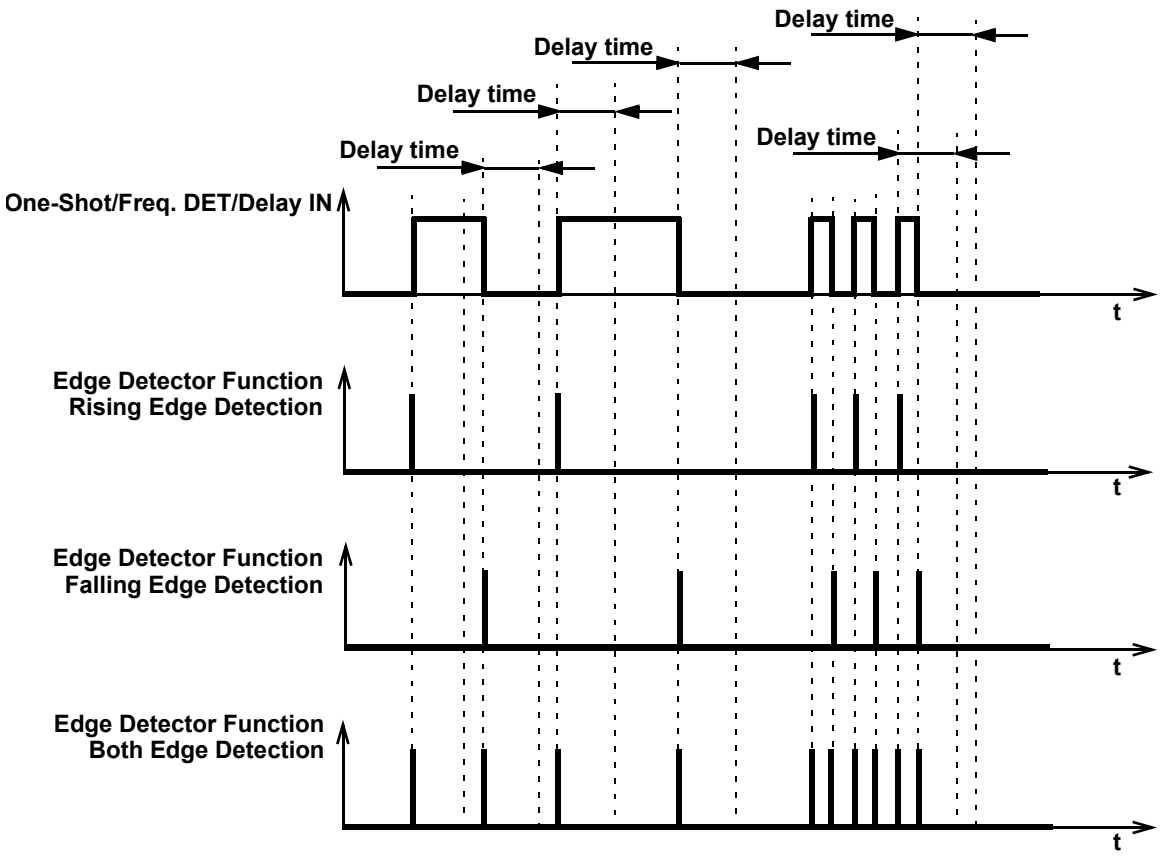


Figure 38: Edge Detection Mode Timing Diagram

8.2.6 Delay Mode CNT/DLY0 to CNT/DLY7

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

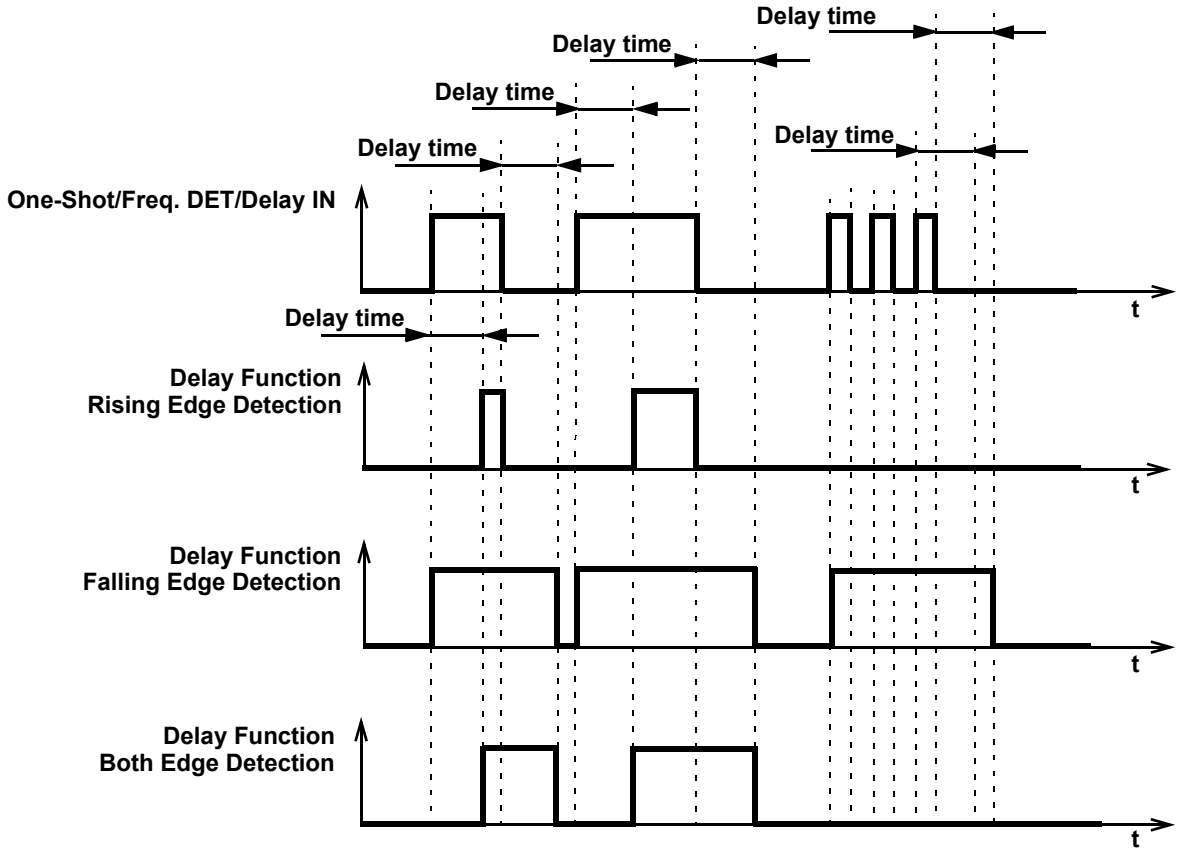


Figure 39: Delay Mode Timing Diagram

8.2.7 CNT/FSM Mode CNT/DLY0

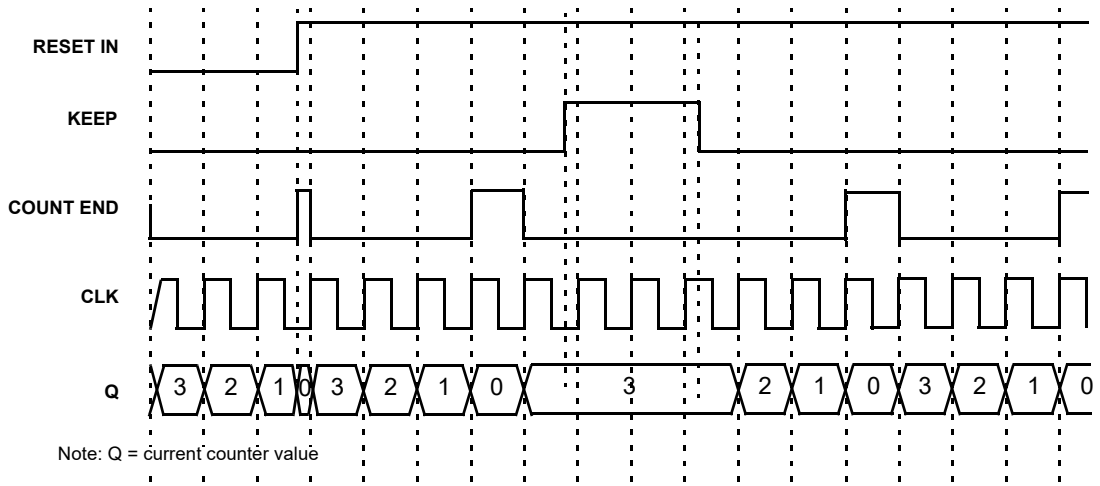


Figure 40: CNT/FSM Timing Diagram (reset rising edge mode, oscillator is forced on, UP=0) for Counter Data = 3

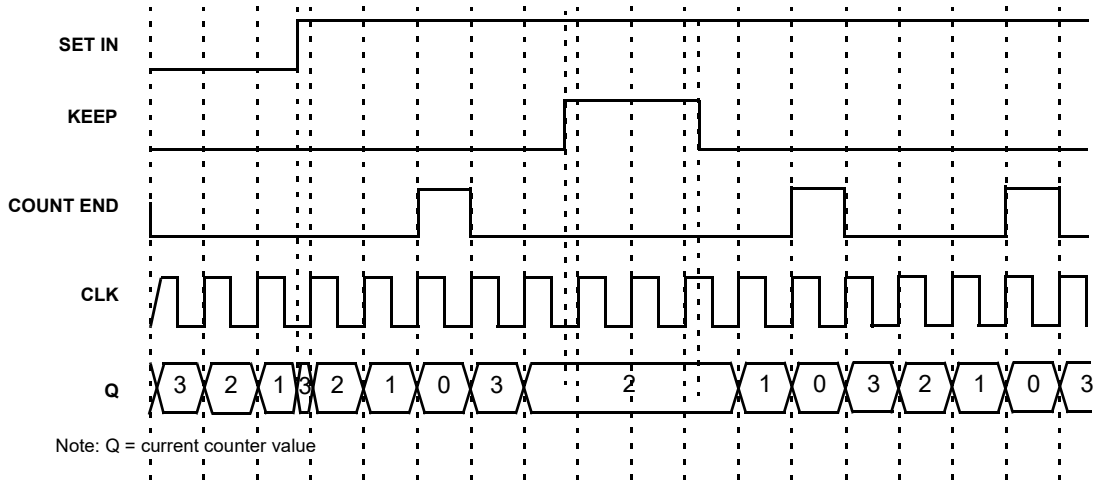


Figure 41: CNT/FSM Timing Diagram (set rising edge mode, oscillator is forced on, UP=0) for Counter Data = 3

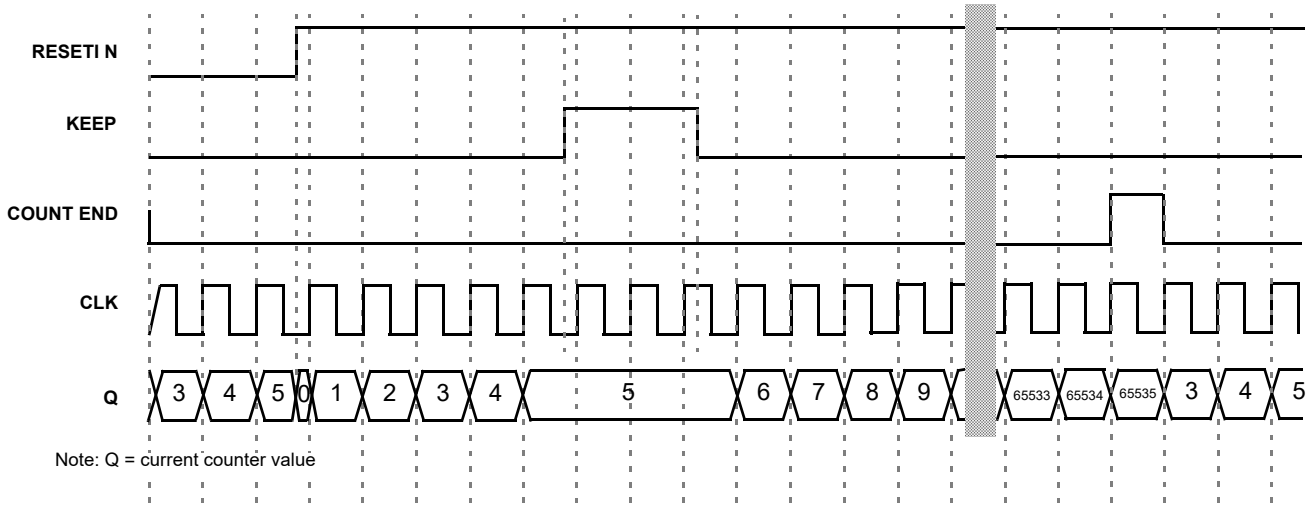


Figure 42: CNT/FSM Timing Diagram (reset rising edge mode, oscillator is forced on, UP=1) for Counter Data = 3

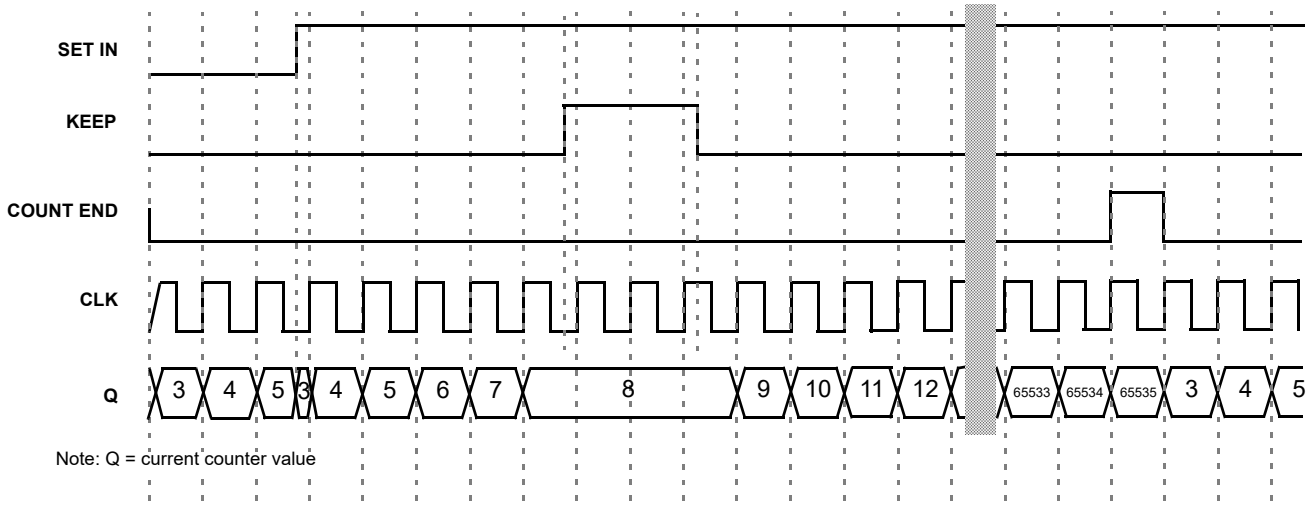


Figure 43: CNT/FSM Timing Diagram (set rising edge mode, oscillator is forced on, UP=1) for Counter Data = 3

8.2.8 Difference in Counter Value for Counter, Delay, One-Shot and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 44

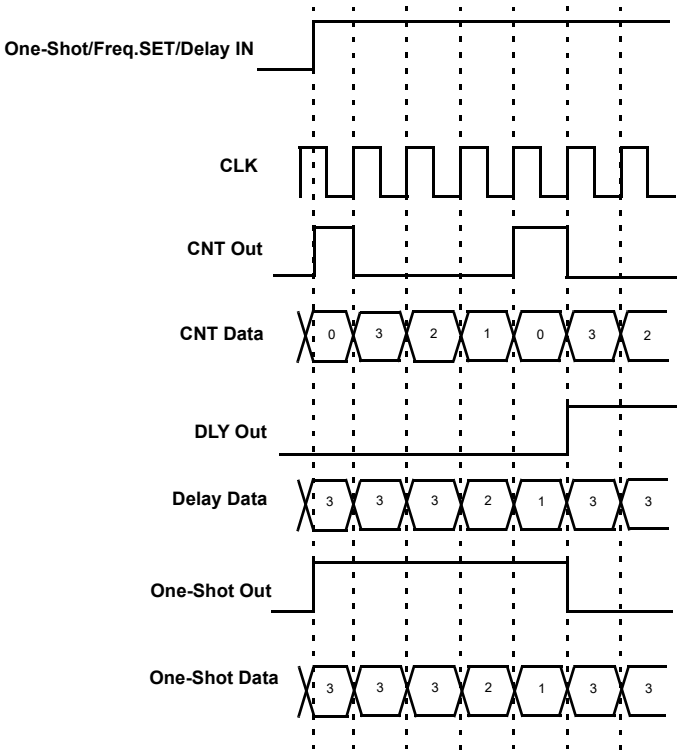


Figure 44: Counter Value, Counter Data = 3

8.3 4-BIT LUT OR 16-BIT COUNTER / DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter / Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix or can be connected to CNT/DLY's input or LUT/DFF's input. When used to implement 16-Bit Counter / Delay function, two of the four input signals from the connection matrix go to the external clock (ext_CLK) and reset (DLY_in/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.
This macrocell can also operate in a frequency detection.
This macrocell can have its active count value read via I^2C. See Section 15.5.3 for further details

8.3.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

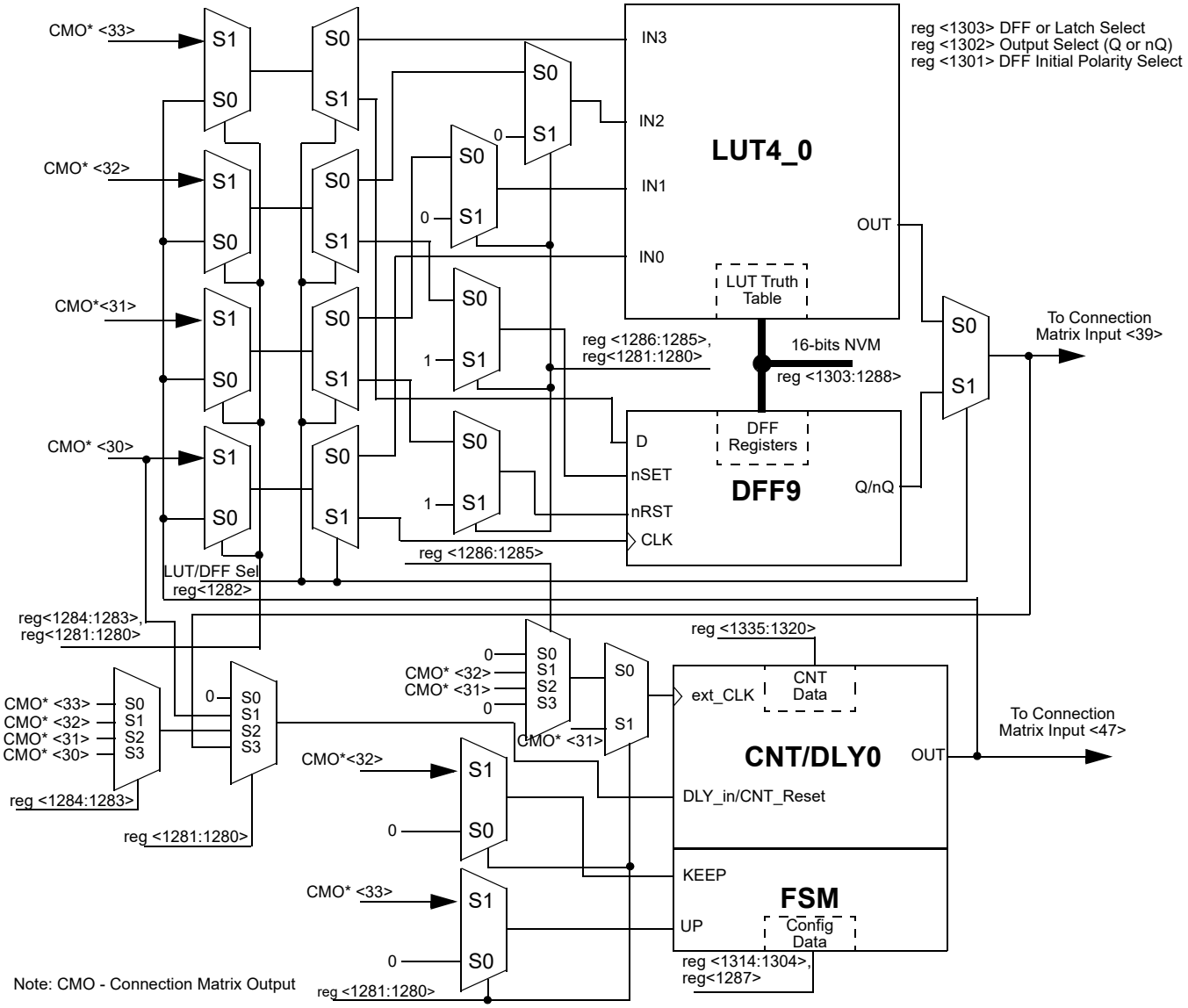


Figure 45: 4-bit LUT0 or CNT/DLY0

8.3.2 4-Bit LUT or 16-Bit Counter / Delay Macrocells Used as 4-Bit LUTs

Table 43: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	reg<1288>	LSB
0	0	0	1	reg<1289>	
0	0	1	0	reg<1290>	
0	0	1	1	reg<1291>	
0	1	0	0	reg<1292>	
0	1	0	1	reg<1293>	
0	1	1	0	reg<1294>	
0	1	1	1	reg<1295>	
1	0	0	0	reg<1296>	
1	0	0	1	reg<1297>	
1	0	1	0	reg<1298>	
1	0	1	1	reg<1299>	
1	1	0	0	reg<1300>	
1	1	0	1	reg<1301>	
1	1	1	0	reg<1302>	
1	1	1	1	reg<1303>	MSB

This Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg<1303:1288>

Table 44: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

9 Analog Comparators

There are two General Purpose Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG46824. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0L_pd and ACMP1L_pd) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

ACMPs are optimized for low power operation.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then become valid TBD µs (max) after power up signal goes high for ACMP0L and ACMP1L. Vref accuracy is optimized near TBD mV selection. Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 1 MΩ resistors. IN- voltage range: 0 – 2.016 V.

It is possible to enable Low Pass Filter (LPF) either on ACMP IN+ or on ACMP OUT.

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV / 32 mV / 64 mV / 192 mV.

ACMP0L IN+ options are IO11
ACMP1L IN+ options are IO12

9.1 ACMP0L BLOCK DIAGRAM

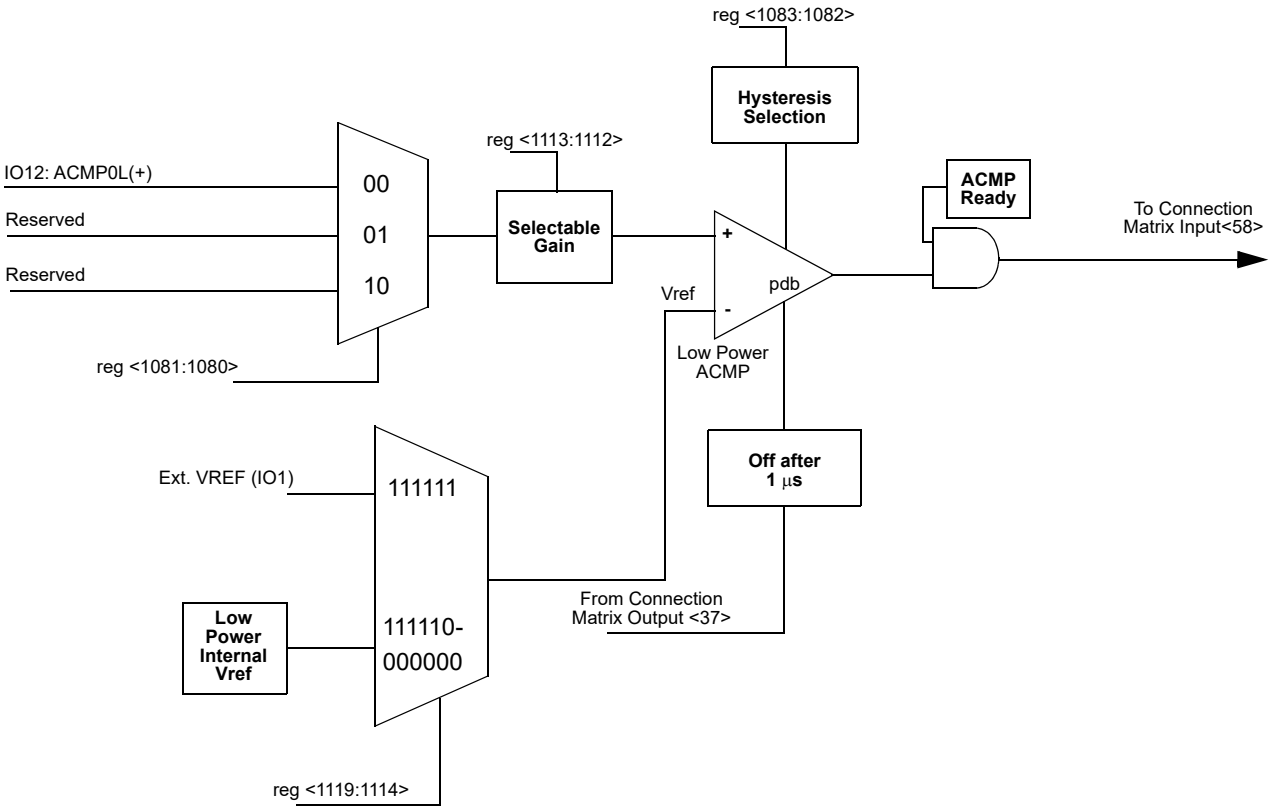


Figure 46: ACMP0L Block Diagram

9.2 ACMP1L BLOCK DIAGRAM

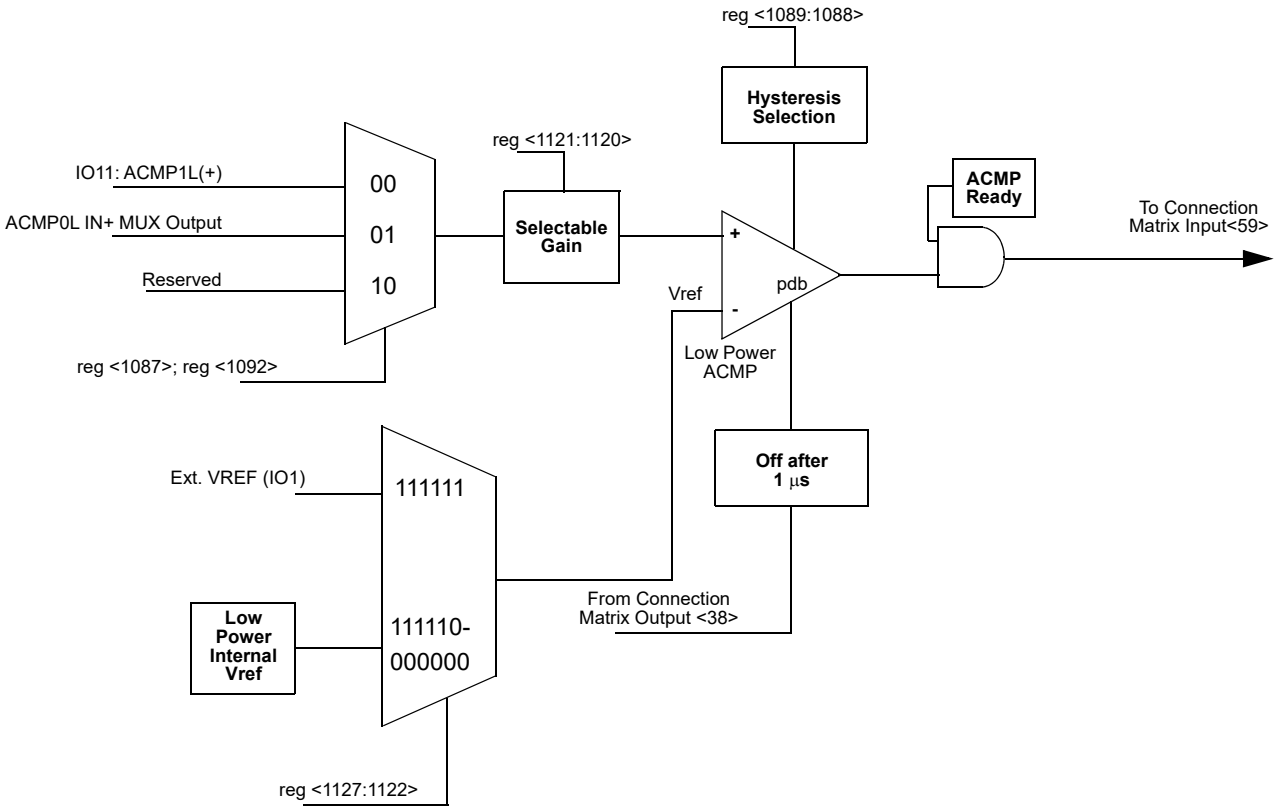


Figure 47: ACMP1L Block Diagram

10 Programmable Delay / Edge Detector

The SLG46824 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time 2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See Figure 49 for further information.

Note 6: The input signal must be longer than the delay, otherwise it will be filtered out.

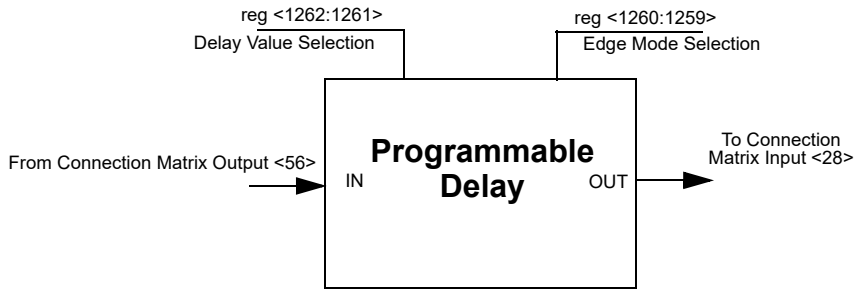


Figure 48: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

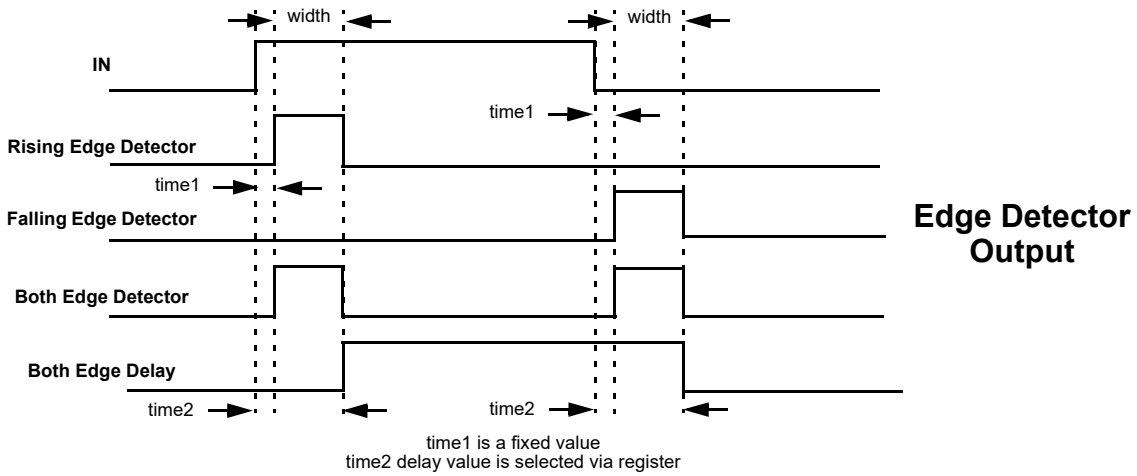


Figure 49: Edge Detector Output

Please refer to Table 8.

11 Additional Logic Function. Deglitch Filter

The SLG46824 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

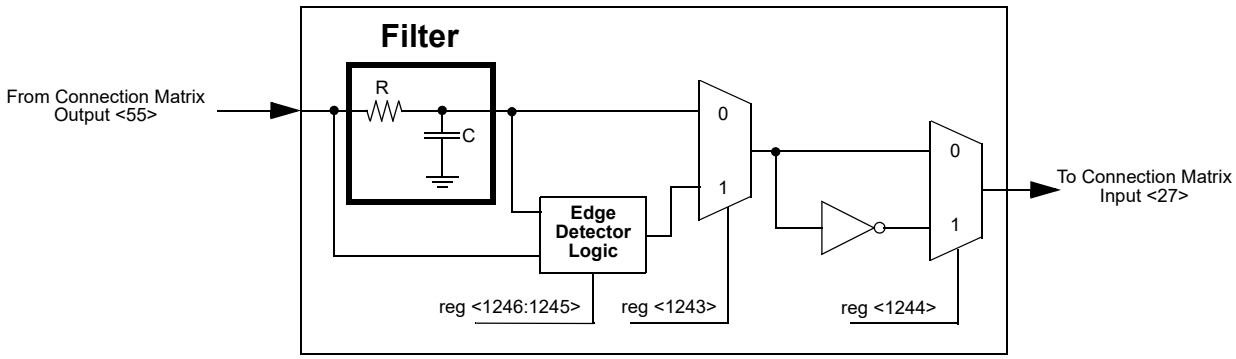


Figure 50: Deglitch Filter / Edge Detector

12 Voltage Reference (VREF)

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46824 has a Voltage Reference Macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage reference. The macrocell also has the option to output reference voltage on IO9. See Table 45 for the available selections for each analog comparator. Also see Figure 51, which shows the reference output structure.

12.2 VREF SELECTION TABLE

Table 45: VREF Selection Table

SEL<5:0>	VREF	SEL<5:0>	VREF
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

12.3 VREF BLOCK DIAGRAM

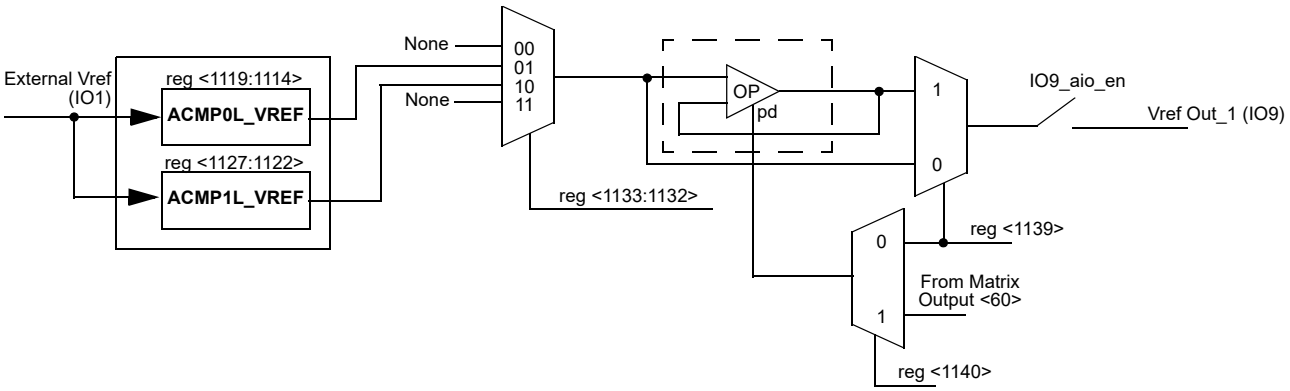


Figure 51: Voltage Reference Block Diagram

13 Clocking

13.1 OSC GENERAL DESCRIPTION

The SLG46824 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The predivider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the predivider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines <27>, <28> and <29>. Please see Figure 55, for more details on the SLG46824 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by reg <1052>. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power Down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power Down/Force On (Connection Matrix Output <72>, <73>, <74>) signal has the highest priority. The OSC operates according to the following table:

Table 46: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power Down or Force On by Matrix Input	Regster: Auto Power On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

Note 7: The OSC will run only when any macrocell that uses OSC is powered on.

13.2 OSCILLATOR0 (2.048 KHZ)

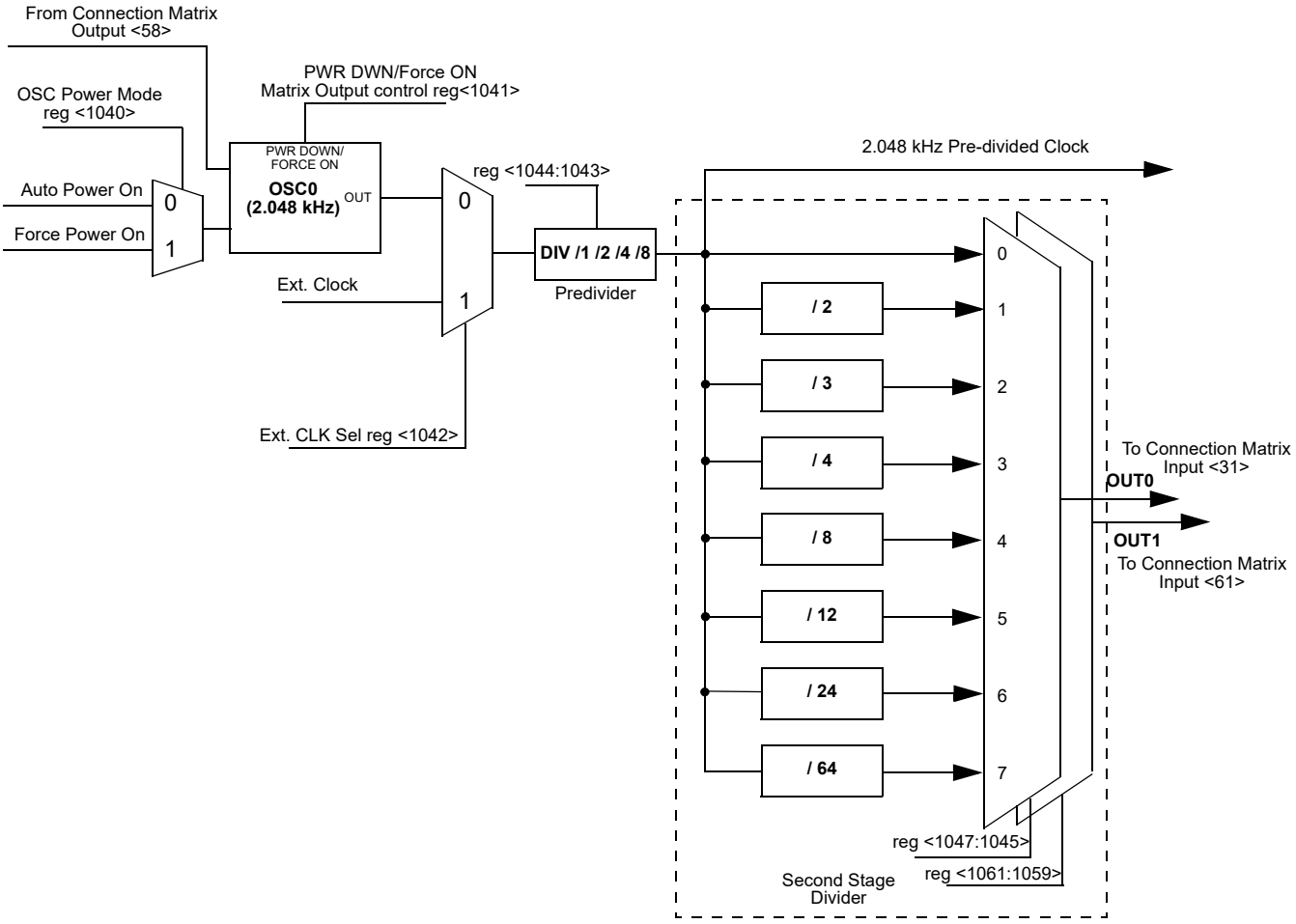


Figure 52: Oscillator0 Block Diagram

13.3 OSCILLATOR1 (2.048 MHZ)

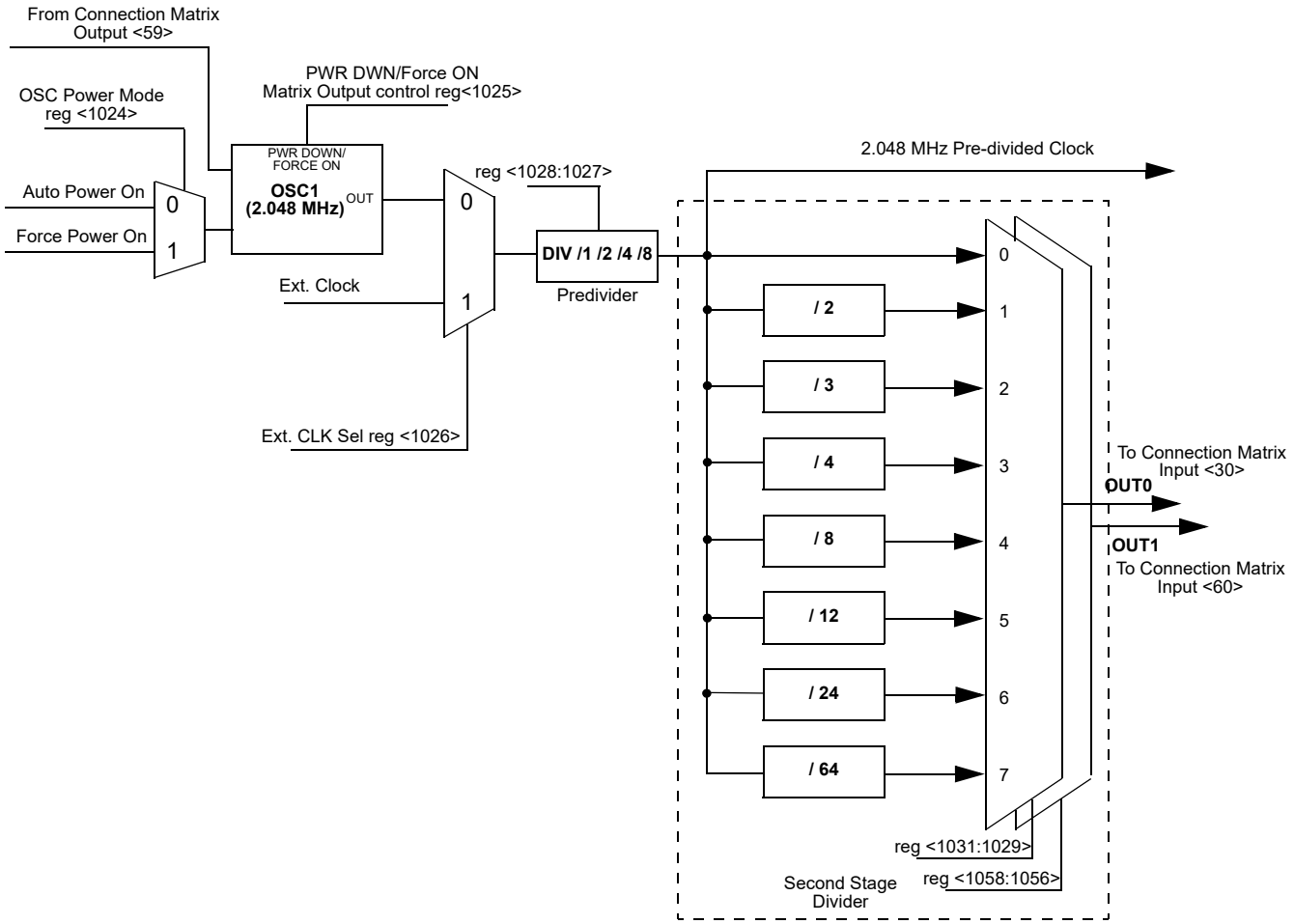


Figure 53: Oscillator1 Block Diagram

13.4 OSCILLATOR2 (25 MHZ)

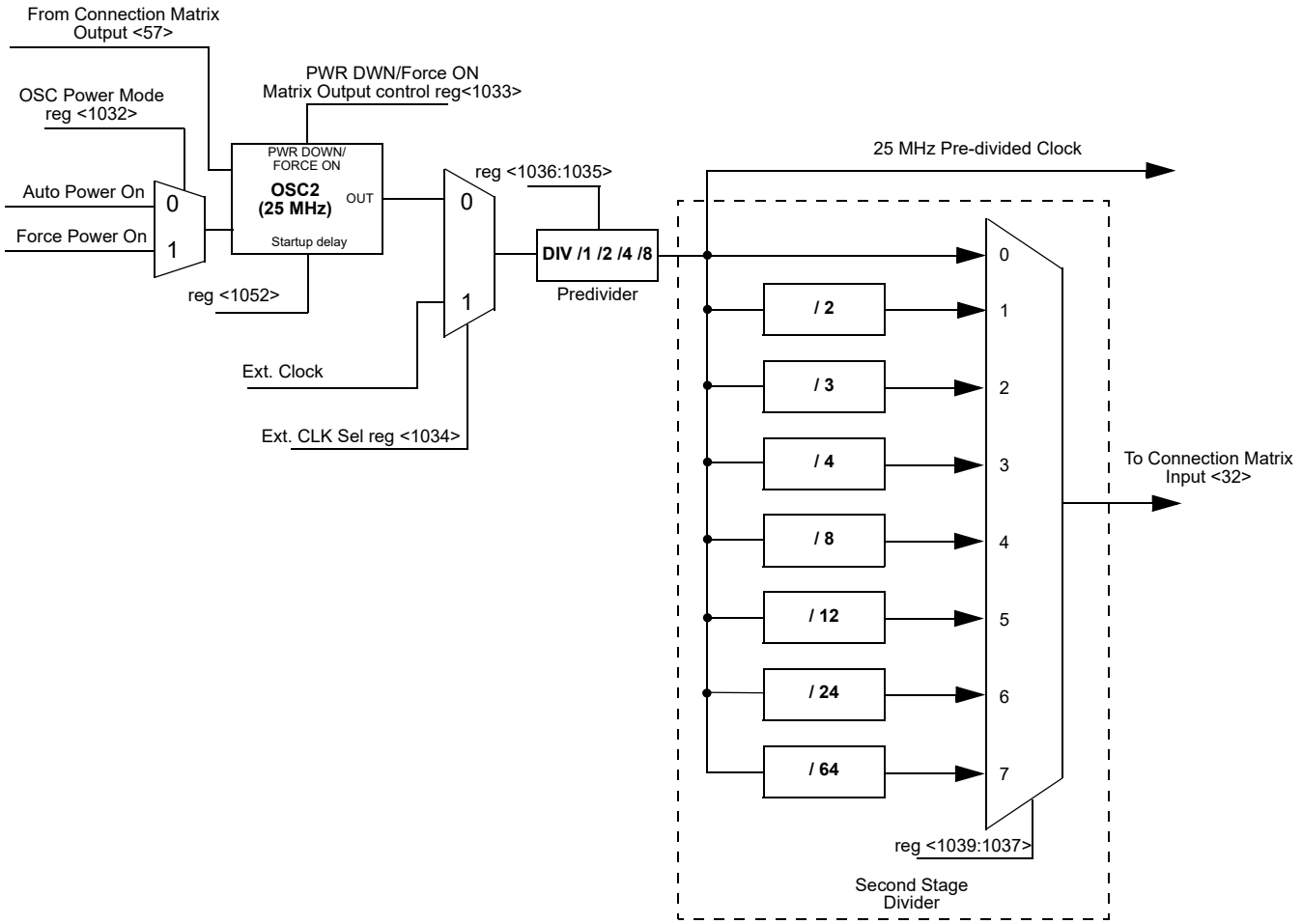


Figure 54: Oscillator2 Block Diagram

13.5 CLOCK SCHEME

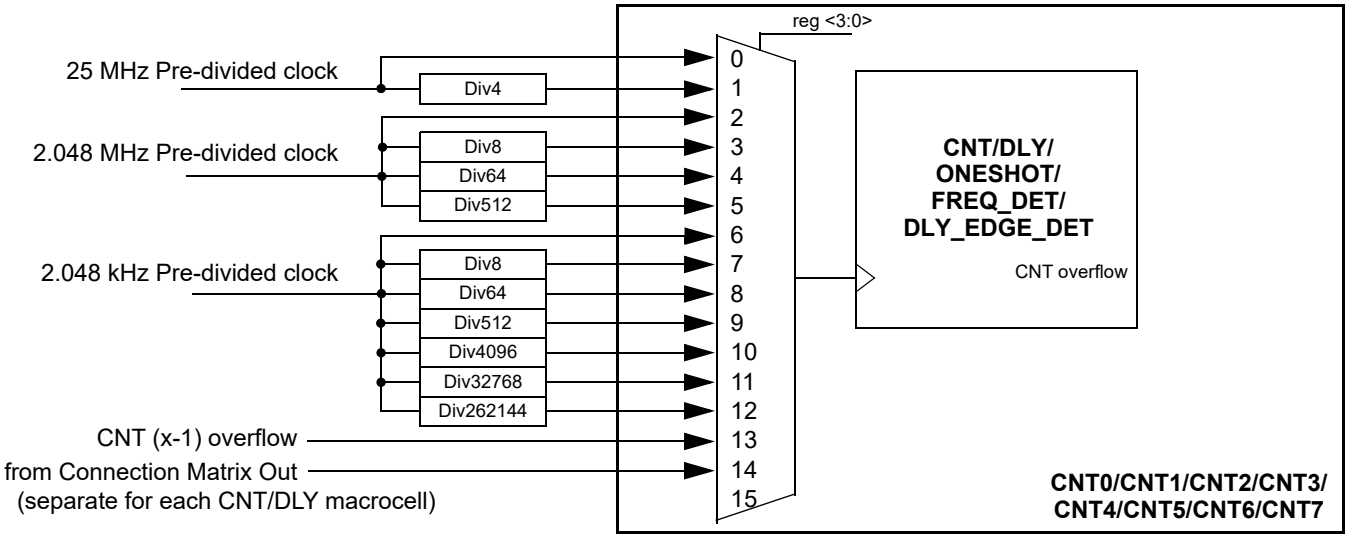


Figure 55: Clock Scheme

13.6 EXTERNAL CLOCKING

The SLG46824 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.6.1 IO0 Source for Oscillator0 (2.048 kHz)

When reg<1042> is set to 1, an external clocking signal on IO0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 52.The high and low limits for frequency that can be selected are TBD MHz and TBD MHz.

13.6.2 IO10 Source for Oscillator1 (2.048 MHz)

When reg<1026> is set to 1, an external clocking signal on IO10 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 53. The high and low limits for frequency that can be selected are TBD MHz and TBD MHz.

13.6.3 IO8 Source for Oscillator2 (25 MHz)

When reg<1034> is set to 1, an external clocking signal on IO8 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 54. The high and low limits for frequency that can be selected are TBD MHz and TBD MHz.

14 Power On Reset (POR)

The SLG46824 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 GENERAL OPERATION

The SLG46824 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than Power Off Threshold (see in Table 4), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher **(Note 8)** than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 8: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46824, the voltage applied on the V_{DD} should be higher than the Power_ON threshold **(Note 9)**. The full operational V_{DD} range for the SLG46824 is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46824 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note 9: The Power_ON threshold is defined in Table 4.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 56.

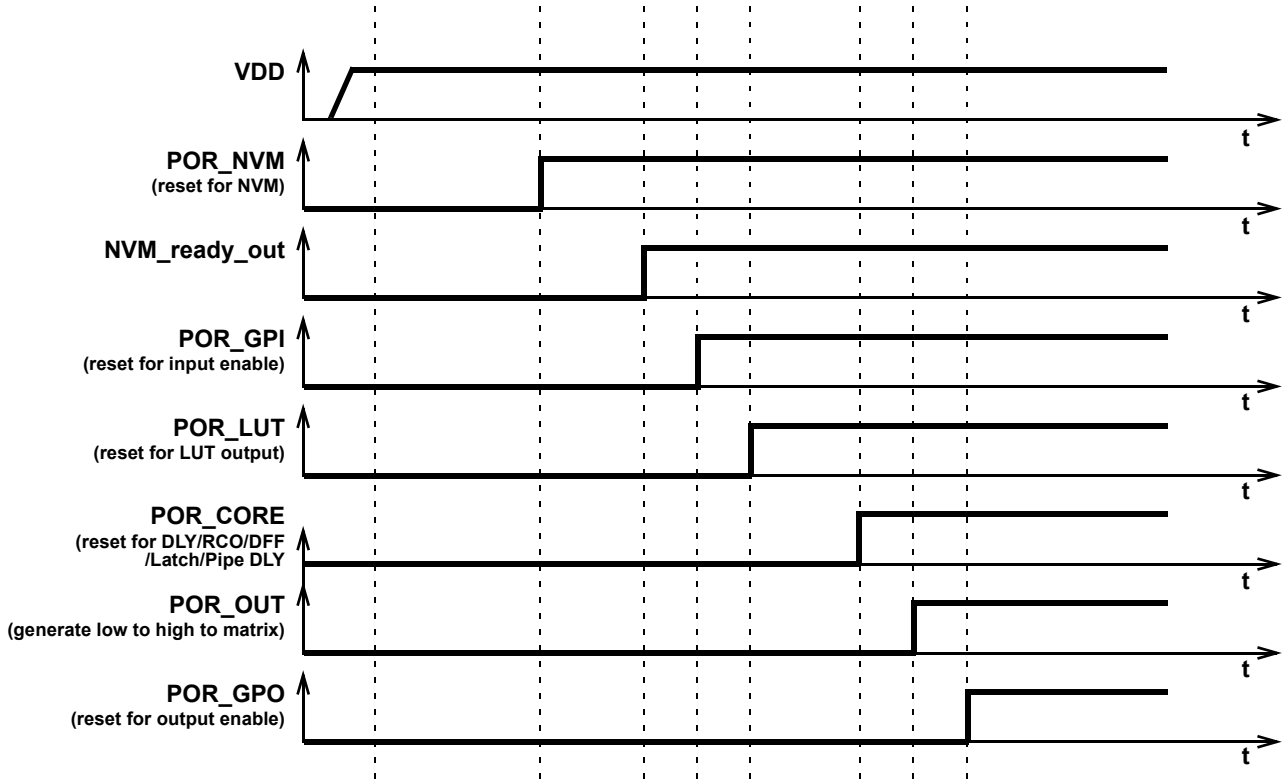


Figure 56: POR sequence

As can be seen from Figure 56 after the V_{DD} has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to a CMOS Latch that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature and even will vary from chip to chip (process influence).

14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46824 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 57 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled.

Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

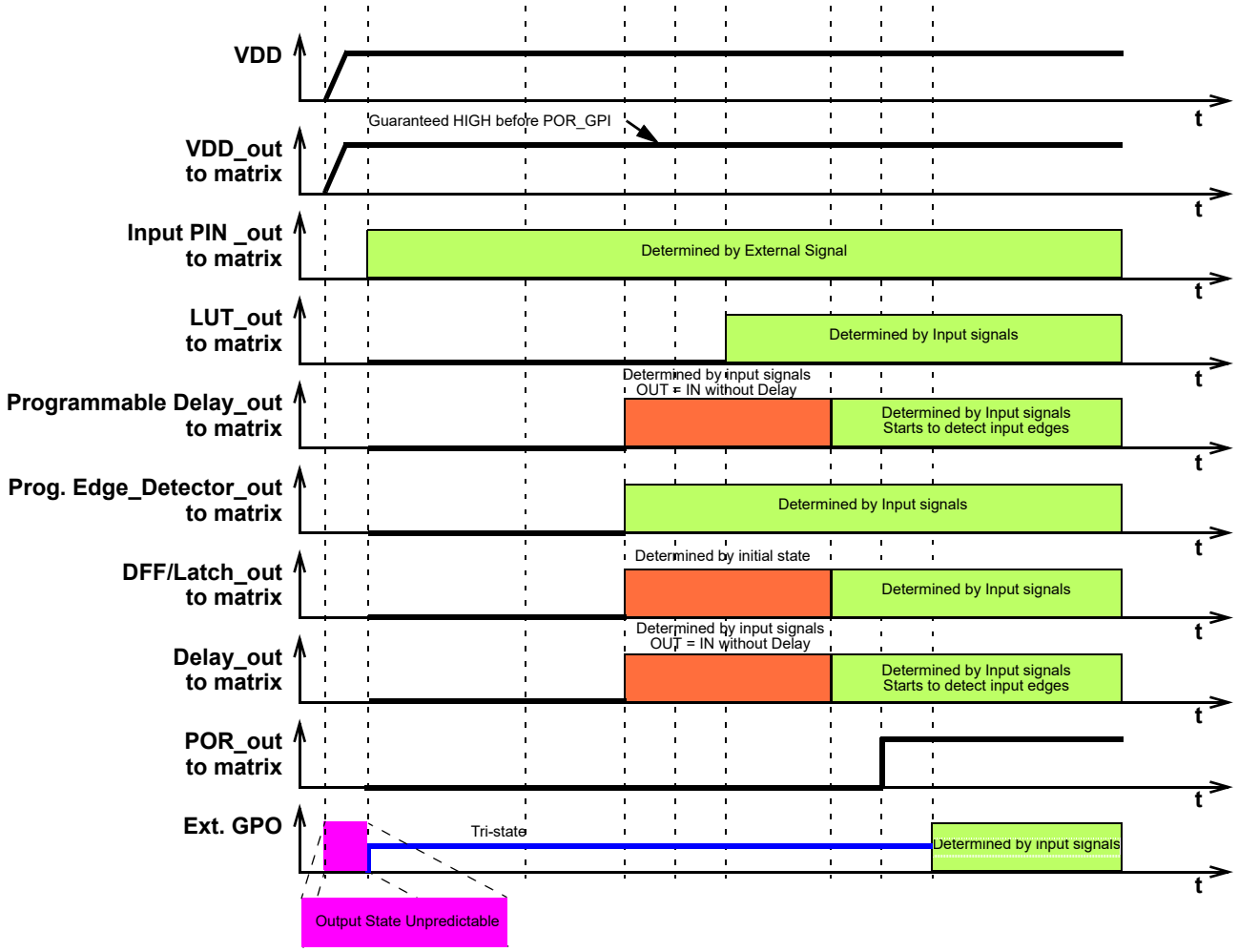


Figure 57: Internal Macrocell States during POR sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.62 V to 1.98 V, macrocells in SLG46824 are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output pin corresponds to the internal logic

The VREF output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note 10: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin –> V_{DD} and pin –> GND on each

pin. So if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power Down

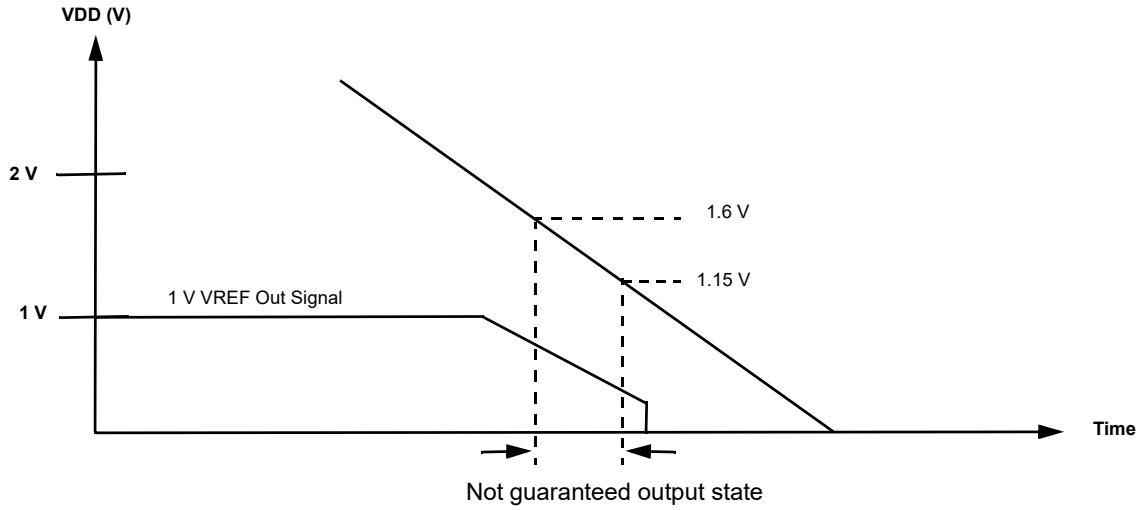


Figure 58: Power Down

During powerdown, macrocells in SLG46824 are powered off after V_{DD} falling down below Power Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15 I²C Serial Communications Macrocell

15.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits reg<1795:1792>. See Section 16 for more details on I²C read/write memory protection.

15.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 59. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by IO5, IO4, IO3 and IO2. The LSB of the control code is defined by the value of IO2, while the MSB is defined by the value of IO5. The address source (either register bit or PIN) for each bit in the control code is defined by reg <1623:1620>. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus.The default control code is 0001. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 16K bytes. The valid addresses are shown in the memory map in Figure 69.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

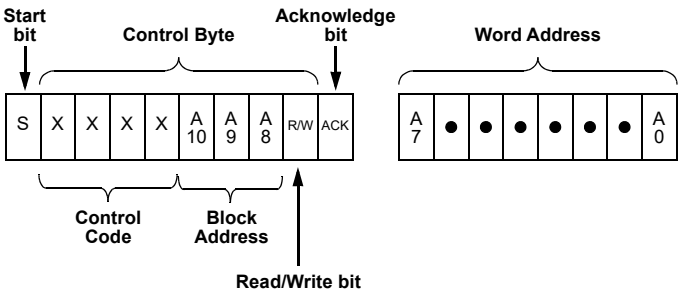


Figure 59: Basic Command Structure

15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 60. Timing specifications can be found in the Section 3.3.

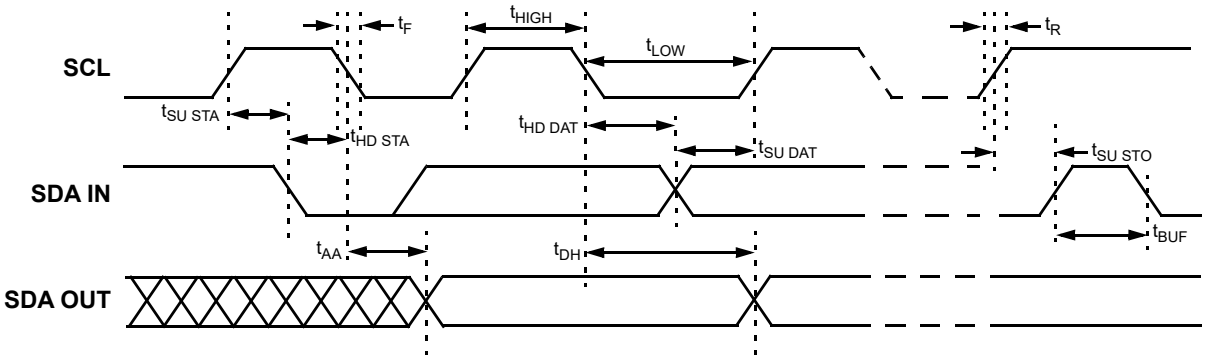


Figure 60: I²C General Timing Characteristics

15.4 I²C SERIAL COMMUNICATIONS COMMANDS

15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits] and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46824 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46824 where the data byte is to be written. After the SLG46824 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46824 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46824 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command to the register configuration data (block address A10A9A8 = 000), reg<1602>=1 - Enable. It means that IOs will remain their state until the write command is done.

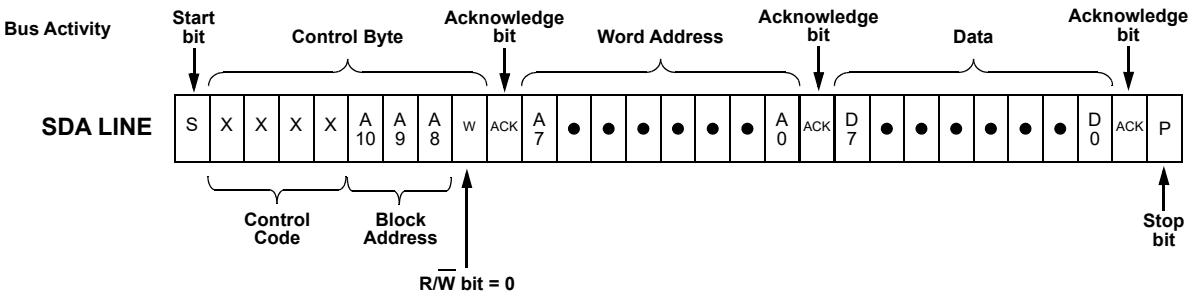


Figure 61: Byte Write Command, R/$\overline{W}$ = 0

15.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46824 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46824. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46824 generates the Acknowledge bit.

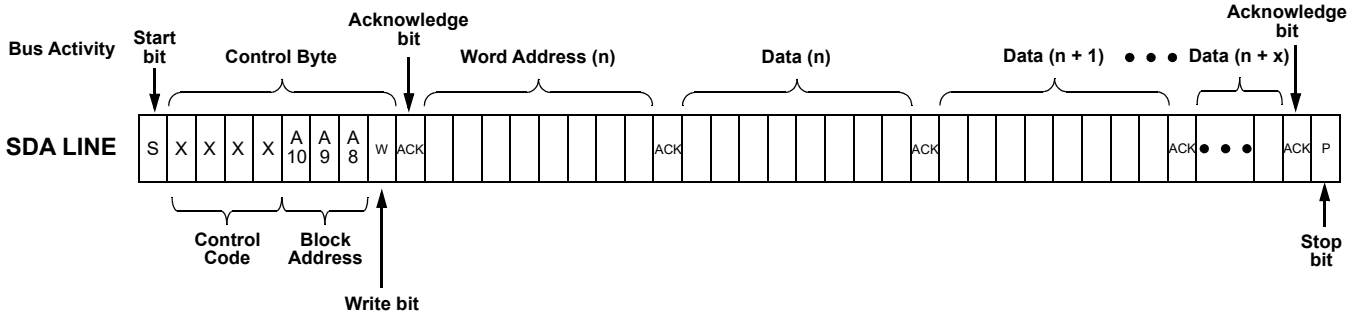


Figure 62: Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46824 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

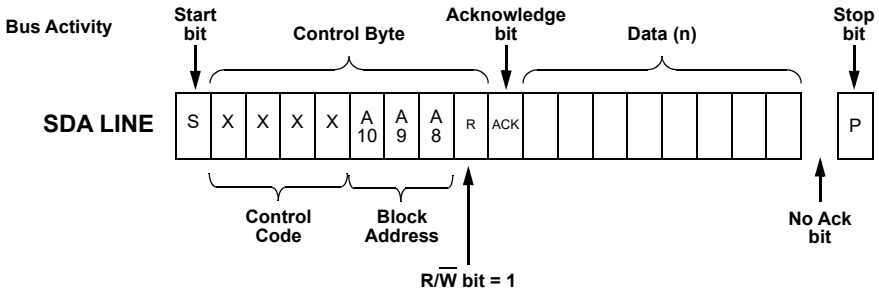


Figure 63: Current Address Read Command, R/$\overline{W}$ = 1

15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address

counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46824 issues an Acknowledge bit, followed by the requested eight data bits.

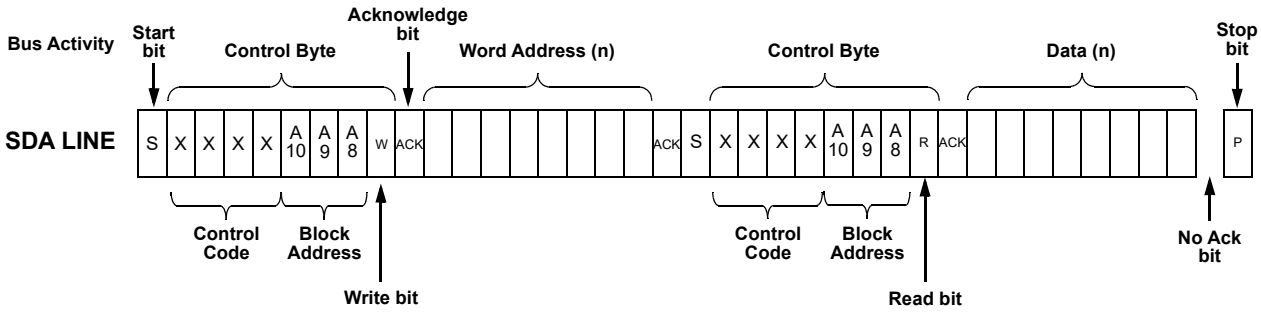


Figure 64: Random Read Command

15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46824 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

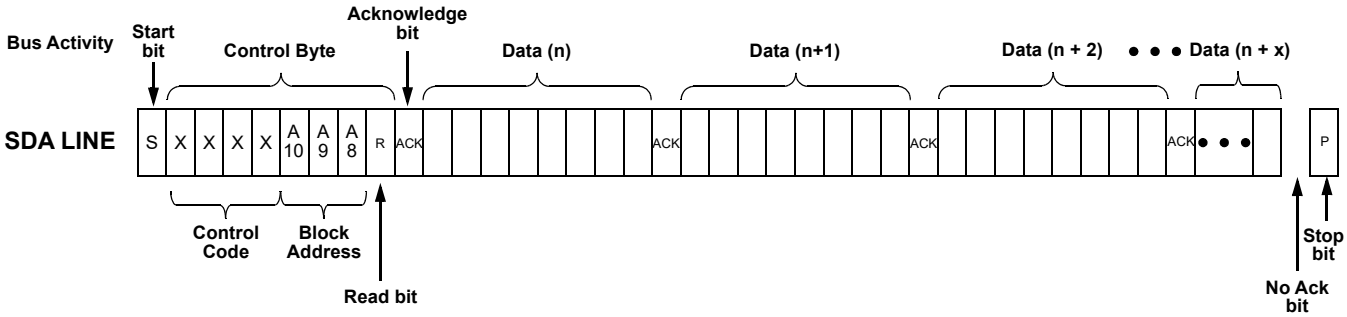


Figure 65: Sequential Read Command

15.5 CHIP CONFIGURATION DATA PROTECTION

The SLG46824 utilizes a scheme that allows a portion or the entire Register and NVM to be inhibited from being read or written/erased. There are two bytes that define the register and NVM access or change. The first byte RPR defines the 2k register read and write protection. The second byte NPR defines the 2k NVM data configuration read and write protection. If desired, the protection lock bit (PRL) can be set so that protection may no longer be modified, thereby making the current protection scheme permanent. The status of the RPR and NPR can be determined by following a Random Read sequence. Changing the state of the RPR and NPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The RPR register is located on H’E0 address, while NPR is located on H’E1 address.

The RPR format is shown in Table 47, and the RPR bit functions are included in Table 48.

Table 47: RPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
RPR					RPRB3	RPRB2	RPRB1	RPRB0

Table 48: RPR Bit Function Description

Bit	Name		Type	Description
3:2	RPRB3	2k Register Write Selection Bits	R/W*	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; Please refer to the Table 51. 10: 2k register data is fully protected for write.
	RPRB2		R/W*	
1:0	RPRB1	2k Register Read Selection Bits	R/W*	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; Please refer to the Table 51. 10: 2k register data is fully protected for read.
	RPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

The NPR format is shown in Table 49, and the NPR bit functions are included in Table 50.

Table 49: NPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
NPR							NPRB1	NPRB0

Table 50: NPR Bit Function Description

Bit	Name		Type	Description
1:0	NPRB1	2k NVM Configuration Selection Bits	R/W*	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase. 11: 2k NVM Configuration data is fully protected for read and write/erase.
	NPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

The protection selection bits allow different levels of protection of the register and NVM Memory Array.

The Protect Lock Bit (PRL) is used to permanently lock (for write and erase) the current state of the RPRL and NPRL as well as NVM protection. A Logic 0 indicates that the protection byte can be modified, whereas a Logic 1 indicates the byte has been locked and can no longer be modified.

In this case it is impossible to erase the whole page E with protection bytes. The PRL is located at E4 address (reg <1824>).

There are nine read/write protect modes for the design sequence from being corrupted or copied. See Table 51 for details.

Table 51: Read/Write Register Protection Options

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
I2C Byte Write Bit Masking (section 15.5.5)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C9
I2C Serial Reset Command (section 15.5.1)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C8b'1

Table 51: Read/Write Register Protection Options

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
Outputs Latching During I2C Write	R/W	R/W	R/W	R/W	R	W	W	R	-	-	C8b'2
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	R	W	W	R	-	-	7A
Configuration Bits for All Macrocells (IOs, ACMPs, Combination Function Macrocells, etc.)	R/W	W	R	-	-	-	W	R	-	-	
Macrocells Inputs Configuration (Connection Matrix Outputs)	R/W	W	R	-	-	-	W	R	-	-	00~47
Protection Mode Selection	R/W	R/W	R	R	R	R	R/W	R	R	R	E4
Macrocells Output Values (Connection Matrix Inputs, section	R	R	R	R	R	-	-	R	-	R	74~79;7B
Counter Current Value	R	R	R	R	R	-	-	R	-	R	7C~7F
Silicon Identification Service Bits	R	R	R	R	R	R	R	R	R	R	F9b'3~F9 b'2
I2C Control Code	R/W	R/W	R	R	R	R	R/W	R	R	R	CAb'3~CA b'0
Page Erase byte	W**	W**	W**	W**	W**	W**	W**	W**	W**	W**	E3

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

R/W* - Becomes read only if protection mode selection (lock bit) is set to 1.

R/W** - Readable/writable depend on the "Trim mode enable" bit. If “Trim mode enable” bit value = 1, then trim bits are enable. If “Trim mode enable” bit value = 0, then trim bits are not writable.

W** - Pages that can be erased are defined by NVM write protection

It is possible to read some data from macrocells, such as counter current value, connection matrix, f(1) computation macrocell stack and connection matrix virtual inputs. The I2C write will do not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, etc.

See Section 17 for detailed information on all registers.

15.5.1 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting reg<1601> I²C reset bit to "1", which causes the device to re-enable the Power On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of reg<1601> will be set to "0" automatically. Figure 66 illustrates the sequence of events for this reset function.

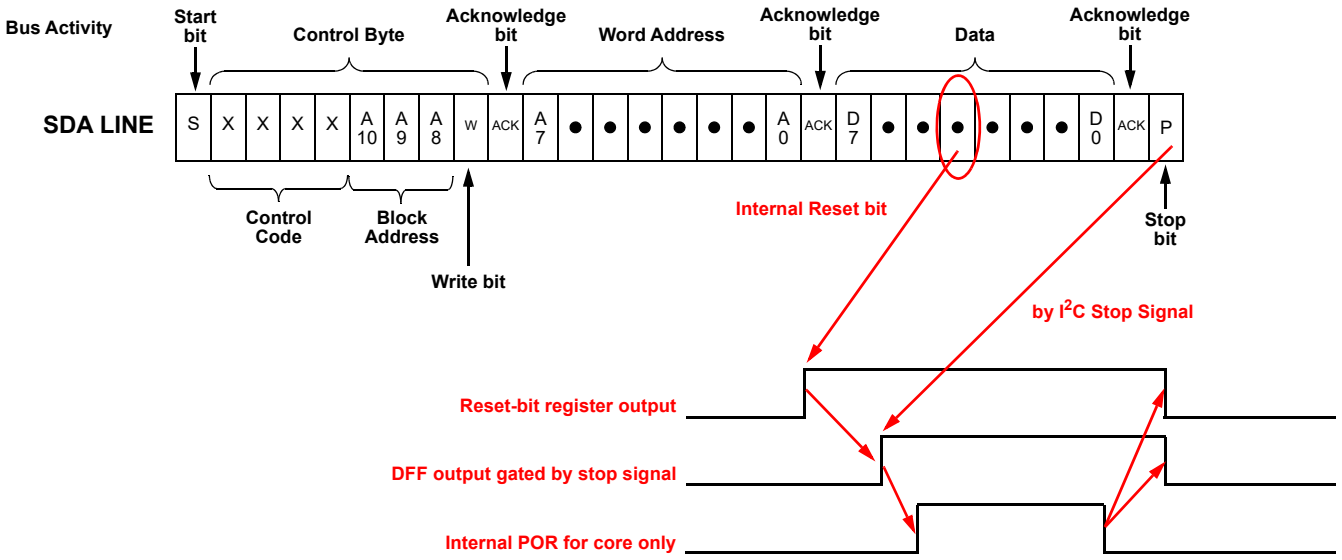


Figure 66: Reset Command Timing

15.5.2 I²C Additional Options

When Output latching during I²C write to the register configuration data (block address A10A9A8 = 000), reg<1602> = 1 allows all PINs output value to be latched while register content is changing. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.

See Section 17 for detailed information on all registers.

15.5.3 Reading Counter Data via I²C

The current count value in three counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

15.5.4 I²C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46824 chip has four pins which can be used as an I²C Expander. These four pins are IO0, IO5, IO6, and IO9.

Each of these pins can be used as an I²C Expander output or used as a normal pin. Also each of these four expander outputs have initial state settings which are specified in reg <1599:1592>.

15.5.5 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46824 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I²C Byte Write Mask Register (address 0C9H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to "1" in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 67 shows an example of this function.

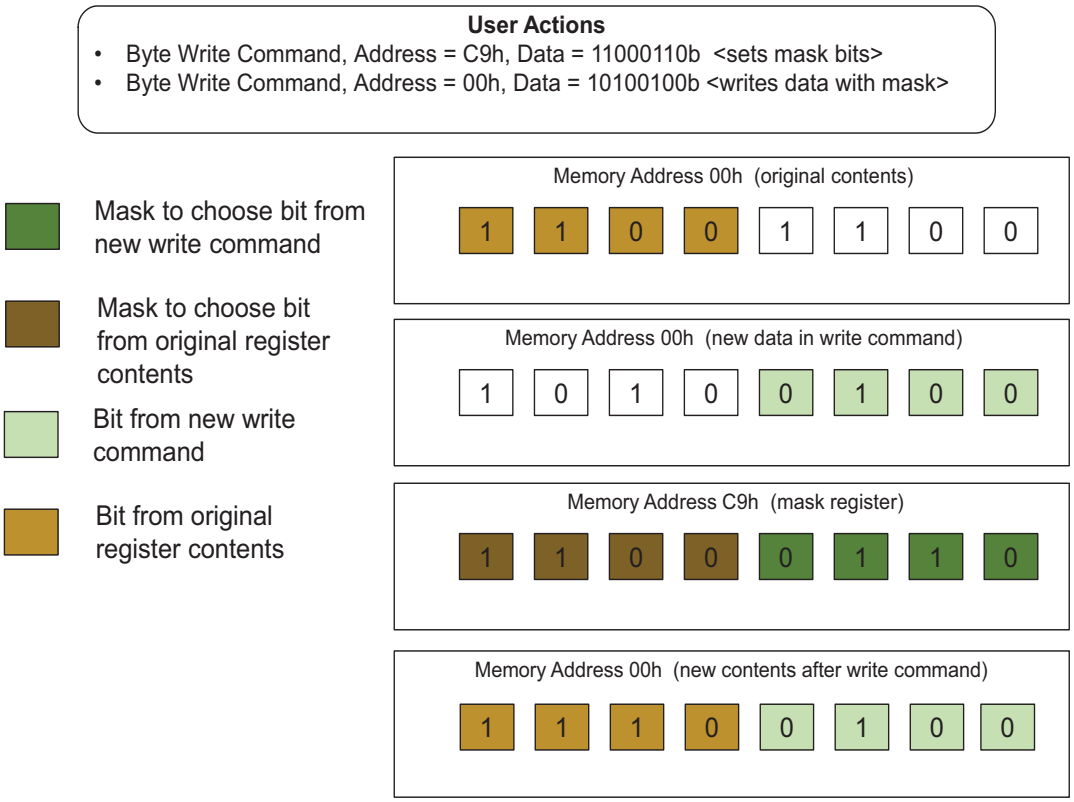


Figure 67: Example of I²C Byte Write Bit Masking

16 NVM with a Software Write Protection 2-Kbit

The SLG46824 provides 2,048 bits of Serial Electrically Erasable Memory internally organized as 16 pages of 16 bytes. The protection settings of the device can be made permanent if desired.

16.1 SERIAL NVM WRITE OPERATIONS

Write access to the NVM is possible by setting A3 A2 A1 A0 to “0000”, which allows serial write data for a single page only. Upon receipt of the proper Device Address and Word Address bytes, the SLG46824 will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG46824 will respond with an ACK after each data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition after all page data is written. At that time the GPAK will enter an internally self-timed write cycle, which will be completed within t_{WR} (20 ms). While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic and I^2C access to the Register data will be operational/valid. Please refer to Figure 69 for the SLG46824 Memory Map.

Note 11: The 16 programmed bytes should be in the same page.

Data “1” cannot be re-programmed as data “0” without erasure. Each byte can only be programmed one time without erasure.

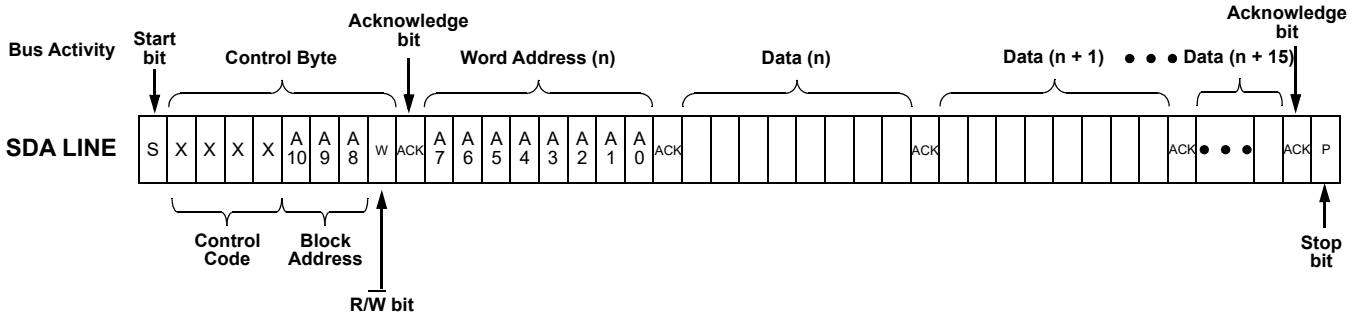


Figure 68: Page Write Command

A10 will be ignored during communication to SLG46824.

A9 = 1 will enable access to the NVM.

A9 = 1 and A8 = 0 corresponds to the 2K bits chip configuration NVM data.

A9 = 1 and A8 = 1A3, A2, A1, and A0 should be 0000 for the page write operation.

In a single page, if the content of only one byte needs to be programmed, the content of the other 15 bytes should be set to 0x00 except for the byte with custom content.

	I²C Block Address			Memory Space
Lowest I²C Address = 000h	A10 = 0	A9 = 0	A8 = 0	**2 Kbits Register Data Configuration**
	A10 = 0	A9 = 0	A8 = 1	**Not Used**
	A10 = 0	A9 = 1	A8 = 0	**2 Kbits NVM Data Configuration**
	A10 = 0	A9 = 1	A8 = 1	**Reserved**
Highest I²C Address = 7FFh	A10 = 1	A9 = X	A8 = X	**Not Used**

Figure 69: Memory Map

16.2 SERIAL NVM READ OPERATIONS

There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Please refer to the Section 15 for more details.

16.3 SERIAL NVM ERASE OPERATIONS

The erase scheme allows a portion or the 2K bits NVM chip configuration to be erased by modifying the contents of the Erase Register (ERSR). Changing the state of the ERSR is accomplished with a Byte Write sequence with the requirements outlined in this section.

The ERSR register is located on E3H address.

The ERSR format is shown in Table 52, and the ERSR bit functions are included in Table 53.

Table 52: Erase Register Bit format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE	--	--	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 53: Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE	Erase Enable	W	Setting b7 bit to “1” will cause the page erase.
6	--	--	--	--
5	--	--	--	--
4	ERSEB4	Page Selection for Erase	W	
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Register Address, the SLG46824 will send an ACK. The device will then be ready to receive Erase Register data. The SLG46824 will respond with an ACK after Erase Register data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition. At that time the GPAK will enter an internally self-timed erase cycle, which will be completed within t_{ER} (max 20 ms). While the data is being written into the Memory Array, all inputs, outputs, internal logic and I^2C access to the Register data will be operational/valid.

After the erase has taken place, the contents of ERSE bits will be set to “0” automatically. Erase will be triggered by Stop Bit in I^2C command.

17 Register Definitions

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Matrix Output					
00	reg<5:0>	Matrix OUT0	IN0 of LUT2_0 or Clock Input of DFF0		
00 01	reg<11:6>	Matrix OUT1	IN1 of LUT2_0 or Data Input of DFF0		
01 02	reg<17:12>	Matrix OUT2	IN0 of LUT2_3 or Clock Input of PGEN		
02	reg<23:18>	Matrix OUT3	IN1 of LUT2_3 or nRST of PGEN		
03	reg<29:24>	Matrix OUT4	IN0 of LUT2_1 or Clock Input of DFF1		
03 04	reg<35:30>	Matrix OUT5	IN1 of LUT2_1 or Data Input of DFF1		
04 05	reg<41:36>	Matrix OUT6	IN0 of LUT2_2 or Clock Input of DFF2		
05	reg<47:42>	Matrix OUT7	IN1 of LUT2_2 or Data Input of DFF2		
06	reg<53:48>	Matrix OUT8	IN0 of LUT3_0 or Clock Input of DFF3		
06 07	reg<59:54>	Matrix OUT9	IN1 of LUT3_0 or Data Input of DFF3		
07	reg<65:60>	Matrix OUT10	IN2 of LUT3_0 or nRST(nSET) of DFF3		
08	reg<71:66>	Matrix OUT11	IN0 of LUT3_1 or Clock Input of DFF4		
09	reg<77:72>	Matrix OUT12	IN1 of LUT3_1 or Data Input of DFF4		
09 0A	reg<83:78>	Matrix OUT13	IN2 of LUT3_1 or nRST(nSET) of DFF4		
0A 0B	reg<89:84>	Matrix OUT14	IN0 of LUT3_2 or Clock Input of DFF5		
0B	reg<95:90>	Matrix OUT15	IN1 of LUT3_2 or Data Input of DFF5		
0C	reg<101:96>	Matrix OUT16	IN2 of LUT3_2 or nRST(nSET) of DFF5		
0C 0D	reg<107:102>	Matrix OUT17	IN0 of LUT3_3 or Clock Input of DFF6		
0D 0E	reg<113:108>	Matrix OUT18	IN1 of LUT3_3 or Data Input of DFF6		
0E	reg<119:114>	Matrix OUT19	IN2 of LUT3_3 or nRST(nSET) of DFF6		
0F	reg<125:120>	Matrix OUT20	IN0 of LUT3_4 or Clock Input of DFF7		
0F 10	reg<131:126>	Matrix OUT21	IN1 of LUT3_4 or Data Input of DFF7		
10 11	reg<137:132>	Matrix OUT22	IN2 of LUT3_4 or nRST(nSET) of DFF7		
11	reg<143:138>	Matrix OUT23	IN0 of LUT3_5 or Clock Input of DFF8		
12	reg<149:144>	Matrix OUT24	IN1 of LUT3_5 or Data Input of DFF8		
12 13	reg<155:150>	Matrix OUT25	IN2 of LUT3_5 or nRST(nSET) of DFF8		
13 14	reg<161:156>	Matrix OUT26	IN0 of LUT3_6 or Input of Pipe Delay or UP Signal of RIPP CNT		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
14	reg<167:162>	Matrix OUT27	IN1 of LUT3_6 or nRST of Pipe Delay or STB of RIPP CNT		
15	reg<173:168>	Matrix OUT28	IN2 of LUT3_6 or Clock of Pipe Delay_RIPP_CNT		
15	reg<179:174>	Matrix OUT29	Reserved		
16					
16	reg<185:180>	Matrix OUT30	MULTFUNC_16BIT_0: IN0 of LUT4_0 or Clock Input of DFF9; Delay0 Input (or Counter0 RST/SET Input)		
17					
17	reg<191:186>	Matrix OUT31	MULTFUNC_16BIT_0: IN1 of LUT4_0 or nRST of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source		
18	reg<197:192>	Matrix OUT32	MULTFUNC_16BIT_0: IN2 of LUT4_0 or nSET of DFF9; Delay0 Input (or Counter0 nRST Input) or Delay/Counter0 External Clock Source or KEEP Input of FSM0		
18	reg<203:198>	Matrix OUT33	MULTFUNC_16BIT_0: IN3 of LUT4_0 or Data Input of DFF9; Delay0 Input (or Counter0 nRST Input) or UP Input of FSM0		
19					
19	reg<209:204>	Matrix OUT34	MULTFUNC_8BIT_1: IN0 of LUT3_7 or Clock Input of DFF10; Delay1 Input (or Counter1 nRST Input)		
1A					
1A	reg<215:210>	Matrix OUT35	MULTFUNC_8BIT_1: IN1 of LUT3_7 or nRST (nSET) of DFF10; Delay1 Input (or Counter1 nRST Input) or Delay/Counter1 External Clock Source		
1B	reg<221:216>	Matrix OUT36	MULTFUNC_8BIT_1: IN2 of LUT3_7 or Data Input of DFF10; Delay1 Input (or Counter1 nRST Input)		
1B	reg<227:222>	Matrix OUT37	MULTFUNC_8BIT_2: IN0 of LUT3_8 or Clock Input of DFF11; Delay2 Input (or Counter2 nRST Input)		
1C					
1C	reg<233:228>	Matrix OUT38	MULTFUNC_8BIT_2: IN1 of LUT3_8 or nRST (nSET) of DFF11; Delay2 Input (or Counter2 nRST Input) or Delay/Counter2 External Clock Source		
1D					
1D	reg<239:234>	Matrix OUT39	MULTFUNC_8BIT_2: IN2 of LUT3_8 or Data Input of DFF11; Delay2 Input (or Counter2 nRST Input)		
1E	reg<245:240>	Matrix OUT40	MULTFUNC_8BIT_3: IN0 of LUT3_9 or Clock Input of DFF12; Delay3 Input (or Counter3 nRST Input)		
1E	reg<251:246>	Matrix OUT41	MULTFUNC_8BIT_3: IN1 of LUT3_9 or nRST (nSET) of DFF12; Delay3 Input (or Counter3 nRST Input) or Delay/Counter3 External Clock Source		
1F					
1F	reg<257:252>	Matrix OUT42	MULTFUNC_8BIT_3: IN2 of LUT3_9 or Data Input of DFF12; Delay3 Input (or Counter3 nRST Input)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
1F 20	reg<263:258>	Matrix OUT43	MULTFUNC_8BIT_4: IN0 of LUT3_10 or Clock Input of DFF13; Delay4 Input (or Counter4 nRST Input)		
21	reg<269:264>	Matrix OUT44	MULTFUNC_8BIT_4: IN1 of LUT3_10 or nRST (nSET) of DFF13; Delay4 Input (or Counter4 nRST Input) or Delay/Counter4 External Clock Source		
21 22	reg<275:270>	Matrix OUT45	MULTFUNC_8BIT_4: IN2 of LUT3_10 or Data Input of DFF13; Delay4 Input (or Counter4 nRST Input)		
22 23	reg<281:276>	Matrix OUT46	MULTFUNC_8BIT_5: IN0 of LUT3_11 or Clock Input of DFF14; Delay5 Input (or Counter5 nRST Input)		
23	reg<287:282>	Matrix OUT47	MULTFUNC_8BIT_5: IN1 of LUT3_11 or nRST (nSET) of DFF14; Delay5 Input (or Counter5 nRST Input) or Delay/Counter5 External Clock Source		
24	reg<293:288>	Matrix OUT48	MULTFUNC_8BIT_5: IN2 of LUT3_11 or Data Input of DFF14; Delay5 Input (or Counter5 nRST Input)		
24 25	reg<299:294>	Matrix OUT49	MULTFUNC_8BIT_6: IN0 of LUT3_12 or Clock Input of DFF15; Delay6 Input (or Counter6 nRST Input)		
25 26	reg<305:300>	Matrix OUT50	MULTFUNC_8BIT_6: IN1 of LUT3_12 or nRST (nSET) of DFF15; Delay6 Input (or Counter6 nRST Input) or Delay/Counter6 External Clock Source		
26	reg<311:306>	Matrix OUT51	MULTFUNC_8BIT_6: IN2 of LUT3_12 or Data Input of DFF15; Delay6 Input (or Counter6 nRST Input)		
27	reg<317:312>	Matrix OUT52	MULTFUNC_8BIT_7: IN0 of LUT3_13 or Clock Input of DFF16; Delay7 Input (or Counter7 nRST Input)		
27 28	reg<323:318>	Matrix OUT53	MULTFUNC_8BIT_7: IN1 of LUT3_13 or nRST (nSET) of DFF16; Delay7 Input (or Counter7 nRST Input) or Delay/Counter7 External Clock Source		
28 29	reg<329:324>	Matrix OUT54	MULTFUNC_8BIT_7: IN2 of LUT3_13 or Data Input of DFF16; Delay7 Input (or Counter7 nRST Input)		
29	reg<335:330>	Matrix OUT55	Filter/Edge detect input		
2A	reg<341:336>	Matrix OUT56	Programmable delay/edge detect input		
2A 2B	reg<347:342>	Matrix OUT57	OSC2 ENABLE from matrix		
2B 2C	reg<353:348>	Matrix OUT58	OSC0 ENABLE from matrix		
2C	reg<359:354>	Matrix OUT59	OSC1 ENABLE from matrix		
2D	reg<365:360>	Matrix OUT60	Reserved		
2D 2E	reg<371:366>	Matrix OUT61	BG power down from matrix		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
2E 2F	reg<377:372>	Matrix OUT62	Reserved		
2F	reg<383:378>	Matrix OUT63	Reserved		
30	reg<389:384>	Matrix OUT64	pd of ACMP0L from matrix		
30 31	reg<395:390>	Matrix OUT65	pd of ACMP1L from matrix		
31 32	reg<401:396>	Matrix OUT66	Reserved		
32	reg<407:402>	Matrix OUT67	IO0 Digital Output		
33	reg<413:408>	Matrix OUT68	IO1 Digital Output		
33 34	reg<419:414>	Matrix OUT69	IO1 Digital Output OE		
34 35	reg<425:420>	Matrix OUT70	IO2 Digital Output		
35	reg<431:426>	Matrix OUT71	IO3 Digital Output		
36	reg<437:432>	Matrix OUT72	IO4 Digital Output		
36 37	reg<443:438>	Matrix OUT73	IO4 Digital Output OE		
37 38	reg<449:444>	Matrix OUT74	IO5 Digital Output		
38	reg<455:450>	Matrix OUT75	IO5 Digital Output OE		
39	reg<461:456>	Matrix OUT76	IO6 Digital Output		
39 3A	reg<467:462>	Matrix OUT77	IO7 Digital Output		
3A 3B	reg<473:468>	Matrix OUT78	IO8 Digital Output		
3B	reg<479:474>	Matrix OUT79	IO8 Digital Output OE		
3C	reg<485:480>	Matrix OUT80	IO9 Digital Output		
3C 3D	reg<491:486>	Matrix OUT81	IO9 Digital Output OE		
3D 3E	reg<497:492>	Matrix OUT82	IO10 Digital Output		
3E	reg<503:498>	Matrix OUT83	IO10 Digital Output OE		
3F	reg<509:504>	Matrix OUT84	IO11 Digital Output		
3F 40	reg<515:510>	Matrix OUT85	IO11 Digital Output OE		
40 41	reg<521:516>	Matrix OUT86	IO12 Digital Output		
41	reg<527:522>	Matrix OUT87	IO12 Digital Output OE		
42	reg<533:528>	Matrix OUT88	IO13 Digital Output		
42 43	reg<539:534>	Matrix OUT89	IO13 Digital Output OE		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
43 44	reg<545:540>	Matrix OUT90	IO14 Digital Output		
44	reg<551:546>	Matrix OUT91	IO14 Digital Output OE		
45	reg<557:552>	Matrix OUT92	Reserved		
45 46	reg<563:558>	Matrix OUT93	Reserved		
46 47	reg<569:564>	Matrix OUT94	Reserved		
47	reg<575:570>	Matrix OUT95	Reserved		
48	reg<583:576>	Reserved			
49	reg<591:584>				
4A	reg<599:592>	Reserved			
4B	reg<607:600>				
4C	reg<615:608>	Reserved			
4D	reg<623:616>				
4E	reg<631:624>	Reserved			
4F	reg<639:632>				
50	reg<647:640>	Reserved			
51	reg<655:648>				
52	reg<663:656>	Reserved			
53	reg<671:664>				
54	reg<679:672>	Reserved			
55	reg<687:680>				
56	reg<695:688>	Reserved			
57	reg<703:696>				
58	reg<711:704>				
59	reg<719:712>	Reserved			
5A	reg<727:720>				
5B	reg<735:728>	Reserved			
5C	reg<743:736>				
5D	reg<751:744>	Reserved			
5E	reg<759:752>				
5F	reg<767:760>	Reserved			
IO Common					
60	reg<768>	IO fast pull up/down enable	0: disable 1: enable		
	reg<769>	I2C mode selection	0: I2C standard/fast mode 1: I2C fast mode+		
	reg<775:770>	Reserved			
IO0					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
61	reg<777:776>	IO0 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<779:778>	IO0 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<781:780>	IO0 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<782>	IO0 pull up/down selection	0: pull down 1: pull up		
	reg<783>	IO0 output enable	0: disable 1: enable		
IO1					
62	reg<785:784>	IO1 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog input		
	reg<787:786>	IO1 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<789:788>	IO1 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<790>	IO1 pull up/down selection	0: pull down 1: pull up		
	reg<791>	Reserved			
Reserved					
63	reg<793:792>	Reserved			
	reg<795:794>	Reserved			
	reg<797:796>	Reserved			
	reg<798>	Reserved			
	reg<799>	Reserved			
IO2					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
64	reg<801:800>	IO2 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<803:802>	IO2 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<805:804>	IO2 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<806>	IO2 pull up/down selection	0: pull down 1: pull up		
	reg<807>	IO2 output enable	0: disable 1: enable		
IO3					
65	reg<809:808>	IO3 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<811:810>	IO3 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<813:812>	IO3 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
65	reg<814>	IO3 pull up/down selection	0: pull down 1: pull up		
	reg<815>	IO3 output enable	0: disable 1: enable		
IO4					
66	reg<817:816>	IO4 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<819:818>	IO4 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<821:820>	IO4 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<822>	IO4 pull up/down selection	0: pull down 1: pull up		
	reg<823>	Reserved			
IO5					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
67	reg<825:824>	IO5 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<827:826>	IO5 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<829:828>	IO5 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<830>	IO5 pull up/down selection	0: pull down 1: pull up		
	reg<831>	Reserved			
SCL					
68	reg<832>	Reserved			
	reg<834:833>	SCL input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: Reserved		
	reg<836:835>	SCL pull up/down resistance selection	00: floating 01: Reserved 10: Reserved 11: Reserved		
	reg<837>	Reserved			
	reg<839:838>	Reserved			
SDA					
69	reg<840>	Reserved			
	reg<842:841>	SDA input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: Reserved		
	reg<844:843>	SDA pull up/down resistance selection	00: floating 01: Reserved 10: Reserved 11: Reserved		
	reg<845>	Reserved			
	reg<847:846>	Reserved			
IO6					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
6A	reg<849:848>	Reserved			
	reg<851:850>	IO6 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<853:852>	IO6 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<854>	IO6 pull up/down selection	0: pull down 1: pull up		
	reg<855>	IO6 output enable	0: disable 1: enable		
IO7					
6B	reg<857:856>	Reserved			
	reg<859:858>	IO7 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<861:860>	IO7 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<862>	IO7 pull up/down selection	0: pull down 1: pull up		
	reg<863>	IO7 output enable	0: disable 1: enable		
IO8					
6C	reg<865:864>	IO8 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: reserved		
	reg<867:866>	IO8 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<869:868>	IO8 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<870>	IO8 pull up/down selection	0: pull down 1: pull up		
	reg<871>	Reserved			
Reserved					
6D	reg<873:872>	Reserved			
	reg<875:874>	Reserved			
	reg<877:876>	Reserved			
	reg<878>	Reserved			
	reg<879>	Reserved			
IO9					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
6E	reg<881:880>	IO9 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog output		
	reg<883:882>	IO9 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<885:884>	IO9 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<886>	IO9 pull up/down selection	0: pull down 1: pull up		
	reg<887>	Reserved			
IO10					
6F	reg<889:888>	IO10 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog output		
	reg<891:890>	IO10 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<893:892>	IO10 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<894>	IO10 pull up/down selection	0: pull down 1: pull up		
	reg<895>	Reserved			
IO11					
70	reg<897:896>	IO11 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog input		
	reg<899:898>	IO11 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<901:900>	IO11 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<902>	IO11 pull up/down selection	0: pull down 1: pull up		
	reg<903>	Reserved			
IO12					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
71	reg<905:904>	IO12 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog input		
	reg<907:906>	IO12 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<909:908>	IO12 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<910>	IO12 pull up/down selection	0: pull down 1: pull up		
	reg<911>	Reserved			
IO13					
72	reg<913:912>	IO13 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog IO		
	reg<915:914>	IO13 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<917:916>	IO13 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<918>	IO13 pull up/down selection	0: pull down 1: pull up		
	reg<919>	Reserved			
IO14					
73	reg<921:920>	IO14 input mode configuration	00: digital in without schmitt trigger 01: digital in with schmitt trigger 10: low voltage digital in mode 11: analog input		
	reg<923:922>	IO14 output mode configuration	00: 1x push-pull 01: 2x push-pull 10: 1x open-drain 11: 2x open-drain		
	reg<925:924>	IO14 pull up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M		
	reg<926>	IO14 pull up/down selection	0: pull down 1: pull up		
	reg<927>	Reserved			
Matrix Input					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
74	reg<928>	Matrix Input 0	Tie low		
	reg<929>	Matrix Input 1	IO0 Digital Input		
	reg<930>	Matrix Input 2	IO1 Digital Input		
	reg<931>	Matrix Input 3	IO2 Digital Input		
	reg<932>	Matrix Input 4	IO3 Digital Input		
	reg<933>	Matrix Input 5	IO4 Digital Input		
	reg<934>	Matrix Input 6	IO5 Digital Input		
	reg<935>	Matrix Input 7	IO8 Digital Input		
75	reg<936>	Matrix Input 8	IO9 Digital Input		
	reg<937>	Matrix Input 9	IO10 Digital Input		
	reg<938>	Matrix Input 10	IO11 Digital Input		
	reg<939>	Matrix Input 11	IO12 Digital Input		
	reg<940>	Matrix Input 12	IO13 Digital Input		
	reg<941>	Matrix Input 13	IO14 Digital Input		
	reg<942>	Matrix Input 14	LUT2_0_DFF0_OUT		
	reg<943>	Matrix Input 15	LUT2_1_DFF1_OUT		
76	reg<944>	Matrix Input 16	LUT2_2_DFF2_OUT		
	reg<945>	Matrix Input 17	LUT2_3_PGEN_OUT		
	reg<946>	Matrix Input 18	LUT3_0_DFF3_OUT		
	reg<947>	Matrix Input 19	LUT3_1_DFF4_OUT		
	reg<948>	Matrix Input 20	LUT3_2_DFF5_OUT		
	reg<949>	Matrix Input 21	LUT3_3_DFF6_OUT		
	reg<950>	Matrix Input 22	LUT3_4_DFF7_OUT		
	reg<951>	Matrix Input 23	LUT3_5_DFF8_OUT		
77	reg<952>	Matrix Input 24	LUT3_6_PIPEDLY_RIPP_CNT_OUT0		
	reg<953>	Matrix Input 25	PIPEDLY_RIPP_CNT_OUT1		
	reg<954>	Matrix Input 26	RIPP_CNT_OUT2		
	reg<955>	Matrix Input 27	EDET_FILTER_OUT		
	reg<956>	Matrix Input 28	PROG_DLY_EDET_OUT		
	reg<957>	Matrix Input 29	MULTFUNC_8BIT_1: DLY_CNT_OUT		
	reg<958>	Matrix Input 30	CKRCOSC_MATRIX: OSC1 matrix input		
	reg<959>	Matrix Input 31	CKLFOSC_MATRIX: OSC0 matrix input		
78	reg<960>	Matrix Input 32	CKRINGOSC_MATRIX: OSC2 matrix input		
	reg<961>	Matrix Input 33	MULTFUNC_8BIT_2: DLY_CNT_OUT		
	reg<962>	Matrix Input 34	MULTFUNC_8BIT_3: DLY_CNT_OUT		
	reg<963>	Matrix Input 35	MULTFUNC_8BIT_4: DLY_CNT_OUT		
	reg<964>	Matrix Input 36	MULTFUNC_8BIT_5: DLY_CNT_OUT		
	reg<965>	Matrix Input 37	MULTFUNC_8BIT_6: DLY_CNT_OUT		
	reg<966>	Matrix Input 38	MULTFUNC_8BIT_7: DLY_CNT_OUT		
	reg<967>	Matrix Input 39	MULTFUNC_16BIT_0: LUT_DFF_OUT		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
79	reg<968>	Matrix Input 40	MULTFUNC_8BIT_1: LUT_DFF_OUT		
	reg<969>	Matrix Input 41	MULTFUNC_8BIT_2: LUT_DFF_OUT		
	reg<970>	Matrix Input 42	MULTFUNC_8BIT_3: LUT_DFF_OUT		
	reg<971>	Matrix Input 43	MULTFUNC_8BIT_4: LUT_DFF_OUT		
	reg<972>	Matrix Input 44	MULTFUNC_8BIT_5: LUT_DFF_OUT		
	reg<973>	Matrix Input 45	MULTFUNC_8BIT_6: LUT_DFF_OUT		
	reg<974>	Matrix Input 46	MULTFUNC_8BIT_7: LUT_DFF_OUT		
	reg<975>	Matrix Input 47	MULTFUNC_16BIT_0: DLY_CNT_OUT		
7A	reg<976>	Matrix Input 48	Virtual Input <7>: reg<976>		
	reg<977>	Matrix Input 49	Virtual Input <6>: reg<977>		
	reg<978>	Matrix Input 50	Virtual Input <5>: reg<978>		
	reg<979>	Matrix Input 51	Virtual Input <4>: reg<979>		
	reg<980>	Matrix Input 52	Virtual Input <3>: reg<980>		
	reg<981>	Matrix Input 53	Virtual Input <2>: reg<981>		
	reg<982>	Matrix Input 54	Virtual Input <1>: reg<982>		
	reg<983>	Matrix Input 55	Virtual Input <0>: reg<983>		
7B	reg<984>	Matrix Input 56	Reserved		
	reg<985>	Matrix Input 57	Reserved		
	reg<986>	Matrix Input 58	ACMP0L OUT		
	reg<987>	Matrix Input 59	ACMP1L OUT		
	reg<988>	Matrix Input 60	2nd CKRCOSC_MATRIX		
	reg<989>	Matrix Input 61	2nd CKLFOSC_MATRIX		
	reg<990>	Matrix Input 62	POR CORE		
	reg<991>	Matrix Input 63	Tie high		
7C	reg<999:992>	CNT0(16-bit) Counted Value	Q<7:0>		
7D	reg<1007:1000>	CNT0(16-bit) Counted Value	Q<15:8>		
7E	reg<1015:1008>	CNT2(8-bit) Counted Value	Q<7:0>		
7F	reg<1023:1016>	CNT4(8-bit) Counted Value	Q<7:0>		
OSC/ACMP					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
80	reg<1024>	OSC1 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on		
	reg<1025>	matrix power down or on select	0: matrix down 1: matrix on		
	reg<1026>	external clock source enable	0: internal OSC1 1: external clock from IO10		
	reg<1028:1027>	post divider ration control	00: div1 01: div2 10: div4 11: div8		
	reg<1031:1029>	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64		
81	reg<1032>	OSC2 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on		
	reg<1033>	matrix power down or on select	0: matrix down 1: matrix on		
	reg<1034>	external clock source enable	0: internal OSC2 1: external clock from IO8		
	reg<1036:1035>	post divider ration control	00: div1 01: div2 10: div4 11: div8		
	reg<1039:1037>	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
82	reg<1040>	OSC0 turn on by register	when matrix output enable/pd control signal=0: 0: auto on by delay cells 1: always on		
	reg<1041>	matrix power down or on select	0: matrix down 1: matrix on		
	reg<1042>	external clock source enable	0: internal OSC0 1: external clock from IO0		
	reg<1044:1043>	post divider ration control	00: div1 01: div2 10: div4 11: div8		
	reg<1047:1045>	matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64		
83	reg<1048>	Reserved			
	reg<1049>	OSC0 matrix out enable	0: disable 1: enable		
	reg<1050>	OSC1 matrix out enable	0: disable 1: enable		
	reg<1051>	OSC2 matrix out enable	0: disable 1: enable		
	reg<1052>	OSC2 100 ns Startup Delay	0: enable 1: disable		
	reg<1053>	OSC0 2nd matrix out enable	0: disable 1: enable		
	reg<1054>	OSC1 2nd matrix out enable	0: disable 1: enable		
	reg<1055>	Reserved			
84	reg<1058:1056>	OSC1 2nd matrix input: matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64		
	reg<1061:1059>	OSC0 2nd matrix input: matrix divider ratio control	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64		
	reg<1063:1062>	Reserved			

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
85	reg<1065:1064>	Reserved			
	reg<1066>	Reserved			
	reg<1067>	Reserved			
	reg<1068>	Reserved			
	reg<1069>	Reserved			
	reg<1070>	Reserved			
	reg<1071>	Reserved			
86	reg<1072>	Reserved			
	reg<1073>	Reserved			
	reg<1075:1074>	Reserved			
	reg<1076>	Reserved			
	reg<1077>	Reserved			
	reg<1078>	Reserved			
	reg<1079>	Reserved n			
87	reg<1080>	Reserved			
	reg<1081>	Reserved			
	reg<1083:1082>	ACMP0L hysteresis	00: 0mV 01: 32mV 10: 64mV 11: 196mV		
	reg<1084>	Reserved			
	reg<1085>	Reserved			
	reg<1086>	Reserved			
	reg<1087>	Reserved			
88	reg<1089:1088>	ACMP1L hysteresis	00: 0mV 01: 32mV 10: 64mV 11: 196mV		
	reg<1090>	Reserved			
	reg<1091>	Reserved			
	reg<1092>	ACMP1L positive input come from ACMP0L's input mux output enable	0: disable 1: enable		
	reg<1093>	Reserved			
	reg<1094>	Reserved			
	reg<1095>	Reserved			
89	reg<1097:1096>	Reserved			
	reg<1103:1098>	Reserved			
8A	reg<1105:1104>	Reserved			
	reg<1111:1106>	Reserved			

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
8B	reg<1113:1112>	ACMP0L Gain divider	00: 1X 01: 0.5X 10: 0.33X 11: 0.25X		
	reg<1119:1114>	ACMP0L VREF	ACMP VREF select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External VREF		
8C	reg<1121:1120>	ACMP1L Gain divider	00: 1X 01: 0.5X 10: 0.33X 11: 0.25X		
	reg<1127:1122>	ACMP1L VREF	ACMP VREF select: 000000: 32mV ~ 111110: 2.016V/ step=32mV; 111111: External VREF		
8D	reg<1128>	Reserved	0: disable 1: enable		
	reg<1130:1129>	Reserved			
	reg<1131>	VREF1 output OP	0: disable 1: enable		
	reg<1133:1132>	VREF0 input selection	00: None 01: ACMP0L vref 10: ACMP1L vref 11: Reserved		
	reg<1134>	Reserved			
	reg<1135>	Reserved			
8E	reg<1136>	Reserved			
	reg<1137>	Reserved			
	reg<1138>	Reserved			
	reg<1139>	VREF_OUT1 PD	0: VREF_OUT1 disable 1: VREF_OUT1 enable		
	reg<1140>	VREF_OUT1 PD selection	0: enable/disable using VREF_OUT1 PD reg<1139> 1: enable/disable using matrix out<60>		
	reg<1143:1141>	Reserved			
8F	reg<1145:1144>	Reserved			
	reg<1151:1146>	Reserved			
Digital Macrocell					

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
90	reg<1155:1152>	LUT2_0/DFF0 setting	<3>: LUT2_0<3> / DFF0 or Latch Select 0: DFF function 1: Latch function <2>: LUT2_0<2> / DFF0 Output Sel 0: Q output 1: QB output <1>: LUT2_0<1> / DFF0 Initial Polarity Select 0: Low 1: High <0>: LUT2_0<0>		
	reg<1159:1156>	LUT2_1/DFF1 setting	<3>: LUT2_1<3> / DFF1 or Latch Select 0: DFF function 1: Latch function <2>: LUT2_1<2> / DFF1 Output Select 0: Q output 1: QB output <1>: LUT2_1<1> / DFF1 Initial Polarity Select 0: Low 1: High <0>: LUT2_1<0>		
91	reg<1163:1160>	LUT2_2/DFF2 setting	<3>: LUT2_2<3> / DFF2 or Latch Select 0: DFF function 1: Latch function <2>: LUT2_2<2> / DFF2 Output Select 0: Q output 1: QB output <1>: LUT2_2<1> / DFF2 Initial Polarity Select 0: Low 1: High <0>: LUT2_2<0>		
	reg<1167:1164>	LUT2_3_VAL or PGEN_data	LUT2_3<3:0> or PGEN 4bit counter data<3:0>		
92	reg<1175:1168>	PGEN data [7:0]	PGEN data [7:0]		
93	reg<1183:1176>	PGEN data [15:8]	PGEN data [15:8]		
94	reg<1191:1184>	LUT3_0_DFF3 setting	<7>: LUT3_0<7> / DFF3 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_0<6> / DFF3 Output Select 0: Q output 1: QB output <5>: LUT3_0<5> / DFF3 0: nRST from Matrix Output 1: nSET from Matrix Output <4>: LUT3_0<4> / DFF3 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_0<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
95	reg<1199:1192>	LUT3_1_DFF4 setting	<7>: LUT3_1<7> / DFF4 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_1<6> / DFF4 Output Select 0: Q output 1: QB output <5>: LUT3_1<5> / DFF4 0: nRST from Matrix Output 1: nSET from Matrix Output <4>: LUT3_1<4> / DFF4 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_1<3:0>		
96	reg<1207:1200>	LUT3_2_DFF5 setting	<7>: LUT3_2<7> / DFF5 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_2<6> / DFF5 Output Select 0: Q output 1: QB output <5>: LUT3_2<5> / DFF5 0: nRST from Matrix Output 1: nSET from Matrix Output <4>: LUT3_2<4> / DFF5 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_2<3:0>		
97	reg<1215:1208>	LUT3_3_DFF6 setting	<7>: LUT3_3<7> / DFF6 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_3<6> / DFF6 Output Select 0: Q output 1: QB output <5>: LUT3_3<5> / DFF6 0: nRST from Matrix Output 1: nSET from Matrix Output <4>: LUT3_3<4> / DFF6 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_3<3:0>		
98	reg<1223:1216>	LUT3_4_DFF7 setting	<7>: LUT3_4<7> / DFF7 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_4<6> / DFF7 Output Select 0: Q output 1: QB output <5>: LUT3_4<5> / DFF7 0: nRST from Matrix Output 1: nSET from Matrix Output <4>: LUT3_4<4> / DFF7 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_4<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
99	reg<1231:1224>	LUT3_5_DFF8 setting	<7>: LUT3_5<7> / DFF8 or Latch Select 0: DFF function 1: Latch function <6>: LUT3_5<6> / DFF8 Output Select 0: Q output 1: QB output <5>: LUT3_5<5> / DFF8 0: RSTB from Matrix Output 1: SETB from Matrix Output <4>: LUT3_5<4> / DFF8 Initial Polarity Select 0: Low 1: High <3:0>: LUT3_5<3:0>		
9A	reg<1232>	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0		
	reg<1233>	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1		
	reg<1234>	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2		
	reg<1235>	LUT2_3 or PGEN Select	0: LUT2_3 1: PGEN		
	reg<1236>	LUT3_0 or DFF3 Select	0: LUT3_0 1: DFF3		
	reg<1237>	DFF3_SECONDQ_Sel	0: Q of first DFF 1: Q of second DFF		
	reg<1238>	LUT3_1 or DFF4 Select	0: LUT3_1 1: DFF4		
	reg<1239>	LUT3_2 or DFF5 Select	0: LUT3_2 1: DFF5		
9B	reg<1240>	LUT3_3 or DFF6 Select	0: LUT3_3 1: DFF6		
	reg<1241>	LUT3_4 or DFF7 Select	0: LUT3_4 1: DFF7		
	reg<1242>	LUT3_5 or DFF8 Select	0: LUT3_5 1: DFF8		
	reg<1243>	Filter or Edge Detector selection	0: filter 1: edge det		
	reg<1244>	output Polarity Select	0: Filter/edge detect output 1: Filter/edge detect output inverted		
	reg<1246:1245>	Select the edge mode	00: Rising Edge Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge DLY		
	reg<1247>	Reserved			

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
9C	reg<1255:1248>	LUT value or pipe delay out sel or nSET/ END value	<7:4>:LUT3_6<7:4>/REG_S1<3:0>pipe delay out1 sel <3:0>:LUT3_6<3:0>/REG_S0<3:0>pipe delay out0 sel at RIPP CNT mode: bit<1250:1248> is the nSET value bit<1253:1251> is the END value bit<1254> functional mode:0: full cycle; 1: ranged cycle bit<1255> not used		
9D	reg<1256>	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted		
	reg<1257>	LUT3_6 or Pipe Delay Select	0: LUT3_6 1: Pipe Delay or RIPP CNT		
	reg<1258>	PIPE_RIPP_CNT_S	0: Pipe delay mode selection 1: Ripple Counter mode selection		
	reg<1260:1259>	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay		
	reg<1262:1261>	Delay Value Select for Programmable Delay & Edge Detector	00: 125ns 01: 250ns 10: 375ns 11: 500ns		
	reg<1263>	Reserved			
9E	reg<1264>	IO14 external reset mode selection	0: edge active 1: high active		
	reg<1265>	IO14 external reset edge mode selection (with reg<1264>=0	0: rising edge 1: falling edge		
	reg<1266>	External reset from IO14	0: disable 1: enable		
9F	reg<1271:1267>	Reserved			
	reg<1276:1272>	Reserved			
	reg<1277>	Reserved			
	reg<1278>	Reserved			
	reg<1279>	Reserved			
Multifunction					
A0	reg <1286> reg< 1285> reg < 1282> reg < 1284> reg < 1283> reg< 1281> reg< 1280>	Single 4-bit LUT	0000000: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	0010000: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_IN - LOW)		
		Single CNT/DLY	0000001: Matrix A - UP (CNT); Matrix B - KEEP (CNT); Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (CNT) (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	0000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A0	reg <1286> reg< 1285> reg < 1282> reg < 1284> reg < 1283> reg< 1281> reg< 1280>	CNT/DLY -> DFF	0000110: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	0100010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3; In2 - LOW)		
		CNT/DLY -> DFF	0100110: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D; nSET - HIGH)		
		CNT/DLY -> LUT	1000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In3; In1 - LOW)		
		CNT/DLY -> DFF	1000110: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to D; nRST - HIGH)		
		CNT/DLY -> LUT	0001010: Matrix A - In3; Matrix B - DLY_IN; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	0001110: Matrix A - D; Matrix B - DLY_IN; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to nSET)		
		CNT/DLY -> LUT	1001010: Matrix A - In3; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In2; In1 - LOW)		
		CNT/DLY -> DFF	1001110: Matrix A - D; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to nSET; nRST - HIGH)		
		CNT/DLY -> LUT	0010010: Matrix A - In3; Matrix B - In2; Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	0010110: Matrix A - D; Matrix B - nSET; Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST)		
		CNT/DLY -> LUT	0110010: Matrix A - In3; Matrix B - EXT_-CLK (CNT); Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1; In2 - LOW)		
		CNT/DLY -> DFF	0110110: Matrix A - D; Matrix B - EXT_-CLK (CNT); Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST; nSET - HIGH)		
		CNT/DLY -> LUT	0011010: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A0	reg <1286> reg< 1285> reg < 1282> reg < 1284> reg < 1283> reg< 1281> reg< 1280>	CNT/DLY -> DFF	0011110: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK)		
		CNT/DLY -> LUT	0111010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0; In2 - LOW)		
		CNT/DLY -> DFF	0111110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK; nSET - HIGH)		
		CNT/DLY -> LUT	1011010: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to In0; In1 - LOW)		
		CNT/DLY -> DFF	1011110: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to CLK; nRST - HIGH)		
		LUT -> CNT/DLY	0000011: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	0000111: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN)		
		LUT -> CNT/DLY	0100011: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN; In2 - LOW)		
		DFF -> CNT/DLY	0100111: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN; nSET - HIGH)		
		LUT -> CNT/DLY	1000011: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (LUT_OUT connected to DLY_IN; In1 - LOW)		
		DFF -> CNT/DLY	1000111: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DFF_OUT connected to DLY_IN; nRST - HIGH)		
	reg<1287>	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data		
A1	reg<1295:1288>	LUT4_0_DFF9 setting <7:0>	<7:0>: LUT4_0<7:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A2	reg<1303:1296>	LUT4_0_DFF9 setting <15:8>	<15>: LUT4_0<15>/DFF or Latch Select 0: DFF function; 1: Latch function <14>: LUT4_0<14>/DFF Output Select 0: Q output; 1: QB output <13>: LUT4_0<13>/DFF Initial Polarity Select 0: Low; 1: High <12:8>: LUT4_0<12:8>		
A3	reg<1305:1304>	DLY/CNT0 Mode Selection	00: DLY 01: one shot 10: frequency det 11: CNT		
	reg<1307:1306>	DLY/CNT0 edge Mode Selection	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)		
	reg<1311:1308>	DLY/CNT0 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
A4	reg<1312>	CNT0 output pol selection	0: Default Output 1: Inverted Output		
	reg<1314:1313>	CNT0 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
	reg<1315>	Reserved			
	reg<1316>	Reserved			
	reg<1317>	Keep signal sync selection	0: bypass 1: after two DFF		
	reg<1318>	UP signal sync selection	0: bypass 1: after two DFF		
	reg<1319>	CNT0 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
A5	reg<1327:1320>	REG_CNT0_Data<7:0>	Data<7:0>		
A6	reg<1335:1328>	REG_CNT0_Data<15:8>	Data<15:8>		
A7	reg<1336>	CNT0 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg <1339> reg< 1341> reg < 1340> reg < 1338> reg < 1337>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A7	reg <1339> reg< 1341> reg < 1340> reg < 1338> reg < 1337>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
	reg<1343:1342>	CNT1 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
A8	reg<1351:1344>	LUT3_7_DFF10 setting	<7>: LUT3_7<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_7<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_7<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_7<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_7<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A9	reg<1355:1352>	DLY/CNT1 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1359:1356>	CNT1 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq dectect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
AA	reg<1367:1360>	REG_CNT1_Data<7:0>	Data<7:0>		
AB	reg<1368>	CNT1 output pol selection	0: Default Output 1: Inverted Output		
	reg<1369>	Reserved			
	reg<1370>	CNT1 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1371>	CNT1 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1394>, reg<1375:1372>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
AB	reg<1394>, reg<1375:1372>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
AC	reg<1383:1376>	LUT3_8_DFF_11 setting	<7>: LUT3_8<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_8<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_8<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_8<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_8<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
AD	reg<1387:1384>	DLY/CNT2 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1391:1388>	CNT2 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
AE	reg<1393:1392>	CNT2 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
	reg<1395>	CNT2 output pol selection	0: Default Output 1: Inverted Output		
	reg<1396>	Reserved			
	reg<1397>	CNT2 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1398>	CNT2 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1399>	Reserved			
AF	reg<1407:1400>	REG_CNT2_Data<7:0>	Data<7:0>		
B0	reg<1408>	Reserved			
	reg <1411> reg< 1413> reg < 1412> reg < 1410> reg < 1409>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	00100: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B0	reg <1411> reg< 1413> reg < 1412> reg < 1410> reg < 1409>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
	reg<1415:1414>	CNT3 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
B1	reg<1423:1416>	LUT3_9_DFF12 setting	<7>: LUT3_9<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_9<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_9<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_9<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_9<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B2	reg<1427:1424>	DLY/CNT3 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1431:1428>	CNT3 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
B3	reg<1439:1432>	REG_CNT3_Data<7:0>	Data<7:0>		
B4	reg<1440>	CNT3 output pol selection	0: Default Output 1: Inverted Output		
	reg<1441>	Reserved			
	reg<1442>	CNT3 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1443>	CNT3 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1466>, reg<1447:1444>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B4	reg<1466>, reg<1447:1444>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
B5	reg<1455:1448>	LUT3_DFF setting	<7>: LUT3<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B6	reg<1459:1456>	DLY/CNT4 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1463:1460>	CNT4 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
B7	reg<1465:1464>	CNT4 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
	reg<1467>	CNT4 output pol selection	0: Default Output 1: Inverted Output		
	reg<1468>	Reserved			
	reg<1469>	CNT4 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1470>	CNT4 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1471>	Reserved			
B8	reg<1479:1472>	REG_CNT4_Data<7:0>	Data<7:0>		
B9	reg<1480>	Reserved			
	reg <1483> reg< 1485> reg < 1484> reg < 1482> reg < 1481>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	00100: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B9	reg <1483> reg< 1485> reg < 1484> reg < 1482> reg < 1481>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	00110: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	01110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	10010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	00111: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
	reg<1487:1486>	CNT5 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
BA	reg<1495:1488>	LUT3_11_DFF14 setting	<7>: LUT3_11<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_11<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_11<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_11<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_11<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
BB	reg<1499:1496>	DLY/CNT5 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1503:1500>	CNT5 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
BC	reg<1511:1504>	REG_CNT5_Data<7:0>	Data<7:0>		
BD	reg<1512>	CNT5 output pol selection	0: Default Output 1: Inverted Output		
	reg<1513>	Reserved			
	reg<1514>	CNT5 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1515>	CNT5 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1538>, reg<1519:1516>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
BD	reg<1538>, reg<1519:1516>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
BE	reg<1527:1520>	LUT3_12_DFF15 setting	<7>: LUT3_12<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_12<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_12<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_12<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_12<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
BF	reg<1531:1528>	DLY/CNT6 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1535:1532>	CNT6 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
C0	reg<1537:1536>	CNT6 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
	reg<1539>	CNT6 output pol selection	0: Default Output 1: Inverted Output		
	reg<1540>	Reserved			
	reg<1541>	CNT6 CNT mode SYNC selection	0: bypass 1: after two DFF		
	reg<1542>	CNT6 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1543>	REG_TEST_EN			
C1	reg<1551:1544>	REG_CNT6_Data<7:0>	Data<7:0>		
C2	reg<1556:1552>	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)		
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
C2	reg<1556:1552>	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)		
		CNT/DLY -> LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)		
		CNT/DLY -> DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)		
		CNT/DLY -> LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)		
		CNT/DLY -> DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)		
		CNT/DLY -> LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)		
		CNT/DLY -> DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)		
		LUT -> CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)		
		DFF -> CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)		
	reg<1557>	CNT7 output pol selection	0: Default Output 1: Inverted Output		
	reg<1558>	Reserved			
	reg<1559>	CNT7 CNT mode SYNC selection	0: bypass 1: after two DFF		
C3	reg<1567:1560>	LUT3_13_DFF16 setting	<7>: LUT3_13<7>/DFF or Latch Select 0: DFF function; 1: Latch function <6>: LUT3_13<6>/DFF Output Select 0: Q output; 1: QB output <5>: LUT3_13<5>/DFF 0: nRST from Matrix Output; 1: nSET from Matrix Output <4>: LUT3_13<4>/DFF Initial Polarity Select 0:Low; 1: High <3:0>: LUT3_13<3:0>		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
C4	reg<1571:1568>	DLY/CNT7 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT_END; 1110: External; 1111: No-used		
	reg<1575:1572>	CNT7 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay; 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT		
C5	reg<1577:1576>	CNT7 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1		
	reg<1578>	CNT7 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection		
	reg<1583:1579>	Reserved			
C6	reg<1591:1584>	REG_CNT7_Data<7:0>	Data<7:0>		
C7	reg<1592>	IO0 I²C output expander data			
	reg<1593>	IO0 I²C output expander select	0: IO0 output come from matrix 1: IO0 output is register		
	reg<1594>	IO5 I²C output expander data			
	reg<1595>	IO5 I²C output expander select	0: IO5 output come from matrix 1: IO5 output is register		
	reg<1596>	IO6 I²C output expander data			
	reg<1597>	IO6 I²C output expander select	0: IO6 output come from matrix 1: IO6 output is register		
	reg<1598>	IO9 I²C output expander data			
	reg<1599>	IO9 I²C output expander select	0: IO9 output come from matrix 1: IO9 output is register		
C8	reg<1600>	Reserved			
	reg<1601>	I²C reset bit with reloading NVM into Data register(soft reset)	0: Keep existing condition 1: Reset execution		
	reg<1602>	IO Latching Enable During I²C Write Interface	0: disable 1: enable		
	reg<1607:1603>	Reserved			
C9	reg<1615:1608>	I²C write mask bits	0: overwrite 1: mask		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
CA	reg<1619:1616>	I²C slave address			
	reg<1620>	Slave address selection A4	0: from reg 1: from IO5		
	reg<1621>	Slave address selection A5	0: from reg 1: from IO4		
	reg<1622>	Slave address selection A6	0: from reg 1: from IO3		
	reg<1623>	Slave address selection A7	0: from reg 1: from IO2		
CB	reg<1631:1624>	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]			
CC	reg<1639:1632>	Reserved			
Reserved					
CD	reg<1643:1640>	Reserved			
	reg<1647:1644>	Reserved			
CE	reg<1648>	Reserved			
	reg<1652:1649>	Reserved			
	reg<1653>	Reserved			
	reg<1654>	Reserved			
	reg<1655>	Reserved			
CF	reg<1657:1656>	Reserved			
	reg<1658>	Reserved			
	reg<1659>	Reserved			
	reg<1660>	Reserved			
	reg<1661>	Reserved			
	reg<1662>	Reserved			
	reg<1663>	Reserved			
D0	reg<1671: 1664>	Reserved			
D1	reg<1679: 1672>	Reserved			
D2	reg<1687: 1680>	Reserved			
D3	reg<1695: 1688>	Reserved			
D4	reg<1703: 1696>	Reserved			
D5	reg<1711: 1704>	Reserved			
D6	reg<1719: 1712>	Reserved			
D7	reg<1727: 1720>	Reserved			
D8	reg<1735: 1728>	Reserved			
D9	reg<1743: 1736>	Reserved			
DA	reg<1751: 1744>	Reserved			
DB	reg<1759: 1752>	Reserved			
DC	reg<1767: 1760>	Reserved			
DD	reg<1775: 1768>	Reserved			
DE	reg<1783: 1776>	Reserved			
DF	reg<1791: 1784>	Reserved			

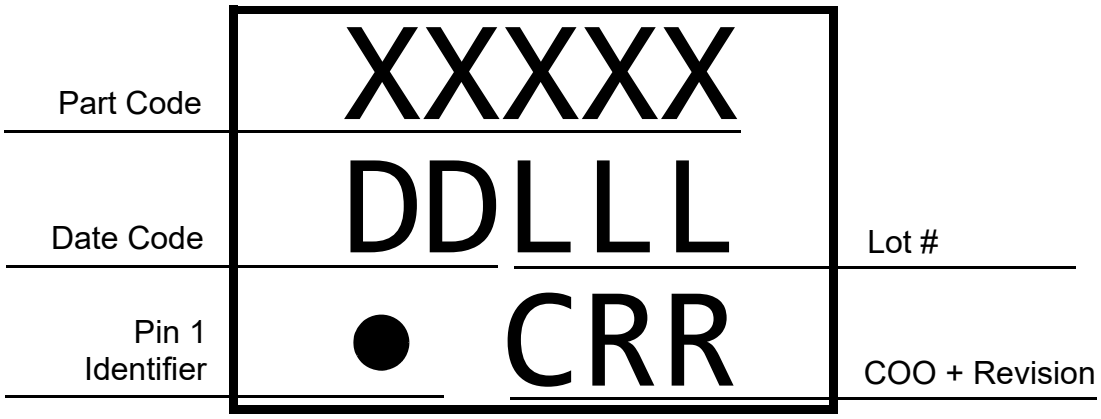
Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
E0 RPR	reg<1793:1792>	2k Register Read Selection Bits RPRB<1:0>	00: 2k register data is unprotected for read; 01: 2k register data is partly protected for read; 10: 2k register data is fully protected for read; 11: reserved		
	reg<1795:1794>	2k Register Write Selection Bits RPRB<3:2>	00: 2k register data is unprotected for write; 01: 2k register data is partly protected for write; 10: 2k register data is fully protected for write; 11: reserved		
	reg<1796>	Reserved			
	reg<1797>	Reserved			
	reg<1798>	Reserved			
	reg<1799>	Reserved			
E1 NPR	reg<1801:1800>	2k NVM Configuration Selection Bits NPRB<1:0>	00: 2k NVM Configuration data is unprotected for read and write/erase; 01: 2k NVM Configuration data is fully protected for read; 10: 2k NVM Configuration data is fully protected for write/erase; 11: 2k NVM Configuration data is fully protected for read and write/erase.		
	reg<1802>	Reserved			
	reg<1803>	Reserved			
	reg<1804>	Reserved			
	reg<1805>	Reserved			
	reg<1806>	Reserved			
	reg<1807>	Reserved			
E2 WPR	reg<1809:1808>	Reserved			
	reg<1810>	Write Protect Register Enable	0: No Software Write Protection enabled (default). 1: Write Protection is set by the state of the WPB[1:0] bits.		
	reg<1815:1811>	Reserved			
E3	reg<1820:1816>	Page Selection for Erase ERSEB<4:0>	Define the page address, which will be erase. ERSB4=0 corresponds to the Upper 2k NVM used for chip configuration.		
	reg<1821>	Reserved			
	reg<1822>	Reserved			
	reg<1823>	Erase Enable ERSE	Setting ERSE=1 will cause the NVM erase: full NVM (4k bits) erase for ERSCHIP=1 (reg<1973>) if DIS_ERSCHIP=0 (reg<1972>) or page erase for ERSCHIP=0 (reg<1973>).		

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
E4	reg<1824>	Protection Lock	0: RPR/WPR/NPR setting can be changed 1: RPR/WPR/NPR setting cannot be changed		
	reg<1831:1825>	Reserved			
E5	reg<1839: 1832>	Reserved			
E6	reg<1847: 1840>	Reserved			
E7	reg<1855: 1848>	Reserved			
E8	reg<1863: 1856>	Reserved			
E9	reg<1871: 1864>	Reserved			
EA	reg<1879: 1872>	Reserved			
EB	reg<1887: 1880>	Reserved			
EC	reg<1895: 1888>	Reserved			
ED	reg<1903: 1896>	Reserved			
EE	reg<1911: 1904>	Reserved			
EF	reg<1919: 1912>	Reserved			
F0	reg<1926:1920>	Reserved			
	reg<1927>	Reserved			
F1	reg<1932:1928>	Reserved			
	reg<1934:1933>				
	reg<1935>	Reserved			
F2	reg<1940:1936>	Reserved			
	reg<1943:1941>				
F3	reg<1949:1944>	Reserved			
	reg<1951:1950>				
F4	reg<1957:1952>	Reserved			
	reg<1959:1958>				
F5	reg<1965:1960>	Reserved			
	reg<1967:1966>				
F6	reg<1968>	Reserved			
	reg<1971:1969>	Reserved			
	reg<1972>	Reserved			
	reg<1973>	Reserved			
	reg<1974>	Reserved			
	reg<1975>	Reserved			
F7	reg<1983:1976>	Reserved			
F8	reg<1991:1984>	Reserved			
F9	reg<1992>	Reserved			
	reg<1993>	Reserved			
	reg<1995:1994>	Reserved			
	reg<1999:1996>	Reserved			

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
FA	reg<2000>	Reserved			
	reg<2001>	Reserved			
	reg<2002>	Reserved			
	reg<2006:2003>				
	reg<2007>	Reserved			
FB	reg<2015:2008>	Reserved			
FC	reg<2023:2016>	Reserved			
FD	reg<2031:2024>	Reserved			
FE	reg<2039:2032>	Reserved			
FF	reg<2047:2040>	Reserved			

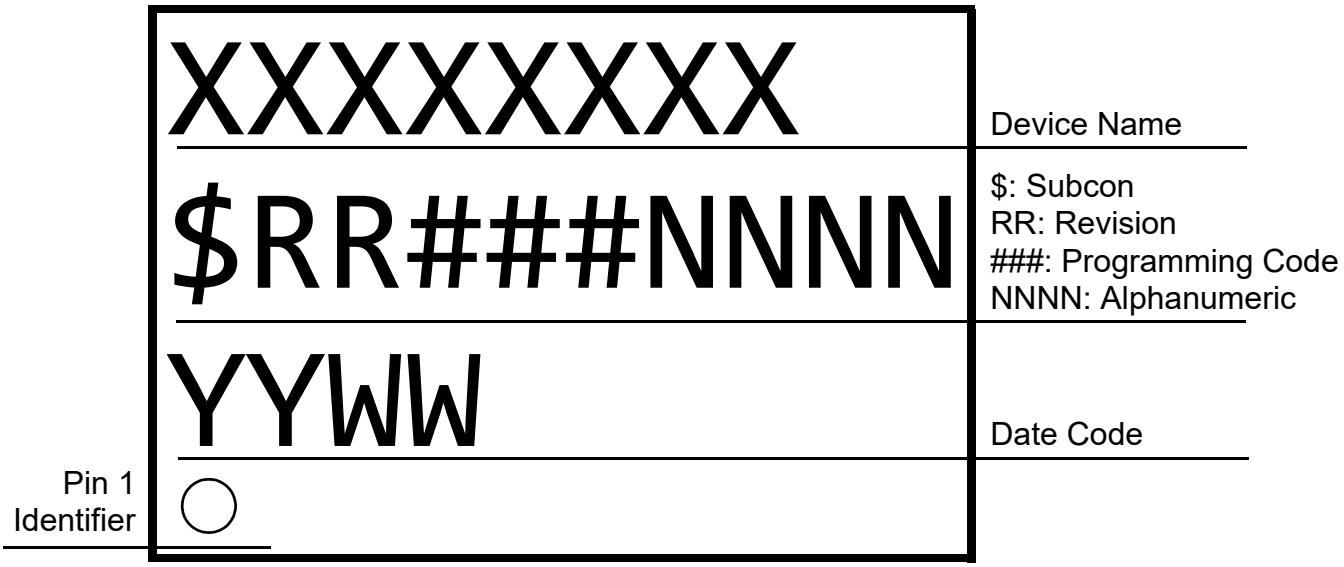
18 Package Top Marking System Definition

18.1 STQFN 20L 2X3MM 0.4P FCD PACKAGE



XXXXX - Part ID Field identifies the specific device configuration
DD - Date Code Field: Coded date of manufacture
LLL - Lot Code: Designates Lot #
C - Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR - Revision Code: Device Revision

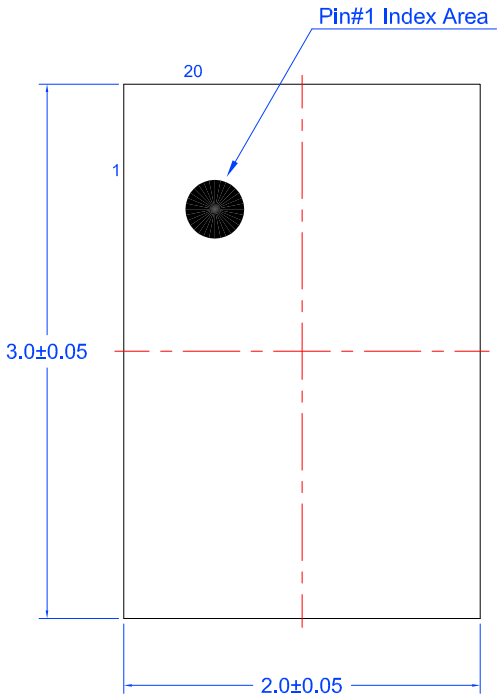
18.2 TSSOP-20



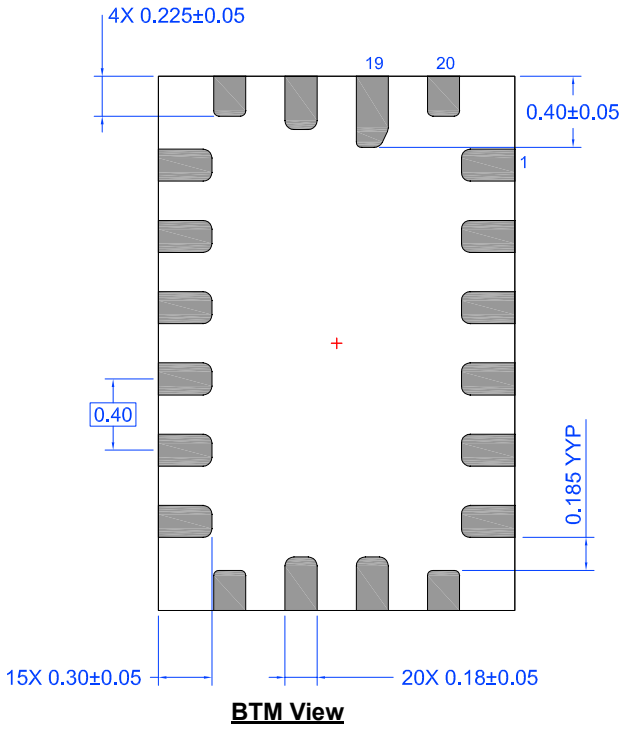
19 Package Information

19.1 PACKAGE OUTLINES FOR STQFN 20L 2X3MM 0.4P FCD

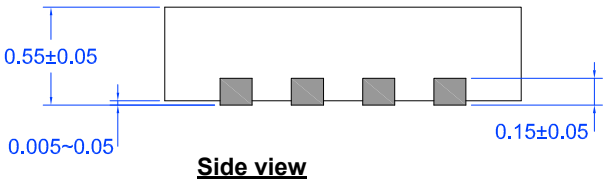
JEDEC MO-220, Variation WECE
IC Net Weight: TBD g



Marking View



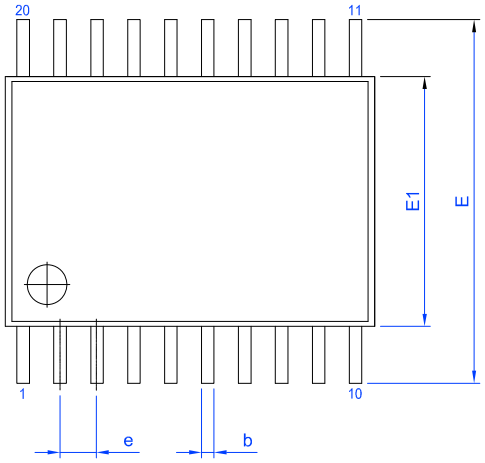
BTM View



Side view

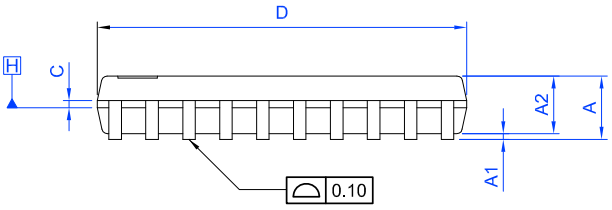
Unit: mm

19.2 PACKAGE OUTLINES FOR TSSOP 20L 173 MIL GREEN

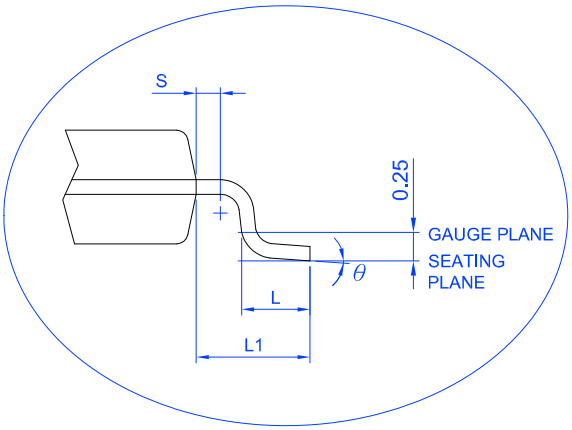


Marking View

Side View



Side view



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E1	4.30	4.40	4.50
A2	0.80	0.90	1.05	E	6.40 BSC		
b	0.19	-	0.30	L	0.50	0.60	0.75
C	0.09	-	0.20	L1	1.00 REF		
e	0.65 BSC			S	0.20	-	-
				Θ	0°	-	8°

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H

20 STQFN and TSSOP Handling

Manual handling of STQFN and TSSOP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of STQFN and TSSOP packages will cause damage to the solder balls. Therefore a removed sample cannot be reused.

STQFN and TSSOP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

21 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal) for STQFN 20L Package and package volume of 25.74 mm^3 (nominal) for TSSOP-20 Package. More information can be found at www.jedec.org.

22 Ordering Information

Part Number	Type
SLG46824V	20-pin STQFN
SLG46824VTR	20-pin STQFN - Tape and Reel (3k units)
SLG46824G	20-pin TSSOP
SLG46824GTR	20-pin TSSOP Tape and Reel (4k units)

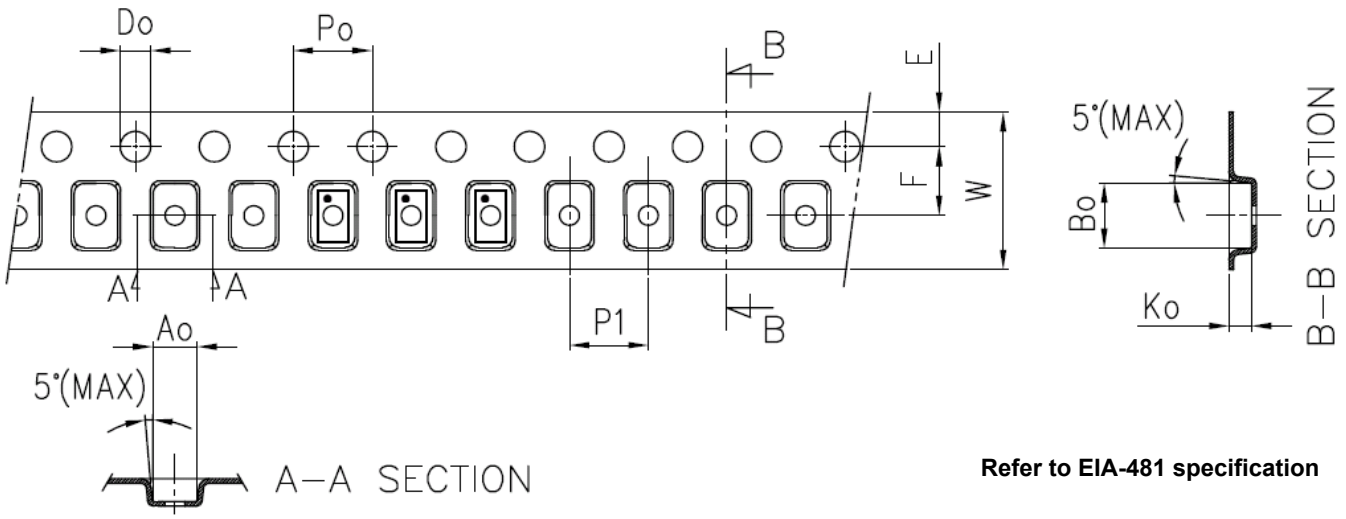
22.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P FCD	20	2 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4
TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4	4,000	4,000	330 / 100	42	336	42	336	16	8

22.2 CARRIER TAPE DRAWING AND DIMENSIONS

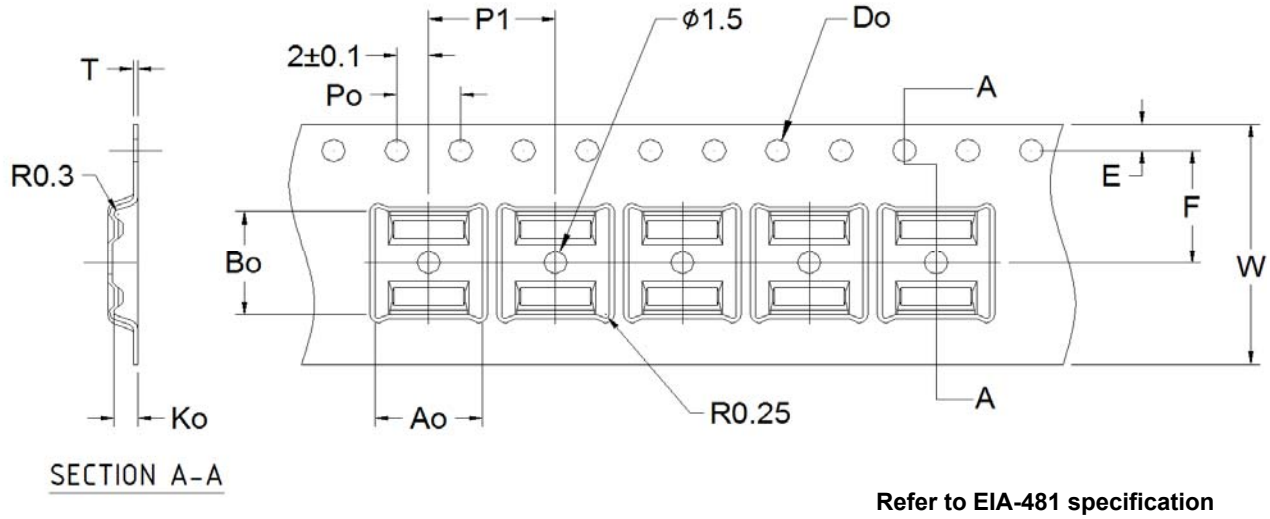
Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2 mm x3 mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8
TSSOP 20L 173 MIL Green Package	6.8	6.9	1.6	4	8	1.5	1.75	7.5	16

22.3 STQFN-20L



Refer to EIA-481 specification

22.4 TSSOP-20L



Refer to EIA-481 specification

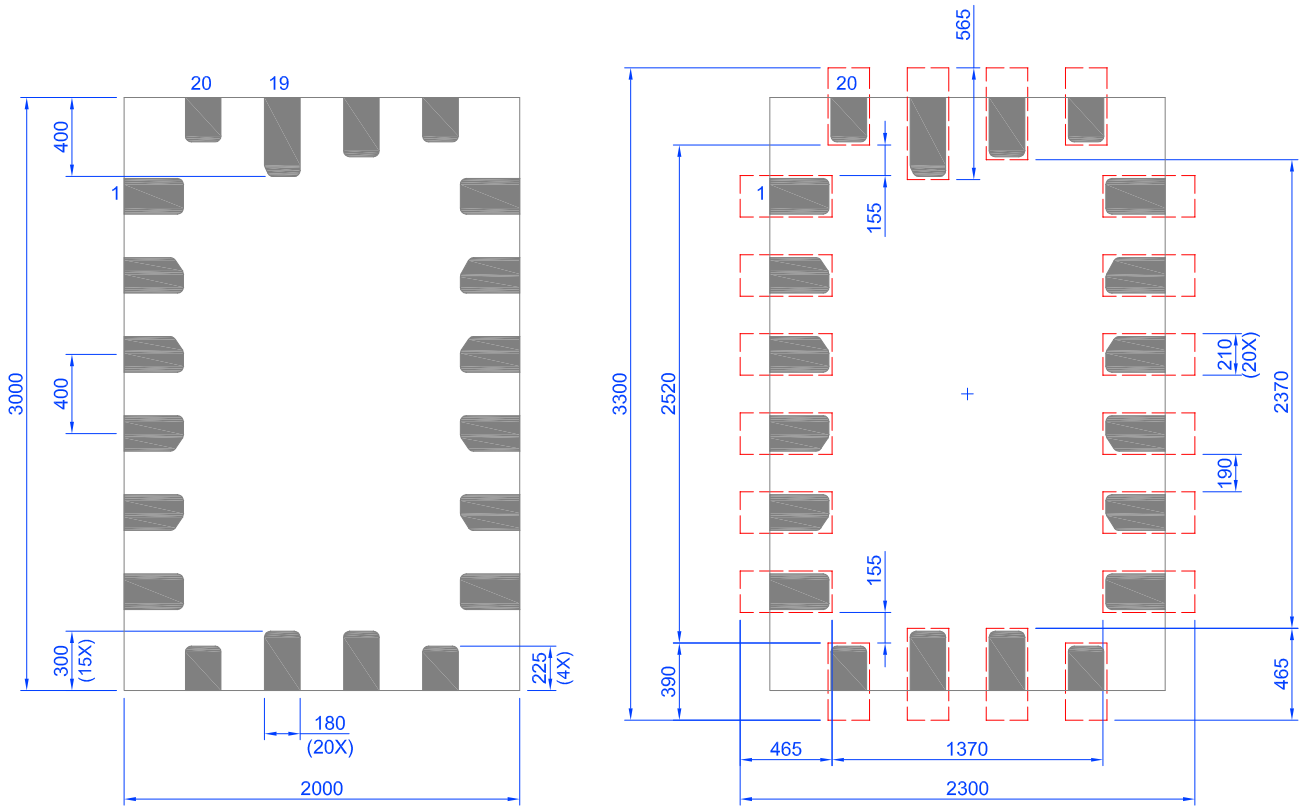
Note 12: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

23 Layout Guidelines

23.1 STQFN 20L 2X3MM 0.4P FCD PACKAGE

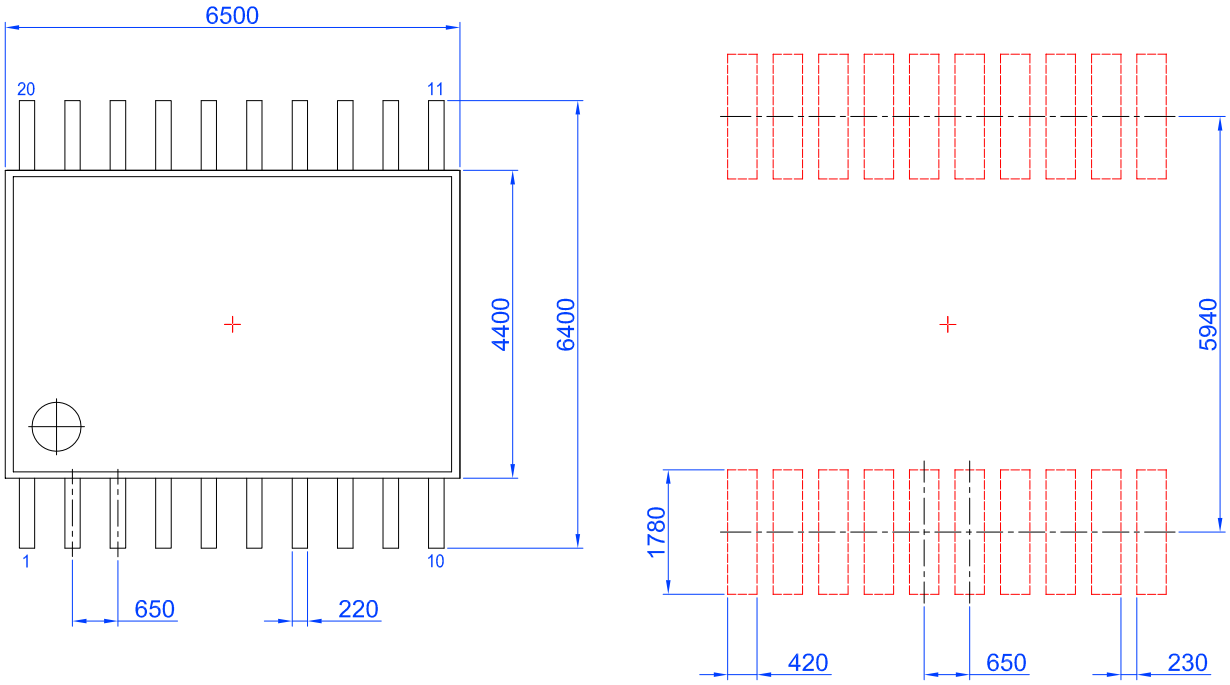
Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



Unit: µm

23.2 TSSOP-20



Unit: µm

Glossary

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
BG	Bandgap
CLK	Clock
CMO	Connection matrix output
CNT	Counter
DFF	D Flip Flop
DLY	Delay
ERSE	Erase Enable
ERSR	Erase Register
ESD	Electrostatic discharge
EV	End Value
FSM	Finite State Machine
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
IN	Input
IO	Input/Output
LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
LV	Low Voltage
MSB	Most Significant Bit
MTP	Multiple-Time-Programmable
MUX	Multiplexer
NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory
OD	Open Drain
OE	Output Enable
OSC	Oscillator
OUT	Output
PD	Power Down
PGEN	Pattern Generator
POR	Power-On Reset
PP	Push Pull

PRL	Protect Lock Bit
PWR	Power
P DLY	Programmable Delay
RPR	Register Read/Write Protection
RPRB	Register Read/Write Protection Bit
RPRL	Register Protection Read/Write/Erase Lock
REG	Register
R/W	Read/Write
SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value
TS	Temperature Sensor
VREF	Voltage Reference
WOSMT	Without Schmitt Trigger
WPB	Write Protect Bit
WPR	Write Protection Register
WPRE	Write Protect Enable
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
2.1	23-Jan-2018	Updated Electrical Spec Fixed typos Updated register definitions: reg<191:186> to reg<329:324>, reg<1066>, reg<1068>, reg<1073>, reg<1077>, reg<1084>, reg<1085>, reg<1090>, reg<1091>, reg<1079>, reg<1316>, reg<1983:1967>, reg<1991:1984>
2.0	29-Dec-2017	Preliminary version

Status Definitions

Version	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request

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