Application Note for an LLC Resonant Converter Using Resonant Controller HR1000

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ABSTRACT

This application note presents design guidelines for an LLC resonant converter using resonant controller HR1000 in applications such as the one shown in Figure 1. The first part introduces the HR1000's features. This section is followed by an introduction to the LLC resonant converter and a time-domain and frequency-domain analysis of its operating principle. The third section discusses a step-by-step design methodology for an LLC resonant converter using the HR1000. The last section discusses a methodology to verify a design, using a 90W adapter prototype as an example.

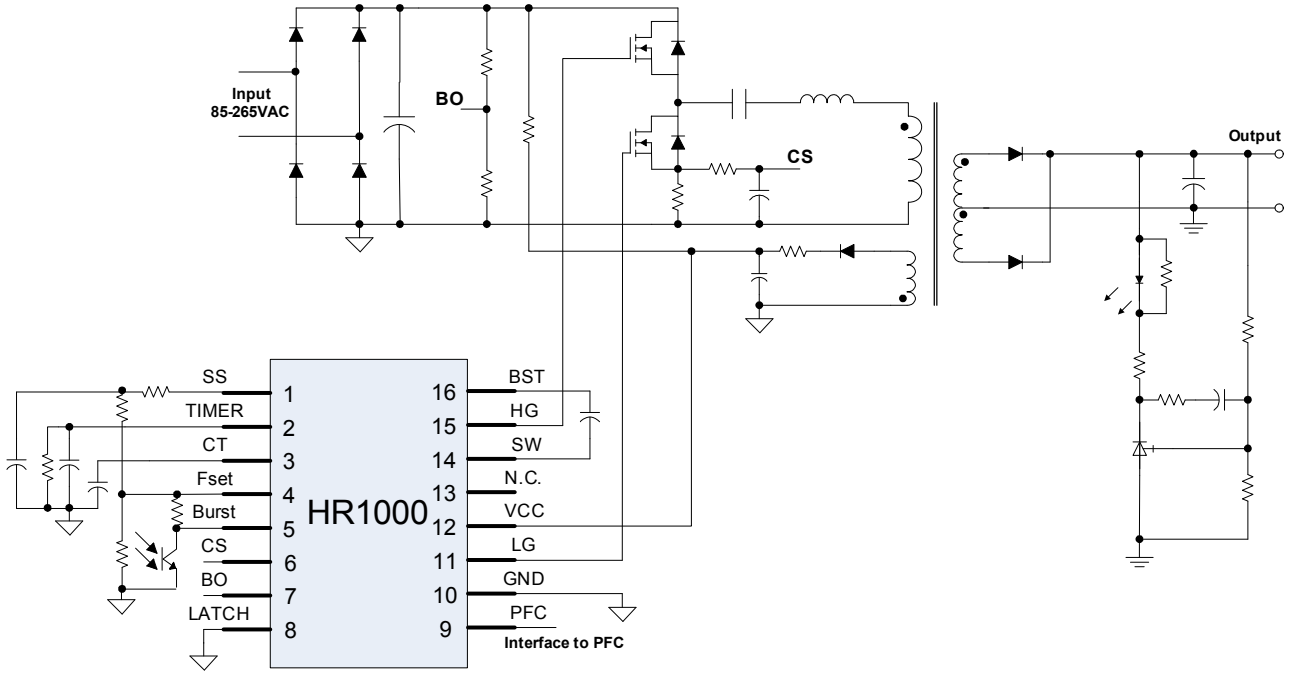

Figure 1: LLC Resonant Converter Using Resonant Controller—HR1000

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1. AN INTRODUCTION TO THE HR1000

The HR1000 is a controller designed specifically for the resonant half-bridge topology. It has two output channels of complementary driving signals that run at 50% duty cycle. An integrated bootstrap diode simplifies the external driving circuit for the high-side switch. A fixed dead-time inserted between the two complementary gate drivers guarantees soft-switching during the transient and enables high-frequency operation. Modulating the operating frequency regulates the output voltage. A programmable oscillator sets both the maximum and minimum switching frequency.

The IC initially works at the programmed maximum switching frequency that gradually falls until the control loop takes over in order to prevent the excessive inrush current. The IC can be forced to enter a controlled burst-mode operation at light-load to minimize the power consumption and tighten output regulation.

Protections features—such as latched shutdown or auto-recovery for over-current or over-voltage conditions or brown-outs—contribute to a safer converter design without increasing circuitry complexity.

This paper provides practical design guidelines for an LLC resonant converter using the HR1000, and includes step-by-step design guidelines that include a resonant parameters selection, transformer design, resonant inductor design and control parameters design.

2. AN INTRODUCTION TO THE LLC RESONANT CONVERTER

2.1 LLC Resonant Converter Introduction

Conventional PWM converters regulate the output voltage by adjusting the switching-cycle pulse width. The maximum duty cycle and main component parameter must be designed for the minimum input voltage condition so that the duty cycle gradually decreases as the input voltage increases. However, this causes the convert efficiency to drop substantially at normal input and at high line. The problem becomes serious when an application requires optimal converter efficiency at a high input voltage with a wide voltage range. By comparison, the LLC resonant converter can realize a wide input voltage range without sacrificing efficiency.

Another of the LLC resonant converter's merits is the capacity to achieve zero-voltage switching (ZVS) for primary side switches and zero-current switching (ZCS) for the secondary side rectifier. LLC converters do not suffer from reverse recovery issues and severe switching noise when compared against conventional converters, which generally have serious reverse recovery issues induced by hard switching. Soft-switching greatly reduces switching losses, allowing for LLC use in high-frequency applications. Operating at higher frequencies reduces the size of passive component, such as transformer and inductor, considerably and permits higher power densities.

Figure 1 shows the half-bridge LLC topology. The circuit can be divided into the following function blocks: the square-wave generator, the series resonant tank, the transformer, the output rectifier circuit, and the output filter. S1 and S2 implement the square wave generator, which commutates at a 50% duty cycle. The series resonant tank is composed of a series resonant inductor, L_r, a series resonant capacitor, C_r, and the L_m formed by the magnetizing inductance of transformer T1. The series resonant inductor can be an external component or the leakage inductance of T1. The rectifier circuit—which includes D1 and D2—converts the resonant current into a unidirectional current. The output filter, C_f, modulates the

high-frequency ripple current.

A conventional series resonant converter (SRC)—which features an infinite magnetizing inductor, L_m and can only work above the resonant frequency to achieve the ZVS condition: The SRC DC gain is always <1. However an LLC converter that substitutes L_m, with a shunt inductor can not only work above the $L_r \cdot C_r$ resonant frequency (f_s), but also below f_s and above the $C_r \cdot (L_r + L_m)$ resonant frequency (f_m).

The resonant frequency, f_s, is defined as:

$$f_s = \frac{1}{2\pi\sqrt{L_r \cdot C_r}} \quad (1)$$

The resonant frequency, f_m, is defined as:

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m) \cdot C_r}} \quad (2)$$

To reiterate, the LLC-SRC can operate not only in the range of $f>f_s$, but also in the range of $f_m<f<f_s$.

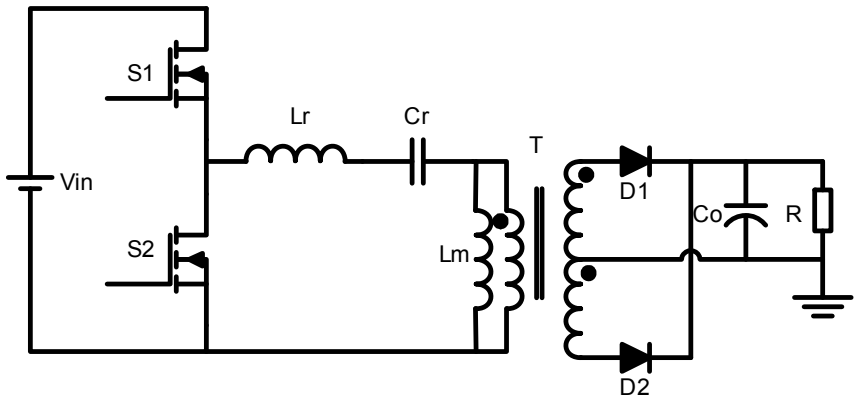
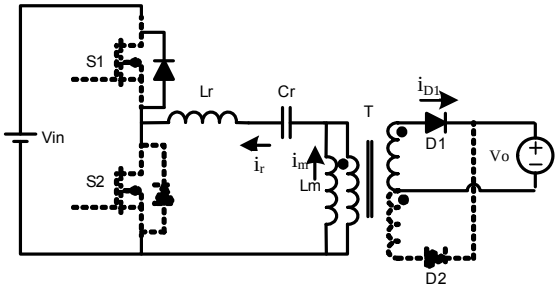
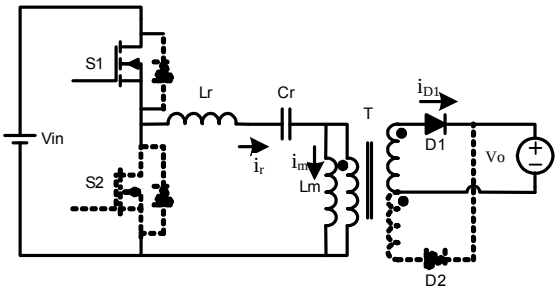


Figure 2: Half-Bridge LLC Converter

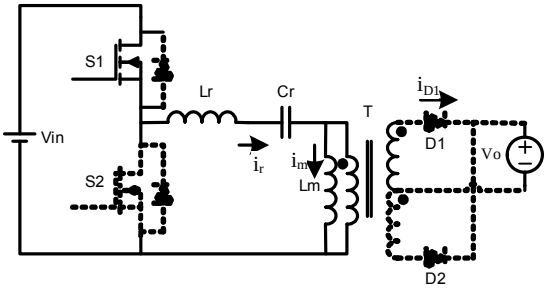
2.2 Key Operating Principle



(a) Stage 1 [t_0, t_1]



(b) Stage 2 [t_1, t_2]



(c) Stage 3 [t_2, t_3]

Figure 3: Equivalent main circuit at $f_m<f<f_s$

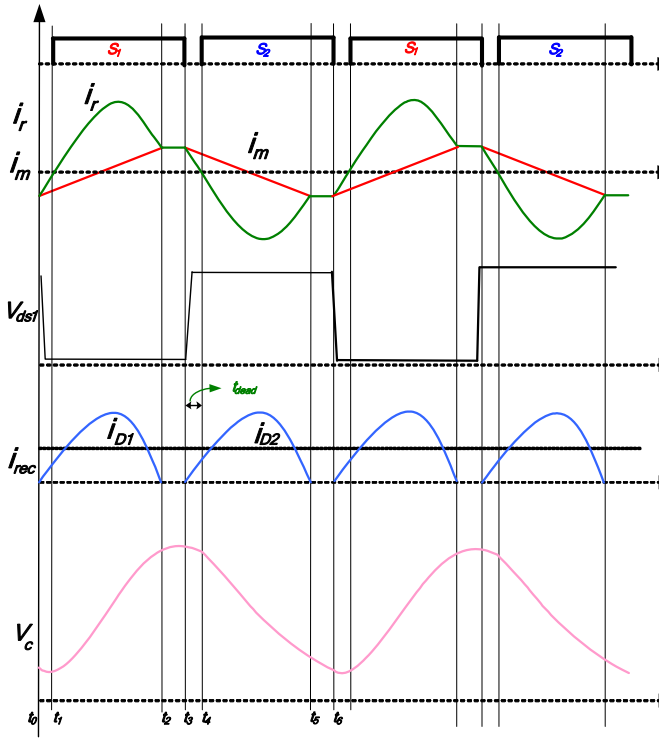


Figure 4: Operating waveform at $f_m<f_s<f_r$

A. Operating Waveform at $f_m<f_s<f_r$

The equivalent circuit and operating waveform are illustrated in Figure 3 and Figure 4, respectively. The switch turns off at time t_0 and the resonant current firstly discharges the parasitic capacitor and then flows through the body diode of S1. The output rectifier diode, D1, continues to deliver energy to the load. C_r and L_r resonate because the voltage across L_m is clamped at the reflected output voltage. The magnetizing current, i_m, increases linearly during this period.

At t_1, S1 turns on due to the ZVS condition. The current drops to 0A and before reversing and flowing through the switch, S1. The resonant current waveform increases in amplitude from being clamped by the voltage difference between Vin and the reflected output voltage. The load current is proportional to the difference between the resonant current, i_r, and i_m. At t_2, the load current drops to zero due to the resonant current, i_r, equaling i_m, and causes D1 to turn off. Since the switching period is longer than the $L_r \cdot C_r$ resonant period, S1 continues to conduct until t_3. In the $f_m<f_s<f_r$ operating range, i_m implements the primary-side ZVS condition—which is independent of the load current and input voltage, thus extending the ZVS range beyond that of most of soft-switching topologies. Also, the secondary-side diode turns off after the current drops to 0A, thus eliminating the reverse-recovery problem, and diodes operate under the ZCS condition.

B. Operating Principle at $f_s=f_r$

When the switching frequency equals the $L_r \cdot C_r$ resonant frequency, the resonant current waveform shape resembles a sinusoid beginning at t_3 and ending at t_6. The diode currents on the secondary-side are in boundary mode. Under this condition, the conduction loss is at its lowest and the conversion efficiency is at its best.

C. Operating Waveform at $f_s > f_r$

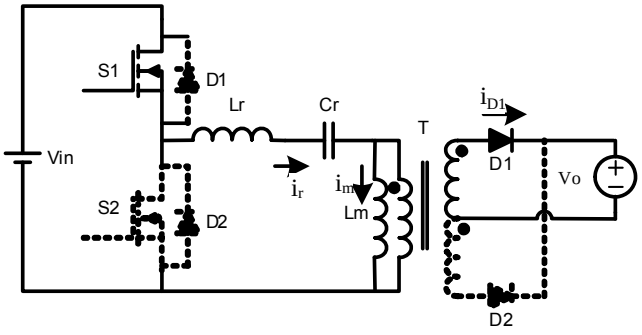
Figure 5 and Figure 6 show the equivalent circuit and operation waveform, respectively.

From t_0 to t_1, the S1 and D1 switch on and C_r and L_r resonate because the voltage across L_m is clamped at the reflected output voltage. i_m increases linearly from $-i_m$ to $+i_m$.

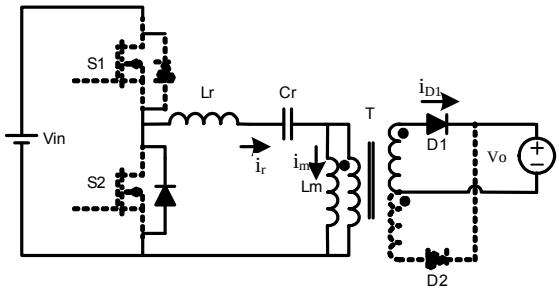
From t_1 to t_2, the S1 turns off before the resonance current equals the magnetizing current as the switching period drops to the resonant period. The resonance current is still larger than the magnetizing current, thus the current difference i_r-i_m is still fed to the load. The resonance current starts to flow through the body diode D2 after discharging the parasitic capacitor. The V_O reflection voltage blocks i_r and it decreases rapidly.

At stage to t_2 to t_3, the switch S2 turns on at the ZVS condition, the resonant current decreases to i_m and D1 turns off.

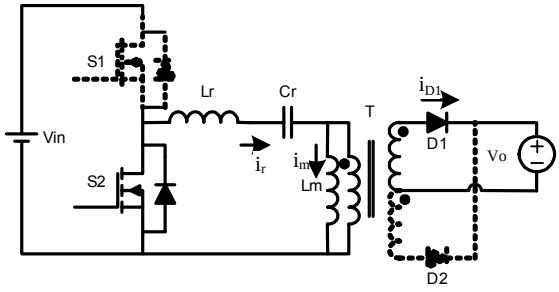
For $f_s > f_r$, the primary-side ZVS condition remains, while the ZCS condition is lost because V_O forces the diode current to 0A.



(a) Stage 1 [t0, t1]



(b) Stage 2 [t1, t2]



(c) Stage 3 [t2, t3]

Figure 5: Equivalent main circuit at $f_s > f_r$

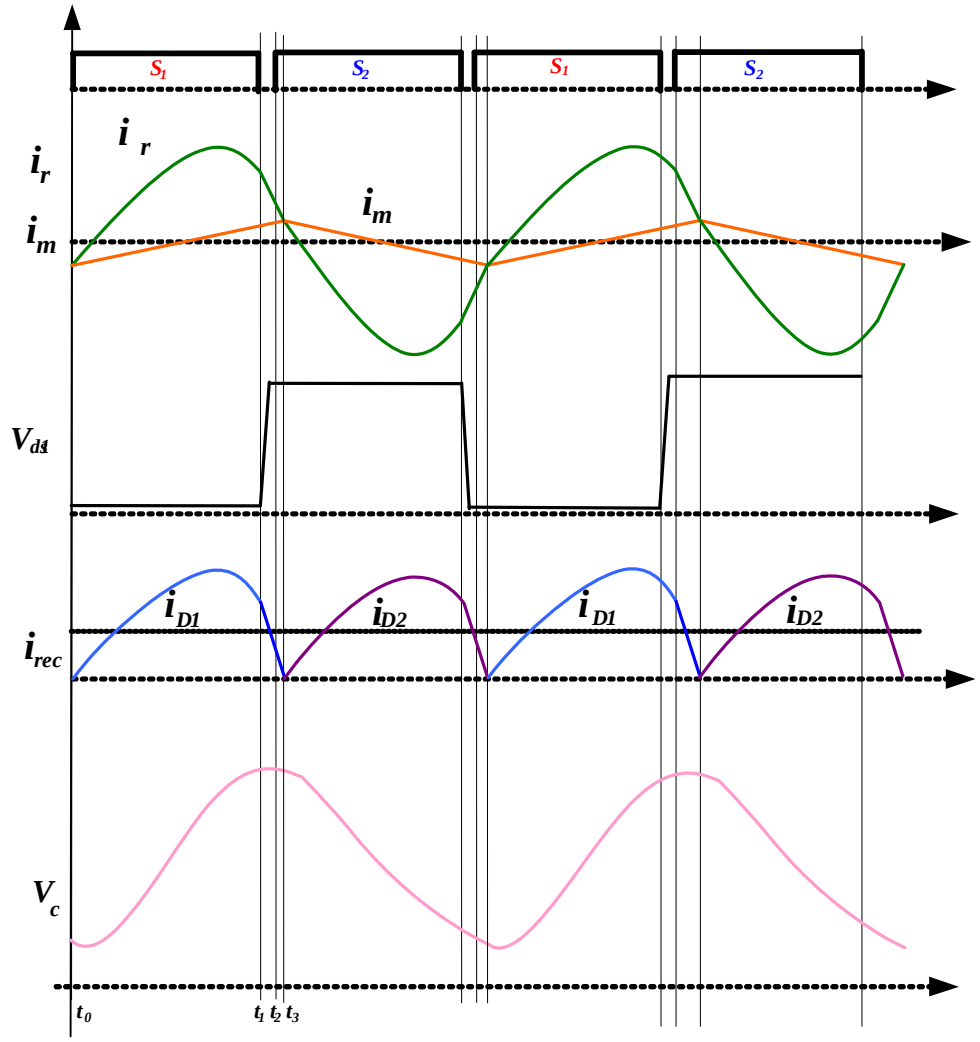


Figure 6: Operating waveform at $f_s>f_r$

2.3 Frequency Domain Analysis

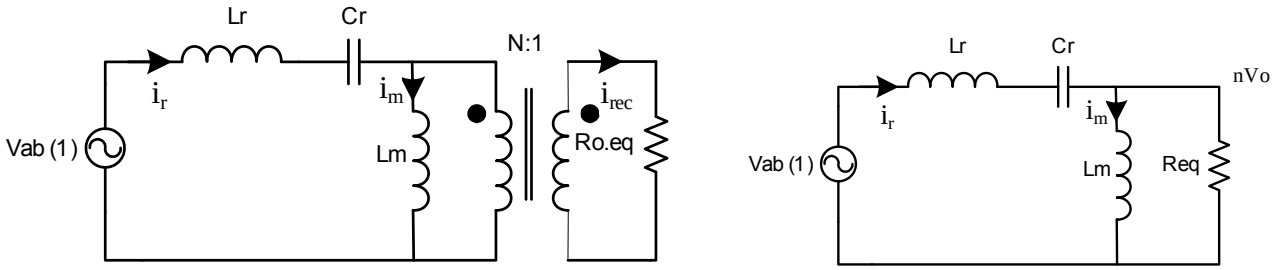


Figure 7: Simplified AC circuit of LLC-SRC

Exact analysis of LLC-SRC converter requires the time-domain method, which leads to complex models without a useful design methodology. Instead, this paper uses first-harmonic approximation (FHA) to simplify calculations by assuming that the input-output power transfer is due to first order harmonics of

the fundamental Fourier series of the currents and voltages.[i]

This approach neglects the harmonic current and assumes that the resonant current is purely sinusoidal. This is accurate when the switching frequency is equal to or greater than the resonant frequency in continuous mode. It is still valid, though less accurate, when the switching frequency drops below the resonant frequency when the current is discontinuous.

Figure 7 shows the LLC-SRC circuit simplified via FHA. During operation, the two half-bridge MOSFETs turn on and off symmetrically at a 50% duty cycle. Thus the tank input voltage V_{ab} is a square waveform at the amplitude V_{DC} with a DC component of $V_{DC}/2$. Thus, C_r acts as not only the resonant tank capacitor but also the DC-blocking capacitor.

The circuit on the left in Figure 7 can be further simplified as the circuit on the right, where R_{eq} is,

$$R_{eq} = N^2 \frac{8}{\pi^2} R_L \tag{3}$$

and R_L is the load impedance.

The fundamental of the Fourier component analysis of the input voltage can be expressed as,

$$V_{ab(1)} = \frac{2}{\pi} V_{dc} \sin(2\pi f_{sw} t) \tag{4}$$

Also the fundamental of the Fourier component analysis of the output voltage can be expressed as,

$$V_{o(1)} = \frac{4}{\pi} V_o \sin(2\pi f_{sw} t - \phi) \tag{5}$$

Based on the simplified AC circuit illustrated in Figure 7, the voltage gain of the output and input can be reduced to:

$$M(h, Q, f_n) = \frac{NV_0}{V_{dc}/2} = \left| \frac{j\omega L_m // R_{eq}}{j\omega L_m + \frac{1}{j\omega C_r} + j\omega L_m // R_{eq}} \right| = \frac{1}{\sqrt{(1+\frac{1}{h}-\frac{1}{hf_n^{\,2}})^2 + Q^2(f_n - \frac{1}{f_n})^2}} \tag{6}$$

Where the parameters defined as follows:

The inductor ratio:

$$h = \frac{L_m}{L_r} \tag{7}$$

Normalized frequency:

$$f_n = \frac{f_s}{f_r} \tag{8}$$

Characteristic impedance:

$$Z_0 = \sqrt{L_r / C_r} \tag{9}$$

Quality factor:

$$Q = \frac{Z_0}{N^2 R_{eq}} = \frac{\sqrt{L_r / C_r}}{N^2 R_{eq}} \tag{10}$$

Figure 8 shows a family of plots of voltage gain versus normalized frequency. For different Q values at the inductance value, h=10, the LLC-SRC has a load-independent point at the resonant frequency (f_n=1) where all curves are tangential to its unity gain. This load-independent point is located at an inductive zone which means the current lags behind the voltage.

In Figure 9 we can see that as h decreases, the gain curve shrinks towards to f_n=1, meaning that the minimum gain at no-load decreases.

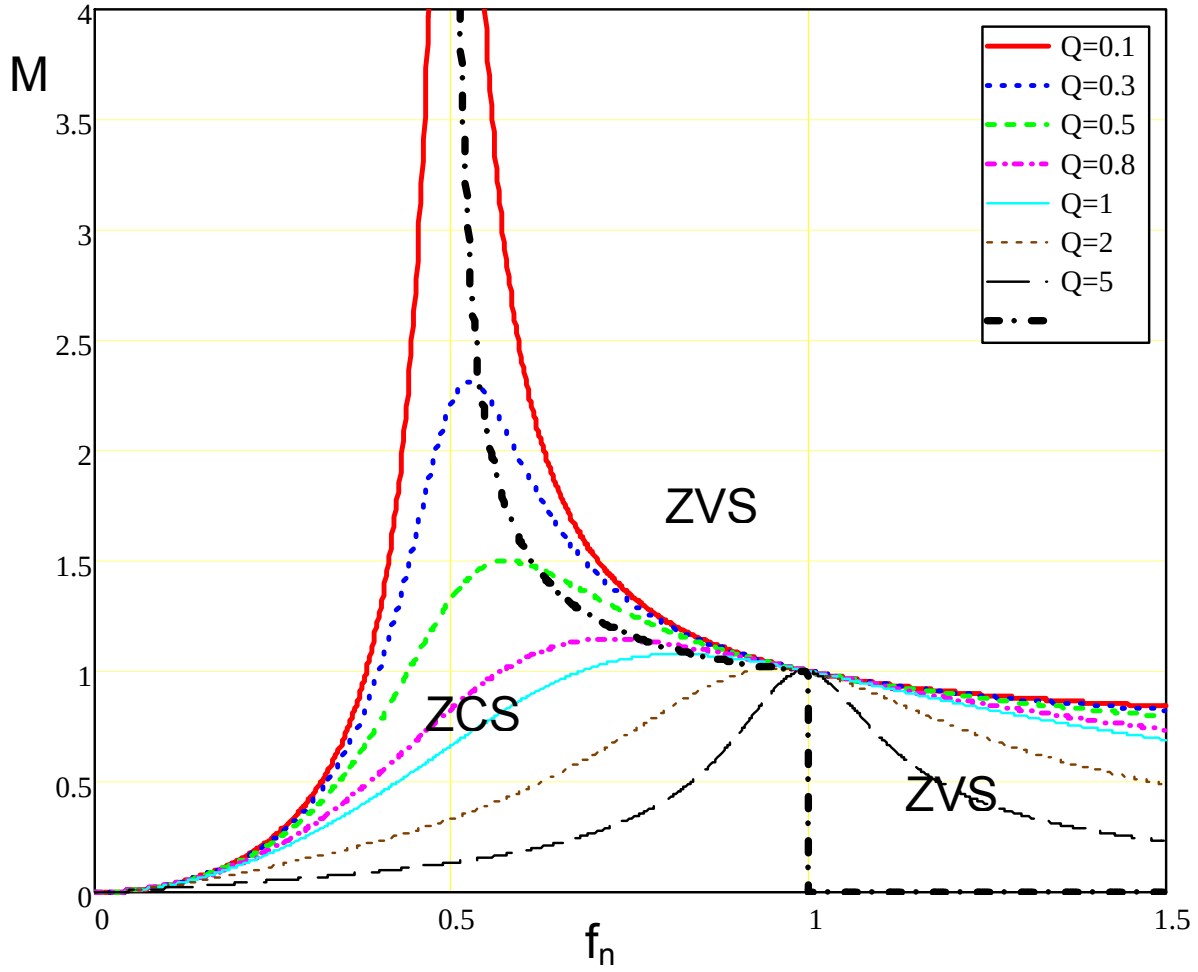


Figure 8: Gain characteristics of LLC-SRC

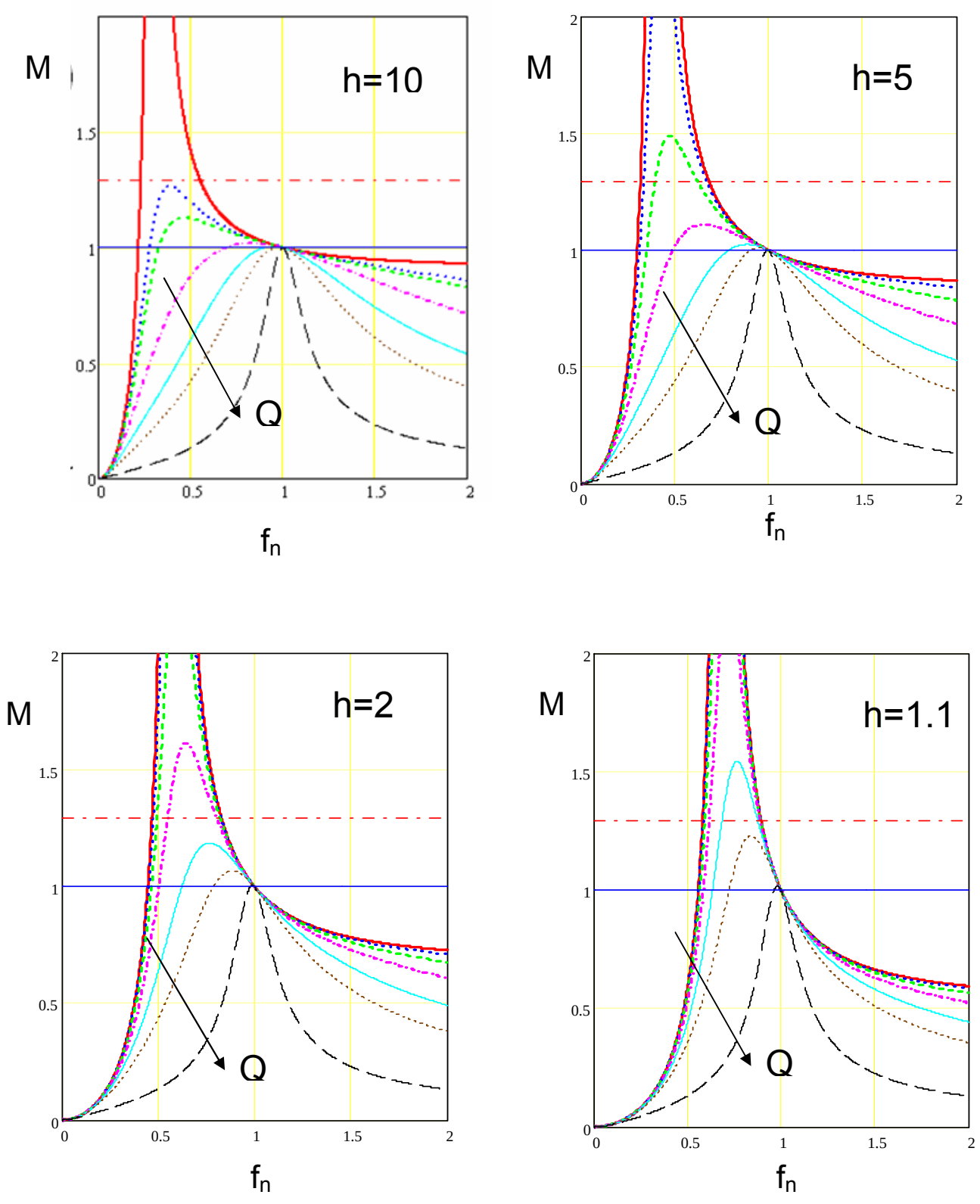


Figure 9: Shrinking Effect as h Increases

2.4 Performance Analysis of LLC resonant converter

A. Loss analysis on the operation at resonant frequency

At the resonance frequency, the resonant current is purely sinusoidal after ignoring the dead-time, and the magnetizing current is a triangle waveform, as shown in Figure 10.

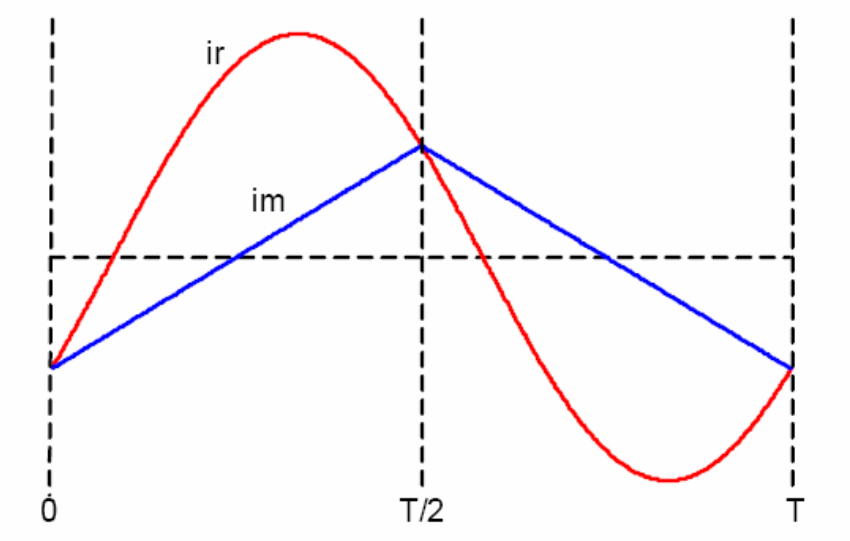


Figure 10: Waveforms of Resonant Current and Magnetizing Current

The resonant current can be expressed by:

$$i_r(t) = \sqrt{2} I_{rms\_pri} \sin(\omega t - \phi) \qquad \omega = 2\pi f_s = \frac{2\pi}{T} \tag{11}$$

Where I_{rms_pri} is the rms current of the resonant current, ω is the angular representation of the resonant frequency, and T is the switching period predetermined by the switching converter.

Since the output voltage clamps the magnetizing inductor in the first half of a PWM cycle and negative output voltage in the second half, it can be reduced to:

$$i_m(t) = \begin{cases} -I_m + \dfrac{NV_0}{L_m} t & if \quad 0 < t < \dfrac{T}{2} \\ I_m - \dfrac{NV_0}{L_m}(t - \dfrac{T}{2}) & if \dfrac{T}{2} < t < T \end{cases} \tag{12}$$

At time t, $i_m(t)$ is equal to the peak magnetizing current, I_m. Therefore, I_m can be represented as:

$$I_m = \frac{NV_0 T}{4L_m} \tag{13}$$

At time T, the resonant current equals the magnetizing current, therefore:

$$\sqrt{2}I_{rms\_pri}\sin(-\phi) = -\frac{NV_0T}{4L_m} \quad (14)$$

The current fed to the load is the difference between i_r and i_m,

$$\frac{1}{T/2}\int_0^{T/2}[\sqrt{2}I_{rms\_pri}\sin(\omega t-\phi)+\frac{NV_0T}{4L_m}-\frac{NV_0}{L_m}t]dt = \frac{V_0}{N\cdot R_L} \quad (15)$$

Where R_L is the load resistance.

From this equation, the rms of the tank current can be solved as:

$$I_{rms\_pri} = \frac{V_0\sqrt{4\pi^2+N^4R_L{}^2\frac{T^2}{L_m{}^2}}}{4\sqrt{2}\cdot N\cdot R_L} \quad (16)$$

The turn ratio N, the load resistance R_L, the output voltage V_O, and switching period T are predetermined for a specific converter, so the rms current is only related to L_m. The lower rms value of the primary side current translates to lower conduction loss generated by the MOSFET $R_{DS(ON)}$ and the inductor R_{DC}.

Based on the turn ratio and quality factor, Q, equation (16) can be rewritten as below:

$$I_{rms\_pri} = \frac{1}{4\sqrt{2}}\frac{V_0}{NR_L}\sqrt{4\pi^2+\frac{\pi^6}{16(h\cdot Q)^2}} \quad (17)$$

Normalizing the equation with the load current reflected on the primary side produces:

$$I_{rms\_pri\_norm} = \frac{1}{4\sqrt{2}}\sqrt{4\pi^2+\frac{\pi^6}{16(h\cdot Q)^2}} \quad (18)$$

The relationship between the h and Q and the primary rms current is shown Figure 11. The primary-side RMS current decreases as h×Q increases. However, the effectiveness of increasing h×Q is limited when it exceeds 6.

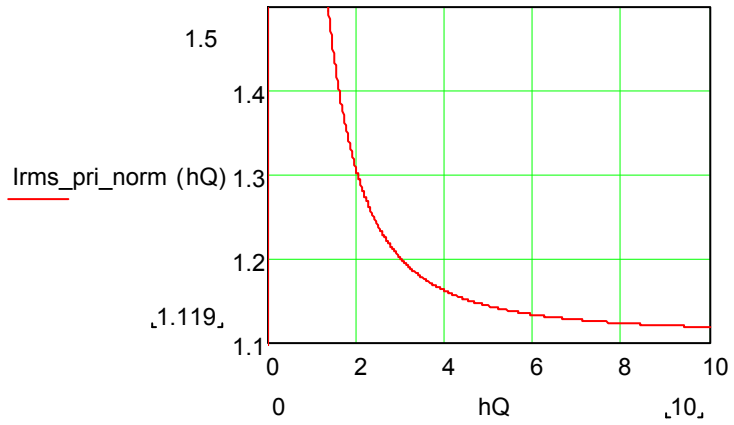


Figure 11: $I_{rms\_pri\_norm}$ vs. h×Q

Secondary-side conduction loss is still a concern, especially in low-voltage high-output–current applications. Although the conduction loss is related to the forward voltage drop of diode and output current, minimize the secondary-size RMS current when accounting for the diode's equivalent resistance or using SR. The output current is thus the difference between the resonant current and magnetizing current, and its RMS is:

$$I_{rms\_sec} = \sqrt{3}\frac{V_0\sqrt{12\pi^4 + \frac{5\pi^2 - 48}{L_m^{\ 2}} N^4 R_L^{\ 2} T^2}}{24\pi R_L} \tag{19}$$

Based on h and Q, the equation (19) can be rewritten as:

$$I_{rms\_sec} = \sqrt{3}\frac{V_0}{R_L}\frac{\sqrt{12\pi^2 + \frac{5\pi^2 - 48}{16(h\cdot Q)^2}\pi^4}}{24} \tag{20}$$

It can further be normalized with the load current:

$$I_{rms\_sec\_norm} = \sqrt{3}\frac{\sqrt{12\pi^2 + \frac{5\pi^2 - 48}{16(h\cdot Q)^2}\pi^4}}{24} \tag{21}$$

The relationship between h and Q and the secondary rms current is shown in Figure 12. The secondary-side RMS current decreases with the increasing hQ. However, the effectiveness of increasing of hQ is limited when it is larger than 1.

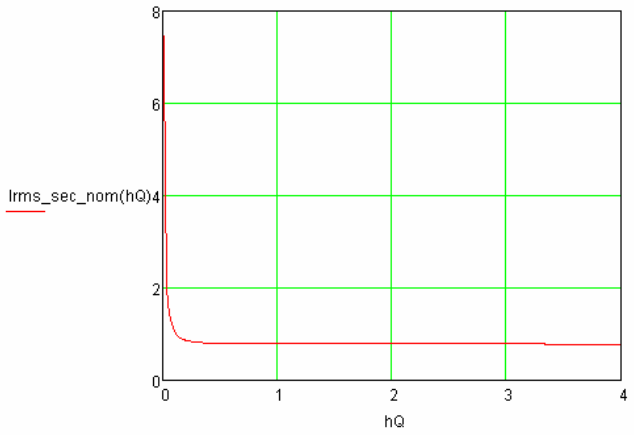


Figure 12: $I_{rms\_sec\_norm}$ vs. h×Q

As previously discussed, both the primary and secondary rms currents are determined by the magnetizing inductor. An hQ value higher than 6 limits its effectiveness on the rms current. Increasing the inductance of the magnetizing inductor increases hQ, which reduces the rms current and the conduction loss but needs to choose a larger core. Decreasing the inductance of the magnetizing inductor decreases hQ, which increases the rms current and the conduction loss but a smaller core could be used. So it is a trade-off for hQ between the core size and the rms current. Also, the hQ value will affect the peak gain of the converter and affect the holdup time. There is a trade-off between them.

In addition to conduction loss, the switching loss—which is composed of the turn-on and turn-off losses—contributes substantially to the circuit efficiency. The primary-side MOSFET has zero turn-on loss due to the ZVS condition, however hard-switching turn-offs at the peak magnetizing current generates substantial losses. Selecting a suitable magnetizing inductance can reduce both ZVS turn-on and turn-off loss.

B. Performance Analysis during Holdup

During holdup, the LLC boosts the output voltage by reducing the switching frequency. The minimum input voltage that can be regulated to the normal output voltage depends on the peak voltage gain. Efficiency is not a concern during holdup as it only last 20ms. For example, if the minimum required input voltage is 200V and the normal input voltage is 400V, then the minimum peak gain required here is 2 since the switching frequency is designed at the resonant frequency, which has unity voltage gain.

As shown in the family of curves of voltage gain versus h and Q values in Figure 9, the peak gain equals to one when the converter runs at the resonant frequency regardless of the h and Q values. However, the achievable peak gain changes with the h and Q values. This estimate is based on the FHA method for simplicity, though with an increase in error because the tank current is not precisely sinusoidal when converter runs below the resonant frequency.

Figure 13 shows the achievable peak gain with different h-Q combinations with a 3D plot. For each h-Q combination, there is one corresponding peak gain. This peak gain increases when h×Q drops. The map helps to narrow down the range of valid h-Q values that meet the peak gain. For instance, if the converter requires a peak gain that exceeds 2, then use a plane with gain equal to 2 to intersect with the peak gain surface: The h and Q values above the plane are valid design choices.

Given the high number of h-Q combinations that meet the gain requirement, narrowing h and Q values requires examining trade-offs between the efficiency, size, and active-component stress.

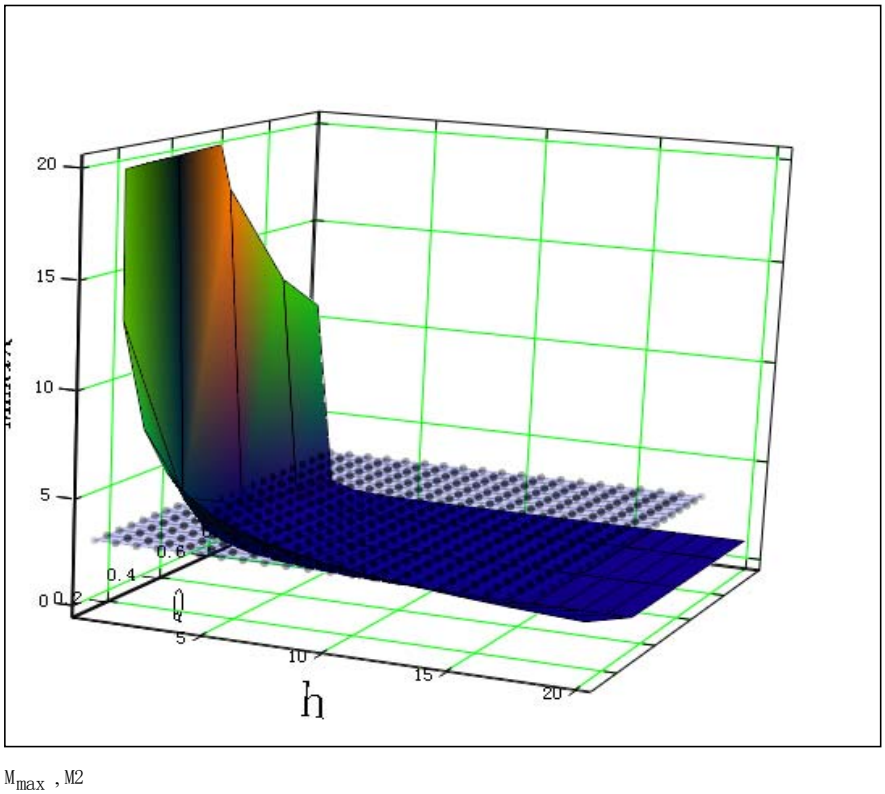


Figure 13: Peak Voltage Gain for Different h-Q Combinations

3. DESIGN PROCEDURE

The design goal for an LLC converter is to minimize power loss and to achieve a suitable peak gain that ensures a wider input voltage range. As previously discussed, the conduction and switching losses relate only to the magnetizing inductance, and discusses the relationship between the achievable peak gain and h-Q combinations. The following methodology for LLC converter design uses these analyses, and Figure 14 shows the flowchart of the LLC design procedure.

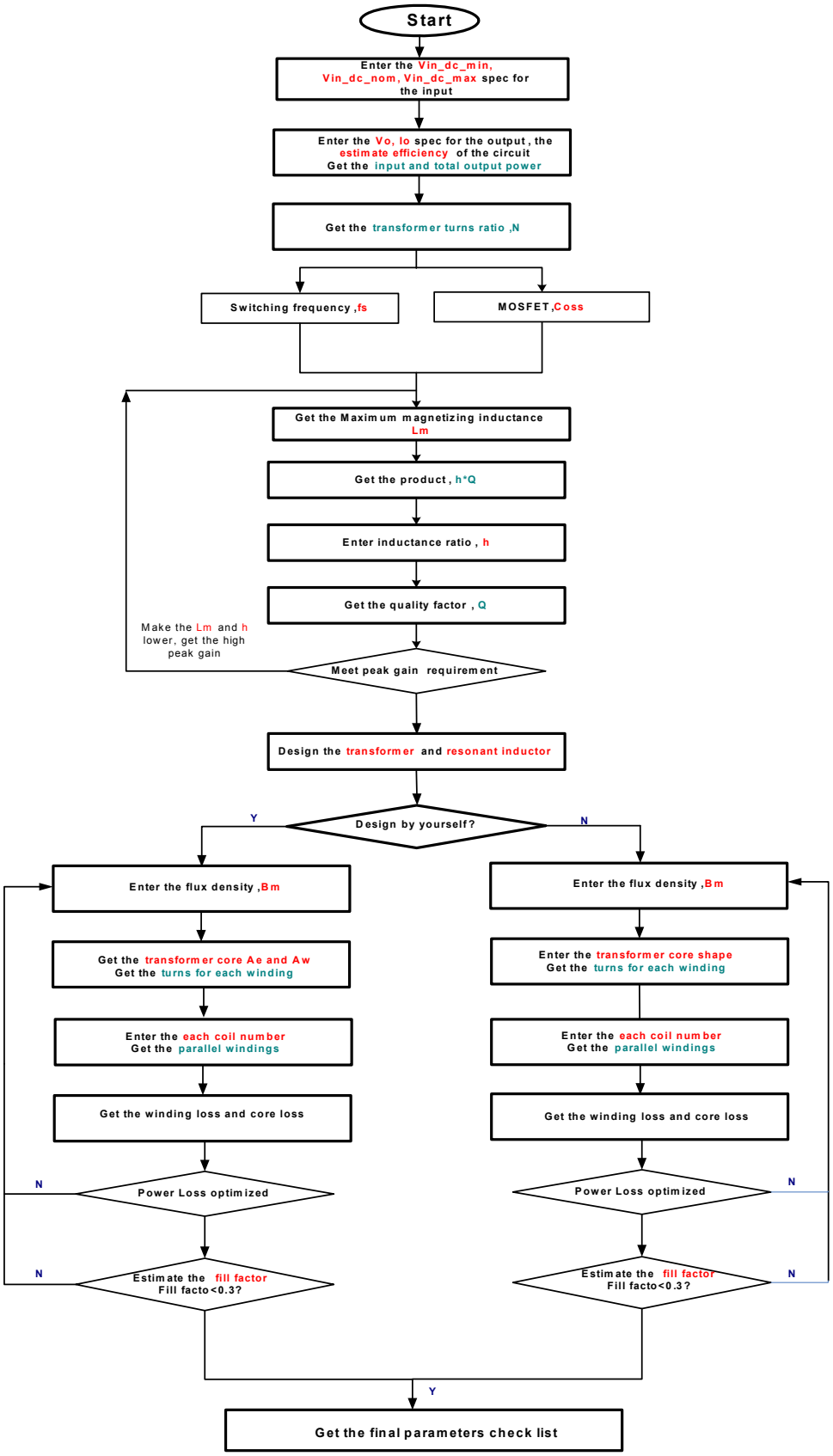


Figure 14: LLC Design Procedure

3.1 Predetermined Input and Output Specifications

The following specifications a predetermined in each LLC converter design:

- DC input voltage range: $V_{in\_dc\_min}$, $V_{in\_dc\_nom}$, $V_{in\_dc\_max}$, for example $V_{in\_dc\_min}$ =320V_{DC}, $V_{in\_dc\_nom}$=390V_{DC}, $V_{in\_dc\_max}$=400V_{DC}.
- Output: V_O, I_O, P_{OUT}
- Switching frequency: f_s
- Estimated power conversion efficiency: η

Then the maximum input power can be given as:

$$P_{in} = \frac{P_{OUT}}{\eta} \tag{22}$$

Generally, LLC-SRC switching frequency is designed for the load-independent resonant frequency, f_r, at the normal input voltage for optimizing the efficiency. This leaves the resonant tank's step-up capability to handle the minimum input voltage during voltage dips.

The series resonant frequency of an LLC-SRC can be set as:

$$f_r = f_s \tag{23}$$

3.2 Determining the Transformer Turns Ratio

Selecting the transformer turns ratio provides control over the design of LLC-SRC switching frequency at the load-independent point in normal input conditions where the voltage gain is unity. To ensure that the LLC-SRC operates at f_r, the turns ratio should meet the equation below:

$$N = \frac{V_{in\_dc\_nom}/2}{V_O} \quad or \quad N = \frac{V_{in\_dc\_nom}}{V_O} \tag{24}$$

Where V_O is the output voltage and $V_{in\_dc\_nom}$ is the normal DC input voltage: the left equation is for half-bridge applications, and the right equation is for full-bridge applications.

3.3 Design of Primary-Side Inductor, L_m

The previous section discusses the relationship between the conduction loss and switching loss; that the conduction loss is determined by the magnetizing inductance, and that the larger inductance of magnetizing inductor leads to lower conduction loss. Besides the conduction loss, the turn-off loss depends on the switch-off current, which is equal to I_m. Also larger inductors result in lower turn-off losses. As discusses earlier in this document, the LLC converter has the advantage of easily achieving the ZVS turn-on condition regardless of the load current. Discharging the MOSFET junction capacitor during dead time ensures the ZVS condition: The discharge current equals the peak magnetizing current, which is inversely proportional to the inductance of L_m: a larger magnetizing inductance results in a smaller magnetizing current.

Figure 15 shows the equivalent circuit during dead time. Discharge the voltage on the MOSFET V_{DS} to zero during dead time to ensure the ZVS such that,

$$I_m t_{dead} = 2C_{eq} V_{in} \quad (25)$$

where I_m is the peak magnetizing current during dead time, t_{dead} is the dead time, C_{eq} is MOSFET equivalent output capacitance, and V_{in} is the LLC bus voltage.

Given I_m as expressed in Equation (13), the magnetizing inductance should satisfy the following term for a half-bridge topology:

$$L_m < \frac{T \cdot t_{dead}}{16C_{eq}} \quad (26)$$

Where T is the switching period (which equals the resonant period), t_{dead} is the dead time, and C_{eq} is equivalent output capacitor of MOSFET.

For full-bridge applications, the magnetizing inductance should meet the following term:

$$L_m < \frac{T \cdot t_{dead}}{8C_j} \quad (27)$$

So the conduction loss is determined by the magnetizing inductance, and the larger inductance of the magnetizing inductor leads to lower conduction loss. Given that soft-switching maximizes the magnetizing inductor, the optimizing the magnetizing inductor design is a matter of meeting the soft-switching requirement.

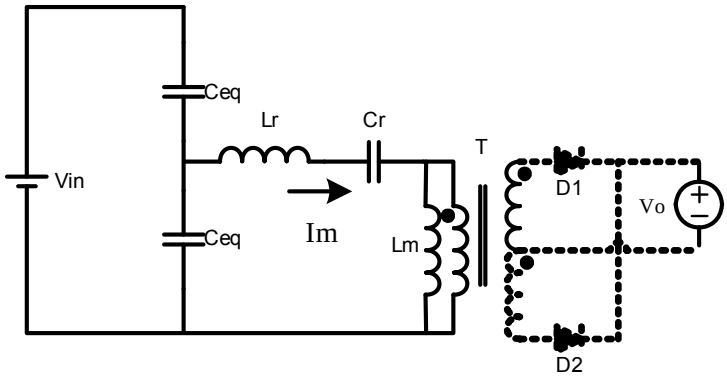


Figure 15: Equivalent Circuit during Dead Time

3.4 Determining L_r, C_r.

During holdup, the LLC boosts the output voltage by reducing the switching frequency, and regulating the minimum input voltage to the normal output voltage relies on the peak voltage gain. Figure 13 gives the achievable peak gain for different combinations of h and Q.

There are apparent choices to meet the minimum peak gain. To further narrow the design parameters, we examine the magnetizing inductor. The soft-switching and conduction loss requirement determines the magnetizing inductor. However, choosing the magnetizing inductor fixes the relationship between h and Q in place. From the definition of h and Q, we get:

$$h \cdot Q = \frac{L_m}{L_r}\frac{\sqrt{L_r / C_r}}{R_{eq}} = \frac{L_m}{L_r}\frac{\sqrt{L_r / C_r}}{N^2 \frac{8}{\pi^2} R_L} = \frac{\pi^2}{8}\frac{2\pi f_r L_m}{N^2 R_L} \quad (28)$$

Where f_r is resonant frequency, which equals the switching frequency, R_L is the load resistor. Using the STP11NK60 as an example, L_m can be calculated based on the ZVS requirement. Then the product of h and Q is:

$$h \cdot Q = 2.38 \quad (29)$$

Narrowing down the number valid h and Q further requires a trade-off between peak voltage gain and the efficiency, size and stress the active components. Figure 16 shows a family of gain curves with the same product of h and Q. If h decreases, then L_r increases due to L_m; thus the L_r loss and size increases, and Q increases accordingly. C_r decreases and leads to high voltage stress on the resonant capacitor. This leads the peak gain and the peak current will to decrease following the expression:

$$I_{pk} = \frac{V_{in} / 2}{\sqrt{L_r / C_r}} \sin(\pi \frac{f_r}{f_{start}}) \quad (30)$$

Where the V_{in} is the input voltage, f_r is the resonant frequency and f_{start} is the startup frequency.

For optimized design, select h between 4 and 10.

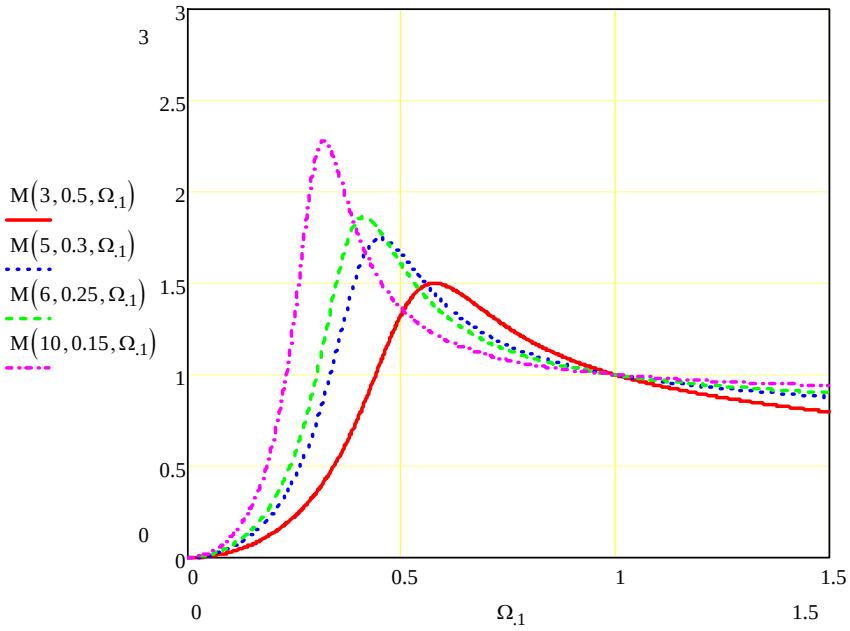


Figure 16: Family of Gain Curves with the Same h×Q

As long as the inductance ratio h is define, then L_r can be calculated according equation (7), and the C_r derived from equation (1).

3.5 Transformer Design

A. Transformer Core Selection

Select an appropriate core for the specific output power at the operating frequency; typically ferrite for most applications. The core area product (AP) — the core magnetic cross-section area multiplied by window area available for winding—provides an initial estimate of core size for a given application. A rough indication of the required $A_E A_W$ (cm^4) is given by following equation 31[ii]:

$$A_E \cdot A_W = \left(\frac{L_m \cdot I_p \cdot I_{rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j} \right)^{\frac{4}{3}} cm^4 \quad (31)$$

Where K_u is winding factor (typically 0.1 to 0.25 for an off-line transformer), K_j is the current-density coefficient (typically 400 to 450 for a ferrite core), B_{max} is the maximum allowable flux density at normal operation (usually preset to be the saturation flux density of the core material; 0.1T to 0.3T), and I_{peak} is the primary-side peak current from equation (16):

$$I_p = \sqrt{2} \cdot I_{rms\_pri}$$

Where I_{rms} is the transformer's total RMS current that includes the current through the primary side and the current reflected from the secondary side. The RMS current can be derived as.

$$I_{rms} = I_{rms\_pri} + \frac{I_{rms\_sec}}{N} \quad (32)$$

B. Primary and Secondary Winding Turns

With a defined core size, the turns of secondary side can be easily deduced since the output voltage clamps the winding:

$$N_s = \frac{V_o}{4 f_r B_{max} A_e} \quad (33)$$

Where:

V_O is the output voltage,

B_{max} is the allowable flux density (generally selected according to the core loss), and

A_e is the effective area cross sectional core,

Secondary winding (N_s) is a function of N and N_p, as shown in equation (34).

$$N_p = N_s \cdot N \quad (34)$$

C. Wire Size

Once all the winding turns are determined, select the wire size to minimize the winding conduction loss. The winding loss depends on the RMS current value, the length and the cross section of the wire, and the transformer structure.

Determine the wire size through the winding RMS current. For an LLC converter, the RMS current on primary side and the secondary side are represented by equation (16) and equation (19), respectively.

The required wire size for the primary and secondary side is (respectively):

$$S_{pri} = \frac{I_{rms\_pri}}{J} \qquad (35)$$

$$S_{sec} = \frac{I_{rms\_sec}}{J}$$

Where J is the current density of the wire, which is typically 450A/cm^2.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire should be less than 2*Δd (where Δd is the skin-effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}} * 10^3 (mm) \qquad (36)$$

Where μ is the magnetic permeability of the conductor, which usually equals to the permeability of vacuum for most conductor, i.e. 4π×10^{-7}H/m, and σ is the conductivity of the wire (for copper, σ is typically 6×10^{7}S/m at 0° that increases with the temperature, which means Δd decreases).

If the required winding size is larger than Δd, use multiple strands of thinner wire or Litz wire to minimize the AC resistance. The effective cross section area of multiple wire strands or Litz wire must meet the requirement set by the current density.

After determining the wire size, determine whether the window area with the selected core can accommodate the windings. Calculate the window area required by each winding and include the area for inter-winding insulation, bobbin and spaces existing between the turns. Select a fill factor (the winding area to the whole window area of the core) well below 1 because of the inter-winding insulation and spaces between turns: For best results, select a fill factor no greater than about 30%. Use smaller fill factors for transformers with multiple outputs.

Compare the total window area required to the available window area of a selected core based on these considerations. If the required window area exceeds the selected one, either reduce the wire size select a larger core. However, reducing the wire size increases the copper loss of the transformer.

D. Air Gap

With the selected core and winding turns, the air gap of the core is given as equation (38):

$$l_a = \frac{\mu_0 * N_p^2 * A_e}{L_m} - \frac{l_c}{\mu_r} \qquad (38)$$

Where:

A_e is the cross sectional area of the selected core,

μ_0 is the permeability of vacuum $4\pi\times10^{-7}$H/m,

L_m and N_p are the primary winding inductance and turns, respectively,

l_C is the magnetic path core length and

μ_r is the relative magnetic permeability of the core material.

For a ferrite core, μ_r is very large, so l_a can be approximated as:

$$l_a = \frac{\mu_0 * N_p^2 * A_e}{L_m} \quad (39)$$

3.6 Inductor Design

A. Inductor Core Selection

To design the transformer, choose an appropriate core based on the AP value. The AP value is the product of effective are of core (A_E) and the winding window (A_w). The following equation estimates A_EA_W (cm^4)[1]:

$$AP = A_E \cdot A_W = \left(\frac{L_r \cdot I_p \cdot I_{rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j} \right)^{\frac{4}{3}} cm^4 \quad (40)$$

Where:

K_u is winding factor (typically 0.2 to 0.3),

K_j is the current-density coefficient (typically 400 to 450 A/cm^2 for a ferrite core),

B_{max} is the maximum allowable flux density in normal operation, which is usually preset to the saturation flux density of the core material (0.3T to 0.4T)

I_{peak} is the primary-side peak current (the maximum peak current occurs at startup, so use equation (30)).

Based on the design notes in transformer design section, the wire size is:

$$S_L = \frac{I_{rms\_pri}}{J} \quad (41)$$

Where J is the current density of the wire (typically 450A/cm^2).

3.7 Parameter Design

A. Fset, CT, SS

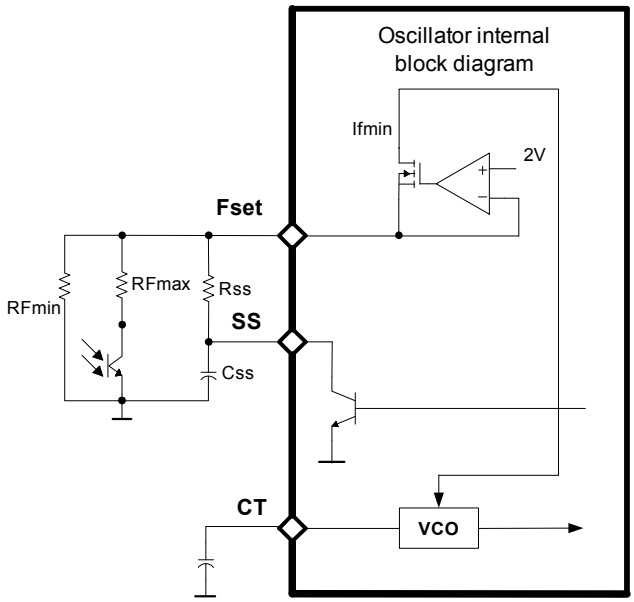


Figure 17: Oscillator Internal Block Diagram

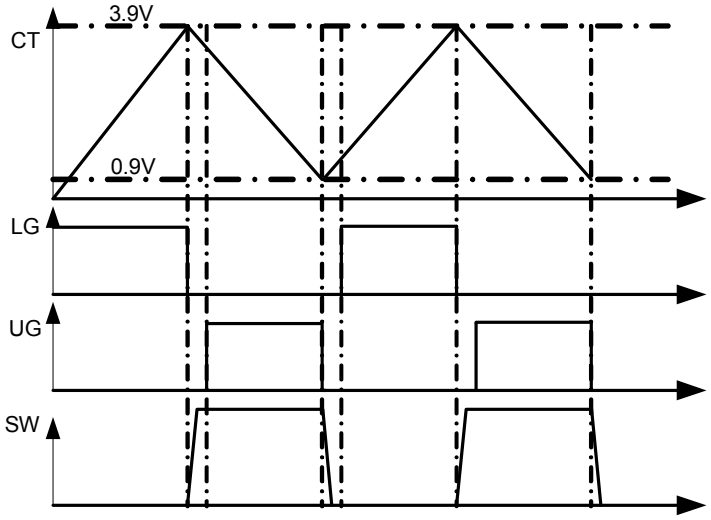


Figure 18: Operating Oscillator Waveform

The LLC-SRC regulates the output voltage by adjusting the operating frequency. The voltage-controlled oscillator (VCO) shown in Figure 17 changes the frequency as programmed by the external capacitor on CT pin. This capacitor alternately charges and discharges from a current value determined by an external network on the Fset pin. Larger current sources lead to higher oscillator frequency. The pin provides a 2V reference voltage with about a 2mA source-current capacity. The network on the Fset pin is as follows:

1) RF_{min}. Resistor that determines the minimum frequency.

2) RF_{max}. Resistor connected between the Fset pin and the collector of optocoupler. The optocoupler

transfers the feedback signal from the secondary side to the primary side by modulating the collector current—and therefore the frequency—to regulate the voltage. RF_{max} defines the maximum frequency where the optocoupler is fully saturated.

3) An RC-series network. This connects between the pin and ground to form the soft-start circuit, which sets a frequency shift during startup. Note that the contribution of this branch is zero during steady state.

Figure 18 shows the timing diagram between the oscillator waveform, the gate driver, and the swing node of the half bridge. Note that the low-side driver is on while the triangle waveform is ramping up, and the high-side driver is on while the triangle waveform is ramping down. This procedure ensures that the low-side MOSFET turns on first to charge the bootstrap capacitor at startup or when the IC resumes operation during burst mode, and guarantees the bootstrap capacitor is charged and ready to supply the high-side driver. The triangle waveform swings between 0.9V and 3.9V as defined by internal two comparators. Thus the minimum frequency (f_{min}) and maximum frequency (f_{max}) are:

$$f_{min} = \frac{1}{3 \cdot CF \cdot RF_{min}} \quad (42)$$

$$f_{max} = \frac{1}{3 \cdot CF \cdot (RF_{min} // RF_{max})} \quad (43)$$

After CF is fixed at hundreds of PF or nF, depending on the maximum source current capability and the device power consumption. Select RF_{min} and RF_{max} so that the selected oscillator frequency can cover the regulatory range; from the minimum frequency (minimum input and maximum load), to the maximum frequency (maximum input and minimum load).

$$RF_{min} = \frac{1}{3 \cdot CF \cdot f_{min}} \quad (44)$$

$$RF_{max} = \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (45)$$

Here RF_{max} determines the maximum frequency where the controller will enter burst mode operation at the minimum load. However, if the controller enters the burst mode operation under some load, P_{OUT}, the RF_{max} can be determined as:

$$RF_{max} = \frac{3}{8} \frac{RF_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (46)$$

P_{OUT} is such that the transformer peak current is low enough not to cause audible noise.

The soft-start circuit progressively increases the converter power to avoid large inrush current. The soft-start circuit can be implemented by R_{SS} and C_{SS}. Since the voltage gain is inversely proportion to the

switching frequency, the soft-start functions by sweeping from the maximum frequency until the control loop takes over.

Initially, C_{SS} is fully discharged and R_{SS} is effectively in parallel with RF_{min} so that the initial frequency is:

$$f_{start} = \frac{1}{3 \cdot CF \cdot (RF_{\min} // R_{ss})} \quad (47)$$

Then determine R_{SS} and C_{SS} as：

$$R_{ss} = \frac{RF_{\min}}{\frac{f_{start}}{f_{\min}} - 1} \quad (48)$$

$$C_{ss} = \frac{3 \cdot 10^{-3}}{R_{ss}} \quad (49)$$

Where f_{start} is less 3 times of the resonant frequency, and C_{SS} selection is a compromise between the soft-start function and the OCP function.

B. Burst Mode

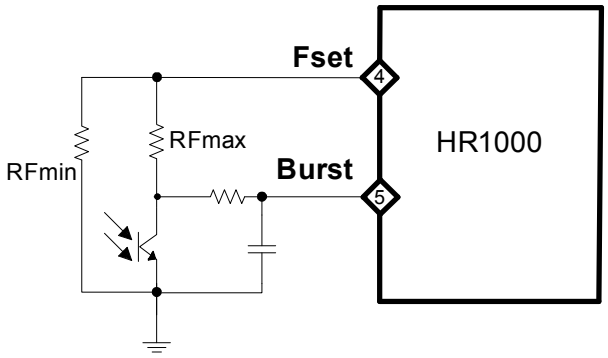


Figure 19: Functional Diagram of Burst Mode

When the converter runs at light load or no load, the switching frequency approaches the maximum frequency. The magnetizing current must be high enough to continue soft-switching. This results in large switch-off and conduction losses that keep the no-load power loss relatively high. To overcome this issue, design the burst mode function to allow the converter to operate intermittently at no-load or at light-load. It operates with only a few switching cycles spaced out by a long idle period where the two MOSFETs are OFF. The result is a substantially reduced equivalent switching frequency, which reduces the associated power loss. This facilitates converter compliance with the energy-saving no-load requirement.

To implement burst mode, connect a resistor between the optocoupler collector and the Burst pin. If the Burst pin voltage is lower than 1.25V, the HR1000 enters burst mode where not only the two MOSFETs are OFF, but the oscillator stops and the output voltage continues to drop. Then the voltage on the

optocoupler collector ramps up until it exceeds 1.25V and then the IC resumes operations.

C. Current Sensing Methods

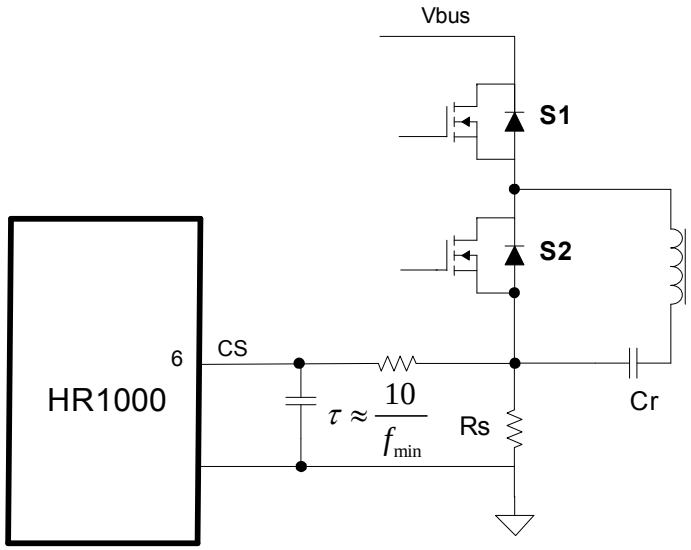


Figure 20: Current Sensing with a Sense Resistor

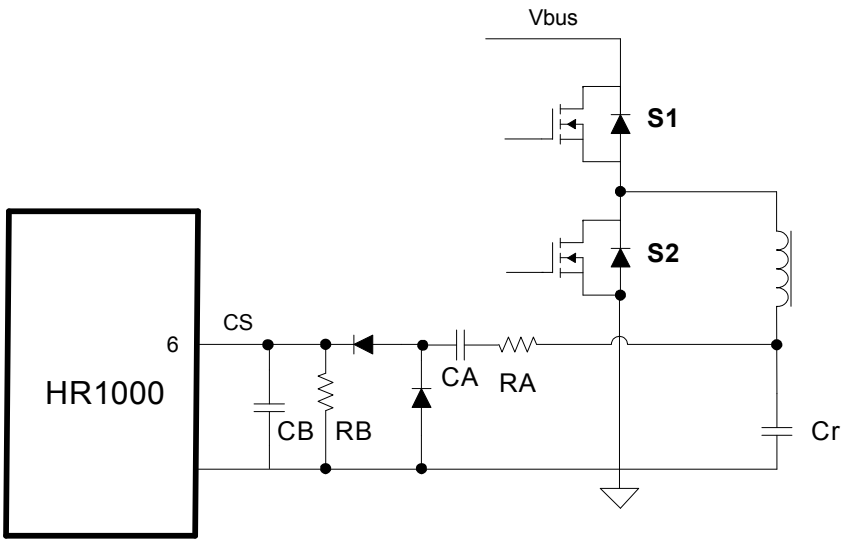


Figure 21: Current Sensing with Lossless Network

The LLC resonant converter is essentially a voltage-mode converter. Unlike conventional PWM converters where the duty cycle controls the power, the LLC resonant converter duty cycle is fixed and its switching frequency controls its output power. In addition, when the current exceeds a preset value, the converter increases the switching frequency to limit the current. Frequency changes take at least until the next cycle, making cycle-by-cycle limitation impossible.

Figure 20 shows current sensing for over-current protection using a sense resistor, and Figure 21 shows current sensing with a lossless network

The HR1000 integrates a sophisticated over-current protection system using the CS pin. The CS pin connects to two comparators: the first comparator has a 0.8V threshold, and the second comparator has a 1.5V threshold. When the voltage on CS pin exceeds the 0.8V threshold, the first comparator trips and discharges C_{SS}. The switching frequency increases quickly to decrease the power delivered. The discharge continues until the voltage on the CS pin drops by 50mV. Under the output-short condition, the peak current is nearly constant by this frequency change.

If the voltage on the CS pin exceeds 1.5V, the second comparator triggers the IC to shutdown and latch off. Restarting the IC requires that VCC drop below the UVLO threshold before rising again.

Using sense resistor for current sensing requires assuming that the RC filter's time constant is ten times the minimum frequency, such that the sense resistor value is:

$$R_s \approx \frac{4}{I_{crpk}} \tag{50}$$

Where the I_{crpkx} is the desired peak current through the primary switch or the resonant capacitor.

Using a lossless network requires two conditions.

1) If R_A in series with C_A is small (> several hundred Ωs), C_A operates like a current divider. Use the following equations to design the lossless sensing circuit.

$$C_A < \frac{C_r}{100} \tag{51}$$

$$R_B = \frac{0.8\pi}{I_{Crpk}}(1+\frac{C_r}{C_A}) \tag{52}$$

(2) If the resistor R_A is not small (~10kΩ), then the sensing network works like a divider for the ripple voltage on C_r. Use the following equations:

$$C_A < \frac{C_r}{100} \tag{53}$$

$$R_B = \frac{0.8\pi}{I_{Crpk}} \frac{\sqrt{R_A{}^2 + X_{C_A}{}^2}}{X_{Cr}} \tag{54}$$

Where the reactance calculations of C_A and C_r are based on the frequency where the maximum peak resonant current occurs. Empirically, the R_B and C_B time constant is in range of $10/f_{min}$.

With either circuit, Consider the calculated value a cut value that needs adjustment based on experimental results to meet the design goals.

D. Input Voltage Sensing

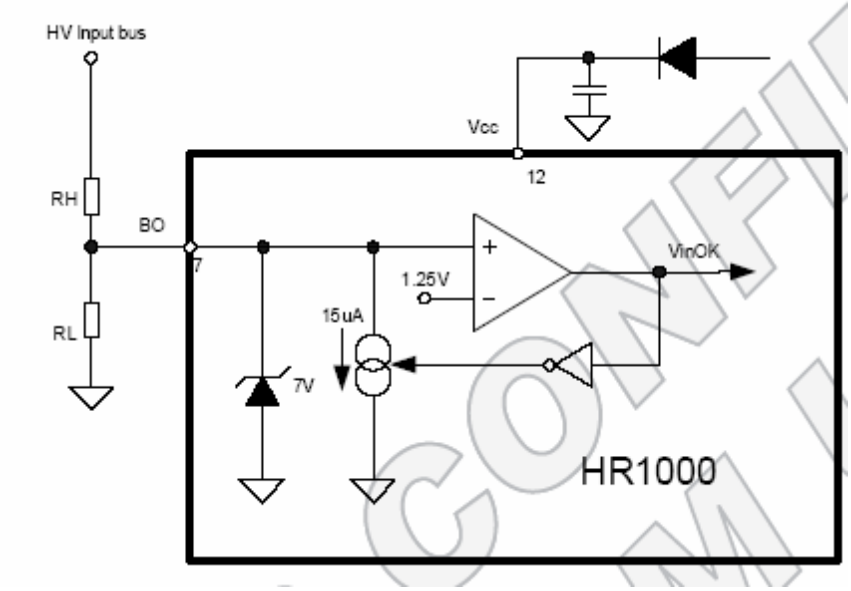


Figure 22: Input-Voltage Sensing Block

The HR1000 provides a brown-out function when the voltage on the BO pin goes below 1.25V. The controller then remains OFF under this condition until the soft-start capacitor discharges, the PFC-STOP pin is open, and the IC is disabled. As the voltage on the BO pin rises and exceeds 1.25V, the IC restarts. The internal comparator provides a current hysteresis of 15μA; this hysteresis is off, which occurs when the BO voltage rises above the internal 1.25V reference, and on when the BO voltage drops below the 1.25V reference. This ensures the LLC resonant controller works within the defined input voltage range to prevent over-current and voltage stress. Connect the BO pin to the tap of a resistor divider connected to either the AC rectifier voltage or the DC bus voltage.

Based on Figure 22, the R_H and R_L resistors can be expressed as:

$$R_H = \frac{Vin_{on} - Vin_{off}}{15 \cdot 10^{-6}} \quad (51)$$

$$R_L = R_H \frac{1.25}{Vin_{off} - 1.25} \quad (52)$$

Where the Vin_{on} and Vin_{off} are the ON/OFF threshold of the input voltage.

E. Boot-Strap Capacitor

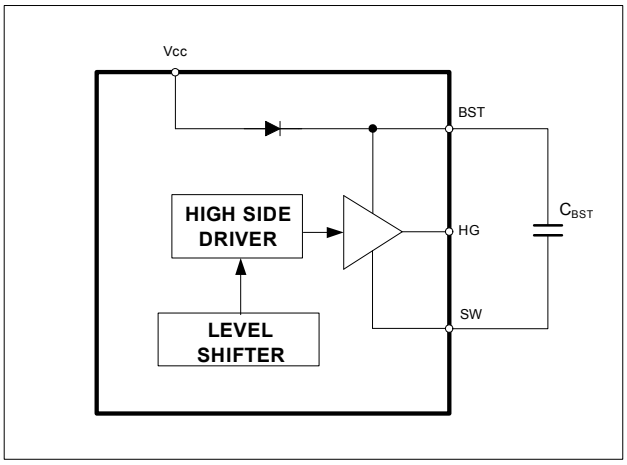


Figure 23: High-Side Gate Driver

The external BST capacitor powers the high-side gate driver. VCC charges this capacitor through an integrated bootstrap diode, which simplifies the external driving circuit for the high-side switch by allowing to the BST capacitor to be charged when the low-side MOSFET is ON. To provide sufficient energy and without a long charge time, select a BST capacitor value in the range of from 470nF to 1μF.

F. Low-Side Gate Driver

The LG pin provides the gate-drive signal for the low-side MOSFET. As the maximum absolute rating table shows, the maximum voltage on the LG pin is 16V. During severe conditions—such as a short circuit—hard-switching is unavoidable and will generate high voltage spikes on the LG pin due to the oscillations from the long gate-drive wire and the MOSFET's parasitic capacitance and small gate drive resistor. This high voltage spike poses a threat on the LG pin, so add a 15V Zener diode placed close to the LG and GND pins.

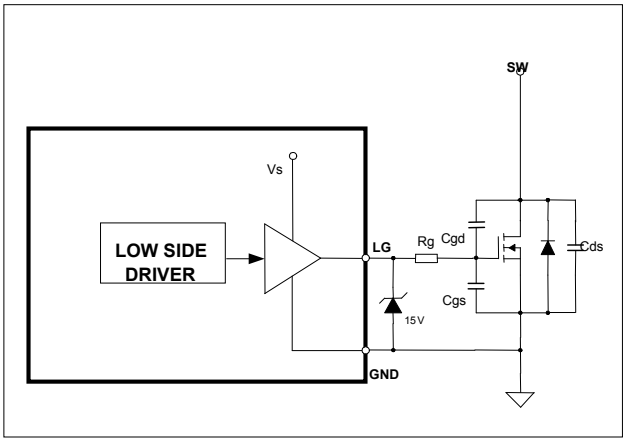


Figure 24: Low-Side Gate Driver

4. EXAMPLE DESIGN

This application note describes a 90W adapter as a reference design for the LLC resonant converter as

shown in Figure 25. The circuit consists of two stages: a front-end PFC using the MP44010, and a resonant DC/DC converter using the HR1000. The PFC stage delivers a stable 400V_{DC} and reduces the mains harmonic to meet European standard EN61000-3-2. The second stage is a resonant converter with a half-bridge topology that works in ZVS. The HR1000 controller incorporates the necessary functions to properly drive the half-bridge with a 50% fixed-duty cycle with dead-time, and works using a variable frequency.

This note only introduces the LLC design and the spreadsheet design tool. For PFC design, please refer to AN045.

4.1 Specification

Table 1: Specifications for a 90W Adapter

Parameter	Symbol Value Unit	Value	Unit
Input Voltage	VAC	90 to 265	VAC
Line Frequency	f_{line}	47 to 63	Hz
Output Voltage	V_O	19.2	V
Output Current	I_O	4.7	A

4.2 Schematic

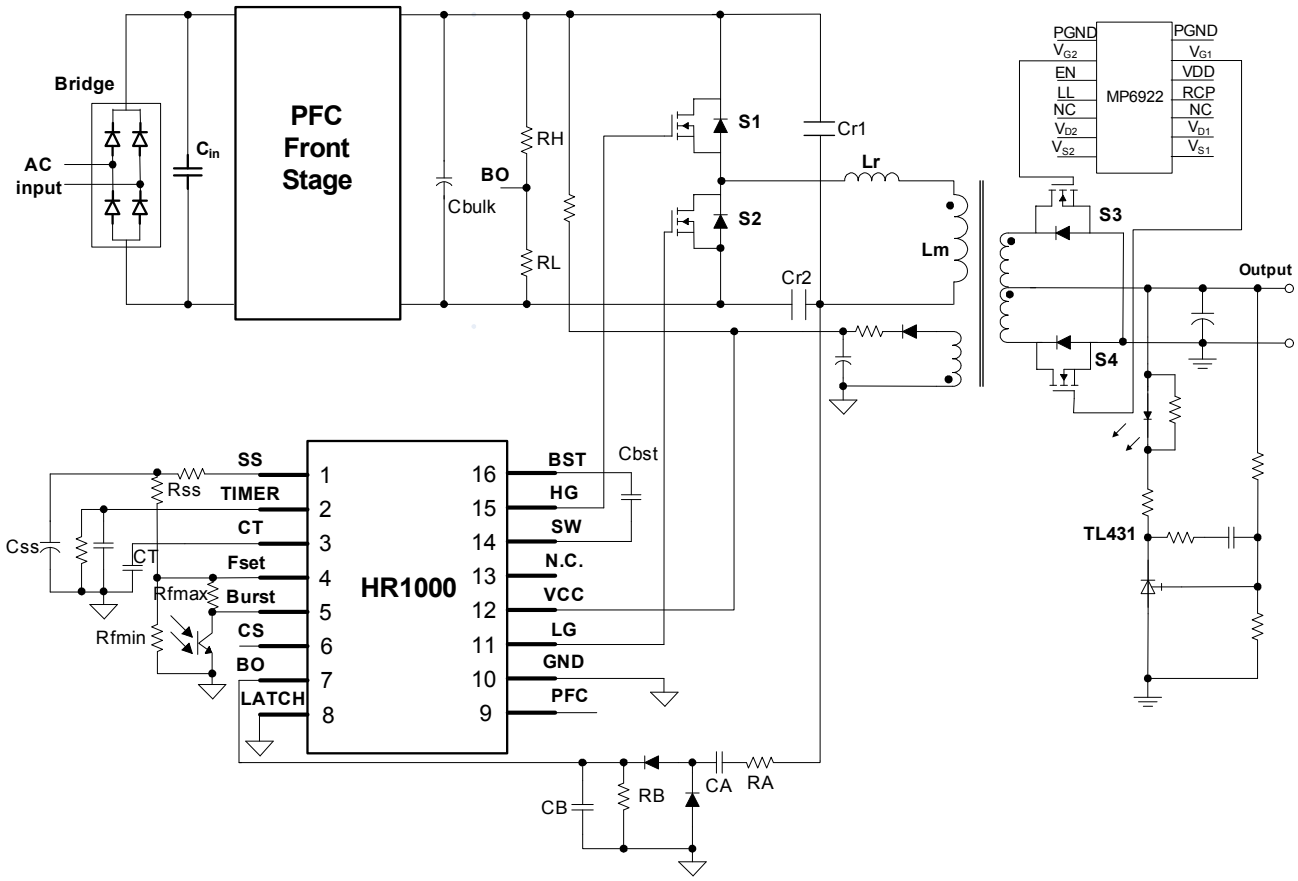


Figure 25: Schematic for a 90W Adapter

4.3 Design Spreadsheet Using MPS's Design Tool[iii]

A. Input and Output Specifications

The underlined red data is user input. This tool can calculate the values shown in cyan.

Input Spec		○ Full Bridge	● Half Bridge				
Converter Topology							
Minimum DC Voltage	Vin_dc_min	320	V				
Normal DC Voltage	Vin_dc_nom	390	V				
Maximum DC Voltage	Vin_dc_max	400	V				
Higher Resonant Frequency	fs	100	kHz				
Effecitive Output Cap. of MOSFET energy related	Coss	180	pF				
Output Spec		Vo		Io		Po	
output 1		19.20	V	4.70	A	90.24	W
output 2		0.00	V	0.00	A	0	W
Total Output Power	Po_total	90.24	W				
Estimate Efficiency	η	0.93	%				
Input Power	Pin	97.030	W				

B. Transformer Turns Ratio

The LLC-SRC switching frequency can be designed at a load-independent point for normal input conditions where the voltage gain is at unity. The turns ratio only depends on the input and output voltage.

2. Main Circuit Design

transformer turns ratio		
Transformer Turns Ratio 1 (Np:Ns1)	N1	10
Transformer Turns Ratio 2 (Np:Ns2)	N2	

C. Transformer Primary Inductance

The peak magnetizing current must fully discharge the MOSFET's capacitance during dead time to satisfy the ZVS condition. The primary inductance must be lower than the value calculated in equations 26 and 27.

magnetizing inductance			
Primary Inductance	Lm	900	uH
Resonant Inductance and capacitance			
Inductance Ratio(h=Lm/Lr)	h	9.0	
Resonant Inductance	Lr	100	uH
Resonant Capacitance	Cr	24	nF

D. h, Lr, and Cr

Selecting the magnetizing inductor cements the relationship between h and Q. Valid h and Q values must trade off between the peak voltage gain, efficiency, size and stress on active components. To optimize the design, select an inductance ratio between 4 and 10 and then check whether the achievable peak gain satisfies the minimum input voltage requirement. The required peak gain is:

$$Gain\max = \frac{Vin\_dc\_nom}{Vin\_dc\_\min} = 1.25 \quad (53)$$

As shown in plot of gain vs. fn, the achievable gain is 1.41 at the minimum frequency, 60kHz, thus it exceeds the 1.25 gain requirement. If the peak gain exceeds the gain requirement, increase h to decrease $L_{r..}$ The Lr loss and size decreases accordingly, and increase C_r to lower the voltage stress on the resonant capacitor.

As long as the inductance ratio h is defined, then calculate L_r using equation (7) and C_r using equation (1).

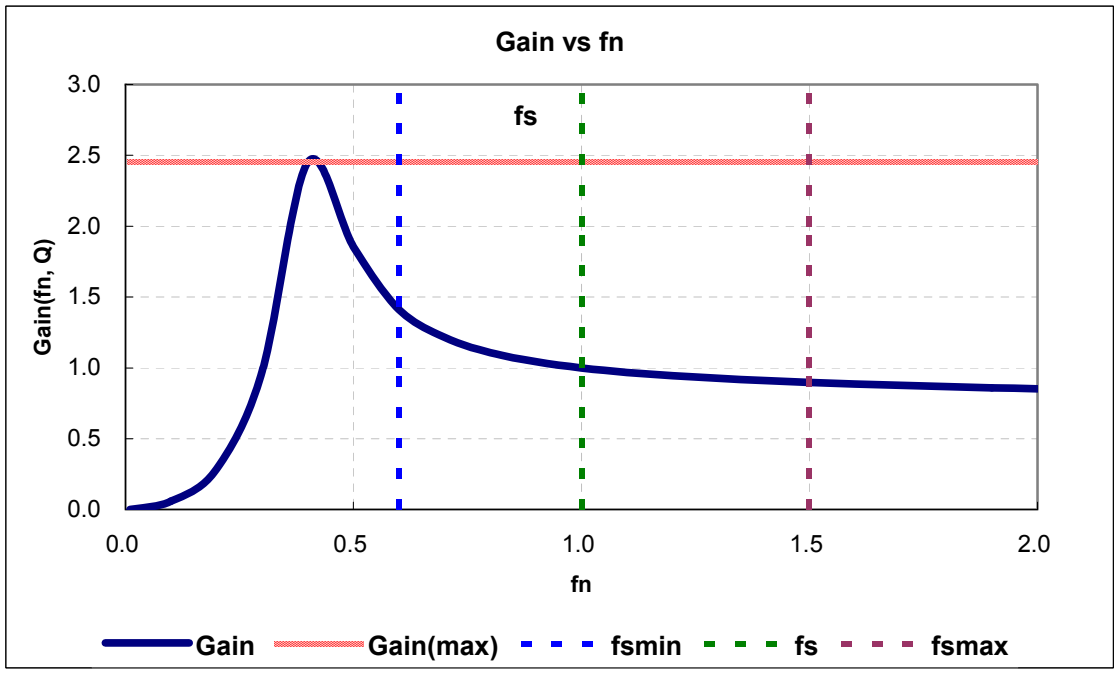


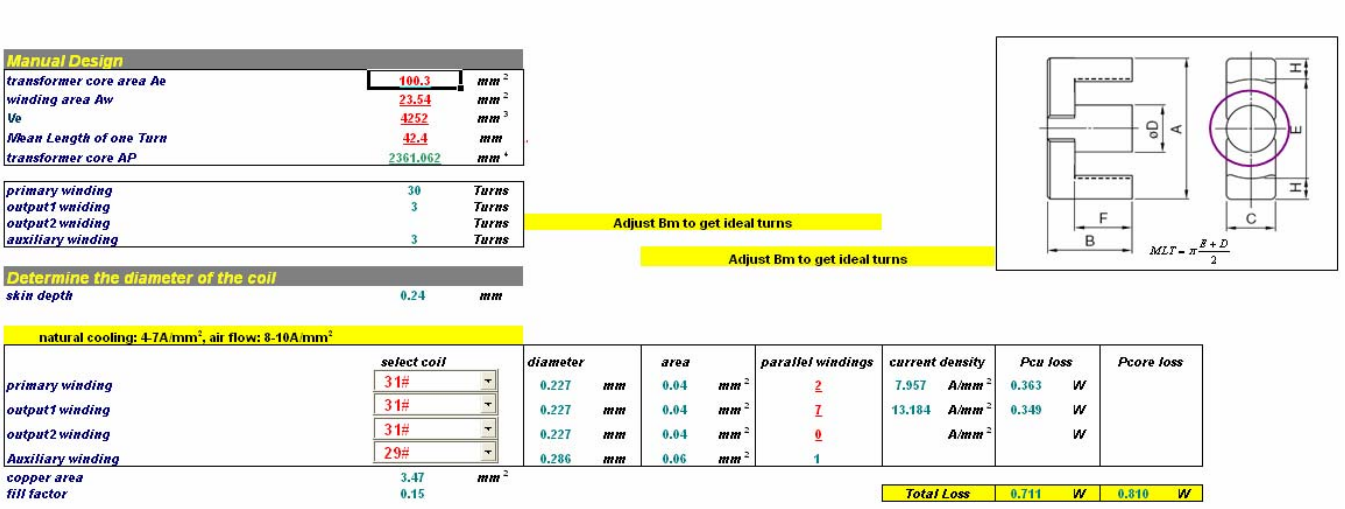
Figure 26: Gain vs. f_n with Fixed h and Q

4.4 Transformer Core and Winding Turns

The tool provides a transformer auto-design feature: The user selects the core shape, and the tool selects a suitable core for the specifications and calculates the number of windings. The user then determines the diameter of the windings, and the tool calculates the fill factor. The tool also calculates the winding loss and core loss.

If the winding loss far exceeds the core loss, using a larger winding area reduces the winding loss. To keep the same fill factor, the user must increase the flux density (B_m) to reduce the number of turns. Adjust B_m to balance the winding loss against the core loss to optimize transformer design.

The tool also allows for manual design. The user determines which core to use and then input A_e and A_w. This tool calculates the number of turns, and the user determines the diameter of the windings. The tool calculates the fill factor and the winding and core losses. Here show the transformer design based on manual design.



Manual Design		
transformer core area Ae	100.3	mm^2
winding area Aw	23.54	mm^2
Ve	4252	mm^3
Mean Length of one Turn	42.4	mm
transformer core AP	2361.062	mm^4

primary winding	30	Turns
output1 winding	3	Turns
output2 winding		Turns
auxiliary winding	3	Turns

Adjust Bm to get ideal turns

Adjust Bm to get ideal turns

Determine the diameter of the coil

skin depth 0.24 mm

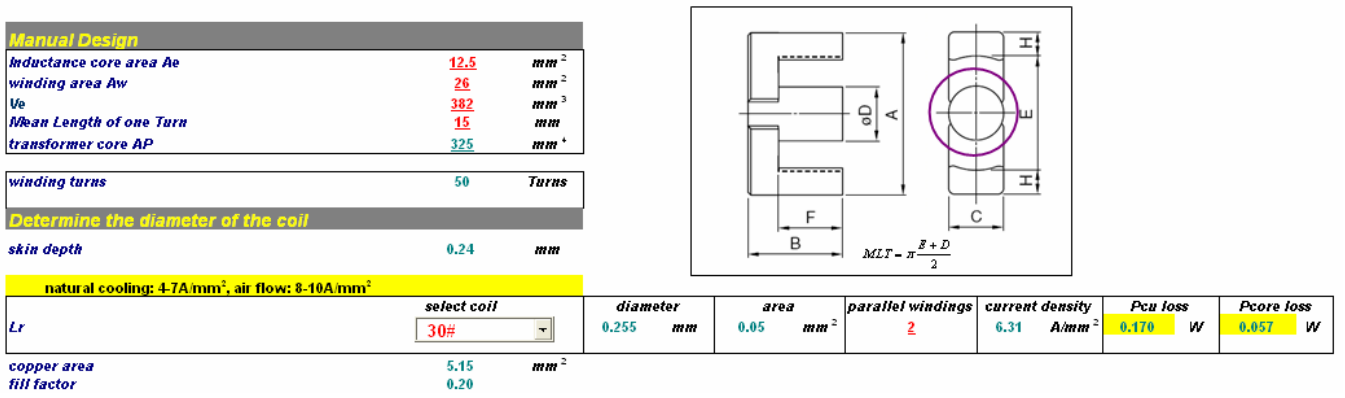
natural cooling: 4-7A/mm^2, air flow: 8-10A/mm^2

	select coil	diameter		area		parallel windings	current density		Pcu loss		Pcore loss
primary winding	31#	0.227	mm	0.04	mm^2	2	7.957	A/mm^2	0.363	W	
output1 winding	31#	0.227	mm	0.04	mm^2	7	13.184	A/mm^2	0.349	W	
output2 winding	31#	0.227	mm	0.04	mm^2	0		A/mm^2		W	
Auxiliary winding	29#	0.286	mm	0.06	mm^2	1					
copper area	3.47	mm^2					Total Loss		0.711	W	0.810 W
fill factor	0.15										

4.5 Resonant Inductor Core and Winding Turns

The tool can automatically design a resonant inductor. The user selects the core shape, and the tool auto-selects a suitable core for the specifications and calculate the number of windings. The user needs to determine the diameter of the windings. The tool calculates the fill factor; if the fill factor exceeds 0.3, the user must choose a larger core to accommodate the windings. The tool also calculates the winding loss and core loss. But it is not shown here.

This tool also provides a manual design tool for inductor, just shown as follows.



Manual Design		
Inductance core area Ae	12.5	mm^2
winding area Aw	26	mm^2
Ve	382	mm^3
Mean Length of one Turn	15	mm
transformer core AP	325	mm^4

winding turns	50 Turns

Determine the diameter of the coil

skin depth 0.24 mm

natural cooling: 4-7A/mm^2, air flow: 8-10A/mm^2

	select coil	diameter		area		parallel windings	current density		Pcu loss		Pcore loss	
Lr	30#	0.255	mm	0.05	mm^2	2	6.31	A/mm^2	0.170	W	0.057	W
copper area	5.15	mm^2										
fill factor	0.20											

4.6 Control Circuit Design

The tool can calculate the control parameters, given the following user inputs:

- fstart: start frequency,
- fs_min: minimum switching frequency,
- fs_max: maximum frequency.

Select a minimum frequency range that not only guarantees inductive operation mode but also meets the gain requirement. To guarantee inductive operation mode, select an fs_min larger than f_r—the resonant frequency between the Cr and Lr+Lm in series—and below f_{min} as defined as:

$$f_{min} = f_r \sqrt{\frac{1}{1+h(1-\frac{1}{M_{max}})}} \quad (54)$$

Where M_{max} is:

$$M_{max} = \frac{NV_O}{Vin\_dc\_min/2} \quad (55)$$

At no-load condition, the converter will regulate to the maximum frequency,

$$f_{max} = f_r \sqrt{\frac{1}{1+h(1-\frac{1}{M_{min}})}} \quad (56)$$

Start Frequency	fstart	280	kHz	
Timing Capacitence	CT	470	pF	fstart should be less than 3*fs !
Minimum Switching Frequency	fs_min	60	kHz	fs_min suggeted range: 33.02 kHz ≤fs_min≤ 58 kHz !
Maximum Switching Frequency	fs_max	190	kHz	fs_max is suggeted less than 248 kHz !
fs_min Set Resistor	Rfmin	12	kohm	
fs_max Set Resistor	Rfmax	2	kohm	
Softstart Resistence	Rss	3.3	kohm	
Softstart Capacitence	Css	2.2	uF	
Highside Divider Reisistor	RH	4.7	Mohm	
lowside Divider Resistor	RL	18	kohm	

○ Current sensing technique with sense resistor				
Current Sensing Resistor	Rs	2.2	ohm	
◉ Lossless current sensing rechnique with capacitive shunt				
Shunt Capacitor CA	CA	100	pF	CA is suggested less than 240 pF !
RA	RA	100	ohm	
CB	CB	470	nF	
Current Sensing Resistor	RB	360	ohm	

Generate the parameters check list

System Spec

Minimum DC Voltage	320	V		
Normal DC Voltage	390	V		
Maximum DC Voltage	400	V		
Higher Resonant Frequency	100	kHz		
Coss	180	pF		
	Vo		Io	
Output1	19.2	V	4.7	A
Output2	0	V	0	A
Estimate Efficiency	.93	%		
Total Output Power	90.24	W		
Iutput Power	97.03	W		

Control Circuit Design

Start Frequency	280	kHz
CT	470	pF
fs_min	60	kHz
fs_max	190	kHz
fs_min Set Resistor	12	kohm
fs_max Set Resistor	2	kohm
Softstart Resistor	3.3	kohm
Softstart Capacitence	2.2	uF
Highside Divider Resistor	2	Mohm
Lowside Divider Resistor	16	kohm
Resonant Inductance	100	uH
Resonant Capacitance	24	nF

Transformer

Tranformer Core Area Ae		100.3	mm^2			
Tranformer Winding Area Aw		23.54	mm^2			
Ve		4252	mm^3			
Primary inductance		900	uH			
	Turns		Coil Diameter			Parallel Windings
Primary Winding	30		.227	mm	X	2
Output1 Winding	3		.227	mm	X	7
Output2 Winding			.227	mm	X	0
Auxiliary Winding	3		.286	mm	X	1

Resonant Inductance Lr

Lr Core Area Ae		12.5	mm^2			
Lr Winding Area Aw		26	mm^2			
Ve		382	mm^3			
Lr inductance		100	uH			
	Turns		Coil Diameter			Parallel Windings
Lr Winding	50		.255	mm	X	2

4.7 Transformer and Inductor Design

The transformer used in this design has a turns ratio of 31:3:3:3 (N1:N2:N3:N4) with 850uH primary inductance. The core selected is EC26B.

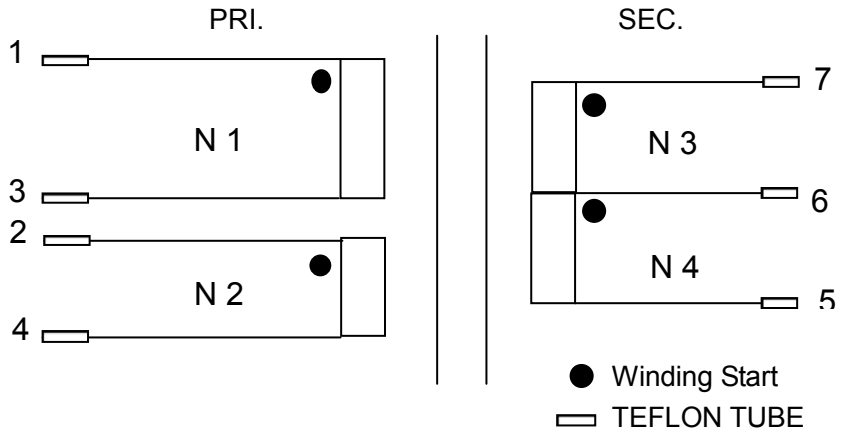


Figure 27: Transformer Connection Diagram

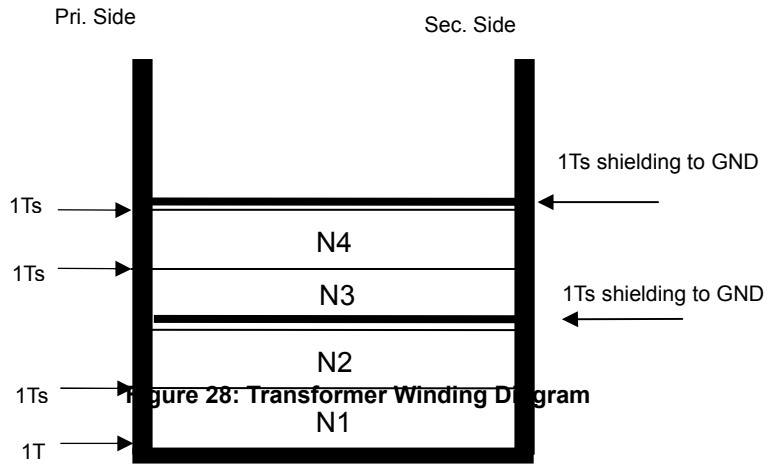


Figure 28: Winding Diagram

Table 2: Transformer Winding Order

Tape(T)	Winding	Terminal (start-end)	Wire size (φ)	Turns (T)
1	N1	1→3	0.23mm*2	31
1	N2	2→4	0.3mm*1	3
1				

	Shielding to GND			
1	N3	5→6	0.23mm*7 3 layers insulated wire	3
	N4	6→7	0.23mm*7 3 layers insulated wire	3
	Shielding to GND			
1				

The resonant inductor used in this design has a turn of 50 with 100uH inductance. The core selected is EPC13.

Table 3: Inductor Winding Order

Tape(T)	Winding	Terminal (start-end)	Wire size (φ)	Turns (T)
1	N1	5→6	0.25mm*2	50

4.8 Evaluation Board for 90W Slim Adapter

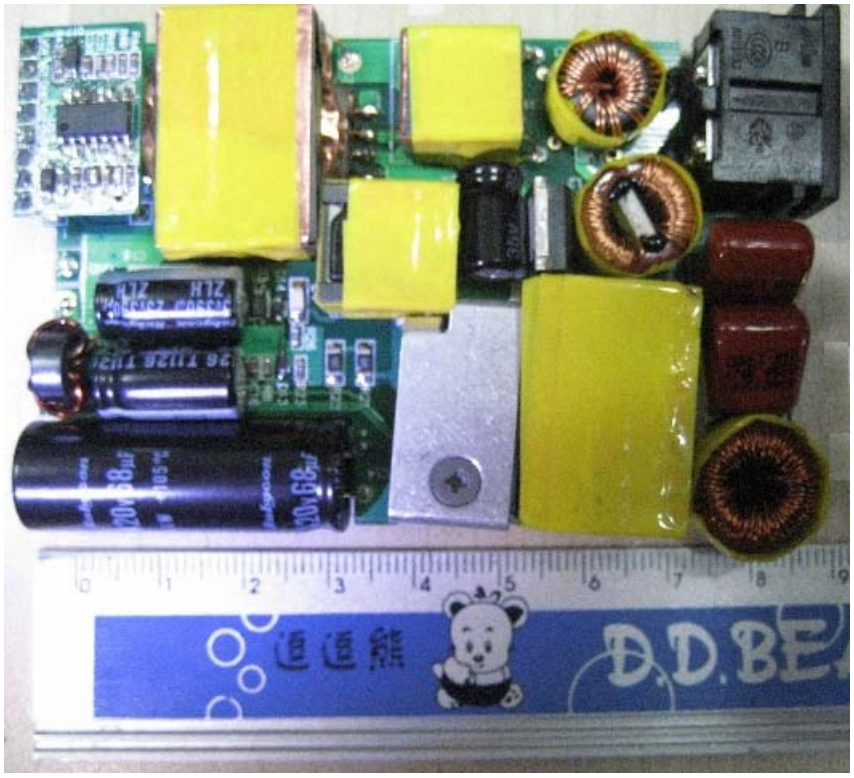


Figure 29: EV44010-S+HR1000-S-01B: 90W Slim Adapter

Based on the above design, an evaluation board for 90W slim adapter is made as shown in Figure 29.For more detailed information of this evaluation board, please refer to the EV44010-S+HR1000-S-01B Datasheet[iv].

5. EXPERIMENTAL VERIFICATION

5.1 Efficiency

Table 4 and Table 5 show measured AC input power and output voltage at nominal mains with different

load conditions. Then the efficiency is calculated.

Table 4: Efficiency Measurement vs. Load at 115VAC

	Vout(V)	Iout(A)	Po(W)	Pin(W)	Efficiency(%)
Full load	18.93	4.7513	89.94	99.55	90.34
3/4 load	18.95	3.965	75.14	82.95	90.57
1/2 load	18.99	2.3844	45.28	50.17	90.24
1/4 load	19.01	1.2013	22.84	26.27	86.92

Table 5: Efficiency measurement VS load at 230Vac

	Vout(V)	Iout(A)	Po(W)	Pin(W)	Efficiency(%)
Full load	19.03	4.7513	90.42	97.37	92.86
3/4 load	18.97	3.9650	75.22	81.52	92.26
1/2 load	19.00	2.3838	45.29	49.31	91.84
1/4 load	19.03	1.2000	22.84	25.95	88.01

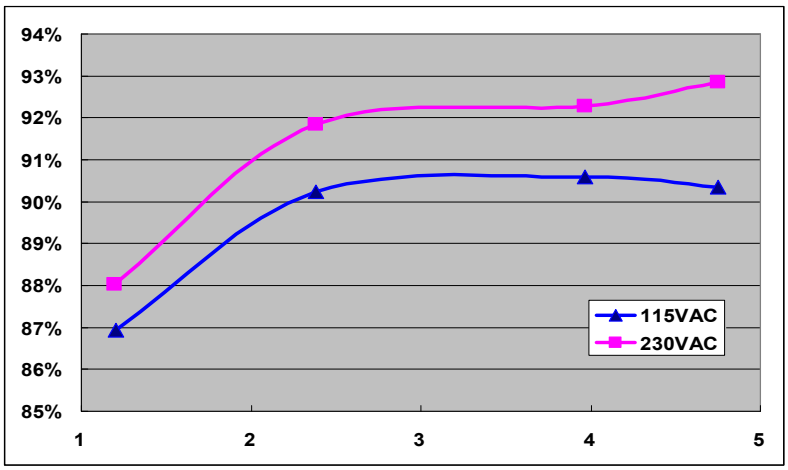


Figure 30: Efficiency Curve vs. Load

The measured efficiency at low AC input is shown in Table 6, which is also quite good.

Table 6: Efficiency Measurement at Low Line

Vac	Vout(V)	Iout(A)	Po(W)	Pin(W)	Efficiency(%)
90Vac	18.91	4.7075	89.02	100.4	88.64
100Vac	18.91	4.7075	89.02	99.61	89.36

5.2 Startup Operation

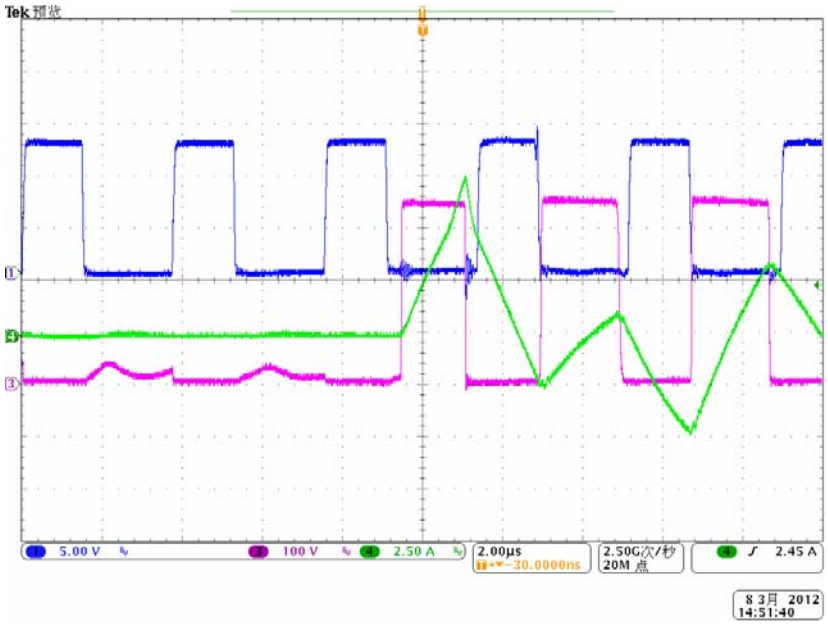


Figure 31: Start-Up Current Waveform

Ch1: Low-Side Driver

Ch3: SW

Ch4: Primary-Side Resonant Current

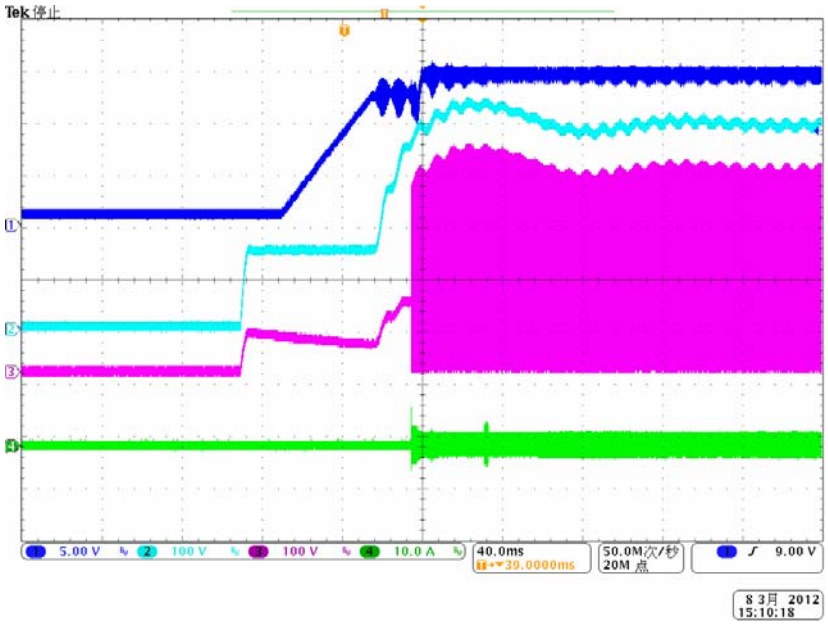


Figure 32: VCC, PFC Output Voltage Waveform at Start-Up

Ch1: VCC

Ch2: PFC Output Voltage

Ch3: SW

Ch4: Primary-Side Resonant Current

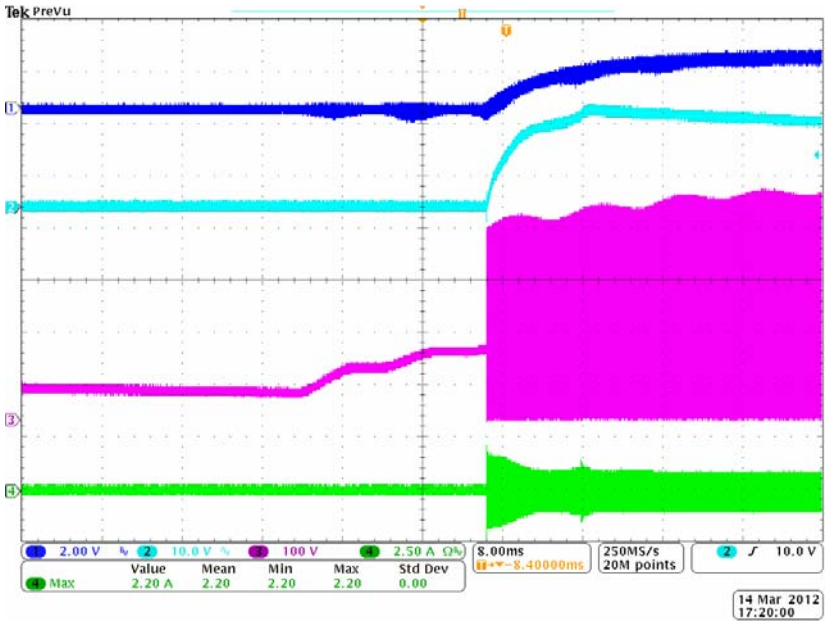


Figure 33: SS (Pin 1), Output Voltage Waveform at Start-Up

Ch1: SS (Pin 1)

Ch2: 19V Output Voltage

Ch3: SW

Ch4: Primary-Side Resonant Current

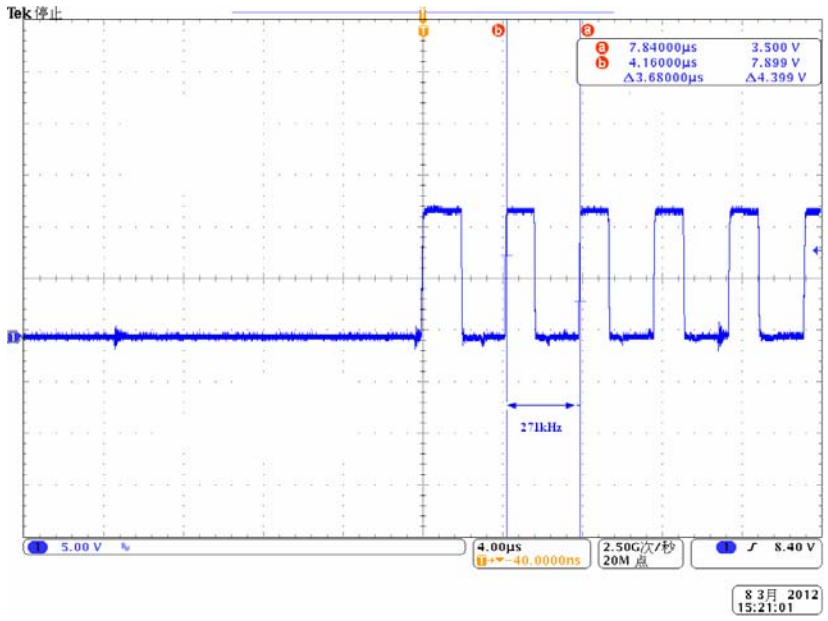


Figure 34: Start-Up Frequency, fstart, Waveform

Ch1: Low-Side Driver

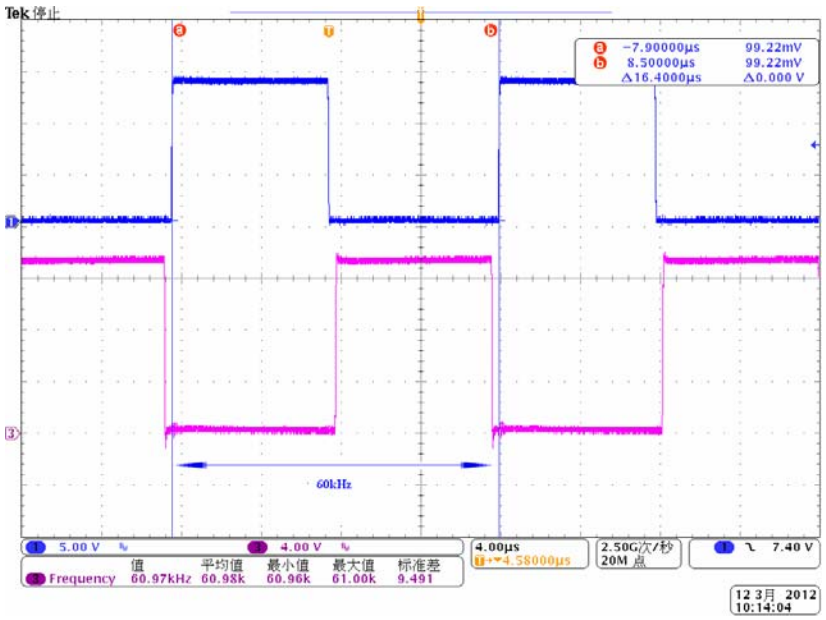


Figure35: Minimum Frequency, fmin, Waveform

Ch1: Low-Side Driver

Ch3: High-Side Driver

5.3 Steady-State Operation

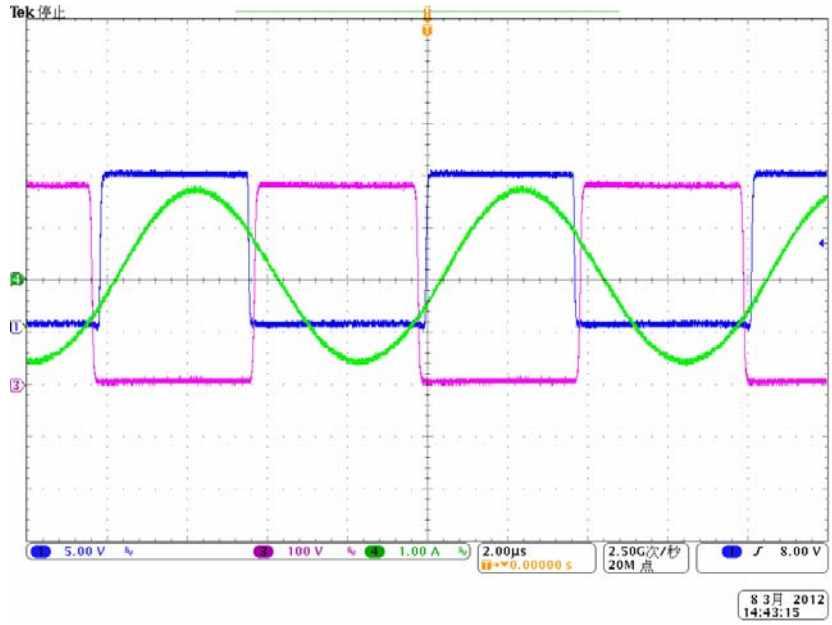


Figure 36: Steady-State Driver and Current Waveform

Ch1: Low-Side Driver

Ch3: SW

Ch4: Primary-Side Resonant Current

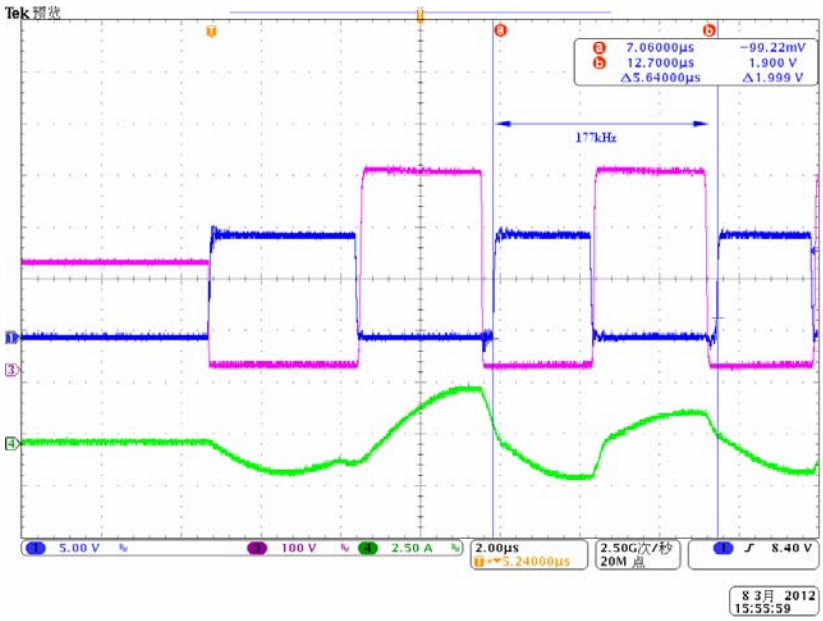


Figure 37: Maximum Frequency, fmax, at No-Load Condition

Ch1: Low-Side Driver

Ch3: SW

Ch4: Primary-Side Resonant Current

5.4 No-Load Operation

Test condition: Vac=115VAC, Vo=19.2V, Po=0W

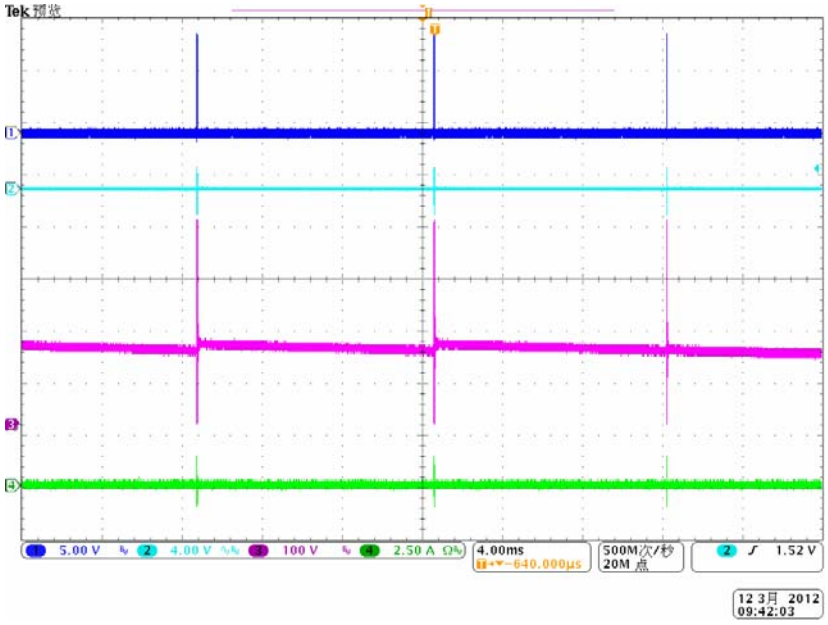


Figure 38: Output Voltage Ripple at No-Load Condition

Ch1: Low-Side Driver

Ch2: Output Voltage Ripple

Ch3: SW

Ch4: Primary-Side Resonant Current

5.5 Transient

Test condition: Vac=115VAC, Vo=19.2V, Io=0A-4.7A

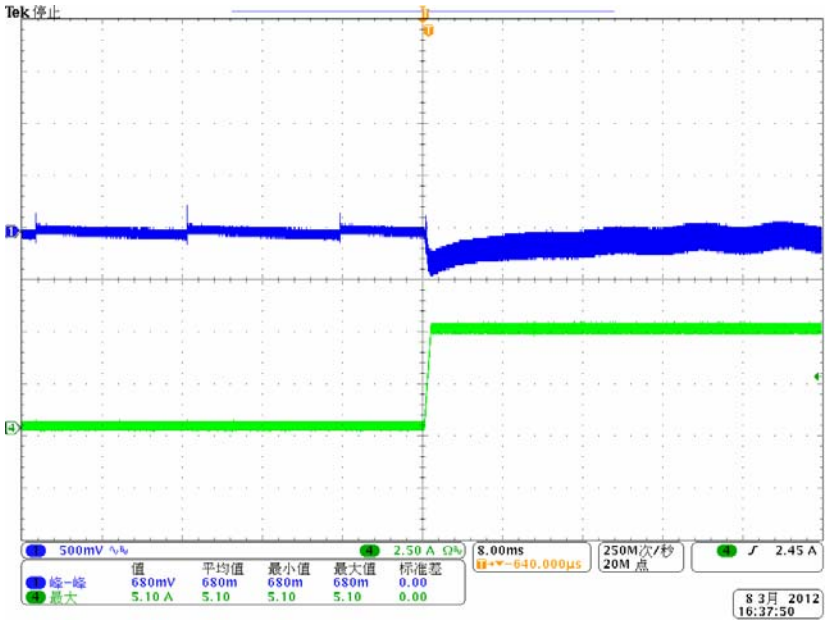


Figure 39: Transient from No-Load to Full-Load

Ch2: Output Voltage Ripple

Ch4: Output Current

5.6 Short-Circuit Protection

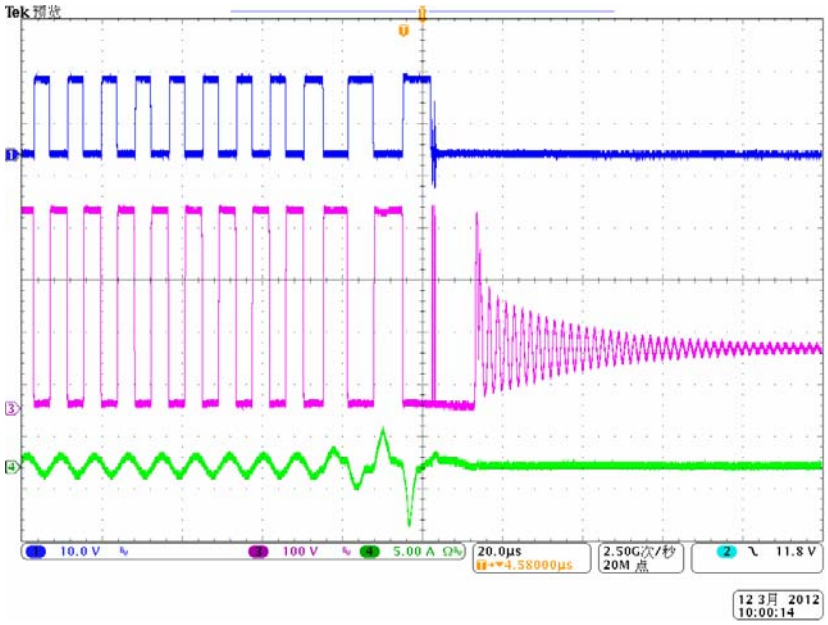


Figure 40: Resonant Current at Short-Circuit

Ch1: Low-Side Driver

Ch3: SW

Ch4: Primary-Side Resonant Current

5.7 Over-Load Protection

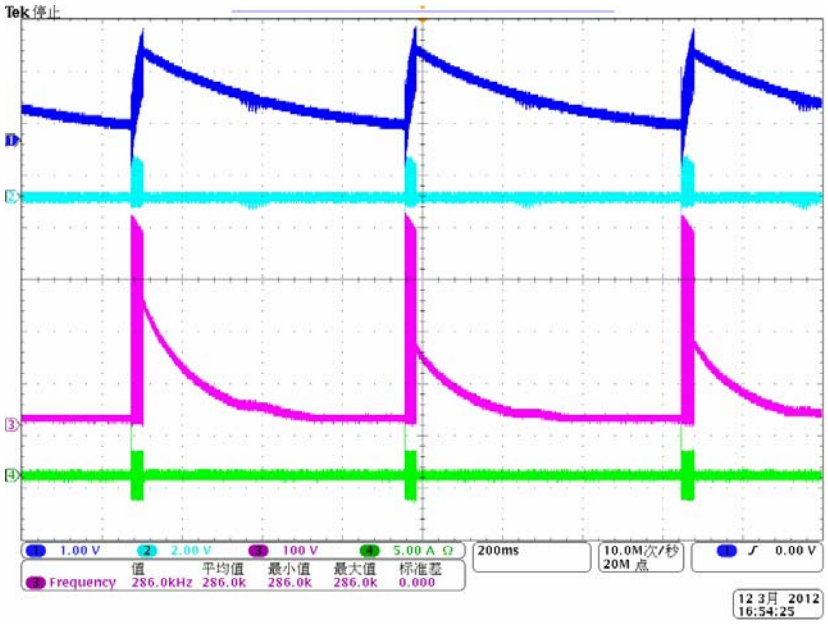


Figure 41: Timer (Pin 2), CS (Pin 6) Waveform at Overload

Ch1: Timer (Pin 2)

Ch2: CS (Pin 6)

Ch3: SW

Ch4: Primary-Side Resonant Current

6. REFERENCES

[i] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," Power Electronics, IEEE Transactions on, vol. 3, pp. 174-182, 1988.

[ii] Dixon, Lloyd H. 1990. Magnetics Design for Switching Power Supplies. *Unitrode Magnetics Design Handbook*. (publisher location, publisher name)

[iii] HR1000 Design Assistant

[iv] EV44010-S+HR1000-S-01B Datasheet