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MOSFET Paralleling
(Parasitic Oscillation
between Parallel Power MOSFETs)

Outline:

This document describes the causes of and solutions for parasitic oscillation between parallel power MOSFETs.

Table of Contents

1. Parallel operation of MOSFETS

Since power MOSFETs are not susceptible to thermal runaway, it is generally easier to parallel multiple power MOSFETs than bipolar transistors.

MOSFETs are paralleled to increase the output current capability. Since MOSFETs switch at high frequencies, differences in their electrical characteristics and circuit stray inductances can cause transient voltage spikes and an imbalance in current sharing among paralleled MOSFETs. A current imbalance could cause excessive power loss and damage to the device.

The most important thing to remember when making parallel connections is to avoid current concentration, including during switching transitions, and to assure a well-balanced, uniform flow of current to all MOSFETs under all possible load conditions. Special care should be exercised as to:
   (1) Current imbalance caused by a mismatch in device characteristics (parallel operation)
   (2) Parasitic oscillation (parallel operation)

2. Current imbalance caused by a mismatch in device characteristics (parallel operation)

2.1. Current imbalance in steady-state operation

During non-switching periods, a current is distributed to parallel MOSFETs in inverse proportion to their on-resistance. The MOSFET with the lowest on-resistance will carry the highest current. The positive temperature coefficient of on-resistance naturally tends to compensate for a current imbalance and equalize the currents through each MOSFET.

It is therefore considered that parallel MOSFETs rarely suffer thermal breakdown in a steady state. The temperature coefficient for the voltage drop across a MOSFET body diode is not positive. Therefore, parallel MOSETs could have a large imbalance in the sharing of a steady-state current while their body diodes are in conduction. In reality, however, the temperature of a MOSFET rises as its body diode passes a current. As a result, its on-resistance increases, reducing the current it is conducting. For this reason, an imbalance in steady-state current rarely poses a problem.

2.2. Current imbalance during switching transitions

Generally, a current imbalance appears during turn-on and turn-off switching transitions. This is caused by differences in switching time among parallel power MOSFETs. Variations in switching times are highly dependent on the value of the gate-source threshold voltage V_{th}. That is, the smaller the value of V_{th}, the faster the turn-on time; and the larger the value of V_{th}, the faster the turn-off time. Therefore, a current imbalance occurs during both turn-on and turn-off when a current concentrates in MOSFETs with a small V_{th}. This current imbalance can apply an excessive load to a device and result in a failure. For parallel connections, power MOSFETs with a close V_{th} are preferable in order to reduce variations in switching time during transient switching periods. MOSFETs with a high transconductance g_m also tend to switch faster.

In addition, the circuit wiring layout can be a cause of a current imbalance during switching transitions if parallel MOSFETs have different stray inductances in their interconnections. In particular, the source inductance affects the gate drive voltage. It is desirable to equalize the lengths of interconnections between parallel MOSFETs.

3. Parasitic oscillation (parallel operation)

3.1. Gate voltage oscillation caused by drain-source voltage oscillation

Surge voltage V_{Surge} occurs across the drain and source terminals of a MOSFET during switching, mainly due to the di/dt during turn-off and stray inductances in the drain terminal and wire leads.

$$V_{Surge} = L_d \text{ (stray inductances)} \times di/dt$$

The oscillating voltage caused by V_{Surge} passes to the gate via the drain-gate capacitance C_{gd} of a MOSFET, forming a resonant circuit with the stray inductance L of the gate wire.

High-current, high-speed MOSFETs have a very small internal gate resistance. Without an external gate resistor, the resonant circuit would have a large Q factor ($1/R \cdot \sqrt{L/C}$). If resonance occurs, the resonance circuit generates a large oscillating voltage across the gate and source terminals of the MOSFET, causing parasitic oscillation. Figure 3.1 shows an example of a circuit with parallel MOSFETs.

Unless the transient switching currents of the parallel MOSFETs are well balanced during turn-off, a current is unevenly distributed to the MOSFET that turns off later. This current causes a large voltage surge (oscillation) across its drain and source terminals, which in turn passes to the gate, causing an oscillating voltage to occur across the gate and source terminals. An excessive oscillating voltage could result in a gate-source overvoltage breakdown, a false turn-on, or an oscillation breakdown.

When the fastest MOSFET turns off, its drain voltage rises. The increase in the drain voltage passes to the gate terminal of the other MOSFET via the gate-drain capacitance C_{gd}, resulting in unintended behavior of the MOSFET, which leads to parasitic oscillation.

In addition, parallel MOSFETs share a common low-impedance path, which is also susceptible to parasitic oscillation.
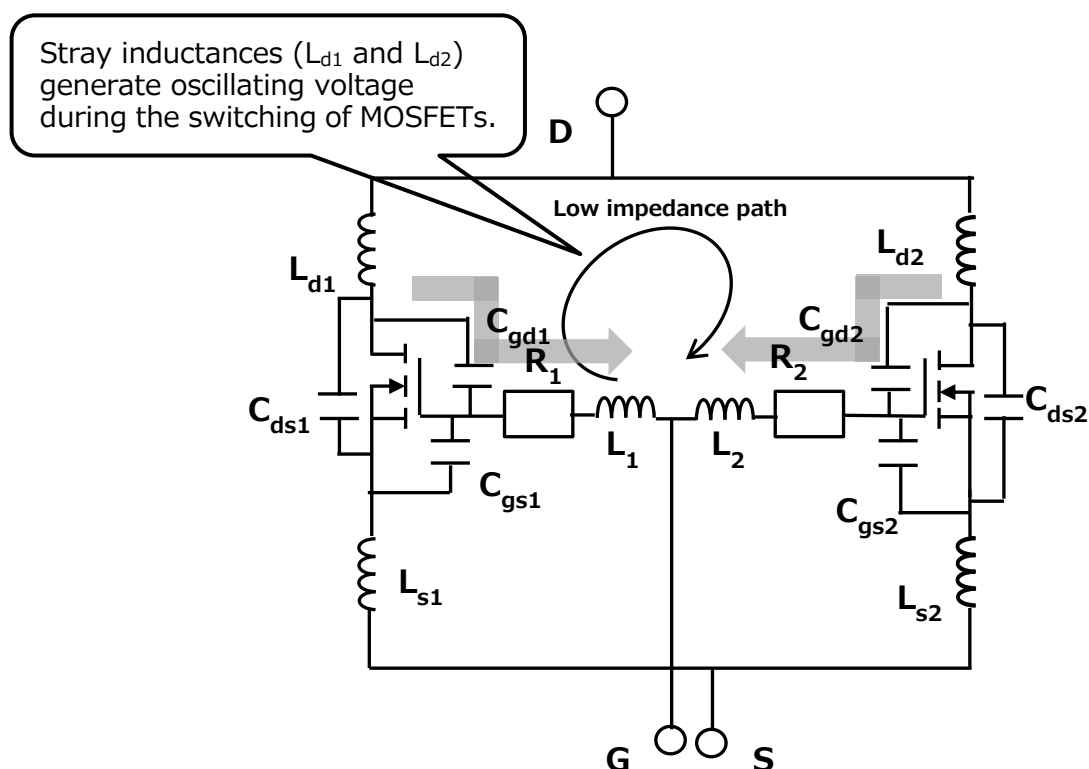

Stray inductances (L_{d1} and L_{d2}) generate oscillating voltage during the switching of MOSFETs.

Figure 3.1 Circuit with parallel MOSFETs

3.2. Parasitic oscillation of parallel MOSFETs

Generally, parallel MOSFETs are more susceptible to parasitic oscillation than a single MOSFET. Figure 3.2 shows a circuit with parallel MOSFETs. Figure 3.3 shows its equivalent circuit model at the parasitic oscillation frequency. In Figure 3.3, L_{d1} and L_{d2} are the stray inductances of the drain wires; L_{s1} and L_{s2} are the stray inductances of the source wires; and L_1 and L_2 are the stray inductances of the gate wires, bonding wires and other wires. C_{ds1}, C_{gd1}, C_{gs1}, C_{ds2}, C_{gd2} and C_{gs2} are capacitances of the MOSFETs.

Suppose that, in Figure 3.3, the parallel MOSFETs, Q_1 and Q_2, have equal inductance and capacitance values ($L_{s1}=L_{s2}$, $L_1=L_2$, $L_{d1}=L_{d2}$, $C_{ds1}=C_{ds2}$, $C_{gd1}=C_{gd2}$, and $C_{gs1}=C_{gs2}$). Then, Q_1 and Q_2 operate in opposite phases when they go into parasitic oscillation in the linear region. In this case, since the voltage along the dashed line is considered to be zero at the parasitic oscillation frequency it can be viewed as a virtual ground. Therefore, at the parasitic oscillation frequency, A and B can be considered to be short-circuited together. This means that parasitic oscillation occurs regardless of a drain-source load, a freewheel diode, a power supply, a common gate resistor and a gate drive circuit, as shown in Figure 3.4.
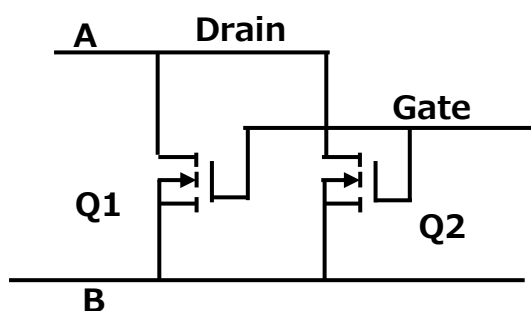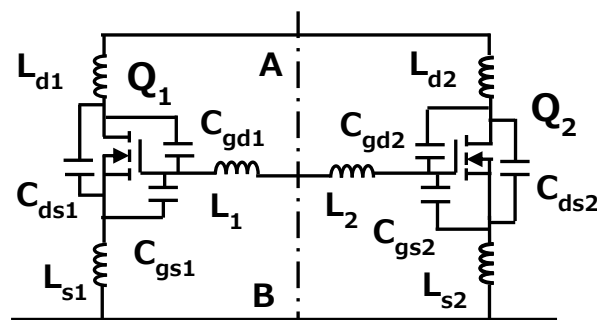

Figure 3.2 Parallel MOSFETs

Figure 3.3 Equivalent circuit at the parasitic oscillation frequency

As an equivalent circuit of the parasitic oscillation loop, it suffices to consider half of the circuit of Figure 3.4, which is shown in Figure 3.5. In Figure 3.5, L_d and L_s normally have the relationship $L_d << L_s$. Therefore, at the frequency of oscillation, the equivalent circuit model can be simplified as shown in Figure 3.6. In Figure 3.6, C_{gd} and L form a parallel resonant circuit.

Furthermore, at a frequency slightly below the resonant frequency, this resonant circuit can be equivalently replaced by the inductance L_x as shown in Figure 3.7. (The assumption is that L_d is smaller than L and that L_s is high enough to block the oscillation frequency.)

The circuit shown in Figure 3.7 is a Colpitts oscillator (see Section 3.4, "Colpitts oscillators"). As described above, since A and B in Figure 3.3 are equivalently short-circuited together, all the devices and loads around the MOSFETs can be ignored (Figure 3.4). In other words, the on-resistance of the freewheel diode and series resistors such as the equivalent series resistors of the capacitors can be ignored. Consequently, parallel MOSFETs form a resonant circuit with a high Q factor, which is highly susceptible to oscillation because of a high-gain feedback loop.
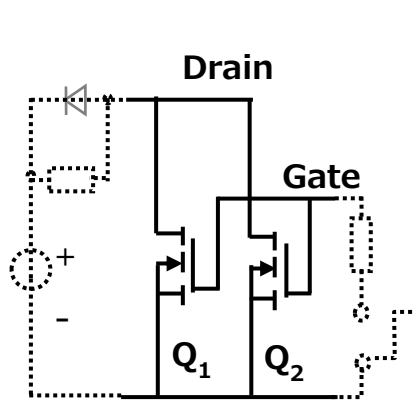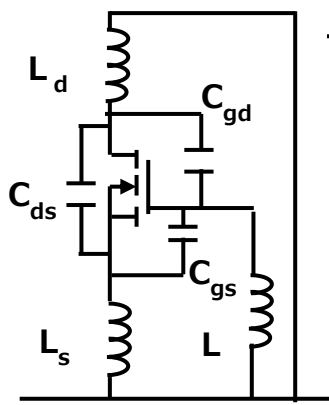
Figure 3.4
Parallel MOSFETs

Figure 3.5
Equivalent circuit model for parasitic oscillation
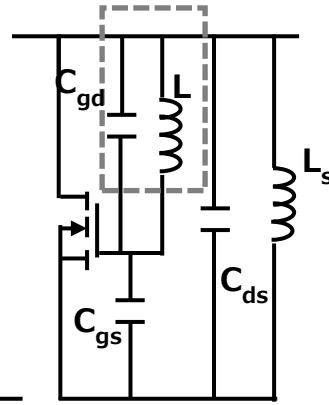
Figure 3.6
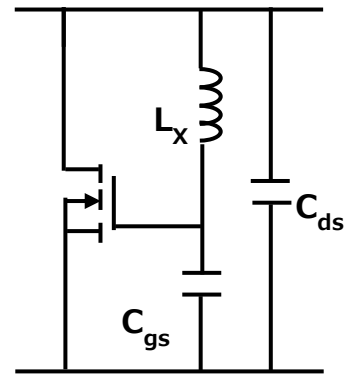**Transformation of the equivalent circuit**

Figure 3.7
Colpitts oscillator

3.2.1. Preventing parasitic oscillation of parallel MOSFETs

The circuit shown in Figure 3.7 forms a feedback circuit consisting of a parasitic inductance and the parasitic capacitances of the resonant circuit, depending on its frequency. This circuit goes into parasitic oscillation when the loop gain is equal to or greater than 1. When the following equation is met, the loop gain becomes one or greater:

$$g_m \cdot R \cdot C_{ds}/C_{gs} > 1 \qquad (1)$$

(1) ($C_{ds}=C_1$, $C_{gs}=C_3$. See Figure 3.19 in Section 3.4, "Colpitts oscillator.")

Therefore, the following must be met **to prevent parasitic oscillation**:

$$\mathbf{R \cdot g_m \cdot C_{ds} / C_{gs} < 1}$$

· Selection of MOSFETs

(a) Select MOSFETs with low C_{ds} / C_{gs}.

(b) Select MOSFETs with low g_m.

· Prevention of parasitic oscillation using an external circuit

(a) Insert either a gate resistor R_1 or a ferrite bead for the gate of each MOSFET as shown in Figure 3.8.

This is equivalent to adding a series resistor R_1 to the gate stray inductance L_1 in the equivalent circuit model for parallel MOSFETs shown in Figure 3.9. The purpose of this is to reduce the Q factor of a resonant circuit in order to reduce the gain of the positive feedback loop. Note, however, that R_1 affects the switching speed of the MOSFETs and that the increased resistance causes a switching loss to increase.
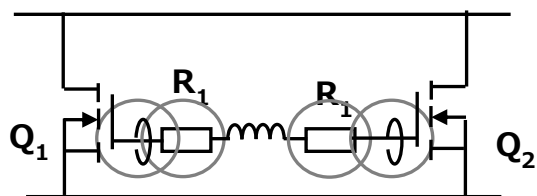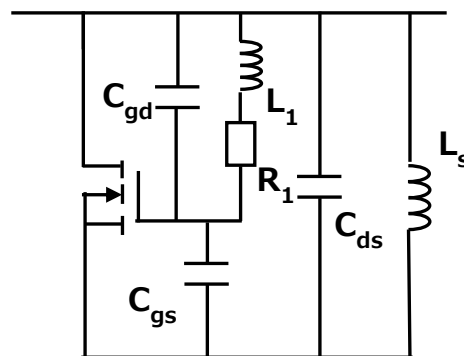

Figure 3.8 Parallel MOSFETs

Figure 3.9 Parallel MOSFETs

(b) Add a ceramic capacitor C between the gate and source terminals of the MOSFET as shown in Figure 3.10. In effect, this ceramic capacitor decreases C_{ds} / C_{gs}. However, C degrades the switching performance of the MOSFET. The equivalent circuit shown in Figure 3.11 can be transformed as shown in Figure 3.12. In cases where the drain stray inductance L_d is lower than the source stray inductance L_s, C is not added to C_{gs}, but to C_{gd} as shown in Figure 3.12. Care should be exercised when adding a capacitor between the gate and source terminals because it often produces a contrary effect.
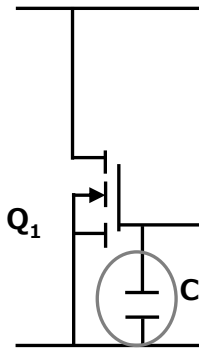
**Figure 3.10
Capacitor between
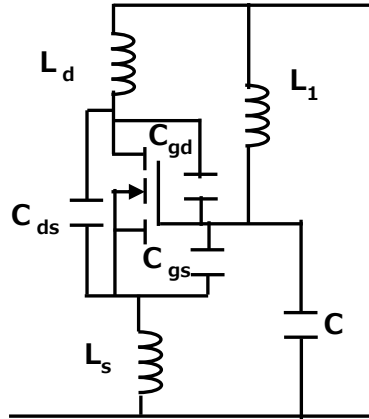the gate and source terminals**
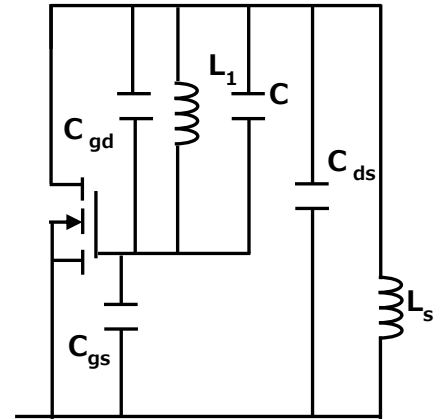
**Figure 3.11
Equivalent circuit**

**Figure 3.12 Adverse effect
produced when L$_d$<<L$_s$**
(L$_d$ is ignored because it is very smaller than L$_s$.)

3.3. Supplemental explanation
3.3.1. Parallel resonant circuit

The parallel LC circuit shown in Figure 3.13 has a resonant frequency f_o of $1/2\pi\sqrt{(LC)}$. As shown in Figure 3.14, the circuit is inductive at frequencies lower than f_o and is capacitive at frequencies higher than f_o.

When the circuit is inductive, it is equivalently considered to be an inductor. When the circuit is capacitive, it is equivalently considered to be a capacitor.

$$f_o=1/2\pi\sqrt{(LC)}$$

Figure 3.13 Parallel resonant circuits

Figure 3.14 Impedance versus frequency
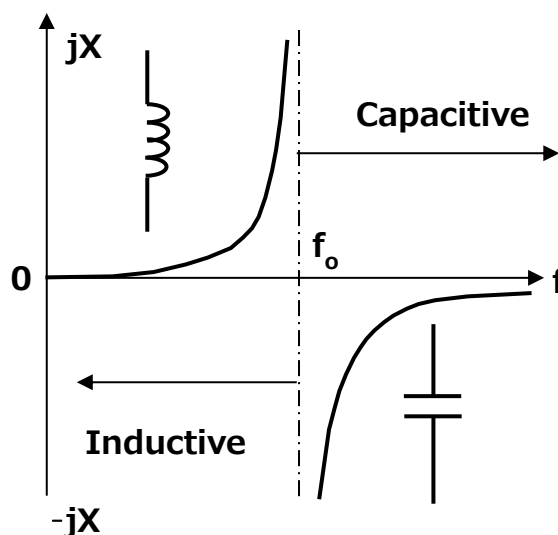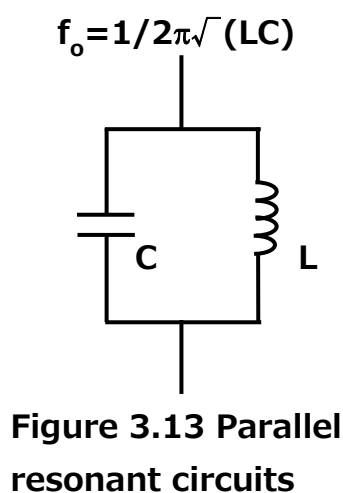
3.3.2. Oscillation

Oscillation is a phenomenon whereby an electronic circuit causes vibration on its own without receiving vibration energy from an external source. In reality, since a circuit has electrical resistance, oscillations decay with time unless the lost energy is supplied to the circuit. The conditions for oscillation are:

(1) Phase condition
The feedback signal from the output to the input is in phase with the input signal at the oscillation frequency. (Positive feedback loop)

(2) Amplitude condition
The loss caused by passive elements in a circuit is lower than the gain obtained by an amplifier.

Oscillation occurs when a circuit has a positive feedback and provides a gain that compensates for a loss.

The gain G of the feedback circuit shown in Figure 3.15 is calculated as:

$$G=v_o/v_i=A/(1-AH) \qquad (2)$$

where, v_i = input voltage, v_o = output voltage, A = loop gain, and H: feedback factor
v_1 = Input voltage applied to the amplifier, v_2 = feedback voltage

This circuit has a positive feedback loop when AH is positive, and a negative feedback loop when AH is negative.

The circuit becomes unstable and oscillates when it has a positive feedback loop and a gain (AH) of 1 or greater.
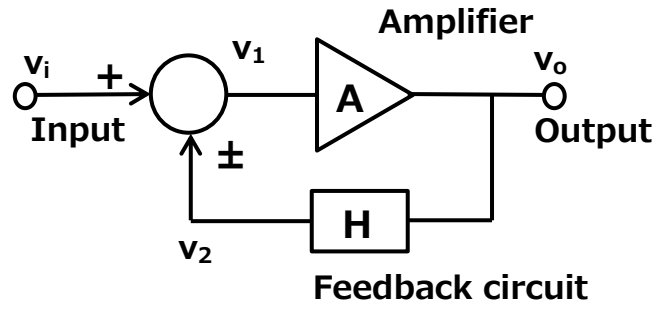

Figure 3.15 Feedback circuit

3.3.3. MOSFET oscillation

Power MOSFETs have a large transconductance g_m and parasitic capacitances. Therefore, wire and other stray inductances (inductances between the gate, source, and drain circuits and in the associated interconnects) could form a positive feedback circuit, causing parasitic oscillation.

When power MOSFETs are in the steady on or off state, parasitic oscillation does not occur because their transconductance g_m becomes zero or negligibly small. Parasitic oscillation could occur while the load is short-circuited or during transient switching periods when g_m becomes large.

· MOSFET feedback loop

Oscillation does not occur without a feedback loop. The following paragraphs discuss the conditions necessary for an oscillation to occur, using a circuit shown in Figure 3.16. Assuming that X_1 to X_3 are the ideal reactances, their losses can be ignored. Since current i is considered not to flow from the MOSFET to each reactance, the circuit shown in Figure 3.16 can be remodeled as shown in Figure 3.17.
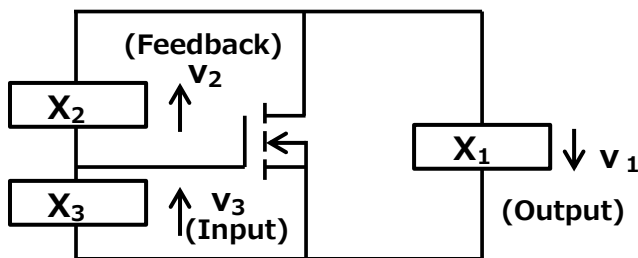

Figure 3.16 Schematic of an oscillation model

Figure 3.17 Current flowing through the oscillation circuit

According to Kirchhoff's circuit laws,

$$v_1+v_2+v_3=i(X_1+X_2+X_3)=0$$

Here, $i \neq 0$.

Hence, $X_1+X_2+X_3=0$

There is a positive feedback loop when the circuit is oscillating. This means that v_3 (input) is in phase with v_1 (output). Therefore, X_3 and X_1 are reactances of the same property; X_2 is not.

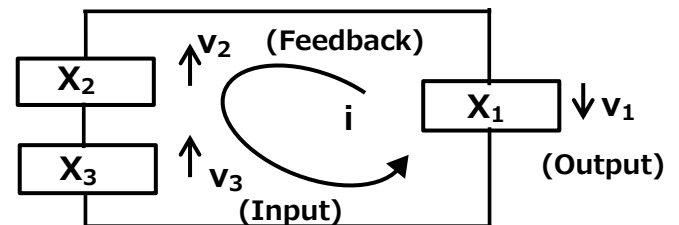Typical oscillators include Colpitts oscillators and Hartley oscillators.

3.4. Colpitts oscillators

Figure 3.18 shows basic Colpitts oscillators.

The equivalent circuit model of Colpitts oscillators is shown in Figure 3.19. Its oscillation frequency and the gain ($g_m \cdot r_d$) necessary to sustain oscillation can be determined by calculating a loop gain. Since the gate current is zero, the wire from v_2 to v_1 can be ignored.
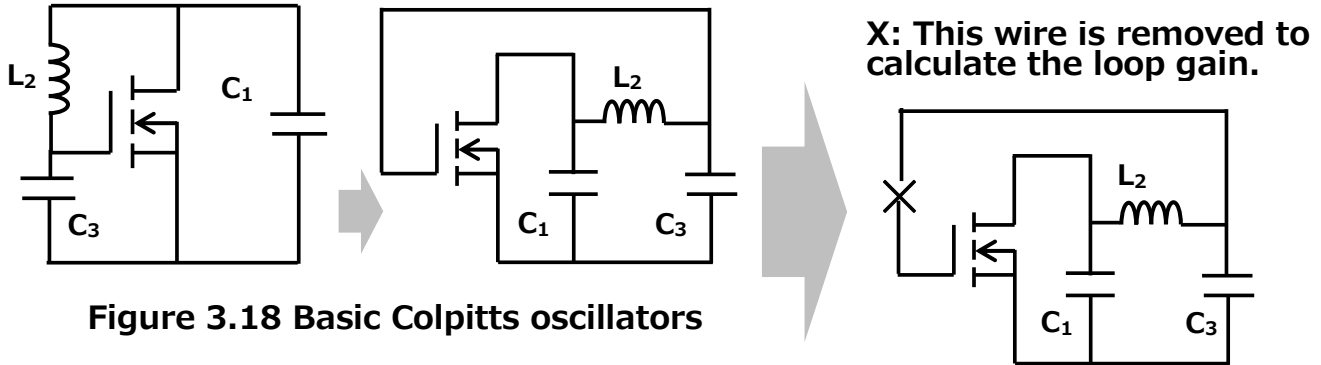

Figure 3.18 Basic Colpitts oscillators

X: This wire is removed to calculate the loop gain.

$$v_2 = (-g_m \cdot v_1)\frac{1}{\frac{1}{r_d} + j\omega C_1 + \frac{1}{j\omega L_2 + \frac{1}{j\omega C_3}}} \times \frac{\frac{1}{j\omega C_3}}{j\omega L_2 + \frac{1}{j\omega C_3}}$$

Figure 3.19 Equivalent circuit of a Colpitts oscillator

$$= (-g_m \cdot v_1)\frac{r_d}{1 - \omega^2 L_2 C_3 + j\omega(C_1 + C_3 - \omega^2 L_2 C_1 C_3)r_d}$$

$$AH = \frac{v_2}{v_1} = \frac{-g_m \cdot r_d}{1 - \omega^2 L_2 C_3 + j\omega(C_1 + C_3 - \omega^2 L_2 C_1 C_3)r_d} \qquad (6)$$
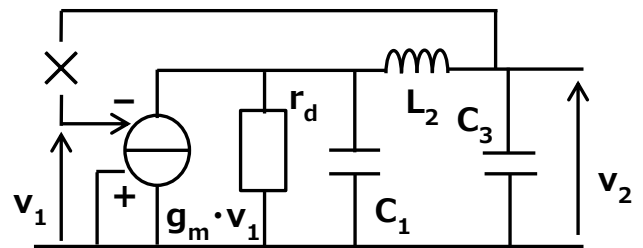
From the above equations, the oscillation frequency and the gain can be calculated as follows:
Oscillation frequency: Im(AH)=0

The circuit is most susceptible to oscillation at a frequency at which the phase of a signal that has looped around the circuit once is delayed by 0° or 360°. Hence,

$C_1 + C_3 - \omega^2 L_2 C_1 C_3 = 0$ (By dividing both sides of the equation by $j\omega C_1 j\omega C_3$, $1/j\omega C_1 + 1/j\omega C_2 + j\omega L_2 = 0$ is obtained.)

$$\omega^2 = \frac{C_1 + C_3}{L_2 C_1 C_3} \qquad (7) \qquad\qquad \omega = \sqrt{\frac{C_1 + C_3}{L_2 C_1 C_3}} \qquad (8)$$

Gain: Substituting Equation (7), $\omega^2 = (C_1 + C_2)/L_2 C_1 C_3$, into Re(AH)≥1:

$$\frac{-g_m \cdot r_d}{1 - \frac{C_1 + C_3}{L_2 C_1 C_3}L_2 C_3} = \frac{g_m \cdot r_d}{\frac{C_3}{C_1}} \geq 1 \qquad \therefore g_m \cdot r_d \geq \frac{C_3}{C_1} \qquad (9)$$

($g_m \cdot r_d$: Voltage loop gain)

4. Simulating and reducing oscillations of parallel MOSFETs

We simulated to find out how parasitic oscillation occurs between parallel MOSFETs and to work out solutions for parasitic oscillation.

Since the purpose of this simulation was to investigate the oscillation phenomenon, the actual component values to be used are different. The circuit was forced to oscillate in order to examine the phenomenon.

4.1. Current imbalance in parallel MOSFETs

As described in Section 2.1, "Current imbalance in steady-state operation," an imbalance in current sharing does not pose any problem to parallel MOSFETs in a steady state. This section discusses a current imbalance during switching transitions caused by differences in V_{th} among parallel MOSFETs.

The component values shown in Figure 4.1 are as follows:

L=250 µH, L_{d1}=20.5 µH, L_{d2}=20.5 µH, L_{s1}=20.5 µH, L_{s2}=20.5 µH, L_1=0 µH, L_2=0 µH, R_1=2 Ω, R_2=2 Ω, R_3=2 Ω
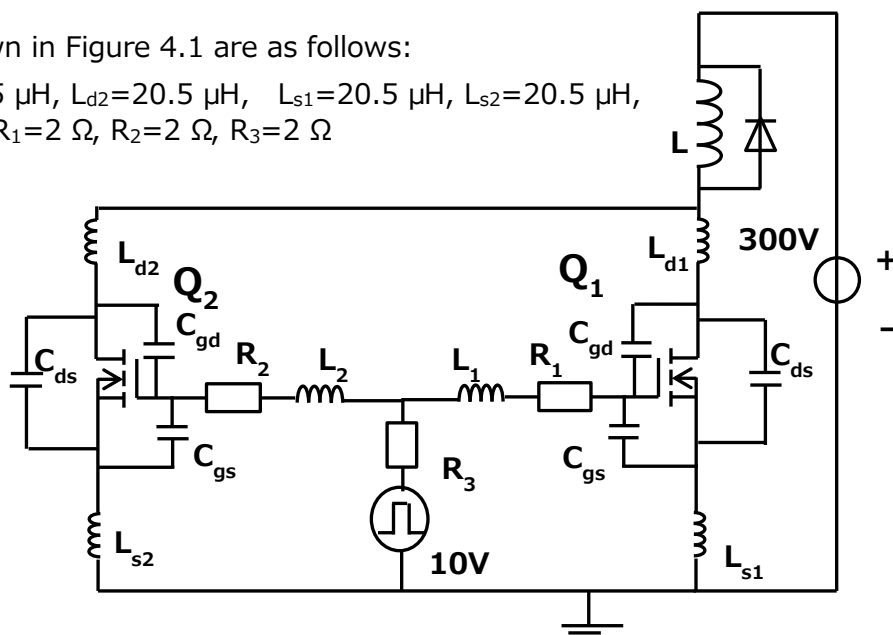

Figure 4.1 Equivalent circuit of parallel MOSFETs

① **When MOSFETs Q_1 and Q_2 have exactly the same electrical characteristics, including V_{th}**

The simulation results show no difference in the drain currents, drain-source voltages and gate voltages of Q_1 and Q_2.

② **When MOSFETs Q_1 and Q_2 have exactly the same electrical characteristics except V_{th}.**

The MOSFET with a lower V_{th} turns on first and most of the current flows until the other MOSFET turns on.

Conversely, the MOSFET with a higher V_{th} turns off first, and the other MOSFET shoulders all the current until it turns off.

Figure 4.2 shows the turn-on waveforms with a current imbalance during turn-on and Figure 4.3 shows the turn-off waveforms.

Since a current concentrates on the MOSFET with the lowest V_{th}, **it is important to use MOSFETs with the same or almost the same V_{th}** when paralleling many MOSFETs.
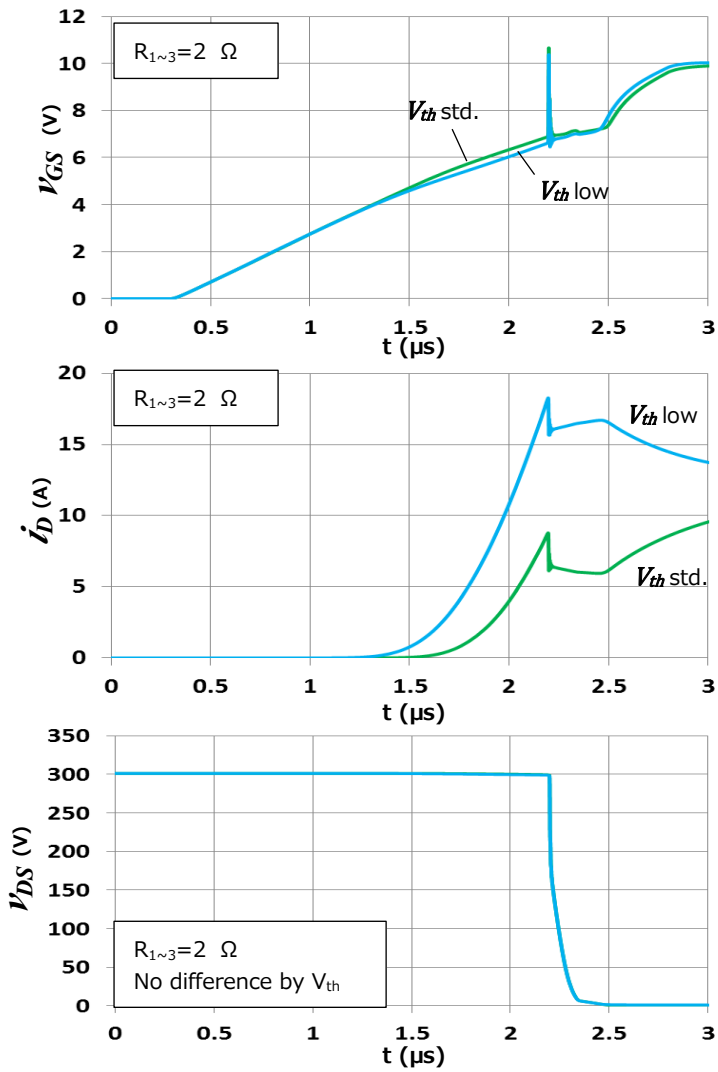
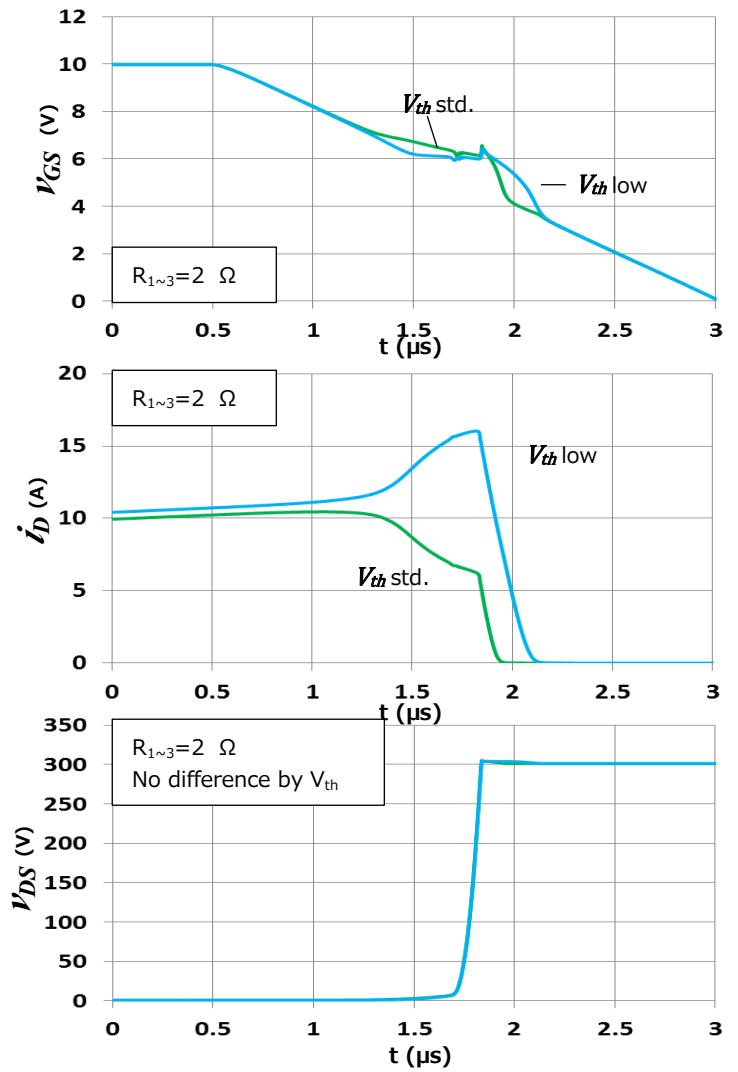**Figure 4.2 Current imbalances between parallel MOSFETs during turn-on**

Figure 4.3 Current imbalances between parallel MOSFETs during turn-off

4.2. Parasitic oscillation between parallel MOSFETs
4.2.1. Oscillation phenomenon

We simulated oscillation of: 1) a single MOSFET, 2) parallel MOSFETs with the same V_{th}, and 3) parallel MOSFETs with different V_{th} levels. The same current and voltage conditions were used for all simulations.

① **Single MOSFET operation**

In order to compare the operation of a single MOSFET with the operation of parallel MOSFETs, a circuit was intentionally programmed with inductance values that would cause the MOSFET to oscillate. Figure 4.6 shows the simulation results. The simulation conditions were:

$$L=500 \text{ μH}, L_d=20.5 \text{ μH}, L_s=20.5 \text{ μH}, L_0=0 \text{ μH}, R_0=0 \text{ Ω}$$

Oscillation occurs when L_s and L_d are relatively large and L_s is larger than L_d. The larger the L_s/L_d, the larger the oscillation amplitude.

② **Operation of parallel MOSFETs**

The circuit shown in Figure 4.5 was programmed with inductance values that provide the same conditions as for the simulation of a single MOSFET operation. For this simulation, we used a pair of MOSFETs with the same electrical characteristics. Figure 4.7 shows the simulation results. The waveforms obtained from the parallel MOSFETs were almost the same as those obtained from a single MOSFET. **As long as parallel MOSFETs had the same electrical characteristics and their interconnections were balanced, their operation did not show any notable difference from the operation of a single MOSFET.** In reality, however, MOSFETs have variations in their characteristics. Extreme care should be exercised as to MOSFET paralleling. The simulation conditions were:

$$L=250 \text{ μH}, L_{d1}=20.5 \text{ μH}, L_{d2}=20.5 \text{ μH}, L_{s1}=20.5 \text{ μH}, L_{s2}=20.5 \text{ μH}, L_1=0 \text{ μH}, L_2=0 \text{ μH}, R_1=0 \text{ Ω},$$

$R_2=0 \text{ Ω}, R_3=0 \text{ Ω}$($L_{d1}, L_{d2}, L_{s1}, L_{s2}, L_1$ and L_2 are stray inductances.)

③ **Operation of parallel MOSFETs (with variations in electrical characteristics)**

Next, we intentionally changed the V_{th} levels of the MOSFETs Q_1 and Q_2 and ran a simulation in the same manner as above. As described in Section 3.2, "Parasitic oscillation of parallel MOSFETs," parallel MOSFETs form a resonant circuit with a high Q factor. Since the feedback loop has a high gain, parallel MOSFETs are highly susceptible to oscillation. Figure 4.8 shows the simulation results. In this simulation, parasitic oscillation caused by a difference in V_{th} was examined. When multiple MOSFETs are connected in parallel, factors other than V_{th} might cause them to oscillate. Here, we changed the V_{th} levels of Q_1 and Q_2 in the circuit of Figure 4.5 and otherwise used the same conditions as for the previous simulation.
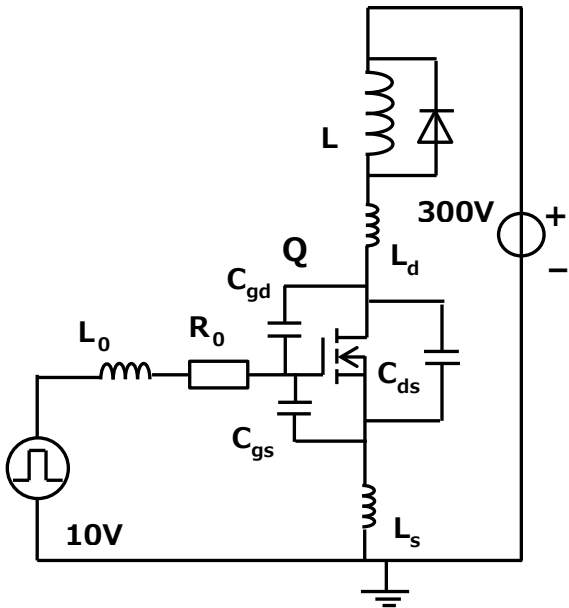
Figure 4.4
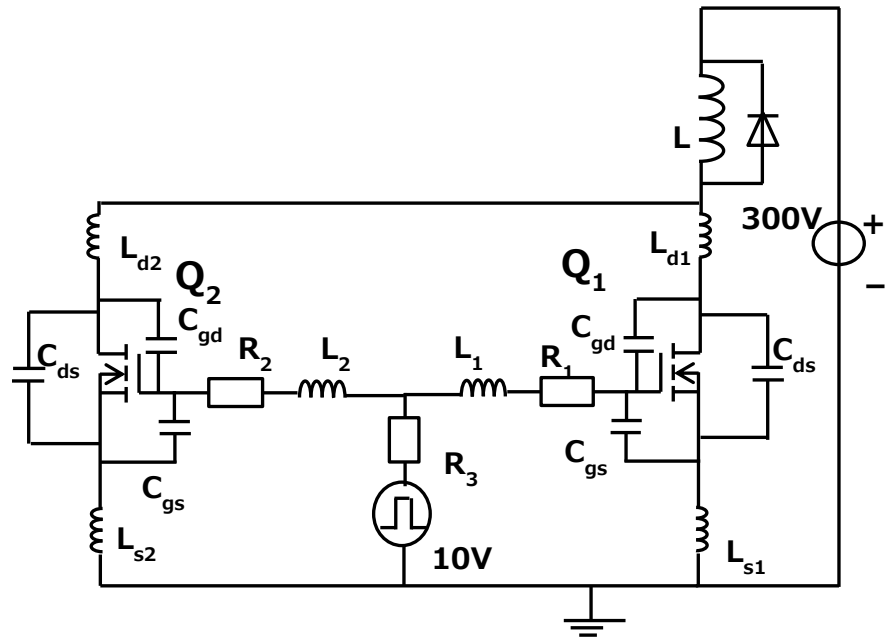**Circuit with a single MOSFET**

Figure 4.5
Equivalent circuit of parallel MOSFETs

Parallel MOSFETs are extremely susceptible to oscillation during switching transitions when there is an imbalance in the current sharing. Parallel MOSFETs could be subjected to a gate voltage considerably higher than their rated voltage.
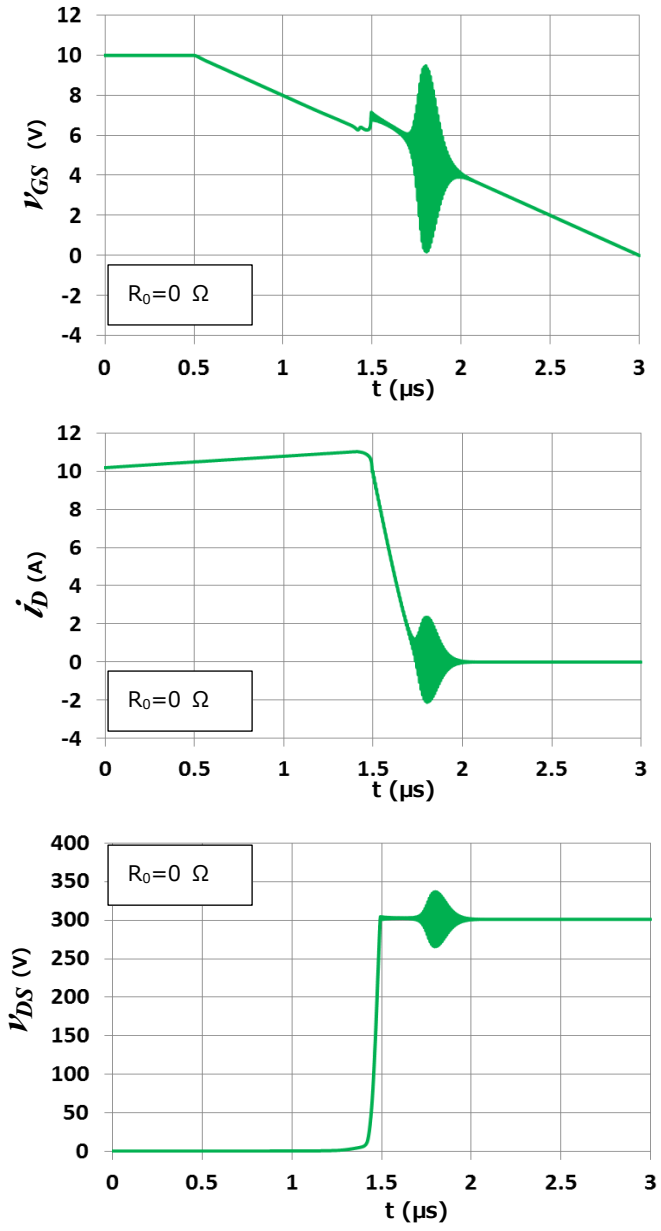
Figure 4.6
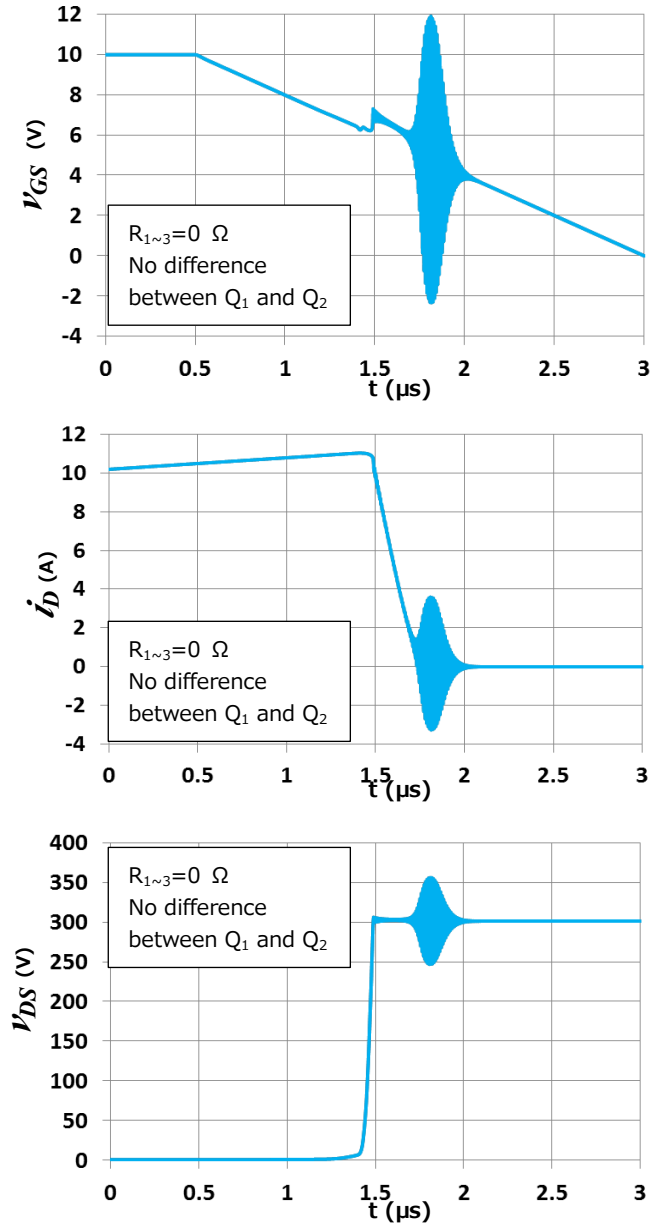**Turn-off waveforms**
of a single MOSFET

Figure 4.7
Turn-off waveforms
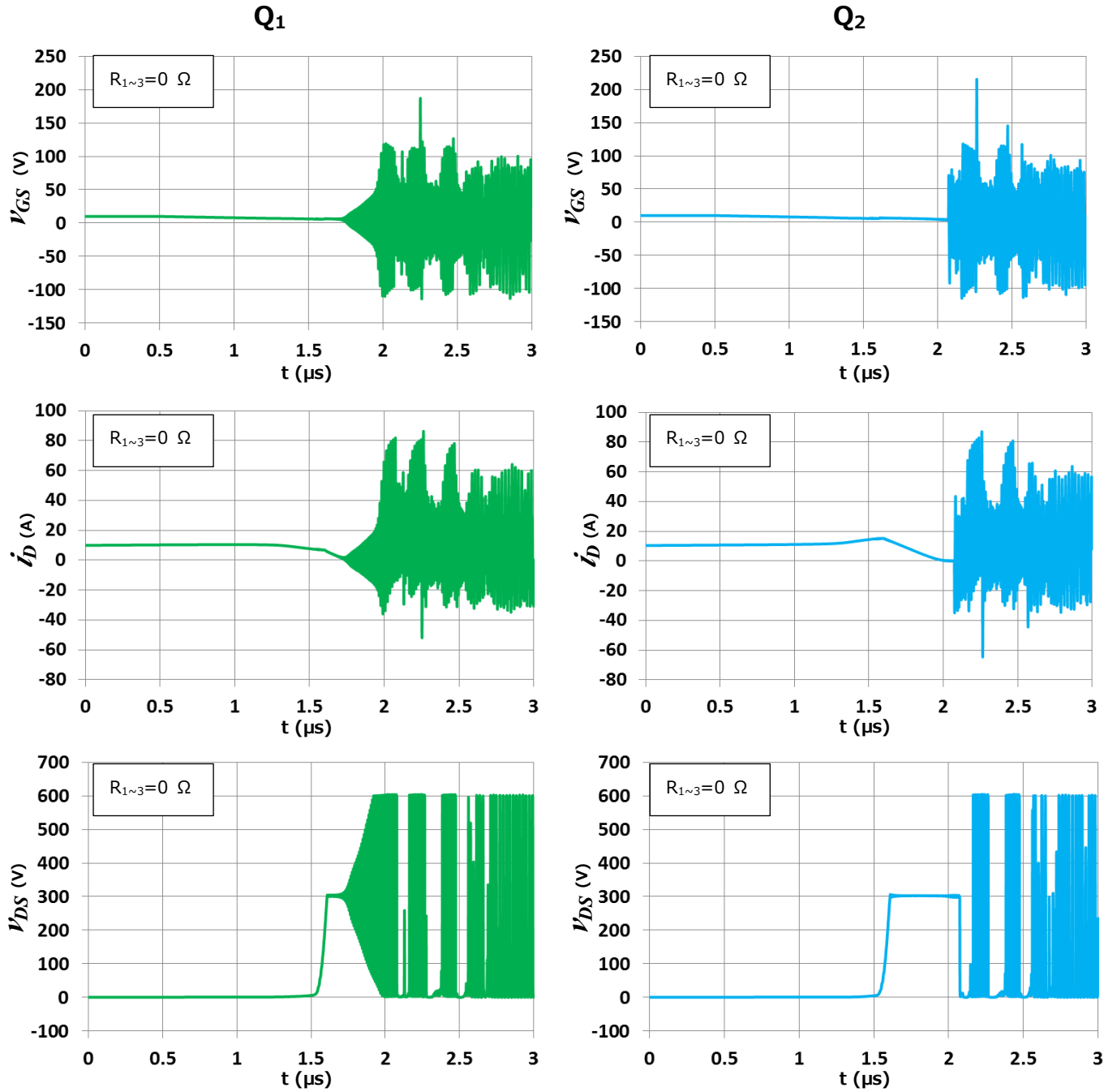**of same parallel MOSFETs**

Q₁

Q₂

Figure 4.8 Turn-off waveforms of parallel MOSFETs
V_{th}: $Q_1 > Q_2$

4.2.2. Preventing oscillation

MOSFETs with a low C_{gd}/C_{gs} and a low g_m are less susceptible to oscillation. It is also important to prevent oscillation using an external circuit. We simulated to verify its effectiveness.

· Gate resistor(s)

To prevent oscillation of parallel MOSFETs, we inserted resistors in series for each MOSFET and verified their effect.

Figure 4.10 shows the results of simulation on a circuit without a gate resistor (i.e., R_1, R_2 and R_3 were programmed to zero).

Figure 4.11 shows the results of simulation on a circuit in which a common gate resistor was inserted for the parallel MOSFETs (i.e., $R_1=R_2=0$ Ω, $R_3=1$ Ω).

Figure 4.12 shows the results of simulation on a circuit in which resistors were inserted in series for each MOSFET ($R_1=R_2=2$ Ω, $R_3=0$ Ω).

It was confirmed that inserting gate resistors in series for each of the parallel MOSFETs is effective in preventing parasitic oscillation.
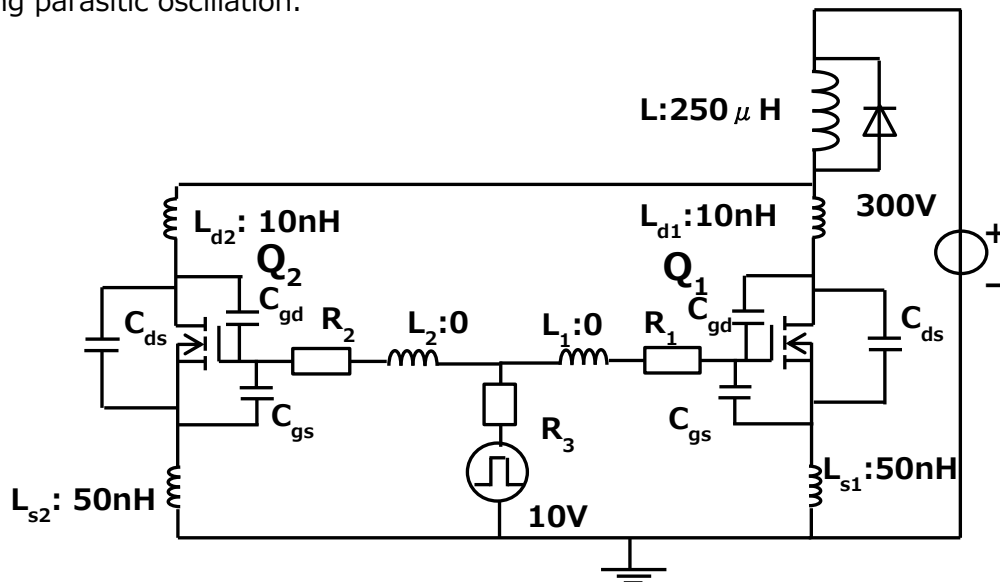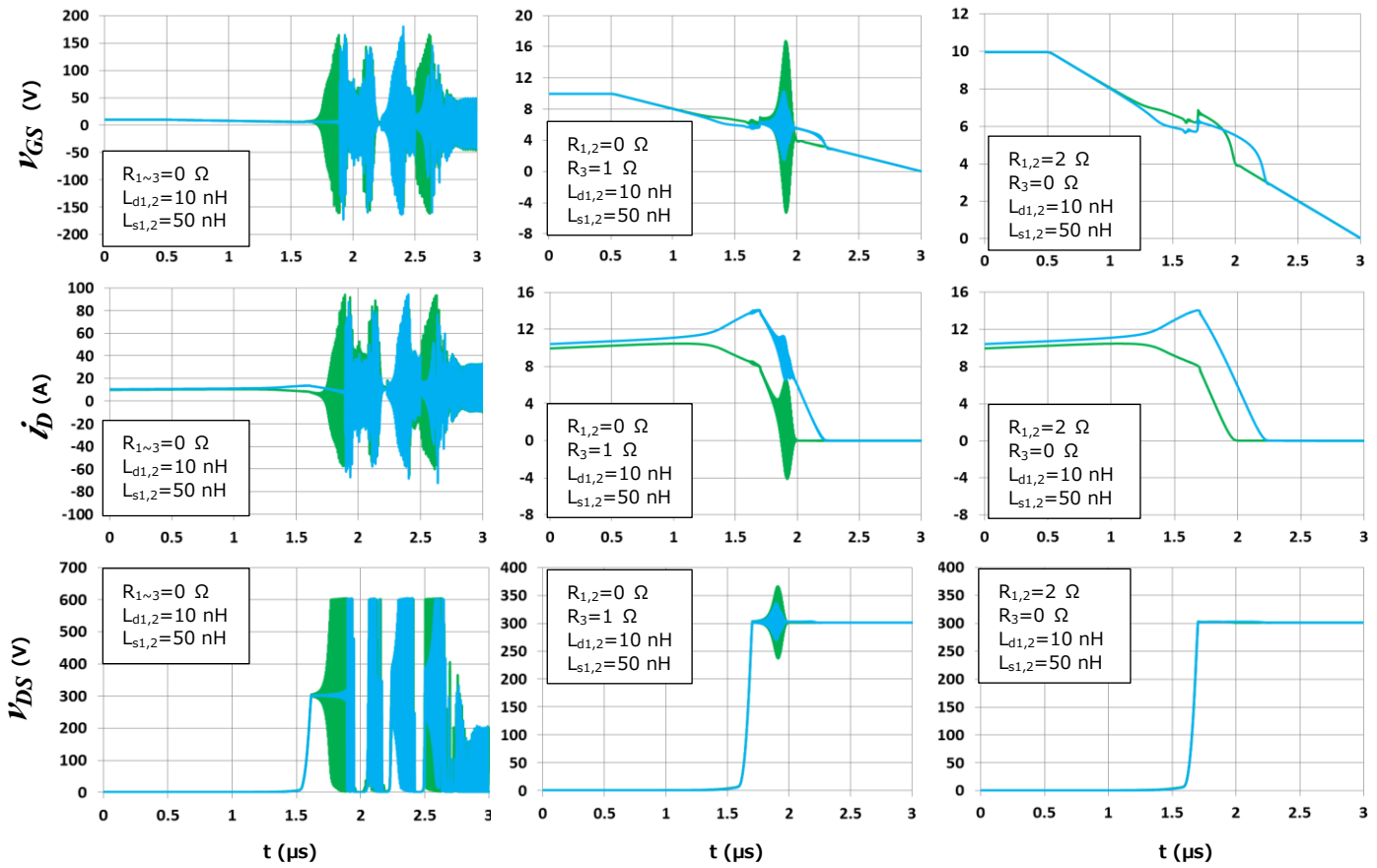

Figure 4.9 Parallel MOSFETs

Figure 4.10 Parallel MOSFETs without a gate resistor; Q₁ and Q₂ waveforms

Figure 4.11 Parallel MOSFETs with a common gate resistor; Q₁ and Q₂ waveforms

Figure 4.12 Parallel MOSFETs with series-connected gate resistors; Q₁ and Q₂ waveforms

Note: At Figure 4.10 to 4.12, blue line: V_{th} low, green line: V_{th} standard

2017-11-16

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