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MOSFET Avalanche Ruggedness

Outline:

When a voltage exceeds breakdown voltage to a MOSFET, the MOSFET enters the avalanche mode and may have a problem.

This document describes the mechanism of avalanche phenomenon, the definition of its ruggedness and the countermeasures against it.

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1. Breakdown phenomena

Figure 1.1 shows a pn junction of a semiconductor device. Very little current flows through the pn junction when it is reverse-biased. As the reverse-bias voltage is increased, a very large current begins to flow above a certain voltage limit. This phenomenon is called **reverse bias breakdown**. The voltage at which the breakdown of a pn junction occurs is called **reverse breakdown voltage**.

There are two types of breakdown: **avalanche breakdown** and **Zener breakdown**.

1.1. Avalanche breakdown

As the reverse-bias voltage increases, the strength of the pn junction electric field increases. When the electric field is strong enough, mobile electrons moving through the depletion layer are accelerated and gain high kinetic energy. When these mobile electrons collide with atoms comprising a crystal lattice, their kinetic energy excites their valence electrons, creating more electron-hole pairs. The knocked-out free electrons are also accelerated to high enough speeds to knock other bound electrons out of atoms, creating more free electrons. Figure 1.2 illustrates electron avalanche breakdown.

1.2. Zener breakdown

Under a high electric field due to a reverse-bias voltage, the distance between the valence and conduction band edges in the p and n regions of the depletion layer decreases. Sufficiently strong electric fields enable quantum tunneling of electrons from the valence band in the p region to the conduction band in the n region. The sudden increase of a reverse current due to the tunneling effect is called Zener breakdown. Figure 1.3 illustrates Zener breakdown.

1.3. Avalanche breakdown versus Zener breakdown

Avalanche breakdown is distinct from Zener breakdown. In semiconductor devices, the pn junction exhibits either avalanche or Zener breakdown, whichever occurs at a lower reverse-bias voltage. These breakdown phenomena occur at different voltages, depending on the semiconductor dopant concentration and temperature.

Zener breakdown tends to occur in heavily doped junctions that produce a narrow depletion region. In contrast, Zener breakdown is less likely to occur in lightly doped junctions. Instead, avalanche breakdown tends to occur in lightly doped junctions that produce a wider depletion region.

An increase in temperature reduces the width of a forbidden band E_g or band gap between the valence and conduction bands, making tunneling of electrons more likely to occur. The random motion of free electrons increases with temperature. However, at high temperature, the flow of free electrons is restricted by the collision with atoms. Therefore, avalanche breakdown is less likely to occur at higher temperatures.

Valence electron: An electron of an atom located in the outermost shell

Electron-hole pair: In a silicon semiconductor crystal, valence electrons are shared between two atoms by a covalent bond. When an energy higher than the covalent bond is applied, valence electrons break free from the atoms and become free electrons. The lack of an electron in an atom is called an electron hole or simply a hole. There are one-to-one relationships between free electrons and holes called electron-hole pairs.

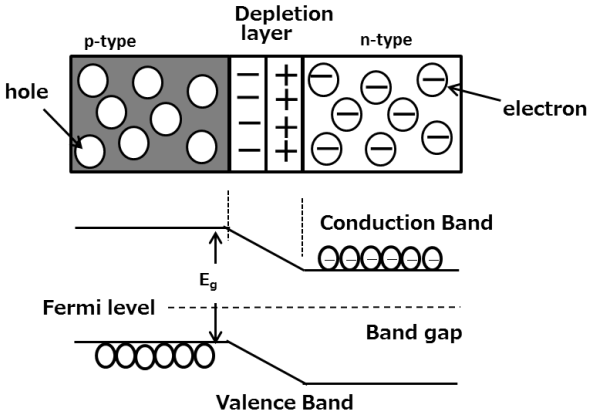

Figure 1.1 Semiconductor pn junction

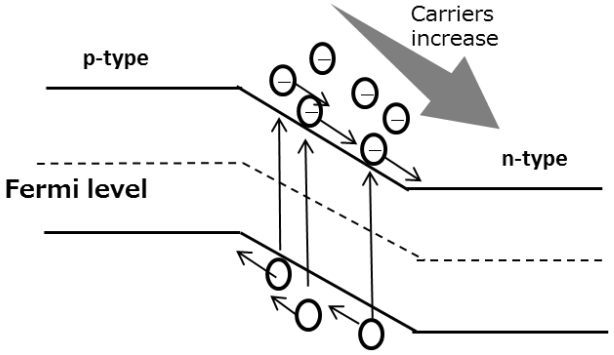

Figure 1.2 Electron avalanche breakdown

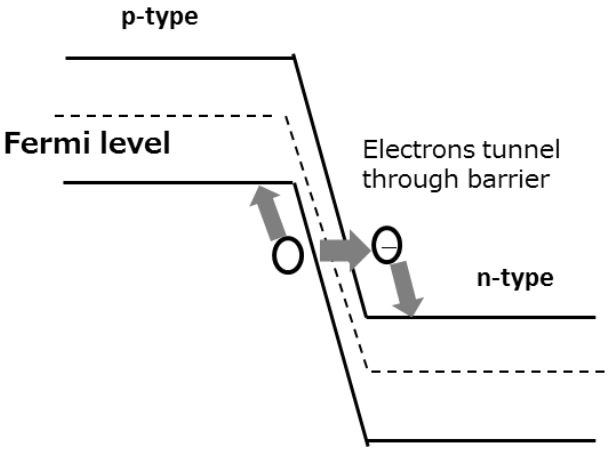

Figure 1.3 Zener breakdown

2. Avalanche breakdown in a MOSFET

Avalanche breakdown occurs when a flyback voltage generated during the turn-off of an inductive load or a spike voltage caused by the parasitic inductance of the drain load exceeds the breakdown voltage BV_{DSS} of a MOSFET.

When avalanche breakdown occurs, the pn junction of the MOSFET is reverse-biased, a strong electric field is produced in the depletion layer, and free electrons gain high kinetic energy as they are accelerated in the strong electric field. As described above, when free electrons collide with atoms comprising a crystal lattice, they knock other bound electrons out of atoms and create electron-hole pairs. This knocking-out process continues, increasing the number of free electrons and leading to avalanche breakdown.

2.1. Mechanism of MOSFET avalanche breakdown

Figure 2.1 shows the cross section of a MOSFET, and Figure 2.2 shows the equivalent circuit for the avalanche behavior of a MOSFET.

When a voltage higher than the breakdown voltage is applied across the drain and the source in Figure 2.2, the diode D (which is the equivalent of the pn junction) enters avalanche breakdown and passes an avalanche current.

(a) Avalanche current breakdown

An avalanche current i flows through the resistor R in the base region of the parasitic npn bipolar transistor. As a result, a voltage $i \times R$ appears across the base and the emitter of the transistor. If this voltage is high enough to turn on the parasitic npn transistor, it passes a current. At this time, if the drain-source voltage is high, the parasitic npn transistor might enter secondary breakdown, causing permanent damage to the MOSFET.

(b) Avalanche energy breakdown

If avalanche behavior causes a MOSFET to enter the breakdown voltage BV_{DSS} region, a current continues flowing from the drain to the source of the MOSFET until the energy stored in the inductive load at the drain is consumed. Because of this current and voltage BV_{DSS}, a power loss occurs. The resulting energy causes the device temperature to increase, and destroys the device if it exceeds the rated channel temperature.

(c) Degradation of avalanche ruggedness due to dv/dt

A MOSFET has a capacitance C between the drain and the source as shown in Figure 2.1. If a voltage rises sharply during the turn-off of the MOSFET, a current equal to $i=C \cdot dv/dt$ flows to the resistor between the base and the emitter of the parasitic bipolar transistor. If this current is excessively high, the parasitic bipolar transistor turns on and degrades the MOSFET breakdown ruggedness.

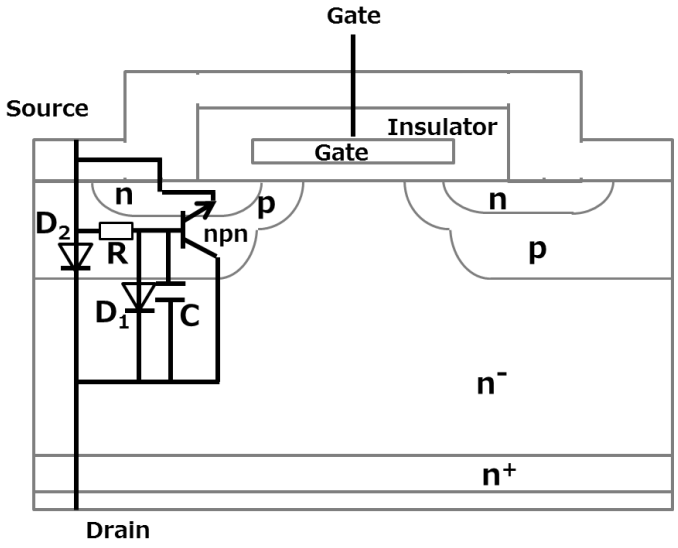

Figure 2.1 Cross section of a MOSFET

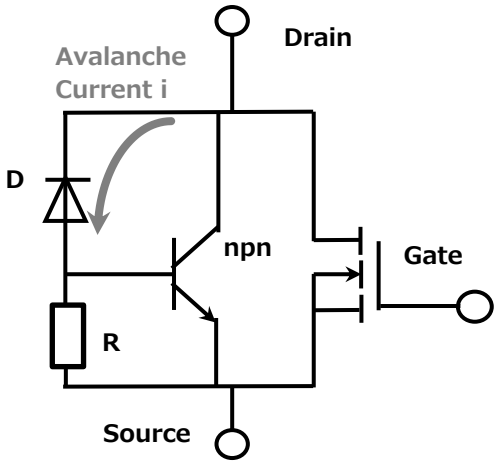

Figure 2.2 Equivalent circuit model for avalanche behavior

2.2. Avalanche ruggedness

Power MOSFETs are commonly used as high-speed switching devices. A power MOSFET experiences a high-voltage spike between the drain and the source during turn-off due to the circuit self-inductance and stray inductances.

Let the sum of the circuit self-inductance and stray inductances be L. Then, the surge voltage is expressed as:

$$v=L \cdot di/dt$$

If the drain-source voltage of the MOSFET exceeds its breakdown voltage BV_{DSS} due to the surge voltage, an avalanche current flows in the MOSFET. An avalanche current exceeding the current or energy limit might cause permanent damage to the MOSFET.

Conventionally, a surge-absorbing device was used to protect electronic devices. Nowadays, a surge absorber circuit is dispensed with in order to reduce the number of parts and thereby the size of a system. To address this requirement, a power MOSFET needs to damp avalanche energy even in the event of a voltage surge exceeding its voltage ratings. In response, Toshiba now provides a product series that can safely operate at up to the self-breakdown voltage as long as avalanche ruggedness conditions are met.

However, avalanche events place an excessive stress on the MOSFET. Therefore, even if the avalanche capability is guaranteed, for the sake of system reliability it is recommended to ensure that MOSFETs will not go into avalanche mode. Note that many MOSFETs do not provide any guarantee for repetitive avalanche ruggedness. There is a case for recommending that the product be used without entering avalanche mode, even though the avalanche energy is specified with the maximum rating of the MOSFET.

2.2.1. Avalanche energy calculation

Figure 2.3 shows a test circuit for avalanche breakdown, and Figure 2.4 shows the waveform of an avalanche current.

When the gate voltage exceeds the threshold voltage in Figure 2.4, a current flows through the channel region of the MOSFET shown in Figure 2.2. However, when the gate voltage drops below the threshold voltage, the channel is shut off. This causes the drain-source voltage to rise and exceed the breakdown voltage BV_{DSS}, causing a current to flow through the diode in Figure 2.2, leading to avalanche breakdown. The energy stored in L is dissipated upon avalanche breakdown.

In Figure 2.4, I_{AS} is the maximum allowable avalanche current, and E_{AS} is the maximum allowable avalanche energy.

The peak channel temperature T_{ch} in avalanche mode must be kept below the rated maximum channel temperature.

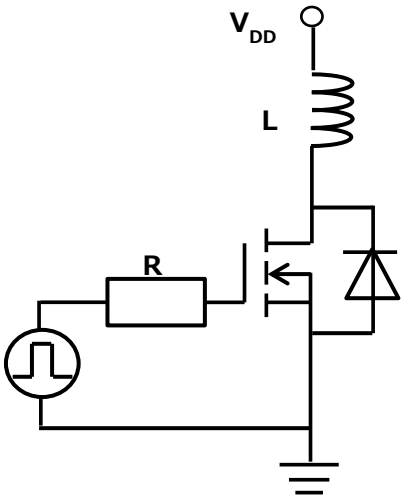

Figure 2.3 Test circuit for avalanche behavior

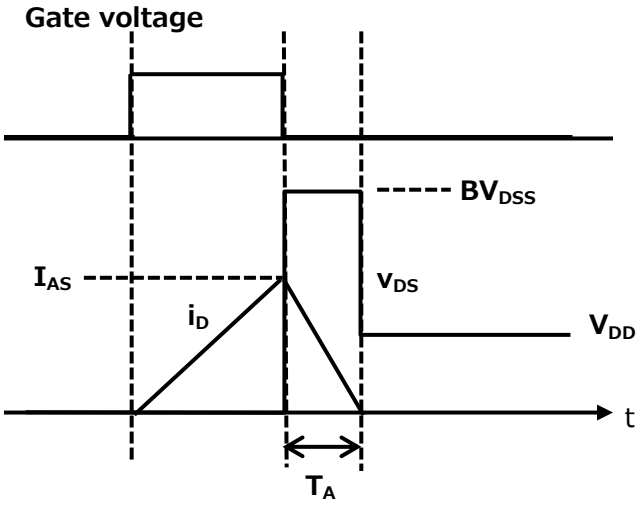

Figure 2.4 Avalanche current waveform

Avalanche energy E_{AS} is calculated as:

$$E_{AS} = P_A \cdot t_A = \frac{1}{2} BV_{DSS} \cdot I_{AS} \cdot T_A = \frac{1}{2} L {I_{AS}}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

$$T_A = \frac{L \cdot I_{AS}}{BV_{DSS} - V_{DD}}$$

E_{AS}: Avalanche energy
I_{AS}: Avalanche current
BV_{DSS}: Drain-source breakdown voltage
V_{DD}: Supply voltage
T_A: Duration of avalanche breakdown
P_A: Power supplied (during avalanche breakdown)

Avalanche ruggedness is the energy allowable in a single pulse. The channel temperature is the maximum channel temperature T_{ch}(max) on the condition that the rated avalanche current I_{AS} will not be exceeded when single-shot avalanche energy is applied under the prescribed conditions.

In practice, an increase in temperature caused by an avalanche event is calculated in order to determine that the channel temperature will not exceed the rated T_{ch}(max) value even after taking into account an ambient temperature and a possible rise in temperature caused by steady-state and switching losses.

The temperature increase in avalanche mode is estimated as follows:

$$\Delta T_{ch} = 0.473 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th(ch-a)} \ (Note)$$

BV_{DSS}: Drain-source breakdown voltage
I_{AS}: Avalanche current
$r_{th(ch-a)}$: Transient channel-to-ambient thermal impedance during avalanche mode (T_A)

Note: Power dissipation, P_D, caused by the current and voltage waveforms shown in Figure 2.5 changes over time in the shape of a triangle as highlighted by oblique lines in Figure 2.6. At this time, the channel temperature changes as indicated by the solid line in Figure 2.6, and peaks at time 1/2 t_w. The maximum channel temperature at 1/2 t_w is calculated as 0.699 times the channel temperature indicated by the square wave. Hence, the approximate increase in channel temperature is as follows:

$$\Delta T_{ch} \cong 0.669 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th(ch-a)}(\frac{1}{2} t_w)$$

$$r_{th(ch-a)}(\frac{1}{2} t_w) \cong \frac{1}{\sqrt{2}} r_{th(ch-a)}$$

* Approximation for MOSFET products with a transient thermal impedance slope of 0.5 in the double logarithmic graph

which can be approximated* as:

$$\Delta T_{ch} \cong 0.669 \cdot \frac{1}{\sqrt{2}} \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th(ch-a)}(t_w)$$
$$\cong 0.473 \cdot BV_{DSS} \cdot I_{AS} \cdot r_{th(ch-a)}(t_w)$$

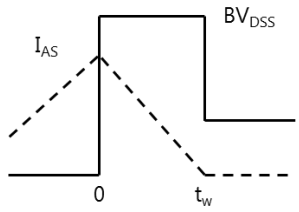

Figure 2.5 Current and voltage waveforms

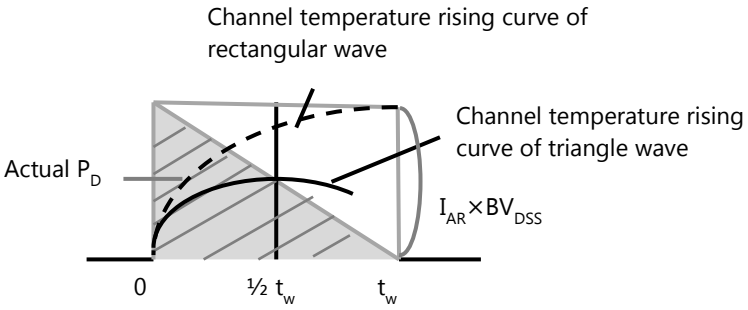

Figure 2.6 Power dissipation P_D

3. Protection against avalanche breakdown

Avalanche breakdown occurs when a voltage exceeding the breakdown voltage BV_{DSS} is applied to a MOSFET. This is due to a back-EMF voltage induced by a circuit's stray inductances. Reducing stray inductances is the most important measure for protection against avalanche breakdown. If stray inductances cannot be reduced sufficiently, it is necessary to consider drive conditions to prevent voltage surge or add a surge-absorbing circuit.

The following are commonly used methods for preventing avalanche breakdown:

(1) Make wires as thick and short as possible to reduce the inductances of wires through which the main current passes.

(2) Increase the value of the turn-off gate resistor to reduce the turn-off speed of the MOSFET in order to reduce the dv/dt during turn-off and suppress voltage surge. Note, however, that this method increases switching losses.

(3) Add a Zener diode or a snubber circuit to damp surge voltage so that the MOSFET will not enter avalanche mode. In this case, care should be exercised as to the wire inductance.

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