

# Reliability and Endurance of FRAM: A case study

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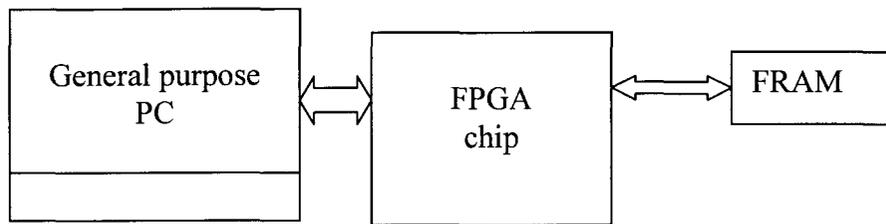
**Abstract** -- This paper describes a case study quantifying reliability and endurance results of two FRAM nonvolatile memories. The need for reliability and endurance testing is vital to space applications where single event upsets (SEUs) can occur in memory and disrupt or disable a flight system. The method used to test the ferroelectric nonvolatile memory FRAM chips incorporates a XILINX XC4010E FPGA performing reads/writes to the memory chips and a PC in tandem to record errors. This method is extremely low cost and comparable in test times to commercially available memory testers with high hourly rates.

## 1. INTRODUCTION

Ferroelectric nonvolatile memory (FRAM) is a relatively new nonvolatile memory technology that has become of large interest to the space applications community. What makes FRAM an attractive alternative to conventional nonvolatile memories, such as electrically erasable programmable read-only memory (EEPROM), is that it has a high resistance to radiation, a high endurance rating, excellent retention over a wide range of temperatures, and fast-programming times. For space applications, each of these feature improvements is beneficial to flight systems. Flight systems exist in an environment where radiation can potentially cause single event upsets (SEUs) within the hardware. SEUs are beyond the scope of this paper, but have

been shown to be extremely harmful to software and hardware required for spacecraft functionality. High endurance is an important factor since memory onboard a spacecraft cannot be readily exchanged for a damaged one once space born. In terms of temperature sensitivity, the space environment presents an extremely varying temperature range, which can degrade the functionality of the memory. Lastly, fast-programming times is beneficial since it implies better performance. Thus, it can be seen that FRAM has technological advantages compared to conventional nonvolatile memories and has become of great interest to the space community for the reasons mentioned above.

Due to its recent introduction, FRAM lacks a thorough amount of data that benchmarks its general performance in terms of reliability and endurance. In this paper, an inexpensive, of-the-shelf, in-situ memory tester developed in [1] was used to perform reliability and endurance testing on two FRAM chips. The chips that were used for our tests were the Ramtron FM24C04 and the Ramtron FM1808. The purpose of this case study is to demonstrate an alternative method to reliability and endurance testing that is low in cost and easy to implement. Additionally, this method of testing is easily applicable to virtually any type of nonvolatile memory that exists today.



**Figure 1: General Test Bed Setup**

The remainder of this paper is split into four sections. Section two discusses related work in this area. Section three will briefly describe the memory tester design (further details can be found in [1]). Section four will present the current results obtained from the tests. Section five will provide a summary and future outlooks.

## 2. RELATED WORK

There has been a considerable amount of research that has characterized the reliability and endurance behavior of nonvolatile memories. In [3], an experimental procedure was developed that first fatigued an FRAM memory at elevated voltages and then tested the data retention characteristics of the FRAM. The FRAM used for testing was a Ramtron FM1608 64 Kb. 105 FRAMs were fatigued to  $1E10$  fatigue cycles at elevated voltages of five to seven volts. Data retention was then tested by setting all data bits to 0 at a temperature of  $200^{\circ}\text{C}$  for 72 hours followed by 10 minutes with the temperature set to  $70^{\circ}\text{C}$  and setting all bits to 1. Using the results of [5,6] the aging of the chip was determined to be a 100 years at  $55^{\circ}\text{C}$  or 7.75 at  $85^{\circ}\text{C}$ .

In [9], a test methodology developed by Ramtron is discussed using a FM24C16 FRAM as the test chip. The FRAMs were written to with a pattern, followed by a bake, and then a reading of the pattern.

There were numerous other studies performed; these are described in [2,5,7,8,9]. All of these studies performed endurance testing on the FRAMs with heat applied to them. The significance of this paper is that normal operating conditions were applied to get “normal” operating environment reliability and endurance characteristics. The heat-accelerated tests of the previously cited works apply theoretical calculations to simulated environments.

## 3. TEST BENCH

The advantages behind the test method used for this paper is that it is low in cost, easy to implement, and versatile, so virtually any nonvolatile memory can be used. Because the test method is low in cost, multiple test benches can be run in parallel to perform reliability and endurance tests in less time. The basic equipment required for this test bench is an FPGA chip, the memory chips to test, and a PC. The PC, which is optional, can be used to log data, such as errors found when reading a written piece of data to the memory. Alternatively, the errors can be logged onto the FPGA itself and displayed via a 7-segment LED, as was present in our test bench. A simple block diagram (Figure 1) displays the basic idea behind the test methodology. For our test bench, we used a XILINX XC4010E, 10,000-gate, 5-V FPGA as the memory interface controller and tester. A XESS XS40

FPGA prototyping board was chosen as a tester. This board provided a parallel port for PC communications and a 7-segment LED and EEPROM socket for PC-independent error logging.

Interfacing the FPGA with the memories tested was relatively simple to implement by referencing the documents specifying the memory chip's interface. The general flow-chart shown in Figure 1 shows the basic implementation steps used to design the memory tester for a specific memory.

The first FRAM chip used for testing was the Ramtron FM24C04, which is a 4-Kb serial FRAM organized as 512 words by 8 bits [11]. The endurance specification of this chip is rated at  $10^{10}$  read/write cycles. The memory was tested at 90% of its maximum rated clock speed (400 KHz). The second chip used for our tests was the Ramtron FM1808 FRAM, which is 256 Kb in size. The chip is organized as 32,768 words of 8 bits each. The endurance rating for this chip is also  $10^{10}$  read or write cycles.

For reliability testing, a MATS+ test was chosen. The MATS+ test can detect address decoder faults and stuck-at faults. The MATS+ test is described in Figure 2.

```

1. UP (W01010101)
2. UP(R; W10101010)
3. DOWN(R; W01010101)
4. LOOP BACK TO (2)

```

**Figure 2: MATS+ Test**

“UP” and “DOWN” are part of the Van de Goor’s memory test notation, which are defined in Figure 3.

```

UP (W10101010; R; W01010101)
- UP = Perform the entire set of
operations in parentheses from
the first memory address to the
last
- W10101010 = Write the data
pattern '10101010'
- R = Read back the data
- W01010101 = Write the data
pattern 01010101
-(Increment address and loop)

```

**Figure 3: Van de Goor’s memory test notation**

The fault coverage of a MATS+ test can be shown informally as follows:

- i. For each cell, both data values have been written and verified. This ensures that the read/write operations can be applied to each cell and that the cell is not stuck at fault.
- ii. The march element with the increasing address order verifies that writing into the current cell does not affect a cell with a higher address, because the contents of the latter cell are verified later on by that march element.
- iii. The march element with the decreasing address order verifies that writing into the current cell does not affect a cell with a lower address.
- iv. From (ii) and (iii), it can be concluded that writing into a particular cell does not affect any other cell. From (i) it can be concluded that the addressed cell can be accessed; hence, the address decoder is correct.
- v. The fault coverage of a MATS+ test has been shown by (i) for stuck-at faults and by (iv) for address faults.

## 5. SUMMARY

The test used for endurance testing can be seen in Figure 4.

```

1. (W01010101; R; W10101010; R)
2. LOOP BACK TO (1)
    
```

**Figure 4: Endurance Test**

To accelerate the test results, only one single address was used for testing endurance. Testing all of the addresses would have been prohibitively long.

## 4. RESULTS

Memory testing is ongoing, and the results to date are preliminary. Two FRAM nonvolatile memories are under test: the Ramtron FM24C04 serial FRAM and the Ramtron FM1808 Parallel FRAM. Reliability tests have produced no errors in any of the memories. Endurance testing on the Ramtron FM24C04 serial FRAM has exceeded the endurance specification of the chip ( $1.0 \times 10^{10}$  read/write cycles) by more than seven times (it has undergone more than  $7.708 \times 10^{10}$  read/write cycles) with no errors. Endurance testing on the Ramtron FM1808 parallel FRAM has exceeded the endurance specification of  $1.0 \times 10^{10}$  by almost ten times, but no errors have surfaced to date.

The goal of this research is to determine the reliability and endurance characteristics of certain nonvolatile memories for use in space applications. A low-cost, highly flexible, FPGA-based test bench has been developed for such testing. Preliminary reliability and endurance characterization of a small sample of parallel and serial FRAMs have been completed. However, the reliability and endurance characterization of these memories is in a preliminary state. There is still considerable work left to do before the research is complete:

- Further reliability and endurance testing should be completed using a larger sample of chips from different lots.
- The nonvolatile memories should undergo accelerated aging by heating and high-voltage testing in order to test data retention characteristics. This would also allow testing for imprint in ferroelectric memory by following the test methods described in [3].
- Radiation testing can be performed using this test bed, assuming appropriate shielding is provided for the FPGA.
- It may be useful to add additional

	Status	# R/W Cycles (Endurance)	Endurance Specification
Ramtron Serial FRAM (FM24C04)	Test bed complete: Both tests running	7.708E10	1E10
Ramtron Parallel FRAM (FM1808)	Test bed complete: Both tests running	9.49E10	1E10

**Table 1: Test Results**

reliability test routines in the Verilog program to test for additional faults. Due to the size limitation of the current FPGA, a larger FPGA would be required.

This test bench offers several advantages over commercial testers when used for reliability and endurance testing. Endurance testing to a chip's specifications could involve more than  $10^{10}$  read/write cycles, which can take up to 28 days for the Ramtron FM24C04 serial FRAM. Commercially available memory testers with high hourly rates may prove extremely expensive for testing nonvolatile memories with  $10^{12}$  to  $10^{15}$  read/write cycles. In comparison, the FPGA-based testers are inexpensive and more flexible. If several FPGA boards are used, many chips can be tested simultaneously at a fraction of the cost compared to the commercial testers. The highly portable, PC-independent nature of the test bench would also make it suitable for use in radiation or accelerated aging heat testing, assuming appropriate shielding is provided for the tester.

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