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1 author:

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Development of Ferroelectric RAM (FRAM) for Mass Production

Takashi Eshita[1], Wensheng Wang[1], Kou Nakamura[1], Souichirou Ozawa[1], Youichi Okita[1], Satoru Mihara[1], Yukinobu Hikosaka[1], Hitoshi Saito[1], Junichi Watanabe[1], Ken'ichi Inoue[1], Hideshi Yamaguchi[2] and Kenji Nomura[2]

1. System Memory Business Division, Fujitsu Semiconductor Limited, Kohoku-ku, Yokoham 222-0033, Japan

2. Factory Engineering Laboratory, Fujitsu Laboratories Limited, 10-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0197, Japan

Abstract: we have developed ferroelectric capacitor fabrication technique to realize low-voltage and high-density ferroelectric random access memory (FRAM). High temperature deposited IrO_x top electrode reveals high crystalline quality which drastically reduces the degradation of ferroelectric film by preventing hydrogen diffusion into ferroelectric film. This improvement enables us to commercialize highly-reliable 1T1C FRAM with memory density of 4 Mb or larger.

Key words: Ferroelectric, PZT, LCSPZT, IrO.

1. Introduction

Ferroelectric random access memory (FRAM) is the first commercialized memory among advanced non-volatile memories such as magnetoresistive RAM (MRAM), phase change RAM (PCRAM), and resistive RAM (ReRAM) [1-4]. FRAM has been reported to have advantages of lower power consumption and higher switching endurance in comparison with commercial base FLASH memory, Spin-Torque-Transfer (STT) MRAM, and PCRAM [5]. We have developed fabrication technologies focusing on reliability, decreasing operation voltage, and power consumption. In our development, an interface control between ferroelectric material and electrode is found to be crucial for decreasing the operation voltages with maintaining the large polarization. This capacitor fabrication improvement with circuit improvements of the sensing amplifier [6, 7] has successfully realized robust reliability of the 4 Mb or larger memory-size FRAM. Our FRAM has evolved from 5 V operation and 0.5 μm node CMOS to 1.8 V operation and 0.18 μm node CMOS. This paper describes the key technologies of FRAM fabrication process and circuit design.

Corresponding author: Takashi Eshita, research field: semiconductor production development. E-mail: eshita@jp.fujitsu.com.

2. Experiments

FRAM fabrication process consists of conventional 0.18 μm CMOS and ferroelectric capacitor fabrication processes which were described elsewhere [3]. IrO_x top electrode, Pt bottom electrode and LCSPZT (La, Sr and Ca doped PZT) were deposited by sputtering. Fabrication procedures of conventional and new ferroelectric capacitor are shown in Fig. 1. We employed two-step annealing process consisting of anneal 1 (about 650 °C) and anneal 2 (about 750 °C) by using rapid thermal annealing (RTA) to obtain good crystalline LCSPZT with uniform sized grain. Both of those two annealing procedures are carried out before depositing the top electrode. While top electrode IrO_x (x is around 2.0) deposited at room temperature in the conventional procedure, the 1st top electrode IrO_y (y is around 1.9) about 350 °C, and then the 2nd top electrode IrO_x was deposited at room temperature in the new capacitor fabrication procedure. Oxidation stages of x and y were measured by the 2nd ion mass spectroscopy.

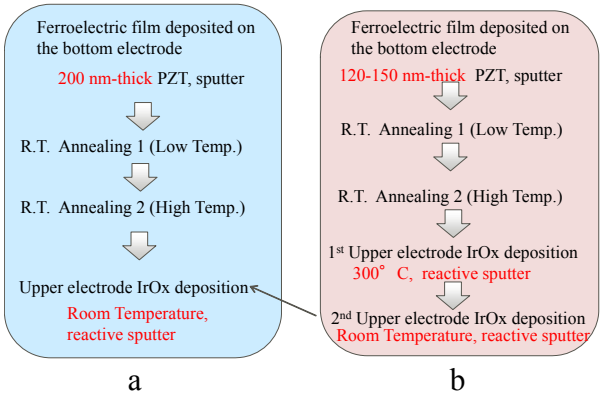

Fig. 1 (a) Fabrication procedures of conventional; (b) new developed ferroelectric capacitor.

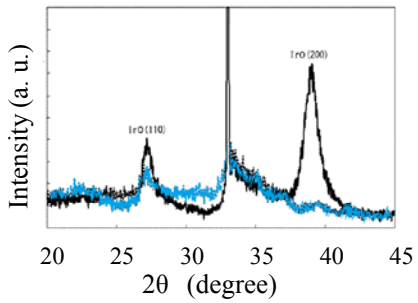

Fig. 2 X-ray diffraction patterns of conventional IrO_x (blue line) and new (black line) IrO_y.

3. Results and Discussion

Although we tried to reduce the thickness of the ferroelectric film from 200 nm to 150 nm to obtain 1.8 V operation ferroelectric capacitor by conventional procedure, ferroelectric capacitor with 150 nm thick LCSPZT had poor ferroelectric properties, such as small switching polarization (Q_{sw}) and large coercive voltage (V_c), which prevents the FRAM from reading and rewriting operations at 1.8 V. Since we found the interface control between the IrO_x top electrode and PZT is important to lower the operation voltage, we improved the top electrode deposition process. We have found that high temperature about 300 °C deposition of IrO_x drastically improved the crystal quality, as shown in Fig. 2. Fig. 3 shows the cross-sectional TEM images of the conventional and new ferroelectric capacitors. It is clear that IrO_x near the interface of new capacitor is very smooth. Improvements of the Q_{sw} and the V_c are also clear as shown in Fig. 4. Leakage current of the new ferroelectric capacitor is slightly larger than that of conventional capacitor, as shown in Fig. 5, however, which does not significantly influence to the FRAM function. Relatively larger leakage current of small capacitor may be due to its large side area of the capacitor. Our reliability examination results of switching endurance and imprint endurance (opposite state (OS) rate) are shown in Fig. 6. In the OS rate, the closer value to zero indicates the better imprint endurance. Reliability of FRAM with new ferroelectric capacitor is clearly superior to that of conventional FRAM.

The interface region of ferroelectric film near the top electrode is degraded by inter-reaction during the heat treatments in metallization, thus resulting in the

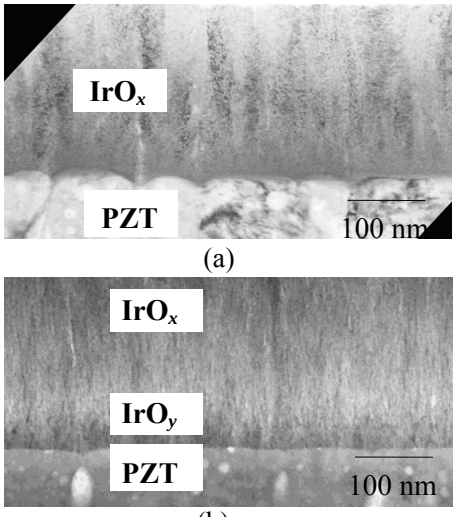

Fig. 3 Cross-sectional TEM micrograph of the ferroelectric capacitors. (a) Conventional; (b) new capacitor. Oxidation state as denoted *x* and *y* are about 1.9 and 1.8, respectively.

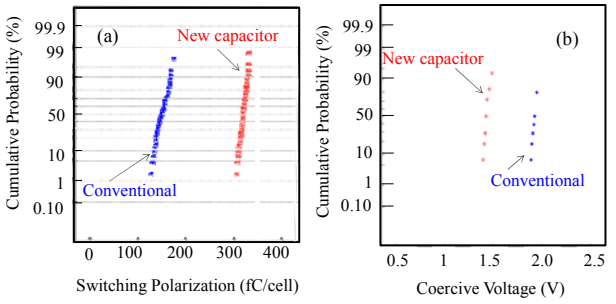

Fig. 4 In-wafer distribution of switching polarization at (a) 1.8 V and (b) coercive voltage.

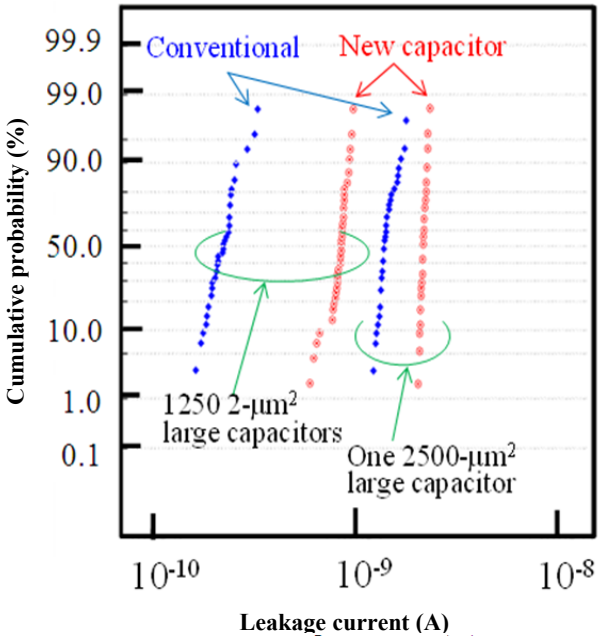

Fig. 5 Leakage currents distribution on a wafer for monitors consisting of (a) 1,250 × 2 μm^2 large capacitors and (b) one 2,500 μm^2 large capacitor.

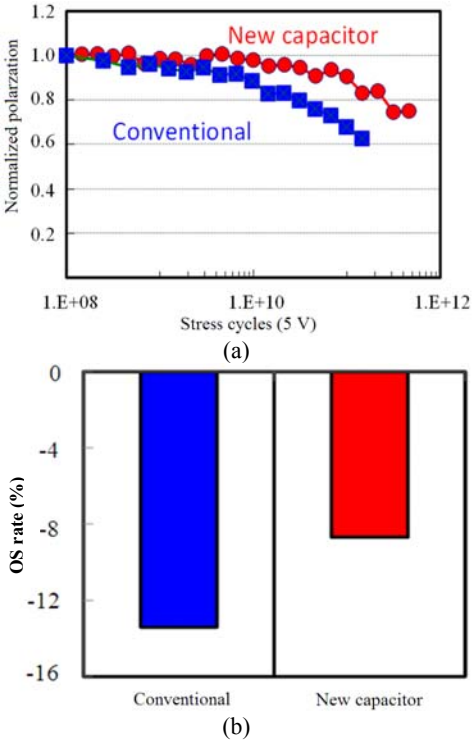

Fig. 6 Reliability examination results of (a) switching endurance and (b) imprint endurance or OS rate.

degradation of ferroelectric properties. Since the thickness of the degraded region does not change unless employing the same fabrication procedure, degradation

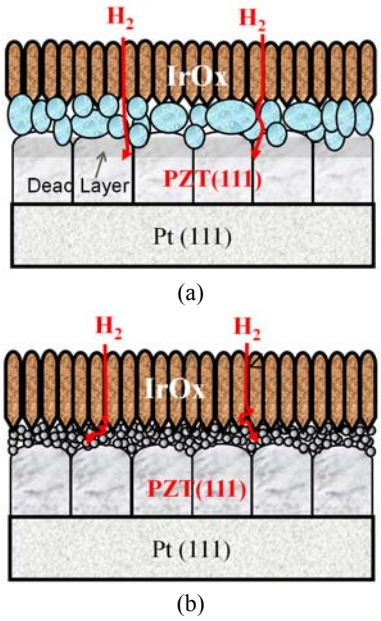

Fig. 7 Schematic cross-sectional ferroelectric capacitors, (a) conventional and (b) new capacitor.

of the ferroelectric properties is more sever for thin ferroelectric film. In the conventional capacitor, above mentioned degraded region of ferroelectric film possibly enlarged by large inter reaction because as-deposited IrO_x is initially amorphous and its diffusion speed is expected to be large. After heat treatment, while the upper portion of the top electrode found to be composed of columnar-shaped grain, the lower portion is composed of round-shaped large grain from precise TEM observation, as schematically shown in Fig. 7a, which may be due to large inter diffusion. Since XRD analysis has proven that IrO_x contains metallic Ir, it is possible that hydrogen generated during the metallization catalytically activated by the metallic Ir reduces IrO_x by itself and the ferroelectric film. When the ferroelectric film is reduced, characteristics of the ferroelectric capacitor are degraded [8]. It is also considered that oxygen vacancies in the IrO_x cause much easier hydrogen diffusion. In the new ferroelectric capacitor fabrication procedure, since precise SEM and TEM observations revealed the as-deposited IrO_y is composed of very fine grain, as schematically depicted in Fig. 7b, it is supposed to be much more

difficult to react with ferroelectric film, as suggested by smoother interface in Fig. 3b, which possibly prevents interface degrading layer from enlarging and also prevents hydrogen from diffusing into ferroelectric film. Hence, we have successfully developed 1.8 V operable 1T1C 4 Mb FRAM with excellent reliability.

4. Conclusions

We have developed new ferroelectric capacitor fabrication technology to realize a mass production of 1.8 V operation 1T1C 4Mb FRAM. Superior characteristics and highly reliable ferroelectric capacitor was obtained by employing high temperature IrO_y top electrode deposition.

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