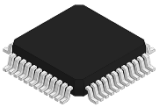
NuMicro® Family
M4521
Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

Features

* **Core**
  - Up to 72 MHz Arm® Cortex®-M4F processor delivering 1.25 DMIPS per MHz
  - DSP instruction set
  - Floating-Point Unit (FPU)
  - Nested Vectored Interrupt Controller (NVIC)
* **Memories**
  - 128 KB zero-wait state Flash memory
  - 32 KB SRAM
* **Cyclic Redundancy Calculation Unit**
* **8-channel Peripheral DMA**
* **External Bus Interface**
  - Supports up to two memory banks
  - Up to 1 MB addressing space for each chip select
* **Clock**
  - External 4 to 24 MHz crystal oscillator
  - External 32.768 kHz crystal oscillator for RTC
  - Internal 22.1184 MHz RC oscillator
  - Internal 10 kHz RC oscillator
  - Internal PLL up to 144 MHz, sourced from HIRC and HXT
* **RTC**
  - Independent V_{BAT} power pin
  - 80 bytes of battery-powered backup registers
* **Power Management**
  - Active: 22mA at 72MHz/3.3V (peripheral off)
  - Idle: 7mA at 72MHz/3.3V (peripheral off)
  - V_{BAT} supply for RTC: 2μA
  - Power down without RTC: 19μA
* **Timer & PWM**
  - Four sets of 32-bit timers
  - Twelve 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels
  - One 24-bit count-down SysTick timer
  - One watchdog timer
  - One window watchdog timer
* **Analog Peripheral**
  - One 12-bit, up to 16-ch 1MSPS SAR ADC



LQFP48 (7x7 mm)
LQFP64 (7x7 mm)

* **Communication Interface**
  - Up to 4 sets of UART interfaces, supporting RS485 and IrDA interfaces
  - One set of ISO-7816 interface
  - Two sets of I^2C interfaces
  - One set of Quad-SPI interface
  - One set of SPI interface
* **Advanced Connectivity**
  - USB 2.0 full speed dual role (device/host) controller with on-chip PHY
* **Operating Characteristic**
  - Voltage range: 2.5V to 5.5V
  - Temperature range: -40°C to +105°C
  - ESD HBM 8KV
* **Voltage Adjustable Interface**
  - Up to six I/O ports support VAI with supply V_{DDIO} from 1.8V to 5.5V
* **Up to 49 I/O pins with interrupt capability**
  - Up to 49 5V-tolerant I/O pins
* **One tamper detection pin**
* **96-bit Unique ID (UID)**
* **128-bit Unique Customer ID (UCID)**

Applications

* Power Distribution Unit (PDU)
* Uninterruptible Power Supply (UPS)
* High Speed MOSFET Control System
* Smart Capacitor
* OLED/TFT LCD Control
* RFID Reader
* Other Industrial and Consumer Electronics

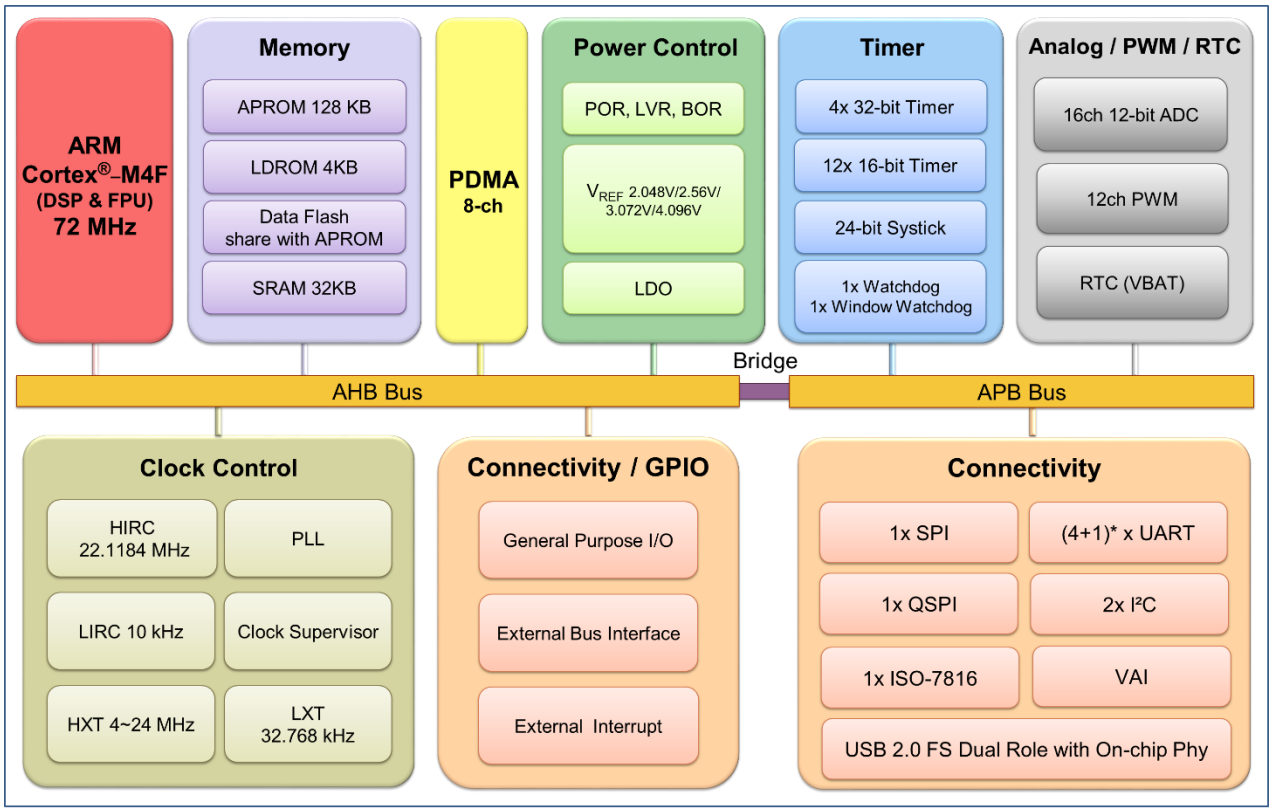
1 INTRODUCTION

The NuMicro® M4521 series 32-bit microcontroller powered by Arm® Cortex®-M4F with DSP and FPU runs up to 72 MHz. It is embedded with 128 KB Flash ROM, 32 KB SRAM and independent 4 KB In System Programming Flash ROM. The M4521 series is equipped with plenty of peripherals: 4 sets of UART with 16-byte FIFO, 2 sets of I^2C that support SMBus and PMBus, SPI and Quad-SPI, ISO-7816, USB full-speed device/host, and EBI that provides great flexibility through adding external memory. It also offers four 32-bit timers, two watchdog timers, 8-ch peripheral DMA, 12-ch 16-bit PWM, and 16-ch 12-bit SAR ADC with 1 MSPS conversion rate.

The M4521 series provides two special designs. One is high-resolution 144 MHz PWM with high-speed timer (resolution<7ns). In conjunction with a driver ADC, it delivers hardware brake protection and pulse capture functions to save MCU computing resource and effectively perform advanced computing task in motor control application, making the M4521 series exceptionally outstanding in industrial automation control. The other is VAI (Voltage Adjustment Interface) which supports voltage level adjustment on individual I/O (1.8V-5.5V) for saving additional cost on adjusting the interface voltage difference with external components.

The M4521 series also provides the wide operating voltage (2.5V-5.5V), industrial operating temperature (-40°C - 105°C), 5V-tolerance input I/O to significantly enhance system stability. The 22.1184 MHz internal RC oscillator (HIRC variation < ±2%) and 32.768 kHz external crystal oscillator can trim HIRC (HIRC variation < ±0.25%) working at -40˚C- 105˚C to enhance system immunity and fulfill the high precision demand of communications. The M4521 series is specifically suitable for high-performance and high-precision applications, such as industrial automation, home automation, security alarm system, and gaming peripherals.

2 BLOCK DIAGRAM



*Marked in the block diagram (4+1) means (4x UART + 1x ISO-7816 UART)

3 FEATURE DESCRIPTION

Core and System	
Arm® Cortex®-M4F	• Arm® Cortex®-M4F processor, running up to 72 MHz • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit SysTick timer • Programmable and mask-able interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option (4.4V/3.7V/2.7V/2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level.
Security	• 96-bit Unique ID (UID). • 128-bit Unique Customer ID (UCID).
Memories	
Boot Loader	• Nuvoton ISP (In-System-Programming) tool for firmware upgrade via UART and full speed USB device • ISP/IAP libraries
Flash	• 128 KB on-chip Application ROM (APROM) • 72 MHz maximum frequency, with performance at zero wait cycle in continuous address read access • 4 KB on-chip Flash for user-defined loader (LDROM) • All on-chip Flash support 2 KB page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Supports 32 KB SRAM including 16 KB bank0 and 16 KB bank1 • Each of these two banks can be accessed simultaneously • Supports Byte-, half-word- and word-access

	• Supports oversize response error
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Eight independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word transfer unit with count up to 16384 • Auto increment of the source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed external crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 22.1184 MHz High-speed internal RC oscillator (HIRC) that can optionally be used as a system clock (variation < 2% at -40℃ ~ 105℃) • 10 kHz Low-speed internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain • RTC clock source includes Low-speed external crystal oscillator (LXT) • RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports up to 1 static tamper pins • Able to wake up CPU from any reduced power mode

	• Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and reset-ting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is gener-ated
PWM	• Twelve 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit resolution pre-scale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC • The window set by 6-bit down counter with 11-bit prescale counter • Supports 16 periods to program maximum 11-bit prescale counter

Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 16-ch 1 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Three internal channels for V_{BAT}, band-gap V_{BG} input and temperature sensor input • Supports external V_{REF} pin or internal reference voltage V_{REF} • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger. • Configurable EADC sampling time • Double data buffers for sample module 0~3 • Supports PDMA operation
Communication Interfaces	
UART	• Auto-Baud Rate measurement • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports PDMA operation
Smart Card Interface	• One set of ISO-7816-3 compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function. • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I^2C	• Two sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast

	mode plus (1 Mbps) • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function
Quad SPI	• One set of SPI Quad controller with Master/Slave mode • Master mode up to 32 MHz, and Slave mode up to 16MHz at V_{DD} =5V • Supports Dual and Quad I/O Transfer mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • Supports PDMA operation
SPI	• One set of SPI controller with Master/Slave mode • SPI provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers • Master mode up to 36 MHz, and Slave mode up to 18 MHz at VDD =5V • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • Supports PDMA operation
External Bus Interface (EBI)	• Supports up to two memory banks • Supports external devices with max 1 MB size for each chip select • 8-/16-bit data width • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting

	• Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O
Advanced Connectivity	
USB 2.0 Full Speed Dual Role (Device/Host) with on-chip transceiver	• On-chip USB 2.0 full speed transceiver **USB 2.0 Full Speed Host Controller** • Compliant with USB Revision 1.1 Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12 Mbps) and low-speed (1.5 Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous transfers • Supports an integrated Root Hub • Supports port power control and port over current detection • Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB full speed 2.0 Specification • Supports suspend function when no bus activity exists for 3 ms • 8 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 512 bytes configurable RAM for endpoint buffer • Remote wake-up capability • Start of Frame (SOF) locked clock pulse generation for crystal-less feature (48MHz internal RC oscillator for USB crystal-less only)

4 PARTS INFORMATION

4.1 M4521 USB FS Series Selection Code

M4	521	L	E	6	A	E
Core	**Series**	**Package**	**Flash Size**	**SRAM Size**	**Reserved**	**Temperature**
Cortex®-M4F	521: USB FS	L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm)	E: 128 KB	6: 32 KB		E:-40°C ~ 105°C

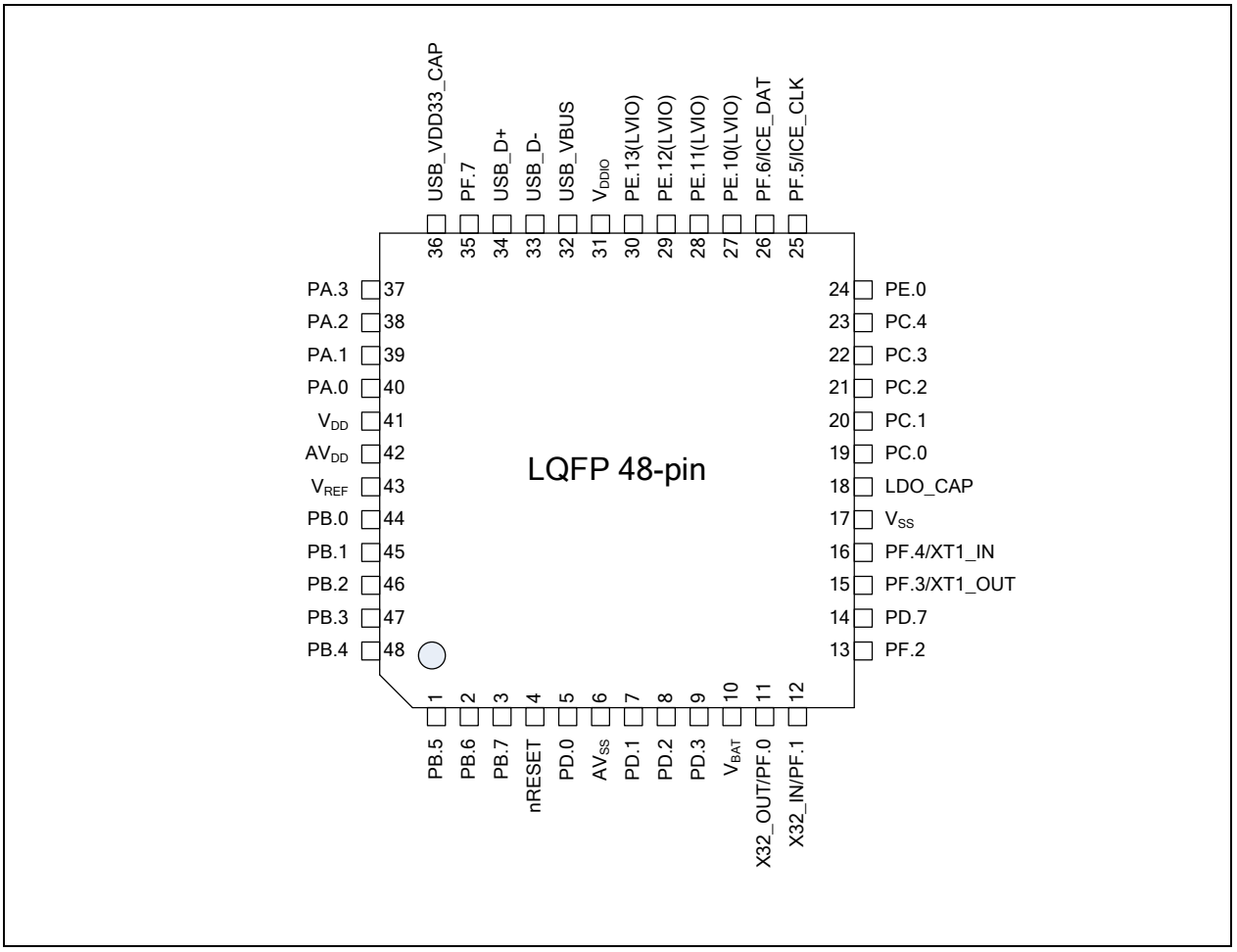
4.2 M4521 USB FS Series Selection Guide

PART NUMBER		M4521	
		LE6AE	SE6AE
Flash (KB)		128	
SRAM (KB)		32	
ISP Loader ROM (KB)		4	
I/O		35	49
32-bit Timer		4	
Tamper		1	
Connectivity	UART	3	4
	ISO-7816	1	
	SPI Master	-	
	Quad SPI	1	
	SPI	1	
	I^2S	-	
	I^2C	2	
	USCI	-	
	CAN	-	
	LIN	-	
	SDHC	-	
16-bit PWM		10	12
USB 2.0 FS Dual Role (Device/Host)		√	
12-bit ADC		10	16
External Bus Interface		√	
Package		LQFP 48	LQFP 64

5 PIN CONFIGURATION

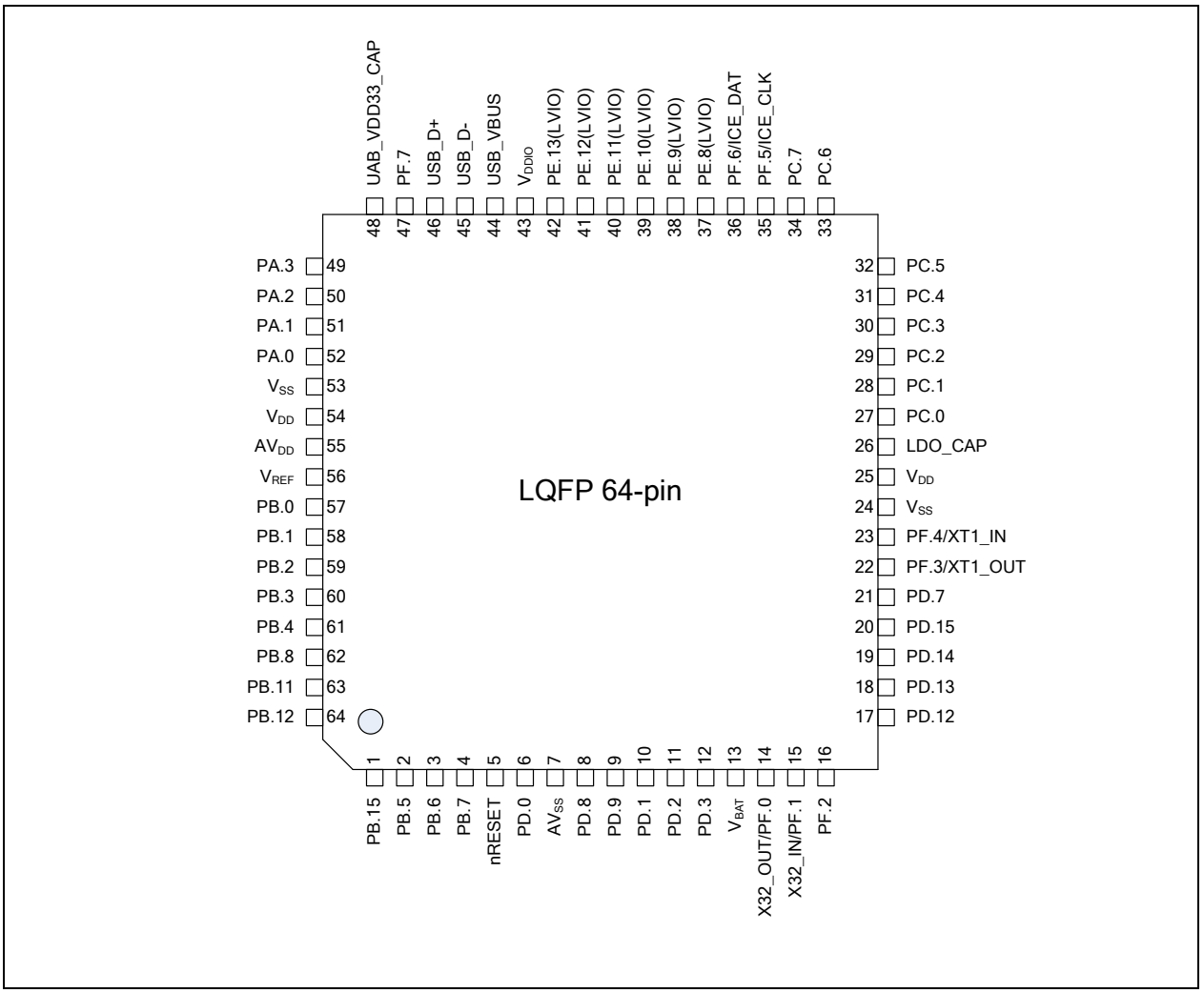
5.1 LQFP-48 Pin Diagram

Corresponding Part Number: M4521LE6AE



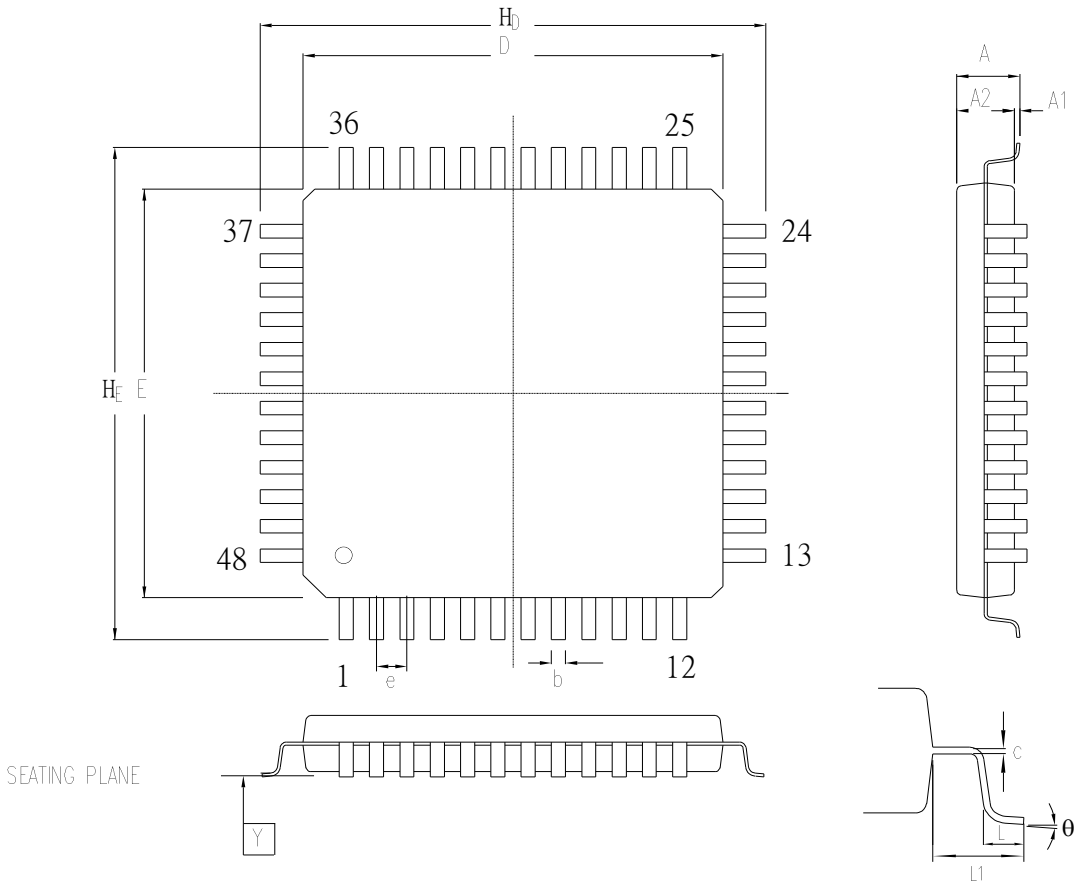
5.2 LQFP-64 Pin Diagram

Corresponding Part Number: M4521SE6AE



6 PACKAGE DIMENSION

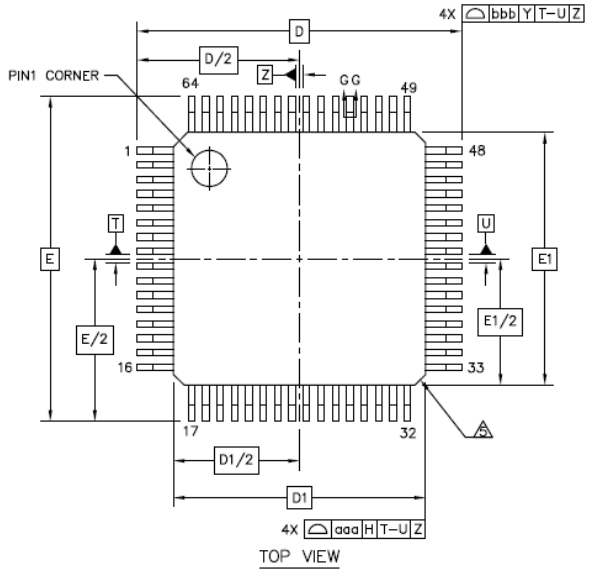
6.1 LQFP 48L (7x7x1.4 mm^3 Footprint 2.0mm)



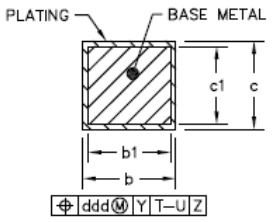
Controlling dimension : Millimeters

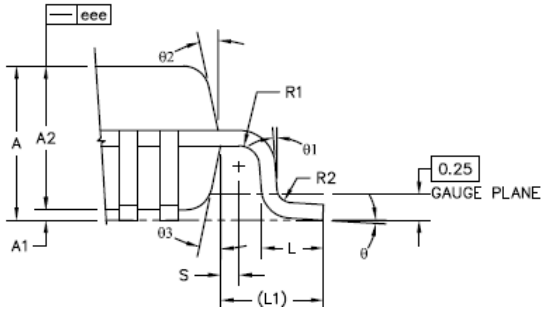
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

6.2 LQFP 64L (7x7x1.4 mm^3 Footprint 2.0mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





7 REVISION HISTORY

Date	Revision	Description
2018.11.23	1.00	Initial version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.