AK3918 HD IP Camera SoC

Specification

Version 1.0

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Document Revision History

The following table provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

VERSION	DESCRIPTION	DATE COMPLETED
1.0	Initial release	July, 2014

About This Manual

This document is the electrical and mechanical specification data sheet for the AK3918 processor. This specification contains a functional overview, mechanical data, package signal locations, electrical specifications (simulated), and bus functional waveforms.

Definitions, Acronyms, and Abbreviations

Unless otherwise specified, all the acronyms and abbreviations used in this annual are defined hereunder.

ADC	Analog to Digital Converter
AHB	Advanced High-performance Bus
ASIC	Application-Specific Integrated Circuit, refers to all the functional blocks of the processor
CMOS	Complimentary Metal-Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DDR	Double Data Rate
DMA	Direct Memory Access
DTE	Data Terminal Equipment
ECC	Error Correction Code
FIFO	First In First Out
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IrDA	Infrared Data Association
JPEG	Joint Picture Expert Group
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MAC	Media Access Control
MMC	Multimedia Card
MMU	Memory Management Unit
MPEG	Moving Picture Experts Group
MSB	Most Significant Bit
PCM	Pulse Code Modulation
PGA	Programmable Gain Amplifier
PWM	Pulse-Width Modulator
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TBD	To be determined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XTAL	Crystal

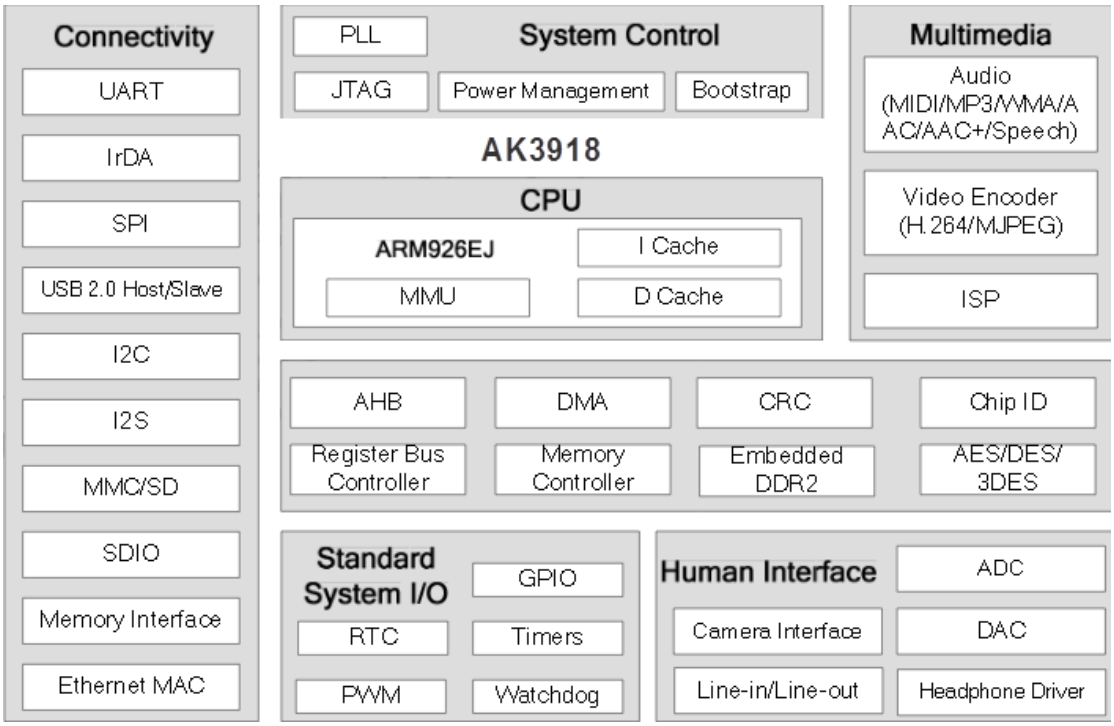
1Introduction

Newly rolled out by Anyka, AK3918 is specially designed for cost-sensitive, low power and high performance HD IP Camera applications to meet the increasing surveillance requirements of high-definition videos.

With the embedded DDR2, H.264 hardware encoder, ISP, AES/DES/3DES encryption, high performance can be easily gained by AK3918. Rich peripheral interfaces, such as MAC,MMC/SD/SDIO, UART and USB HS Host/Slave are integrated in the SoC, thus bringing amore compact system with significant reduction of system cost for HD IP Camera applications.

For applications development on AK3918, a Product Development Kit with completely development platforms and reference designs are available for customers to develop specific applications with simplest structure in a most convenient way.

AK3918 functional block diagram is shown as follows.



(Figure 1-1 AK3918 Functional Block Diagram)

1.1 Conventions

- #Abc is used to indicate a signal that is active when pulled low: for example, #Reset.
- Logic level one is a voltage that corresponds to Boolean true (1) state.
- Logic level zero is a voltage that corresponds to Boolean false (0) state.
- To set a bit or bits means to establish logic level one.
- To clear a bit or bits means to establish logic level zero.
- A signal is an electronic construct whose state conveys or changes in state convey information.
- A pin is an external physical connection. The same pin can be used to connect a number of signals.
- Asserted means that a discrete signal is in active logic state.
- Negated means that an asserted discrete signal changes logic state.
- LSB means least significant bit or bits, and MSB means most significant bit or bits. References to low and high bytes or words are spelled out.
- Numbers ended in letter B are binary. Numbers preceded by 0x are hexadecimal.

1.2 Features

To support a wide variety of applications, AK3918 boasts a robust array of features, including the following:

- ARM926EJ core, 16KB I cache and 16KB D cache
- advanced power management module
- supports little endian only
- Embedded 64MHz DDR2
- audio capability of MP3 encoder, ARM encoder, WAV encoder, Speex encoder
- MJPEG hardware encoder at 720p 30fps
- Multi-Stream encoding synchronously
- H.264 hardware encoder at 720p 30fps
- CCIR 601/CCIR 656 CMOS image sensor interface with programmable image size and smart scaling capability
- Ethernet MAC controller
- two ADCs for voice/music recording and battery measurement
- two Sigma-Delta DACs for stereo speakers

- built-in headphone driver
- I2S slave interface
- I2C master interface
- 2 UARTs, 1 has flow control
- IrDA (under NEC protocol)
- ISP
- AES/DES/3DES Encrytion
- 2 SPI (master or slave operation)
- MMC/SD interface. MMC 4.2; SD 2.0
- SDIO interface, Version 1.1
- USB 2.0 HS Host/Slave
- 64 GPIOs, 7 dedicated, 57 shared with other pins
- JTAG supporting in-circuit debugging
- on-chip PLL and 32.768KHz RTC
- 5 PWMs
- 5 General Purpose timers
- 1 watchdog timer
- 1 RTC timer
- Four bootstrap modes, boot code saved in 32KB ROM
- package: 152-pin LFBGA

1.3 Target Applications

The AK3918 is oriented at IP Camera and mobile surveillance equipments.

1.4 Product Documentation

The following document(s) is (are) required for a complete description of the AK3918 and are necessary to design properly with the device.

- AK3918 Specification

1.5 Ordering Information

PART NUMBER	PACKAGE TYPE	OPERATING VOLTAGE	ORDER NUMBER
AK3918B152	152PIN-LFBGA	I/O: 3.3V, core: 1.2V	

2 Signals and Connections

2.1 Pin Definitions

Table 2-1 identifies and describes the AK3918 signals that are assigned to package pins.

I: input; O: output; IO: input/output; PWR: power supply; GND: ground; A: analog; D: digital.PU: pull-up; PD: pull-down.

(Table 2-1 AK3918 Functional Pin Definitions)

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
A1	MIC_P	I/A	-	MIC_P	Positive input of microphone.
A2	MIC_N	I/A	-	MIC_N	Negative input of microphone.
A3	HPL	O/A	-	HPL	Left channel of Headphone output.
A4	HPR	O/A	-	HPR	Right channel of Headphone output.
A5	VCM3	O/A	-	VCM3	Third reference voltage (3.0V). To filter out noise, it is recommended to connect to a 4.7uF or a 10uF capacitor and a 0.1uF capacitor in parallel between the pin and the GND. This pin is also used as the bias voltage for microphone.
A6	BAT_RTC	I/A	-	BAT_RTC	1. Battery voltage input for RTC module. 2. Test mode signal. It must be larger than 3V in normal working state.
A7	XTAL32KO	O/D	XTAL32KI	XTAL32KO	External 32.768KHz crystal output.
A8	XTAL32KI	I/D	-	XTAL32KI	External 32.768KHz crystal input.
A9	GPIO[60]	IO/D	I/PD	GPIO[60]	GPIO[60]
A10	GPIO[59]	IO/D	I/PD	GPIO[59]	GPIO[59]
A11	GPIO[58]	IO/D	I/PD	GPIO[58]	GPIO[58]
A12	GPIO[56]/PWM5	IO/D	GPIO[56] I/PU	GPIO[56]	GPIO[56]
				PWM5	Pulse-Width Modulated output signal.
A13	CIS_D[3]	IO/D	I/PD	CIS_D[3]	Camera pixel data input.
A14	CIS_D[2]	IO/D	I/PD	CIS_D[2]	Camera pixel data input.
A15	CIS_D[1]/GPIO[9]	IO/D	CIS_D[1]	CIS_D[1]	Camera pixel data input.
			I/PD	GPIO[9]	GPIO[9]

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
A16	CIS_D[0]/GPIO[8]	IO/D	CIS_D[0] I/PD	CIS_D[0]	Camera pixel data input.
				GPIO[8]	GPIO[8]
A17	CIS_HSYNC	I/D	I/PD	CIS_HSYNC	Horizontal sync signal from camera.
B1	VREF	IO/A	-	VREF	1.5V reference voltage. It is recommended to connect to a 4.7uF capacitor between this pin and GND.
B2	VCM2	O/A	-	VCM2	Second reference voltage (1.5V). To filter out noise, it is recommended to connect to a 4.7uF or a 10uF capacitor and a 0.1ufcapacitor in parallel between the pin and the GND.
B3	Linein_R	I/A	-	Linein_R	Right channel of line in (AC coupling).
B4	AIN0	I/A	-	AIN0	A/D input node, maybe used for analog keypad.
B5	#RST	I/D	I/PU	#RST	System reset, external active low. Schmitt trigger input signal. When this signal is active, all modules (with the exception of RTC module) are reset.
B6	GPIO[57]/I2S_DIN	IO/D	GPIO[57] I/PU	GPIO[57]	GPIO[57]
				I2S_DIN	I2S serial data input.
B7	GPIO[50]/PWM3	IO/D	GPIO[50] I/PU	GPIO[50]	GPIO[50]
				PWM3	Pulse-Width Modulated output signal.
B8	GPIO[49]	I/D	I/high-z	GPIO[49]	GPIO [49] is a dedicated GPIO used for USB pull in/out detection.
B9	GPIO[4]/TDI/RXD2/PWM1	IO/D	GPIO[4] I/PU	GPIO[4]	GPIO[4]
				TDI	Debug port serial data input.
				RXD2	Receive data bit of UART 2.
				PWM1	Pulse-Width Modulated output signal.
B10	GPIO[54]/I2S_BCLK	IO/D	GPIO[54] I/PD	GPIO[54]	GPIO[54]
				I2S_BCLK	I2S bit clock.

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
B11	GPIO[48]/PWM1	IO/D	GPIO[48] I/PU	GPIO[48]	GPIO[48]
				PWM1	Pulse-Width Modulated output signal.
B12	SPI1_CLK/GPIO[26]	IO/D	GPIO[26] I/PU	GPIO[26]	GPIO[26]
				SPI1_CLK	SPI clock.
B13	CIS_D[9]/GPIO[11]	IO/D	CIS_D[9] I/PD	CIS_D[9]	Camera pixel data input.
				GPIO[11]	GPIO[11]
B14	CIS_D[7]	IO/D	I/PD	CIS_D[7]	Camera pixel data input.
B15	CIS_D[5]	IO/D	I/PD	CIS_D[5]	Camera pixel data input.
B16	VDDIO_CIS	PWR/D	-	VDDIO_CIS	-
B17	CIS_D[4]	IO/D	I/PD	CIS_D[4]	Camera pixel data input.
C1	HPVDD	PWR/A	-	HPVDD	-
C2	AIN1	I/A	-	AIN1	A/D input node, maybe used for analog keypad.
C3	Linein_L	I/A	-	Linein_L	Left channel of line in (AC coupling).
C4	AVSS	GND/A	-	AVSS	-
C5	AVCC	PWR/A	-	AVCC	-
C6	WAKEUP	O/D	O	WAKEUP	Wake Up indicator for power control processing (active high pulse indicator to Power Supply.) It is in Z (tri-state) state when it is inactive.
C7	OPCLK/GPIO[47]/PWM5		GPIO[47] I/PD	GPIO[47]	GPIO[47]
				OPCLK	Output for specific system applications.
				PWM5	Pulse-Width Modulated output signal.
C8	GPIO[3]/TMS	IO/D	GPIO[3] I/PD	GPIO[3]	GPIO[3]
				TMS	Debug port mode select.
C9	GPIO[53]/I2S_MCLK	IO/D	GPIO[53] I/PU	GPIO[53]	GPIO[53]
				I2S_MCLK	I2S main clock.
C10	#SPI1_CS/GPIO[25]	IO/D	GPIO[25] I/PU	GPIO[25]	GPIO[25]
				#SPI1_CS	SPI chip select, active low.
C11	GPIO[7]/RTCK/RTS2/PWM4	IO/D	GPIO[7] I/PU	GPIO[7]	GPIO[7]
				RTCK	Debug port output clock.
				RTS2	Request to send signal from UART2.
				PWM4	Pulse-Width Modulated output signal.

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
C12	GPIO[6]/TCLK/CTS2/PWM3	IO/D	GPIO[6] I/PU	GPIO[6]	GPIO[6]
				TCLK	Debug port clock, less than 1 MHz, asynchronous with CLK.
				CTS2	Clear to send signal of UART2.
				PWM3	Pulse-Width Modulated output signal.
C13	CIS_SCLK	O/D	I/PD	CIS_SCLK	Programmable frequency from dividing SIC CLK. It provides working clock for image sensor.
C14	CIS_PCLK	I/D	I/PD	CIS_PCLK	Pixel clock from camera.
C15	CIS_VSYNC	I/D	I/PD	CIS_VSYNC	Vertical sync signal from camera.
C16	CIS_D[8]/GPIO[10]	IO/D	CIS_D[8] I/PD	CIS_D[8]	Camera pixel data input.
				GPIO[10]	GPIO[10]
C17	CIS_D[6]	IO/D	I/PD	CIS_D[6]	Camera pixel data input.
D1	USB_DP	IO/A	-	USB_DP	USB Data pin (Data+) of USB 2.0 HS Host/Slave interface.
D2	USB_RREF	IO/A	-	OTG_RREF	External Reference pin. Connect 10K ohm external reference resistor, with 1%tolerance to analog ground.
D3	HPVSS	GND/A	-	HPVSS	-
D15	VDDIO	PWR/D	-	VDDIO	-
D16	RXD1/GPIO[1]	IO/D	GPIO[1] I/PD	RXD1	Receive data bit of UART 1.
				GPIO[1]	GPIO[1]
D17	TXD1/GPIO[2]	IO/D	GPIO[2] I/PD	TXD1	Transmit data bit of UART 1.
				GPIO[2]	GPIO[2]
E1	USB_DM	IO/A	-	USB_DM	USB Data pin (Data-).of USB 2.0 HS Host/Slave interface.
E2	AGND_USB	GND/A	-	AGND_USB	-
E3	AVSS_PLL	GND/A	-	AVSS_PLL	-
E15	VDD	PWR/D	-	VDD	-
E16	I2C_CLK/GPIO[27]	IO/D	GPIO[27] I/PU	I2C_CLK	I2C serial clock.
				GPIO[27]	GPIO[27]
E17	I2C_DAT/GPIO[28]	IO/D	GPIO[28] I/PU	I2C_DAT	I2C serial data input/output.
				GPIO[28]	GPIO[28]
F1	AVDD12_PLL	PWR/A	-	AVDD12_PLL	-

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
F2	VCCA_USB	PWR/A	-	VCCA_USB	-
F3	MCI1_MCK/GPIO[32]	IO/D	GPIO[32] I/PU	MCI1_MCK	MMC/SD operating clock.
				GPIO[32]	GPIO[32]
F6	VDDIO	PWR/D	-	VDDIO	-
F7	VSS	GND/D	-	VSS	-
F8	VSS	GND/D	-	VSS	-
F9	VSSIO	GND/D	-	VSSIO	-
F10	VSSIO	GND/D	-	VSSIO	-
F11	VDD	PWR/D	-	VDD	-
F12	VDD	PWR/D	-	VDD	-
F15	DRAM_VREF	I/A	-	DRAM_VREF	SSTL_2 reference voltage.
F16	PWM5/GPIO[30]/#SPI2_CS /I2S_MCLK	IO/D	GPIO[30] I/PD	PWM5	Pulse-Width Modulated output signal.
				GPIO[30]	GPIO[30]
				#SPI2_CS	SPI chip select, active low.
				I2S_MCLK	I2S main clock.
F17	IRDA_DI/GPIO[29]/SPI2_C LK	IO/D	GPIO[29] I/PU	IRDA_DI	IRDA data input.
				GPIO[29]	GPIO[29]
				SPI2_CLK	SPI clock.
G1	MCI1_D[3]/GPIO[36]	IO/D	GPIO[36] I/PU	MCI1_D[3]	MMC/SD data bus.
				GPIO[36]	GPIO[36]
G2	MCI1_MCMD/GPIO[31]	IO/D	GPIO[31] I/PU	MCI1_MCMD	MMC/SD command.
				GPIO[31]	GPIO[31]
G3	MCI1_D[0]/GPIO[33]	IO/D	GPIO[33] I/PU	MCI1_D[0]	MMC/SD data bus.
				GPIO[33]	GPIO[33]
G6	VSS	GND/D	-	VSS	-
G7	VSS	GND/D	-	VSS	-
G8	VSS	GND/D	-	VSS	-
G9	VSSIO	GND/D	-	VSSIO	-
G10	VSSIO	GND/D	-	VSSIO	-
G11	VDD	PWR/D	-	VDD	-
G12	VDD	PWR/D	-	VDD	-
G15	#DRAM_CS	O/D	O	#DRAM_CS	Chip select signal, active low.
G16	VDD_DDR2	PWR/D	-	VDD_DDR2	Embedded DDR2 power supply.
G17	VDD_DDR2	PWR/D	-	VDD_DDR2	Embedded DDR2 power supply.
H1	XTAL12MI	I/D	-	XTAL12MI	External 12MHz crystal input.

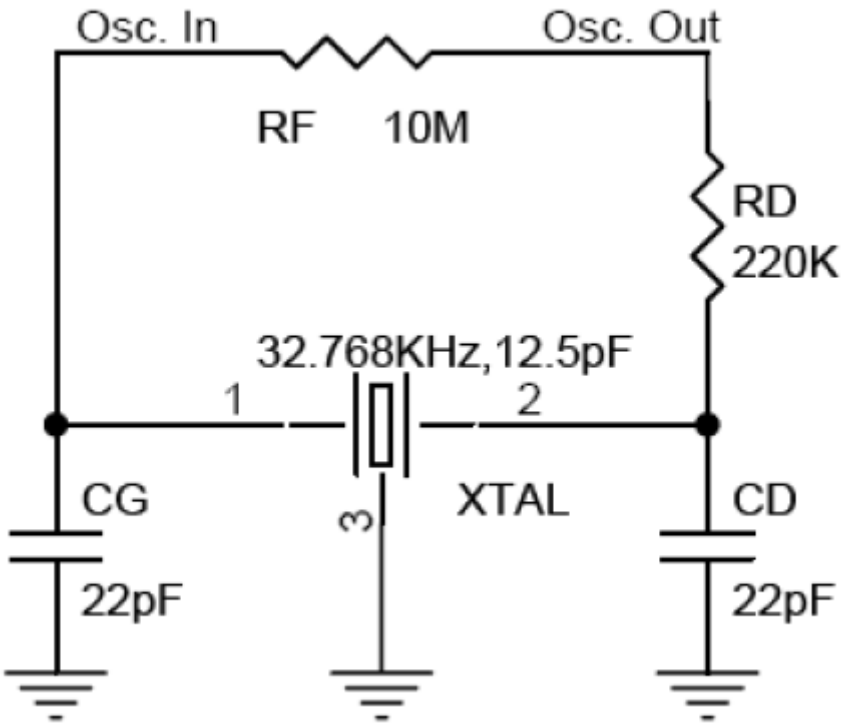
PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
H2	XTAL12MO	O/D	~XTAL12MI	XTAL12MO	External 12MHz crystal output.
H3	MCI1_D[1]/GPIO[34]	IO/D	GPIO[34] I/PU	MCI1_D[1]	MMC/SD data bus.
				GPIO[34]	GPIO[34]
H15	VDD_DDR2	PWR/D	-	VDD_DDR2	Embedded DDR2 power supply.
H16	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
H17	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
J1	MCI1_D[4]/GPIO[37]/SPI2_DIN[note4]/SPI1_DIN[note3]	IO/D	GPIO[37] I/PU	GPIO[37]	GPIO[37]
				MCI1_D[4]	MMC/SD data bus.
				SPI2_DIN	SPI data input.
				SPI1_DIN	SPI data input.
J2	MCI1_D[5]/GPIO[38]/SPI2_DOUT[note4]/SPI1_DOUT[note3]	IO/D	GPIO[38] I/PU	GPIO[38]	GPIO[38]
				MCI1_D[5]	MMC/SD data bus.
				SPI2_DOUT	SPI data output.
				SPI1_DOUT	SPI data output.
J3	MCI1_D[2]/GPIO[35]	IO/D	GPIO[35]	MCI1_D[2]	MMC/SD data bus.
			I/PU	GPIO[35]	GPIO[35]
J15	VSS_DDR2	GND/D	-	VSS_DDR2	Embedded DDR2 ground.
J16	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
J17	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
K1	MCI1_D[7]/GPIO[40]/SPI2_HOLD[note4]/SPI1_HOLD[note3]	IO/D	GPIO[40] I/PU	GPIO[40]	GPIO[40]
				MCI1_D[7]	MMC/SD data bus.
				SPI2_HOLD	SPI hold input.
				SPI1_HOLD	SPI hold input.
K2	MCI1_D[6]/GPIO[39]/SPI2_WP[note4]/SPI1_WP[note3]	IO/D	GPIO[39] I/PU	GPIO[39]	GPIO[39]
				MCI1_D[6]	MMC/SD data bus.
				SPI2_WP	SPI write protect input.
				SPI1_WP	SPI write protect input.
K3	VDDIO_MAC	PWR/D	-	VDDIO_MAC	-
K4	GMII_CRS/GPIO[18]	IO/D	GPIO[18] I/PD	GMII_CRS	Carrier sense output.
				GPIO[18]	GPIO[18]
K5	GMII_RXD[2]/GPIO[21]	IO/D	GPIO[21] I/PD	GMII_RXD[2]	GMII receive data [2].
				GPIO[21]	GPIO[21]
K6	GMII_RXCLK	I/D	I/PD	GMII_RXCLK	Receive clock output.
K7	GMII_RXD[1]/GPIO[20]	IO/D	GPIO[20] I/PD	GMII_RXD[1]	GMII receive data [1].
				GPIO[20]	GPIO[20]
K8	GMII_TXD[0]/GPIO[14]	IO/D	GPIO[14] I/PD	GMII_TXD[0]	GMII transmit data [0].
				GPIO[14]	GPIO[14]
K9	GMII_TXD[1]/GPIO[15]	IO/D	GPIO[15] I/PD	GMII_TXD[1]	GMII transmit data [1].
				GPIO[15]	GPIO[15]

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
K10	GPIO[0]/#TRST	IO/D	GPIO[0] I/PU	GPIO[0]	GPIO [0] is used for Boot Select.
				#TRST	Debug port logic reset.
K11	VSS_DDR2	GND/D	-	VSS_DDR2	Embedded DDR2 ground.
K12	VSS_DDR2	GND/D	-	VSS_DDR2	Embedded DDR2 ground.
K13	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
K14	VSS_DDR2	GND/D	-	VSS_DDR2	Embedded DDR2 ground.
K15	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
K16	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
K17	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
L1	MCI2_MCK/GPIO[42]	IO/D	GPIO[42] I/PU	MCI2_MCK	MMC/SD operating clock.
				GPIO[42]	GPIO[42]
L2	MCI2_D[0]/GPIO[43]/SPI1_HOLD[note3]/SPI2_HOLD[note4]	IO/D	GPIO[43] I/PU	MCI2_D[0]	MMC/SD data bus.
				GPIO[43]	GPIO[43]
				SPI1_HOLD	SPI hold input.
				SPI2_HOLD	SPI hold input.
L3	MCI2_MCMD/GPIO[41]	IO/D	GPIO[41] I/PU	MCI2_MCMD	MMC/SD command.
				GPIO[41]	GPIO[41]
L4	GMII_RXDV/GPIO[23]	IO/D	GPIO[23] I/PD	GMII_RXDV	Receive data valid output.
				GPIO[23]	GPIO[23]
L5	GMII_COL/GPIO[24]	IO/D	GPIO[24] I/PD	GMII_COL	Collision detect output.
				GPIO[24]	GPIO[24]
L6	GMII_MDIO/GPIO[12]	IO/D	GPIO[12] I/PD	GMII_MDIO	Management data.
				GPIO[12]	GPIO[12]
L7	XTAL25MO	O/D	Logic high	XTAL25MO	External 25MHz crystal output.
L8	GMII_TXD[3]/GPIO[17]	IO/D	GPIO[17] I/PD	GMII_TXD[3]	GMII transmit data [3].
				GPIO[17]	GPIO[17]
L9	GMII_TXCLK	I/D	MII_TXCLKI/PD	GMII_TXCLK	Transmit clock output.
L10	GMII_TXEN	O/D	MII_TXENI/PD	GMII_TXEN	Transmit data enable.
L11	GPIO[5]/TDO/TXD2/PWM2	IO/D	GPIO[5]	GPIO[5]	GPIO[5]
			I/PU	TDO	Debug port serial output.
				TXD2	Transmit data bit of UART 2.
				PWM2	Pulse-Width Modulated output signal.

PIN	PIN NAME	TYPE	RESET	PIN MUX	DESCRIPTION
L12	GPIO[52]/I2S_DOUT	IO/D	GPIO[52] I/PU	GPIO[52]	GPIO[52]
				I2S_DOUT	I2S serial data output.
L13	GPIO[61]	IO/D	I/PD	GPIO[61]	GPIO[61]
L14	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
L15	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
L16	VSSIO_DRAM	GND/D	-	VSSIO_DRAM	-
L17	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
M1	MCI2_D[3]/GPIO[46]/SPI1_DIN[note3]/SPI2_DIN[note4]	IO/D	GPIO[46] I/PU	MCI2_D[3]	MMC/SD data bus.
				GPIO[46]	GPIO[46]
				SPI1_DIN	SPI data input.
				SPI2_DIN	SPI data input.
M2	MCI2_D[2]/GPIO[45]/SPI1_DOUT[note3]/SPI2_DOUT[note4]	IO/D	GPIO[45] I/PU	MCI2_D[2]	MMC/SD data bus.
				GPIO[45]	GPIO[45]
				SPI1_DOUT	SPI data output.
				SPI2_DOUT	SPI data output.
M3	MCI2_D[1]/GPIO[44]/SPI1_WP[note3]/SPI2_WP[note4]	IO/D	GPIO[44] I/PU	MCI2_D[1]	MMC/SD data bus.
				GPIO[44]	GPIO[44]
				SPI1_WP	SPI write protect input.
				SPI2_WP	SPI write protect input.
M4	GMII_CLK	O/D	I/PD	GMII_CLK	Management clock reference.
M5	GMII_INT/GPIO[13]	IO/D	GPIO[13] I/PD	GMII_INT	Interrupt output.
				GPIO[13]	GPIO[13]
M6	GMII_RXD[0]/GPIO[19]	IO/D	GPIO[19] I/PD	GMII_RXD[0]	GMII receive data [0].
				GPIO[19]	GPIO[19]
M7	XTAL25MI	I/D	-	XTAL25MI	External 25MHz crystal input.
M8	GMII_RXD[3]/GPIO[22]	IO/D	GPIO[22] I/PD	GMII_RXD[3]	GMII receive data [3].
				GPIO[22]	GPIO[22]
M9	GMII_TXD[2]/GPIO[16]	IO/D	GPIO[16] I/PD	GMII_TXD[2]	GMII transmit data [2].
				GPIO[16]	GPIO[16]
M10	GPIO[62]	IO/D	I/PD	GPIO[62]	GPIO[62]
M11	GPIO[63]	IO/D	I/PD	GPIO[63]	GPIO[63]
M12	GPIO[51]/PWM4	IO/D	GPIO[51] I/PD	GPIO[51]	GPIO[51]
				PWM4	Pulse-Width Modulated output signal.
M13	GPIO[55]/I2S_LRCLK	IO/D	GPIO[55] I/PD	GPIO[55]	GPIO[55]
				I2S_LRCLK	I2S channel selection.
M14	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
M15	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
M16	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-
M17	VDDIO_DRAM	PWR/D	-	VDDIO_DRAM	-

Notes:

1. GPIO [49] is a dedicated GPIO used for USB pull in/out detection.
2. Except for pin #RST, for all pins with pull-up or pull-down function, their pull-up resistance range and pull-down resistance range is (62 ~ 112 Kohm) and (58 ~ 156Kohm)respectively. The pull-up resistance of pin #RST is 80Kohm.
3. SPI1 signals (including SPI1_DIN, SPI1_DOUT, SPI1_WP and SPI1_HOLD) can be respectively shared with GPIO [37:40] or GPIO [46:43] and configurable by software.
4. SPI2 signals (including SPI2_DIN, SPI2_DOUT, SPI2_WP and SPI2_HOLD) can be respectively shared with GPIO [37:40] or GPIO [46:43] and configurable by software.
5. Recommended circuit of the 32K crystal:



6. Table 2-2 shows the drive strength of GPIO

（Table 2-2 AK3918 GPIO Drive Strength）

PARAMETER	GPIO	DRIVE STRENGTH		
		MINIMUM	TYPICAL	MAXIMUM
Low level output current (VOL = 0.4V)	GPIO[7:0]	-	6.6mA	-
	GPIO[63:8]	-	13.3mA	-
High level output current (VOH = 2.4V)	GPIO[7:0]	-	9.6mA	-
	GPIO[63:8]	-	19.2mA	-

Table 2-3 classifies the AK3918 signals according to different modules.

（Table 2-3 AK3918 Functional Pin Classification）

Notes：

1. There are 5 VDD in total.
2. There are 2 VDDIO in total.
3. There are 8 VDDIO_DRAM in total.
4. There are 8 VSSIO_DRAM in total.
5. There are 5 VSS in total.
6. There are 4 VSSIO in total.
7. There are 4 VSS_DDR2 in total.
8. There are 3 VDD_DDR2 in total.

Module	PIN NAME
1. SAR ADC (3)	AIN0
	AIN1
	BAT_RTC
2. Audio Analog Interface (9)	HPL
	HPR
	MIC_P
	MIC_N
	Linein_L
	Linein_R
	VREF
	VCM2
	VCM3
3. Memory Interface (2)	DRAM_VREF
	#DRAM_CS
4. I2C (2)	I2C_CLK
	I2C_DAT
5. JTAG(6)	TMS
	TDI
	TDO
	#TRST
	TCLK
	RTCK
6. MCI1 Interface (10)	MCI1_MCMD
	MCI1_MCK
	MCI1_D[7:0]
7. MCI2 Interface (6)	MCI2_MCMD
	MCI2_MCK
	MCI2_D[3:0]

Module	PIN NAME
8. System Control (9)	WAKEUP
	#RST
	XTAL_32KI
	XTAL_32KO
	XTAL12MI
	XTAL12MO
	XTAL25MI
	XTAL25MO
	OPCLK
9. I2S(5)	I2S_MCLK
	I2S_DOUT
	I2S_DIN
	I2S_BCLK
	I2S_LRCLK
10.Camera (15)	CIS _SCLK
	CIS_PCLK
	CIS_HSYNC
	CIS_VSYNC
	VDDIO_CIS
	CIS_D[9:0]
11. IrDA (1)	IRDA_DI
12. PWM (5)	PWM1
	PWM2
	PWM3
	PWM4
	PWM5

Module	PIN NAME
13. USB Interface (3)	USB_DP
	USB_DM
	USB_RREF
14. SPI (12)	#SPI1_CS
	SPI1_CLK
	SPI1_DIN
	SPI1_DOUT
	SPI1_WP
	SPI1_HOLD
	#SPI2_CS
	SPI2_CLK
	SPI2_DIN
	SPI2_DOUT
	SPI2_WP
	SPI2_HOLD
15. GPIO (64)	GPIO[63:0]
16. UART (6)	TXD1
	RXD1
	TXD2
	RXD2
	CTS2
	RTS2
17. MAC (17)	GMII_CLK
	GMII_MDIO
	GMII_INT
	GMII_TXEN
	GMII_TXCLK
	GMII _TXD[3:0]
	GMII_CRS
	GMII_RXCLK
	GMII_RXD[3:0]
	GMII_RXDV
	GMII_COL
18. Power and Grounds (49)	VDD[note1](5)
	VDDIO[note2](2)
	VDDIO_DRAM[note3](8)
	VSSIO_DRAM[note4] (8)
	VDDIO_MAC
	VDDIO_CIS
	AVSS
	AVCC

Module	PIN NAME
18. Power and Grounds (49)	AGND_USB
	VCCA_USB
	AVDD12_PLL
	AVSS_PLL
	HPVDD
	HPVSS
	VSS[note5] (5)
	VSSIO[note6](4)
	VSS_DDR2[note7](4)
	VDD_DDR2[note8] (3)

2.2 Shared-pin List

（Table 2-4 Shared-pin List）

MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	RESET STATE
JTAG	#TRST	GPIO	GPIO[0]	-	-	-	-	GPIO[0]
UART	RXD1	GPIO	GPIO[1]	-	-	-	-	GPIO[1]
UART	TXD1	GPIO	GPIO[2]	-	-	-	-	GPIO[2]
JTAG	TMS	GPIO	GPIO[3]	-	-	-	-	GPIO[3]
JTAG	TDI	GPIO	GPIO[4]	UART	RXD2	PWM	PWM1	GPIO[4]
JTAG	TDO	GPIO	GPIO[5]	UART	TXD2	PWM	PWM2	GPIO[5]
JTAG	TCLK	GPIO	GPIO[6]	UART	CTS2	PWM	PWM3	GPIO[6]
JTAG	RTCK	GPIO	GPIO[7]	UART	RTS2	PWM	PWM4	GPIO[7]
Camera	CIS_D[0]	GPIO	GPIO[8]	-	-	-	-	CIS_D[0]
Camera	CIS_D[1]	GPIO	GPIO[9]	-	-	-	-	CIS_D[1]
Camera	CIS_D[8]	GPIO	GPIO[10]	-	-	-	-	CIS_D[8]
Camera	CIS_D[9]	GPIO	GPIO[11]	-	-	-	-	CIS_D[9]
MAC	GMII_MDIO	GPIO	GPIO[12]	-	-	-	-	GPIO[12]
MAC	GMII_INT	GPIO	GPIO[13]	-	-	-	-	GPIO[13]
MAC	GMII_TXD[0]	GPIO	GPIO[14]	-	-	-	-	GPIO[14]
MAC	GMII_TXD[1]	GPIO	GPIO[15]	-	-	-	-	GPIO[15]
MAC	GMII_TXD[2]	GPIO	GPIO[16]	-	-	-	-	GPIO[16]
MAC	GMII_TXD[3]	GPIO	GPIO[17]	-	-	-	-	GPIO[17]
MAC	GMII_CRS	GPIO	GPIO[18]	-	-	-	-	GPIO[18]
MAC	GMII_RXD[0]	GPIO	GPIO[19]	-	-	-	-	GPIO[19]
MAC	GMII_RXD[1]	GPIO	GPIO[20]	-	-	-	-	GPIO[20]
MAC	GMII_RXD[2]	GPIO	GPIO[21]	-	-	-	-	GPIO[21]
MAC	GMII_RXD[3]	GPIO	GPIO[22]	-	-	-	-	GPIO[22]
MAC	GMII_RXDV	GPIO	GPIO[23]	-	-	-	-	GPIO[23]
MAC	GMII_COL	GPIO	GPIO[24]	-	-	-	-	GPIO[24]
SPI	#SPI1_CS	GPIO	GPIO[25]	-	-	-	-	GPIO[25]
SPI	SPI1_CLK	GPIO	GPIO[26]	-	-	-	-	GPIO[26]
I2C	I2C_CLK	GPIO	GPIO[27]	-	-	-	-	GPIO[27]
I2C	I2C_DAT	GPIO	GPIO[28]	-	-	-	-	GPIO[28]
SPI	SPI2_CLK	GPIO	GPIO[29]	IrDA	IRDA_DI	SPI	SPI2_CLK	GPIO[29]
SPI	#SPI2_CS	GPIO	GPIO[30]	I2S	I2S_MCLK	PWM	PWM5	GPIO[30]
MCI1	MCI1_MCMD	GPIO	GPIO[31]	-	-	-	-	GPIO[31]
MCI1	MCI1_MCK	GPIO	GPIO[32]	-	-	-	-	GPIO[32]
MCI1	MCI1_D[0]	GPIO	GPIO[33]	-	-	-	-	GPIO[33]

MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	MODULE	PIN NAME	RESET STATE
MCI1	MCI1_D[1]	GPIO	GPIO[34]	-	-	-	-	GPIO[34]
MCI1	MCI1_D[2]	GPIO	GPIO[35]	-	-	-	-	GPIO[35]
MCI1	MCI1_D[3]	GPIO	GPIO[36]	-	-	-	-	GPIO[36]
MCI1	MCI1_D[4]	GPIO	GPIO[37]	SPI	SPI1_DIN note1	SPI	SPI1_ DIN note1	GPIO[37]
MCI1	MCI1_D[5]	GPIO	GPIO[38]	SPI	SPI1_ DOUT note1	SPI	SPI1_ DOUT note1	GPIO[38]
MCI1	MCI1_D[6]	GPIO	GPIO[39]	SPI	SPI1_WP note1	SPI	SPI1_ WP note1	GPIO[39]
MCI1	MCI1_D[7]	GPIO	GPIO[40]	SPI	SPI1_ HOLD note1	SPI	SPI1_ HOLD note1	GPIO[40]
MCI2	MCI2_ MCMD	GPIO	GPIO[41]	-	-	-	-	GPIO[41]
MCI2	MCI2_MCK	GPIO	GPIO[42]	-	-	-	-	GPIO[42]
MCI2	MCI2_D[0]	GPIO	GPIO[43]	SPI	SPI1_ HOLD note1	SPI	SPI1_ HOLD note1	GPIO[43]
MCI2	MCI2_D[1]	GPIO	GPIO[44]	SPI	SPI1_WP note1	SPI	SPI1_WP note1	GPIO[44]
MCI2	MCI2_D[2]	GPIO	GPIO[45]	SPI	SPI1_ DOUT note1	SPI	SPI1_ DOUT note1	GPIO[45]
MCI2	MCI2_D[3]	GPIO	GPIO[46]	SPI	SPI1_DIN note1	SPI	SPI1_DIN note1	GPIO[46]
System Control	OPCLK	GPIO	GPIO[47]	PWM	PWM5	-	-	GPIO[47]
PWM	PWM1	GPIO	GPIO[48]	-	-	-	-	GPIO[48]
PWM	PWM2	GPIO	GPIO[49]	-	-	-	-	GPIO[49]
PWM	PWM3	GPIO	GPIO[50]	-	-	-	-	GPIO[50]
PWM	PWM4	GPIO	GPIO[51]	-	-	-	-	GPIO[51]
I2S	I2S_DOUT	GPIO	GPIO[52]	-	-	-	-	GPIO[52]
I2S	I2S_MCLK	GPIO	GPIO[53]	-	-	-	-	GPIO[53]
I2S	I2S_BCLK	GPIO	GPIO[54]	-	-	-	-	GPIO[54]
I2S	I2S_LRCLK	GPIO	GPIO[55]	-	-	-	-	GPIO[55]
PWM	PWM5	GPIO	GPIO[56]	-	-	-	-	GPIO[56]
I2S	I2S_DIN	GPIO	GPIO[57]	-	-	-	-	GPIO[57]

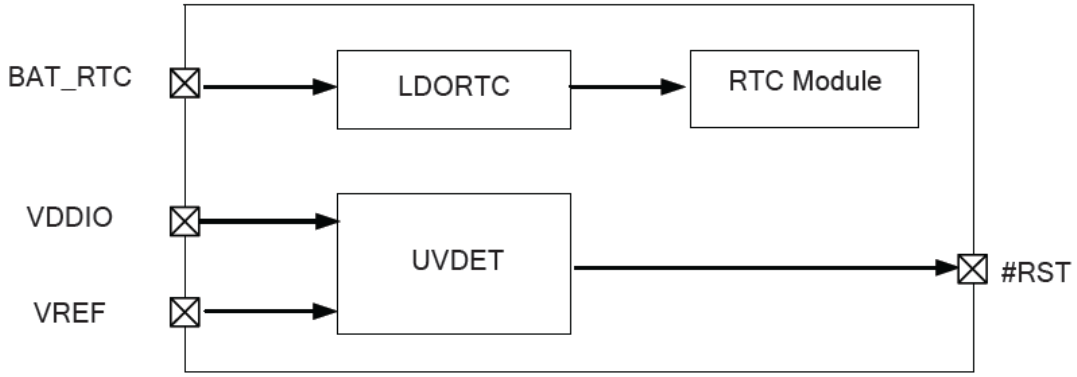
Notes:

1. SPI1 signals (including SPI1_DIN, SPI1_DOUT, SPI1_WP and SPI1_HOLD) can be respectively shared with GPIO [37:40] or GPIO [46:43] and configurable by software.
2. SPI2 signals (including SPI2_DIN, SPI2_DOUT, SPI2_WP and SPI2_HOLD) can be respectively shared with GPIO [37:40] or GPIO [46:43] and configurable by software.

3 Functional Description

3.1 PMU

AK3918 power supply is provided by external PMU and on-chip PMU only provides SOC RTC power supply. It also integrates 32K RC oscillator for none 32K crystal oscillator case.



（**Figure 3-1 PMU block diagram**）

3.1.1 Architecture

3.1.1.1 On-chip LDORTC

On-chip LDORTC will provide 1.2v power rail for RTC. The output of on-chip LDORTC cannot be configured. LDORTC is always on.

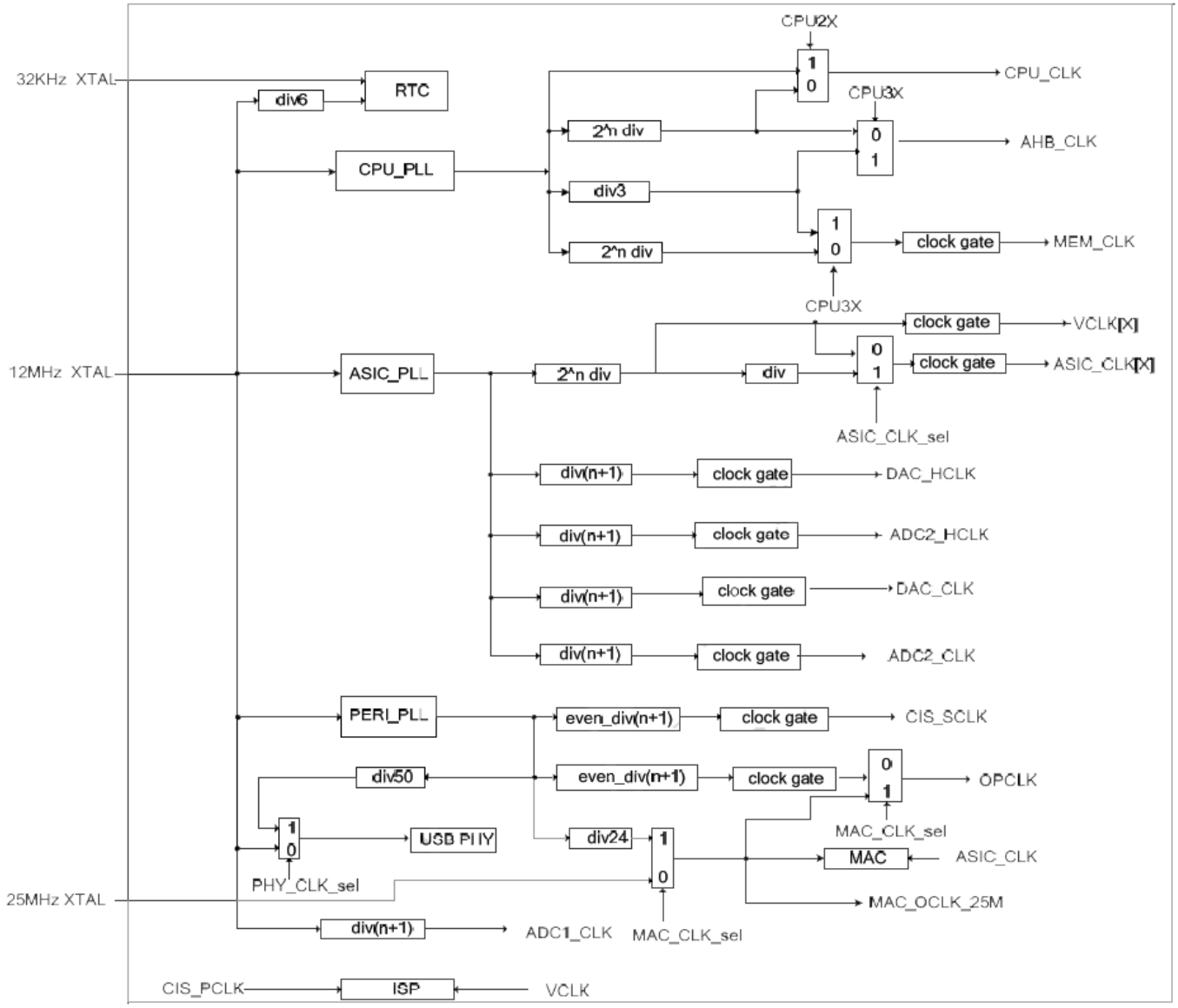
3.1.1.2 UVDET

On-chip under voltage detector detects I/O power. The threshold of under voltage detector from high to low is 2.4v, and from low to high is 2.56v.

3.2 System Control

3.2.1 Clock Generation and Control

Figure 3-2 illustrates the internal clock generation and control of the AK3918 processor. In normal operation, the AK3918 accepts a 32.768 KHz crystal, a 12MHz crystal and a 25MHzcrystal. The first one is input from the pin XTAL32KI and generates a precise clock for the RTC module; the second one is input from the pin XTAL12MI and generates working clocks for all the modules with the exception of RTC and Ethernet MAC; the third one is input from the pin XTAL25MI and generates working clock for Ethernet MAC module.



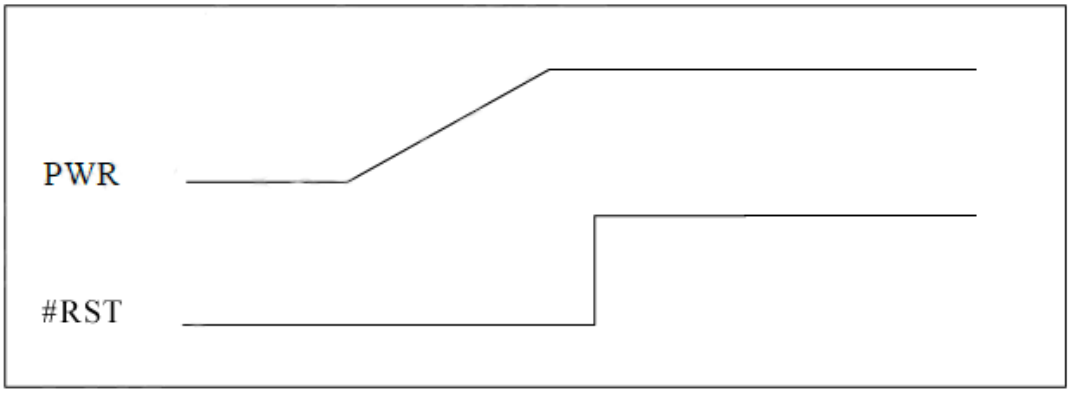
（**Figure 3-2 Clock Generation and Control**）

Notes:

1. CPU_CLK is the working frequency of CPU core. It may be equal to CPU_PLL_CLK or CPU_HCLK.
2. AHB_CLK is the working frequency of ARM Arbiter and AHB Asynchronous Bridge. It is equal to CPU_PLL_CLK/3 or CPU_HCLK.
3. MEM_CLK is working frequency of Memory Controller. It is equal to CPU_PLL_CLK/3 or CPU_DCLK.
4. VCLK[X], X = 0, 1, 2. In which, VCLK[0] is the working frequency of AHB Asynchronous Bridge, VCLK [1] is the working frequency of ISP, and VCLK [2] is the working frequency of Video Encoder.
5. ASIC_CLK[X] is the working frequency of all functional blocks with the exception of CPU core, memory controller, and camera, Video Encoder, ISP, ADCs and DACs. The working frequency for a given functional block is programmable. (Please see details in specific chapters.)
6. DAC_CLK and DAC_HCLK are the working frequency of Audio DAC.
7. ADC2_CLK and ADC2_HCLK are the working frequency of Audio ADC.
8. ADC1_CLK is the working frequency of SAR ADC, which is used for battery measurement, analog button and general purpose.
9. CIS_SCLK provides the working frequency for Image Sensor.
10. CIS_PCLK provides the working frequency for ISP to capture pixel data.
11. OPCLK is output for specific system applications when required. It may be equal to MAC_OCLK_25M.
12. MAC_OCLK_25M is the working frequency of MAC. It is equal to the external 25M crystal or 25M Clock divided from PERI_PLL_CLK.

3.2.2 Reset Module

The #RST signal, when asserted low, puts all internal states (with the exception of RTC module) into predefined values. Figure 3-3 shows the reset timing of AK3918.



（Figure 3-3 AK3918 Power on Reset Timing）

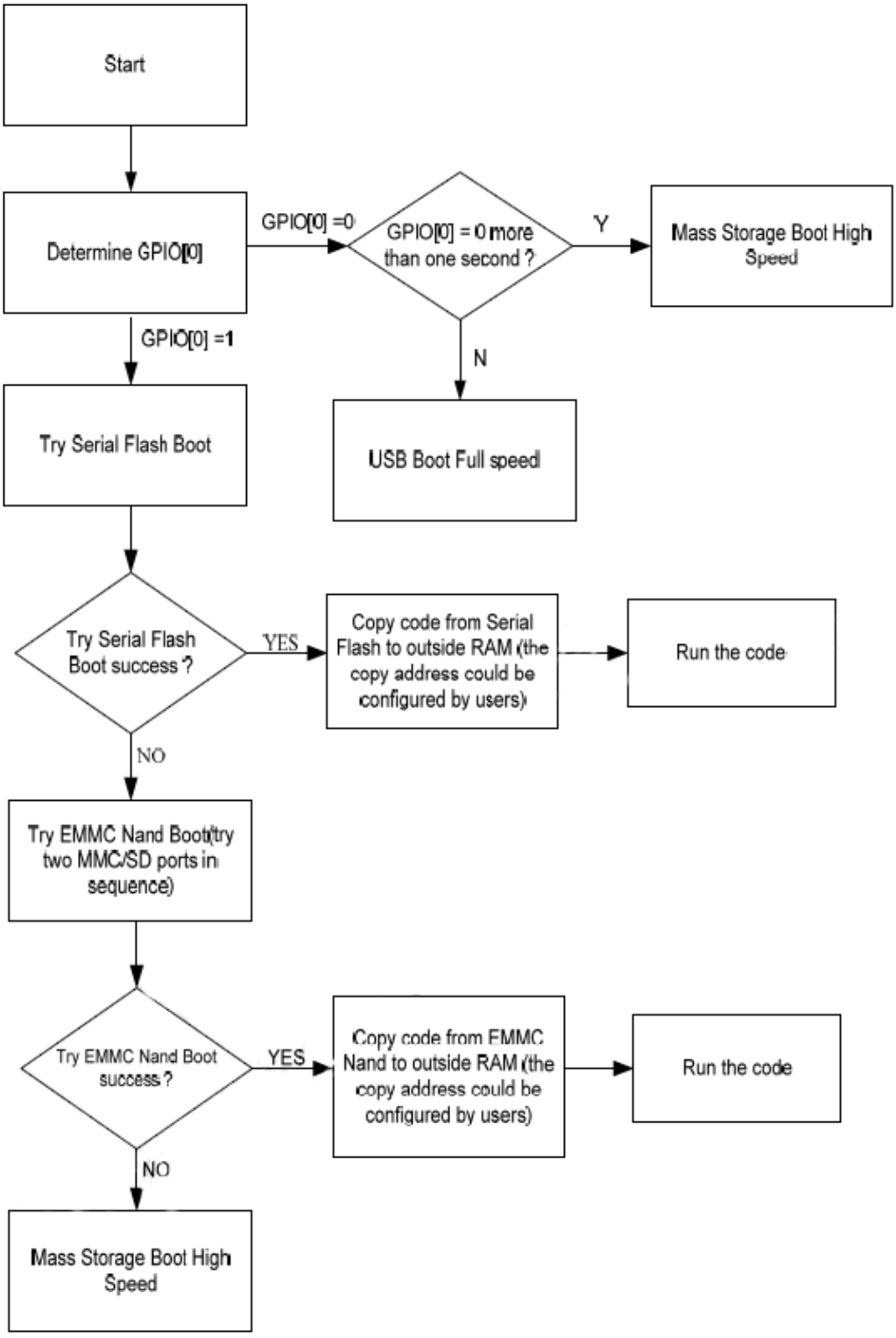
Notes:
AK3918 processor integrates VDDIO low voltage reset function. When the I/O voltage VDDIO (3.3V) drops below 2.4V, the chip resets.
Moreover, each module contained in the AK3918 processor can be reset independently by software.

3.2.3 Interrupt Module

The interrupt module collects interrupt requests from the ASICs and provides an interface to the CPU core.

3.2.4 Bootstrap Module

When the AK3918 processor is reset, all ASIC units except GPIOs, UART1 and JTAG are disabled, and the CPU core gets its first instruction from address 32’0x0000,0000, which belongs to the on-chip ROM address space. It first reads the value of GPIO [0] to judge the boot up mode. If GPIO [0] is set as “0” for more than one second, AK3918 is boot up from mass storage; if GPIO [0] is set as “0” for less than one second, it is boot up from USB port. If GPIO [0] is set as “1”, AK3918 tries Serial Flash boot and eMMC Nand boot in succession. If none of the devices meet the conditions, AK3918 is boot up from mass storage.
Notes: GPIO [0] can be used as general purpose output ports after the system has been booted up from mass storage/USB port.



A. Boot from Mass Storage

USB Mass Storage Boot is the same as the USB Boot, except one point. If the user uses the USB Mass Storage Boot, it doesn't need to install the PC USB driver, but if using USB Boot, Anyka's PC USB driver must be installed.

This mode provides the following function:

1) Loads user testing program to external memory through USB port;
2) Sets the data of memory or register;
3) Directs CPU to go to external memory and start running.

B. Boot from USB port

This program does the following:
1) Loads user testing program to external memory through USB port;
2) Sets the data of memory or register;
3) Directs CPU to go to external memory and start running.

Notes: This program does not initialize the external RAM. Therefore, programmers should initialize it first if external RAM is deployed.

C. Boot from Serial Flash

In this case, the program initializes the SPI1 interface, reads password and checks whether the password is right. If it is right, CPU copies the boot program from serial Flash to external RAM, and then runs the boot program.

Notes:
a) The external Serial Flash should support SPI mode and work in SPI mode.
b) Consecutive-read command format should be: 0x03 + Address Period 0 + [Address Period1] + Address Period 2 + Address Period 3. (The content in square brackets is optional).
c) The address counter must increase by degrees automatically when the address is consecutively read.
d) Prior to Serial Flash boot, programmers should configure corresponding register(s) to enable the pins to be used as those of SPI controller.

D. Boot from eMMC Nand

In this case, the program initializes the MCI interface, reads password and checks whether the password is right. If it is right, CPU copies the boot program from eMMC Nand to external RAM, and then runs the boot program. It should be noted that the boot information should be stored in the third block of eMMC Nand.

3.2.5 Power Management Capability

AK3918 implements a simple and powerful power control mechanism, unit clock enable. During normal operation, only the clock for CPU and the memory controller is turned on; other ASICs' working clocks are turned off. An accelerator is clocked on only when it is needed, and it is immediately clocked off after its use has been finished. All internal memories are in LOWPOWER state, except when they are accessed.

3.2.6 Working Modes

There are three working modes for the AK3918 processor:

1) **Normal operating**

All the functional blocks are clocked on/off in accordance with specific operating requirement.

2) **Standby**

The RTC module is clocked on, PLL is powered down and other modules (including CPU core)are clocked off.

3) **Power down**

The RTC module is powered on, and other modules (including CPU) are powered down.

3.2.7 JTAG

JTAG is AK3918's major software debugging tool. The JTAG of AK3918 supports breakpoints, controlling, monitoring and real-time running otherwise.

3.3 RTC Module

The RTC module accepts solely the working clock from external 32.768 KHz crystal. While the system is powered off, it may be driven by the backup battery.

The RTC module provides following functions:

- ·real-time clock
- ·alarms or wake-up signals in standby mode
- ·alarms in power down mode
- ·interrupts in normal operating mode
- ·a watchdog timer
- ·a RTC timer
- ·watchdog event interrupt output

An alarm or an interrupt may be set by accessing corresponding registers and loading the exact time that the alarm/interrupt should be generated.

The AK3918 processor can be woken up on one of the following two conditions:

1) 32.768 KHz clock alarm time is met;

2) wake-up signal is valid.

Notes:

a) AK3918 contains 32 GPIO wake-up ports, namely, GPIO [57], GPIO [55:47], GPIO [44:39], GPIO [30:27], GPIO [22], GPIO [14:12] and GPIO [7:0] and other wake-up sources, including Ain0, Ain1, USB Host/Slave DP, RTC timer and RTC interrupt.

b) Wake-up signal may be rising triggered or falling triggered.

3.4 CPU core

The CPU core is a microprocessor named ARM926EJ from ARM Limited. The ARM926EJprocessor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ processor supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density. The ARM926EJ processor includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead. The ARM926EJ processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ processor has a Harvard cached architecture and provides a complete high performance processor subsystem, including:

- ·an ARM926EJ integer core
- ·a Memory Management Unit (MMU)
- ·separate instruction and data AMBA AHB bus interfaces

3.5 Memory

3.5.1 On Chip Memory

3.5.1.1 ROM

To improve the AK3918's performance, 32KB ROM is added to for booting the CPU aftereach reset.

3.5.1.2 L2 Memory

L2 memory provides a 1344 x 32 bits buffer for data transfer between two kinds of interfaces and between external memory and a kind of interface.
Its features are as follows:

- ·17 blocks
- ·32-bit data width
- ·fixed priority
- ·supporting data transfer to/from external memory by DMA mode
- ·supporting data transfer between two blocks
- ·CPU can access directly by AHB bus (addresses from 0x4800, 0000 to 0x4800, 14FF)
- ·used as system status and command cache when the processor is booted or in stand by mode

3.5.2 RAM Controller

The RAM controller is the bridge logic that connects an internal unit to the embedded 64MB DDR2.

Its features are as follows:

- ·supporting 16-bit data bus width
- ·RAM controller working clock up to 180MHz
- ·one ODT control pin for DDR2
- ·one chip select only
- ·single-end DQS only
- ·sequential burst type only
- ·4-beat burst length only
- ·configurable CAS latency (2, 2.5, 3, 4, 5 or 6)
- ·DDR2 does not support Additive Latency

3.6 CRC Module

CRC, Cyclic Redundancy Check, is a common technique for detecting data transmission errors. This module can generate CRC code appended onto and sent with the data to be transferred; or recalculate the CRC code and compare it with those appended onto the received data to check whether the received data is correct or not.

Its features are as follows:

- ·serial cyclic code generator and checker
- ·parameterized polynomial length, ranging from 3 bits to 32 bits
- ·parameterized polynomial coefficients
- ·supporting big endian and small endian
- ·checking the data stored in L2 memory only
- ·supporting high-order alignment only

3.7 Advanced High-performance Bus (AHB)

The AHB is a kind of high performance bus for burst data transfer. AK3918 provides one AHB channel for CPU access.

When the CPU wants to access the memory, including the embedded 64MB DDR2 and registers, it sends AHB commands to the corresponding memory controller. Then the memory controller translates the AHB commands into the signals to its module and generates the memory or register access signals to realize loading or storing data.

AHB write and read timing are fully compliant with *AMBA AHB Protocol.*

3.8 Register Bus Controller

The register bus controller translates AHB (Advanced High-performance Bus) transactions targeted at register space into simple WRITE and READ pulses. To simplify the interface design with AHB of CPU core, each register access is carried out in minimum 2 clock cycles.

3.9 I2S Interface

I2S is a popular 3-wire serial bus standard protocol for transmission of 2 channel (stereo) Pulse Code Modulation digital data, where each audio sample is sent MSB first.
The I2S interface supports two kinds of working modes:
1) I2S transmitter slave mode
In this mode, the AK3918 accepts the BCLK and LRCLK signals and outputs the data from DAC controller to the external DAC via the I2S interface. The word length ranges from 4 bits to 24 bits, which is configured by DAC controller. If the word length of external DAC is more than 24 bits, 0s are added to the end of LSB.

2) I2S receiver slave mode
In this mode, the AK3918 accepts the BCLK signal, LRCLK signal and the data from external ADC via the I2S interface. The word length ranges from 3 bits to 16 bits, which is configured by ADC controller. If the word length of external ADC is more than 16 bits, the LSBs are ignored.

A programmable clock output (MCLK) is also provided for external DAC/ADCs.

3.9.1 Typical Applications

3.9.1.1 Transmitter modes

When I2S interface works in transmitter master mode or transmitter slave mode, I2S interface is the bridge connecting DAC controller and off-chip DAC(s).

3.9.1.2 Receiver Mode

When I2S interface works in receiver slave mode, I2S interface is the bridge connecting internal ADC controller and off-chip ADC.

3.10 Video Processor

The video processor of AK3918 provides hardware acceleration to the compression of videos. It supports MJPEG hardware encoder, H.264 hardware encoder and multi-stream encoding synchronously.

3.11 ISP Interface

The ISP (Image Sensor Processor) module of AK3918 is designed mainly to support 16Mlarge image photograph and 720P@30fps.

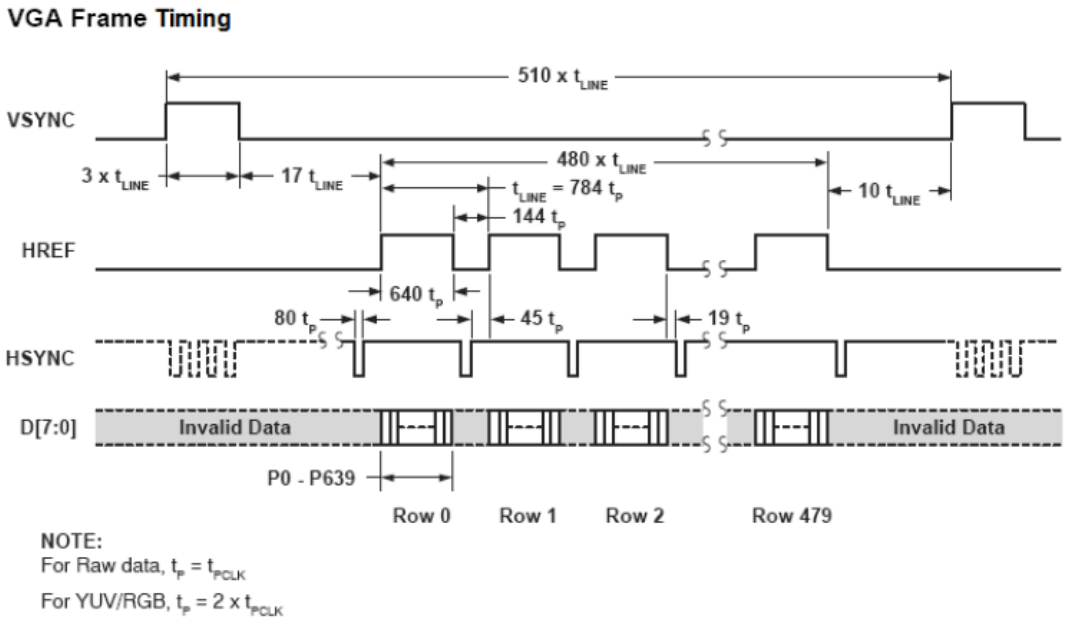
The features of ISP are as follows:

- ·compatible with CCIR 601 and CCIR 656
- ·supporting CMOS/CCD Sensor which output 8/10 Bayer RGB Data (10-bitconfiguration, for 8-bit input, fill the least 2 bits with 0s)
- ·minimum input/output image: 64 pixels (16x4, 8x8)
- ·maximum image size: 4095*4095
- ·supporting single frame capture mode(including large image mode and small image mode) as well as continuous capture mode
- ·supporting RGB Sensor in the order of RGGB, GRBG, GBRG and BGGR. Cut torealize format matching if the input RAW format is different from the expected format.
- ·supporting DMA output of YUV420 only
- ·supporting camera with YUV 422 (CCIR601, CCIR656) format input
- ·supporting camera with JPEG (CCIR601) compressed image input
- ·system supports clock opening and closing of sub-module
- ·supporting image downscaler (1/4, 1/16, 1/64) input and image edge cutter
- ·supporting lens shading correction
- ·supporting window cutter
- ·supporting demosaic
- ·supporting sub-sampling
- ·supporting black balance
- ·supporting RGB white balance
- ·supporting RGB color correction
- ·supporting YUV large image upload
- ·supporting YUV large image download
- ·supporting area mask
- ·supporting OSD blending
- ·supporting frame rate control
- ·supporting YUV special effect process
- ·supporting YUV histogram statistics
- ·supporting UV ISO filter
- ·supporting Y edge enhancement
- ·supporting color space conversion
- ·supporting brightness adjustment
- ·supporting color saturation adjustment

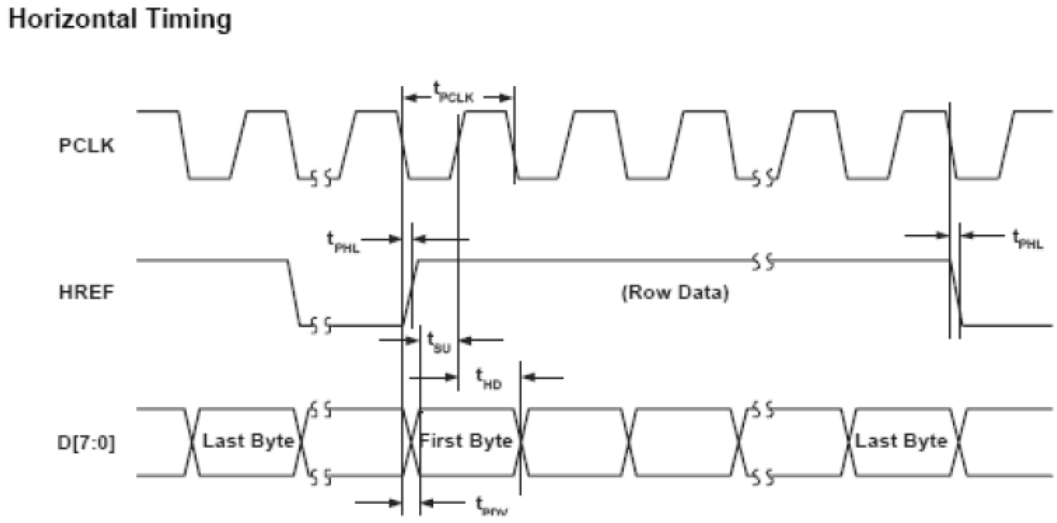
·supporting 0.5～3 scale factor in main channel and 1/8 ~ 1 scale factor in sub channel
·32-bit DMA interface

3.11.1 Timing

3.11.1.1 Bt601 Interface Timing



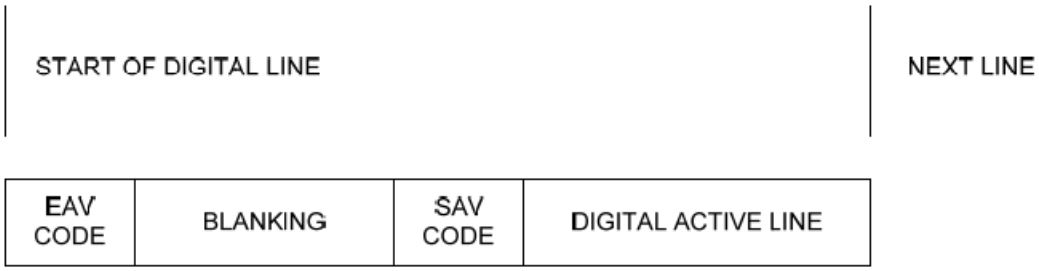
（**Figure 3-5 Bt601 Timing**）



（**Figure 3-6 Bt656 Timing**）

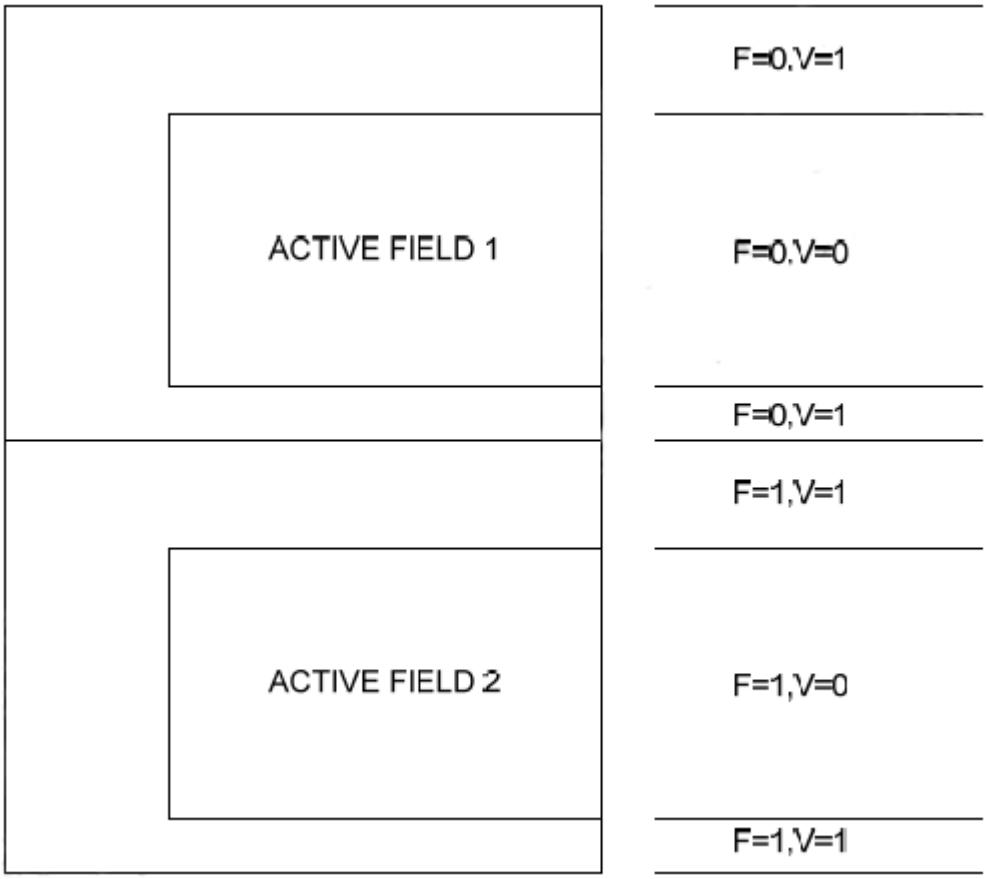
3.11.1.2 Bt656 Interface Timing

It is stipulated in Bt656 that scanning should start from EAV. The Figure below shows the position of EAV and SAV.



（Figure 3-7 EAV and SAV position）

Figure3-10 shows FV value corresponding with a frame.



（Figure 3-8 Corresponding FV Value）

3.12 Encryption

AES/DES/3DES Encryption module is mainly used to encrypt video code stream after being encoded. The data captured by ISP is saved in the memory; H264/MJPEG Encoding module reads the captured data, encodes it, and then saves the code stream in the memory; AES/DES/3DES module reads the code stream data by DMA mode encrypts it and saves the cipher text in the memory by the same way; the cipher text by then can be transmitted to the server by MAC module or network.

3.12.1 Features

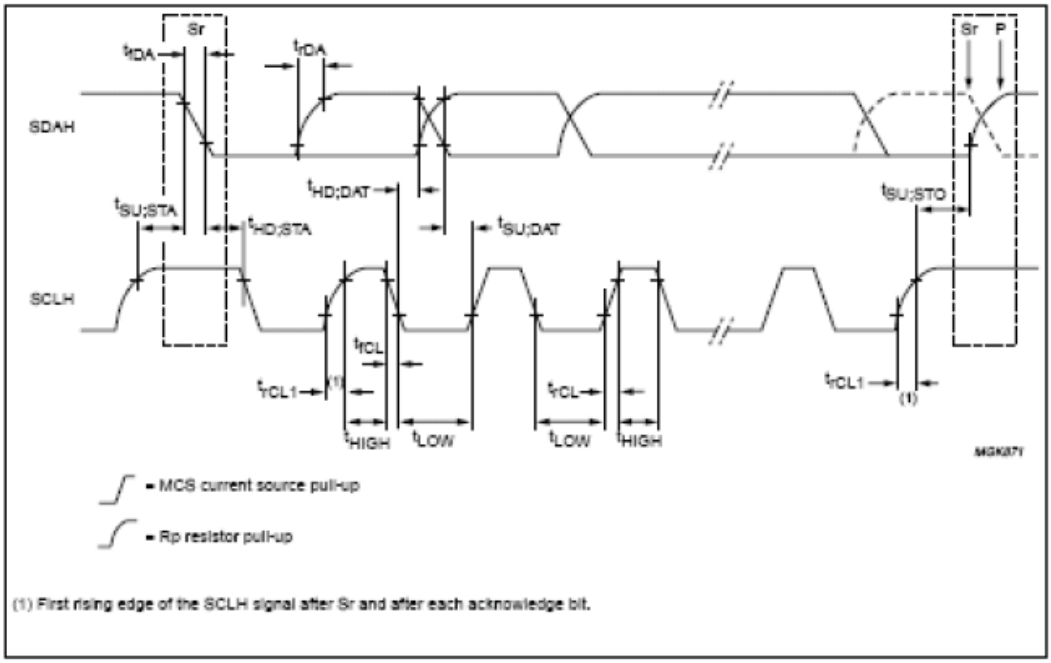
The AES/DES/3DES module has following features:

- AES algorithm conforms with FIPS-197 standard.
- AES key length supports 128, 192, and 256 bits.
- AES supports working modes like ECB, CBC, 1/8/128-CFB, OFB, and CTR, all of which conforming with NIST Special Publication 800-38a standard.
- DES/3DES algorithms conform with FIPS46-3 standard.
- DES key length supports 64 bits.
- 3DES supports 3 keys mode as well as 2 keys mode.
- DES/3DES supports working modes like ECB, CBC, 1/8/64-CFB and 1/8/64-OFB,each of which conforming with FIPS-81 standard.
- ECB, CBC, CFB, OFB working modes support multiple grouping encryption operation in a single run as well as a single grouping encryption operation in a single run.
- CTR working mode of AES supports only AES single grouping encryption operation in a single run.
- Providing forcefully terminating module operation function.
- Providing time-out interrupt function.
- Providing interrupt status inquiry, interrupt mask and interrupt clear function.
- Providing byte sequence adjustment and bit sequence adjustment towards grouping input data and grouping output data.

3.13 I2C Interface

I2C bus is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection between devices. It only supports master mode.

The two pins of I2C interface are shared with GPIOs and have been attached programmable pullup/pulldown function. Please refer to shared-pin control section and pullup/pulldown section for details.



（**Figure 3-9 I2C bus Timing**）

Notes: Please refer to *The I2C Bus Specification* for I2C configuration.

3.14 UART

The UART module includes two independent asynchronous ports, each of which provides serial communication capability with external devices through an RS232 cable.

Key features of UART module are as follows:

- ·containing four asynchronous ports: UART1, UART2.
- ·serving as DTEs
- ·operating in polling-based mode or interrupt-based mode
- ·programmable baud rate, ranging from 2.4Kbps to 2.4Mbps
- ·data packet of 11 bits: 1 start bit (always “0”), 8 data bits, 1 parity bit (optional), and 1stop bit (should be “1”)
- ·UART2 has hardware flow control

Both UARTs transmit/receive a data packet of 11 bits (or 10 bits): 1 start bit (always “0”), 8data bits, 1 parity bit (optional), 1 stop bit (should be “1”). To transmit, data is written from the peripheral data bus to L2 memory. This data is passed serially out on the transmit pin (UTDx). To receive, data is received serially from the receive pin (URDx) and stored in L2 memory.

（**Figure 3-10 Data Format**）

Of the two UARTs (UART1, UART2), UART2 has hardware flow control:

PIN NAME	TYPE	DESCRIPTION
RTS2	O	Request to Send Signal from UART, active low.
CTS2	I	Clear to Send Signal of UART, active low.

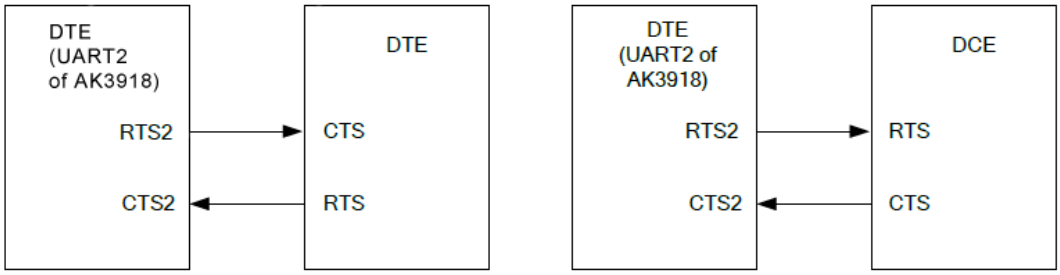
·UART2 receives data

UART2 asserts the RTS signal to indicate that it is ready to receive data. If the data in L2memory is full, or UART2 is not allowed to be used, RTS signal is de-asserted.

·UART2 transfers data

When UART2 wants to send data, it detects the CTS signal. If CTS signal is asserted, it begins to transmit data. Otherwise the data in L2 memory remains undisturbed.

Normally, when the transmitter wants to send data, it detects the CTS signal. If the RTS signal of the receiver is also asserted, then the data transmission begins. Otherwise the data remains in L2 memory.



(Figure 3-11 Flow Control of UART2)

3.15 IrDA

This module supports Infra red data receiving under NEC protocol.

It features as follows:

·Supporting up to 4 continuous WORD (32bit) receiving

·4 data buffers reserved for CPU interrupt response

·Supporting reversing the polarity of data to be received

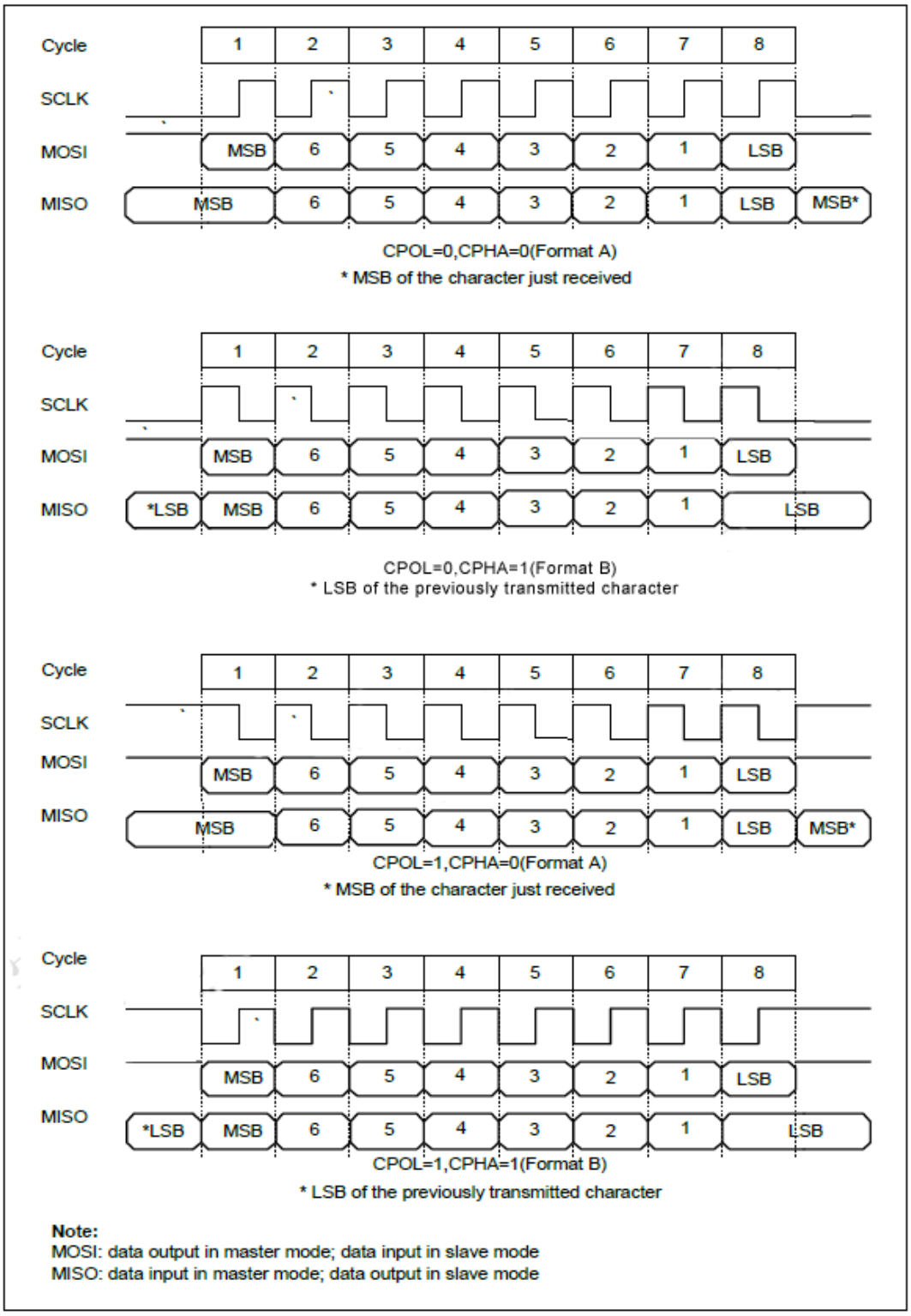
·Supporting synchronously rectify deviation in receiving mode

3.16 SPI

The SPI interface has two serial ports, each of which allows fast synchronous serial communication of 8-bit data length. A serial clock is synchronized with the two data lines for shifting and sampling. When the SPI interface is used as master, transmission frequency is configurable by setting the clock divider ratio, and a byte transmit/receive operation starts with host writing data into the transmit FIFO. When the SPI interface is used as slave, external bus master supplies the clock.

For Slaver mode, there are 4 I/O pin signals associated with SPI: the SPI_CLK, the SPI_DOUT data line, the SPI_DIN data line, and the active low SPI_CS slave select pin.
For Master mode, there are 6 I/O pin signals associated with SPI transfers: the SPI_CLK, the 4-wire bi-direction data line, and the active low SPI_CS slave select pin.

Notes:
1. When the SPI interface works in master mode, AK3918 has to continuously send data to supply the clock.
2. When the SPI interface works in slave mode, AK3918 should provide an instruction set for master's accessing. It fills 0s in the transmit FIFO if the transmit FIFO is empty.



(Figure 3-12 SPI Timing Diagram)

3.17 USB 2.0 HS Host and Slave Controllers

The USB 2.0 HS Host and Slave controller, fully compliant with *USB Specification Version 2.0 (HS)*, provides a 'dual-role' USB controller operating either as the host in point-to-point communications with another USB function or as a function controller for a high-speed/ full speed USB peripheral.
The USB controller provides all the encoding, decoding and checking needed in sending and receiving USB packets. That is, the USB controller interrupts the CPU only when endpoint data has been successfully transferred. When acting as the host for point-to-point communications, the controller additionally maintains a frame counter and automatically schedules SOF, Isochronous, Interrupt and Bulk transfers.

3.18 MCI Interface

The AK3918 contains two MCI interfaces: one is MMC/SD interface supporting 8 data lines;the other is SDIO interface supporting 4 data lines.

The Multimedia Card (MMC) is a universal low cost data storage and communication medium implemented as a hardware card with a simple control unit and a compact, easy-to-implement interface. MMC communication is based on an advanced 7-pin serial bus designed to operate in a low voltage range at medium speed.

The Secure Digital Card (SD) is an evolution of the MMC with an additional 2 pins in the form factor that is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in new audio and video consumer electronic devices. The physical form factor, pin assignment, and data transfer protocol are compatible with the MMC.The SD is composed of a memory card and an I/O card. The memory card includes a copyright protection mechanism that complies with the security requirements of the Secure Digital Music Initiative (SDMI) standard, and is faster and has a higher memory capacity. The I/O card combines high-speed data I/O with low-power consumption for mobile electronic devices.

The SDIO is a standard for accessory devices that extends the functionality of devices with SD card slots. It is compatible with SD standard including the features of mechanical, electrical, power, signaling and software.

The features of MMC/SD/SDIO interface are as follows:

- ·conforming to *The Multimedia Card Specification, Version 4.0* and *SD Memory Card Specification, Version 2.0*
- ·MMC/SD interface supporting one-bit, four-bit, and eight-bit data bus
- ·SDIO interface supporting one-bit and four-bit data bus
- ·maximum reading/writing speed is half of ASIC CLK
- ·32-bit local buffer
- ·working in little endian only
- ·supporting single block operation，multiple block operation and stream mode (MMC card only)

Notes: As defined in the *The Multimedia Card Specification*, the data will not be followed bythe CRC bits when it is transferred in stream mode.

3.19 Ethernet MAC

The Ethernet MAC module is a fast Ethernet NIC/LOM controller with integrated 10 base transceiver and PCI Express host interface.

Its features are as follows:

- ·scattering and gathering transmit/receive DMA
- ·interrupt coalescing
- ·shared internal transmit and receive FIFO(8KB)
- ·automated receive FIFO flow control
- ·IEEE 802.3z compliant
- ·10/100Mbps speed, full-duplex
- ·asymmetric/symmetric flow control
- ·VLAN tag insertion/removal
- ·IPv4, IPv6, TCP, UDP checksum calculation and verification
- ·MIB statictics support
- ·multicast frame filtering
- ·WOL (Wake-On-LAN) support

3.20 Analog

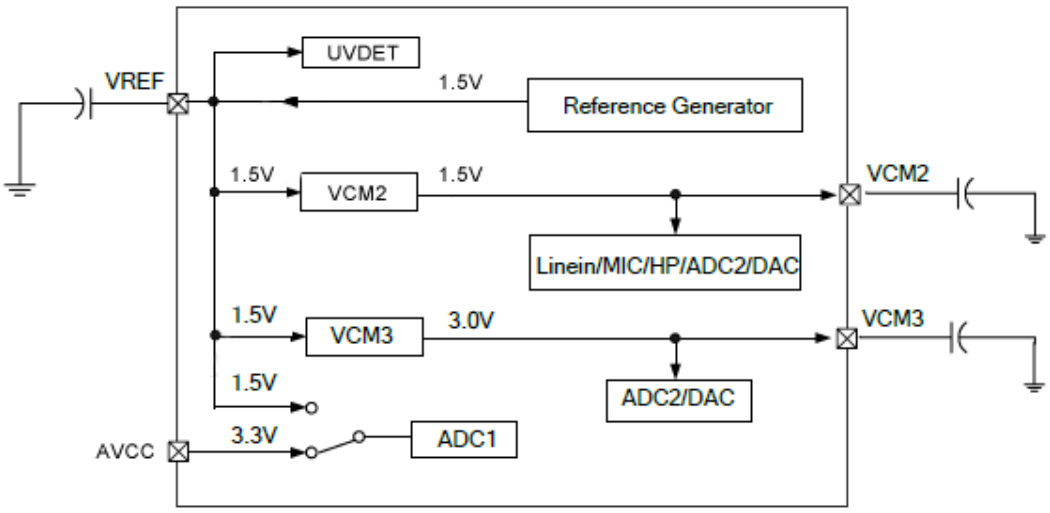
The analog control module includes all analog functions for the AK3918 processor. Its mainly consists of

- ·one 10-bit ADC
- ·one 16-bit ADC
- ·two 22-bit sigma-delta DACs
- ·headphone driver
- ·microphone interface
- ·battery monitor
- ·one reference voltage generator

To make architecture presentation easier, the digital filters associated with the ADCs and DACs are included.

3.20.1 Reference Voltage Generator

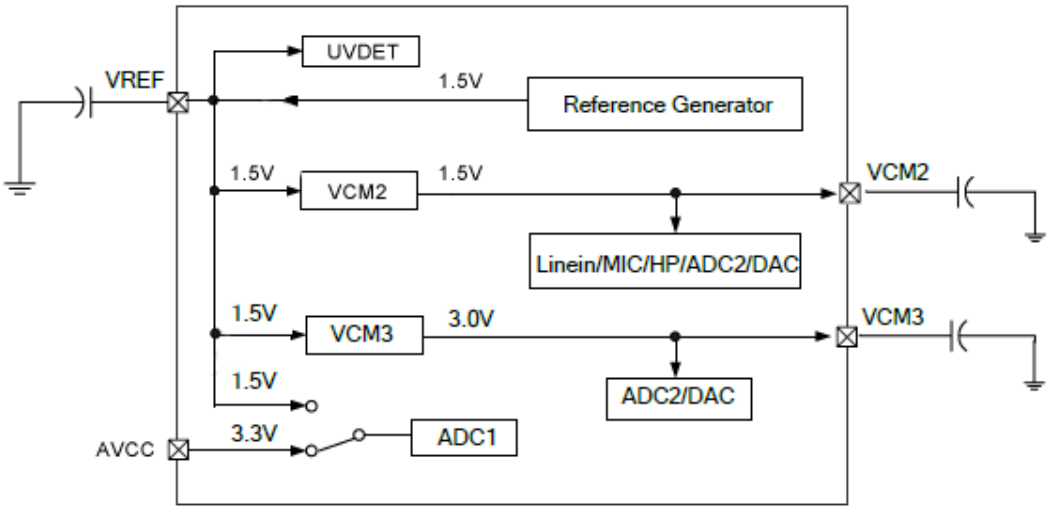
The reference generator generates reference VREF (1.5V), VCM2 and VCM3 for audio codec.



(Figure 3-13 Architecture of Reference Voltage Generator)

3.20.2 Audio Codec

As shown in Figure 3-14, AK3918 has a 16-bit ADC (ADC2) and two DACs. ADC2 can accept signals from microphone interface, from linein interface, and from output of DACs.



(Figure 3-14 Architecture of Audio Codec)

3.20.2.1 ADC2

Aiming to provide high-performance voice and music recording, AK3918 includes a 16-bit ADC: ADC2. As illustrated in Figure 3-14, ADC2 can accept signals from microphone interface, from linein interface, and from output of DACs.

3.20.2.1.1 Microphone Interface

The high impedance and low capacitance microphone interface is compatible with a wide range of microphones of different dynamics and sensitivities. It contains a programmable gain amplifier (PGA), and a passive filter to prevent high frequencies from folding back into the audio band. VCM3 is used as the bias voltage for microphone. The microphone interface supports mono microphone input.

3.20.2.1.2 Linein Interface

In order to meet the requirement of acceptable input range of ADC2, the linein interface also contains a programmable gain amplifier to adjust the amplitude of input signals. Some passive components are recommended to be added to the linein interface to build a voltage divider and anti-alias filter to optimize the sound effect.

3.20.2.2 DACs

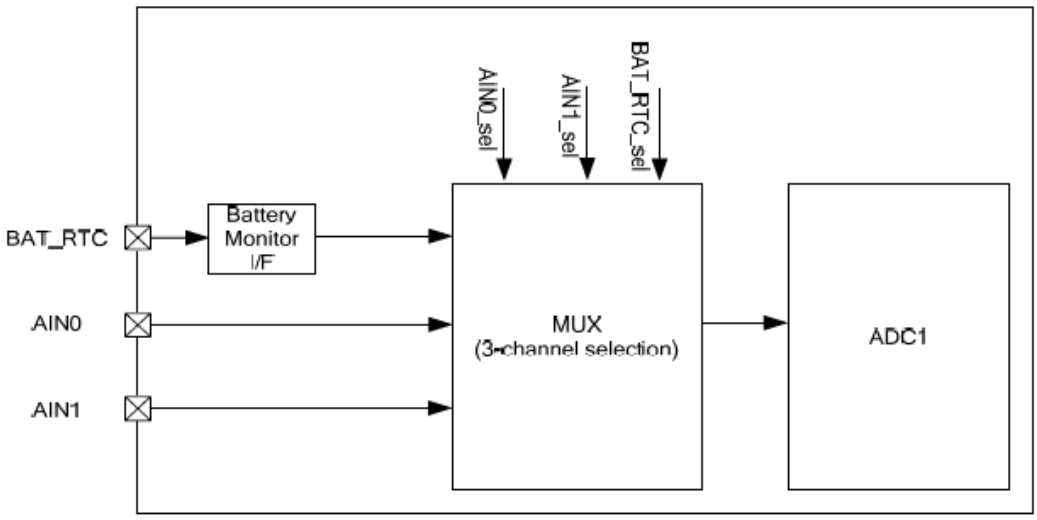
The AK3918 contains two 22-bit DACs, which accept input either from CPU or L2 memory. Their output may be sent to headphone driver.

3.20.2.2.1 Headphone Driver

The headphone driver is able to drive 32ohm headphones. As it only supports AC output, a DC blocking capacitor is required in the output of HPL and HPR, as shown in the following figure. It accepts input either from microphone, from line in, or from the output of DACs. All of these inputs can be switched off independently.

3.20.3 ADC1

The ADC1 includes 3 channels, one for battery monitor, one for analog keypad input measurement and one for general purpose. The former one channel and the latter two channels cannot be enabled simultaneously. That is, once AIN0 or AIN1 is selected, BAT_RTC is powered down.



(Figure 3-15 Architecture of ADC1)

Notes:

1. *BAT_RTC, AIN0, AIN1, MIC_P, MIC_N, Linein_L, Linein_R, HPL and HPR* are external pins. Please refer to *AK3918 Specification* for details.
2. Select battery monitor input (BAT_RTC); AIN0_sel: select AIN0 signal; AIN1_sel: selectAIN1 signal.
3. The maximum input voltage of BAT_RTC, when internal voltage divider is applied, is 5Vwhile when no voltage divider is applied, that of BAT_RTC is (AVDD-0.7) V; the input voltage of AIN0, AIN1 ranges from 0V~AVDD.

3.20.3.1 Battery Monitor

The battery monitor measures the data input from the external pin BAT_RTC. The maximum input voltage of BAT_RTC, when internal voltage divider is applied, is 5V while when no voltage divider is applied, that of BAT_RTC is (AVDD-0.7) V.

3.20.3.2 AIN0 and AIN1 channels

AIN0 and AIN1 are two independent analog channels. It should be noted that once these two channels is enabled, BAT_RTC channel is disabled; and the voltage range that AIN0, AIN1can accept is 0V~AVDD. If the input voltage to be sampled by AIN0 0r AIN1 is over AVDD, an external voltage divider is needed.

3.21 PWM

The PWM controller generates four independent PWM outputs. Everyone can be configuredby its own register to control the rising-edge and falling-edge timing of a single output channel. The supported frequency varies from 92Hz to 6MHz. With 16-bit high-level pulse control and 16-bit low-level pulse control, the duty cycle ranges from$\frac{1}{65536}$(on for$\frac{1}{65536}$, and off for theother$\frac{65535}{65536}$) to$\frac{65535}{65536}$(on for$\frac{65535}{65536}$, and off for the other$\frac{1}{65536}$).

3.22 Timers

AK3918 includes five general purpose timers, each of which has its own 26-bit down counter. The timer counts from the loaded value. When down counter reaches zero, an interrupt is generated to indicate that timer operation has been completed. And the down counter continues next counting operation from loaded value as long as the timer is enabled.

3.23 GPIO

Totally, AK3918 contains 64 GPIOs (GPIO [63:0]), 7 of which is dedicated GPIO, 57 of which are shared with other pins. When the system is powered on, all the ports (excluding GPIO [11:8]) are used as GPIO ports and set to input mode by default. 32 GPIO ports, namely, GPIO [57], GPIO [55:47], GPIO [44:39], GPIO [30:27], GPIO [22], GPIO [14:12] and GPIO [7:0]can work as wake-up ports to wake up the AK3918 from standby mode.

4 Electrical Specifications

4.1 Maximum Ratings

(Table 4-1 AK3918 Maximum Ratings)

RATING	SYMBOL	MINIMUM	MAXIMUM	UNIT
Digital Supply Voltage	VDD	-0.3	1.5	V
Digital I/O Power Voltage	VDDIO	-0.3	4.0	V
Analog Power Voltage	AVDD(USB)	-0.3	4.0	V
	AVDD (ADC/DAC)	-0.3	4.0	V
	HPVDD	-0.3	4.0	V
	VBAT	-0.3	5.0	V
Maximum Operating Temperature Range	T_o	-20	70	^oC
Storage Temperature	T_s	-40	125	^oC

4.2 Recommended Operating Range

(Table 4-2 Recommended Operating Range)

RATING	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Digital Supply Voltage	VDD	1.08	1.20	1.35	V
Digital I/O Power Voltage	VDDIO	2.97	3.30	3.63	V
Analog Supply Voltage	AVDD(USB)	3.0	3.30	3.63	V
	AVDD (ADC/DAC)	3.0	3.30	3.63	V
	HPVDD	3.0	3.30	3.63	V
CPU Normal Operating Clock Frequency	FCPU	-	340	-	MHz
External Bus Clock Frequency	FBUS	-	170	-	MHz

4.3 DC Electrical Characteristics

(Table 4-3 DC Electrical Characteristics)

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input High Voltage	VIH	2.0	-	VDDIO+0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V
Output High Voltage (IOH=2.0mA)	VOH	2.4	-	-	V
Output Low Voltage	VOL	-	-	0.4	V
Input Leakage Current	IL	-	-	±1	uA
Tri-state Output Leakage Current	IOZ	-	-	±1	uA
Input capacitance	CI	-	-	8	pF
Output capacitance	CO	-	-	8	pF
Analog Line in Resistance	R_L	6K	18K	28K	ohm
Microphone Input Resistance	Rmic	-	5K	-	ohm
Stereo-line output load resistance	Rlineout	10	-	-	Kohm
Headphone output load resistance	RHP	-	32	-	ohm

4.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 340 MHz.

(Table 4-4 32K/12M Oscillator Signal Timing)

PARAMETER	MIN.	TYP.	MAX.	UNIT
XTAL32K Startup Time	-	-	0.67	s
XTAL12M Startup Time	-	-	30	ms

4.5 LDORTC Electrical Characteristics

(Table 4-5 Electrical Characteristics of LDORTC)

Typical values are at T_A = +27°C and all Current Values are dynamic, unless other-wise noted.

SYMBOL	PARAMETER	CONDITION	TYP.	UNIT
V_{IN}	Operating Supply Voltage	I_{LOAD_max}=250mA	3.3~4.2	V
V_{OUT}	Output Voltage	0mA<I_{LOAD}<250mA	0.8~1.4	V
I_{LOAD_MAX}	MAX Output Current	3.0V<V_{IN}<4.2V	250	mA
I_{NO_LOAD}	Vin Quiescent Current	I_{LOAD}=0mA	<150	μA
$I_{powerdown}$	Vin Shutdown Current	27°C	<1	μA
V_{ripple}	Output Voltage Ripple	ILOAD=100mA,ESR<40mΩ	<40	mV
η	Efficiency	I_{LOAD}=100mA	83	%
$OSC_{Frequence}$	OSC Frequency	27°C	1000	kHz
I_{Limit}	Peak Current Limit	27°C	650	mA
Rpswitch	P-Channel On-Resistance	VIN=3.3V	500	mΩ

5Package Information

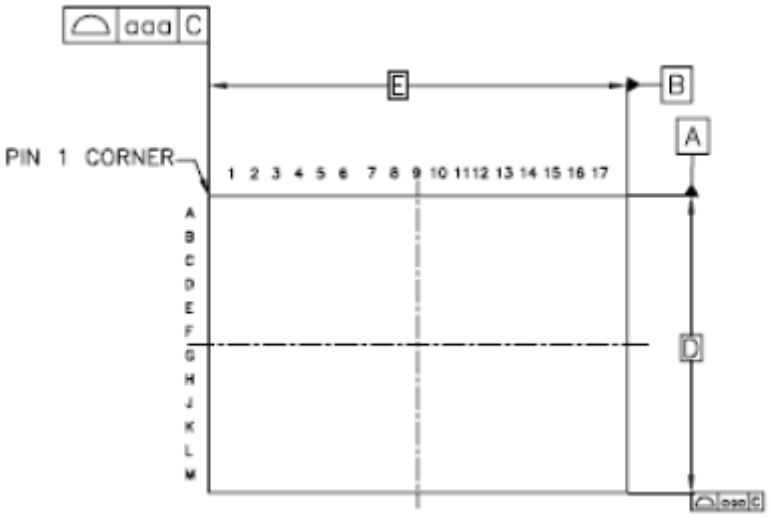
AK3918 is packaged in a 152-pin LFBGA with 10mm x 14mm x 0.80mm;

5.1 PIN Assignment

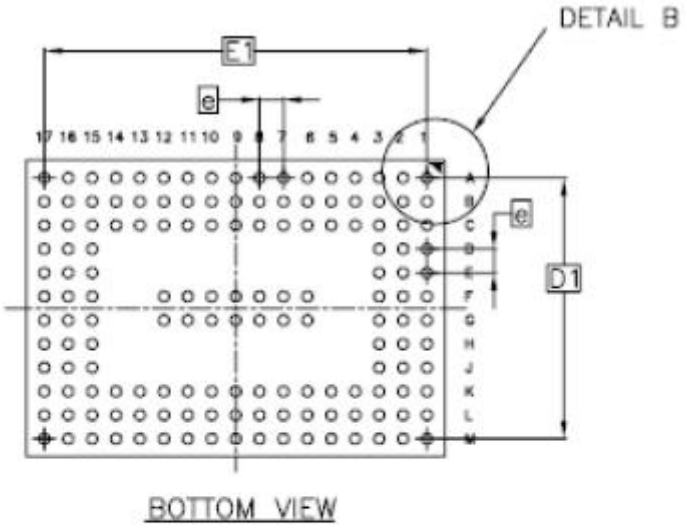
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	MIC_P	MIC_N	HPL	HPR	VCM3	BAT_RTC	XTAL32KO	XTAL32KI	GPIO[60]	GPIO[59]	GPIO[58]	GPIO[56]/ PWM5	CIS_D[3	CIS_D[2]	CIS_D[1]/ GPIO[9]	CIS_D[0]/ GPIO[8]	CIS_HSYNC
B	VREF	VCM2	Linein_R	AIN0	#RST	GPIO[57]/ I2S_DIN	GPIO[50]/ PWM3	GPIO[49]	GPIO[4]/ TDI/ RXD2/ PWM1	GPIO[54]/ I2S_BCLK	GPIO[48]/ PWM1	SPI1_CLK / GPIO[26]	CIS_D[9]/ GPIO[11	CIS_D[7]	CIS_D[5]	VDDIO_CIS	CIS_D[4]
C	HPVDD	AIN1	Linein_L	AVSS	AVCC	WAKEUP	OPCLK/ GPIO[47]/ PWM5	GPIO[3]/ TMS	GPIO[53]/ I2S_MCLK	#SPI1_CS / GPIO[25	GPIO[7]/ RTCK/ RTS2/ PWM4	GPIO[6]/ TCLK/ CTS2/ PWM3	CIS_SCLK	CIS_PCLK	CIS_VSYNC	CIS_D[8]/ GPIO[10]	CIS_D[6]
D	USB_DP	USB_RREF	HPVSS												VDDIO	RXD1/ GPIO[1]	TXD1/ GPIO[2]
E	USB_DM	AGND_USB	AVSS_PLL												VDD	I2C_CLK/ GPIO[27]	I2C_DAT/ GPIO[28]
F	AVDD12_PLL	VCCA_USB	MCI1_MCK/ GPIO[32]			VDDIO	VSS	VSS	VSSIO	VSSIO	VDD	VDD			DRAM_VREF	PWM5/ GPIO[30]/ #SPI2_CS/ I2S_MCLK	IRDA_DI/ GPIO[29]/ SPI2_CLK
G	MCI1_D[3]/ GPIO[36]	MCI1_MCMD/GPIO[31]	MCI1_D[0]/ GPIO[33]			VSS	VSS	VSS	VSSIO	VSSIO	VDD	VDD			#DRAM_CS	VDD_DDR2	VDD_DDR2
H	XTAL12MI	XTAL12MO	MCI1_D[1]/ GPIO[34]												VDD_DDR2	VSSIO _DRAM	VDDIO _DRAM
J	MCI1_D[4]/GPIO[37]/ SPI2_DIN[note4]/ SPI1_DIN[note3]	MCI1_D[5]/GPIO[38]/ SPI2_DOUT[note4] /SPI1_DOUT[note3]	MCI1_D[2]/ GPIO[35]												VSS_DDR2	VSSIO _DRAM	VDDIO _DRAM

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
K	MCI1_D[7]/GPIO[40]/ SPI2_HOLD[note4] / SPI1_HOLD[note3]	MCI1_D[6]/GPIO[39]/ SPI2_WP[note4] /SPI1_WP[note3]	VDDIO_MAC	GMII_CRS/ GPIO[18]	GMII_RXD[2]/ GPIO[21]	GMII_RXCLK	GMII_RXD[1]/ GPIO[20]	GMII_TXD[0]/ GPIO[14]	GMII_TXD[1]/ GPIO[15]	GPIO[0]/ #TRST	VSS_DDR2	VSS_DDR2	VSSIO_DRAM	VSS_DDR2	VSSIO_DRAM	VSSIO_DRAM	VDDIO_DRAM
L	MCI2_MCK/ GPIO[42]	MCI2_D[0]GPIO[43]/SPI2_HOLD[note4] /SPI1_HOLD[note3]	MCI2_MCMD/ GPIO[41]	GMII_RXDV/GPIO[23]	GMII_COL/ GPIO[24	GMII_MDIO/ GPIO[12]	XTAL25MO	GMII_TXD[3]/ GPIO[17]	GMII_TXCLK	GMII_TXEN	GPIO[5]/ TDO/ TXD2/ PWM2	GPIO[52]/ I2S_DOUT	GPIO[61]	VSSIO_DRAM	VSSIO_DRAM	VSSIO_DRAM	VDDIO_DRAM
M	MCI2_D[3]/GPIO[46]/ SPI2_DIN[note4]/ SPI1_DIN[note3]	MCI2_D[2]/GPIO[45]/SPI2_WP[note4] /SPI1_WP[note3]	MCI2_D[1]/ GPIO[44]/ SPI2_WP[note4] / SPI1_WP[note3]	GMII_CLK	GMII_INT/ GPIO[13]	GMII_RXD[0]/ GPIO[19]	XTAL25MI	GMII_RXD[3]/ GPIO[22	GMII_TXD[2]/ GPIO[16]	GPIO[62]	GPIO[63]	GPIO[51]/ PWM4	GPIO[55]/ I2S_LRCLK	VDDIO_DRAM	VDDIO_DRAM	VDDIO_DRAM	VDDIO_DRAM

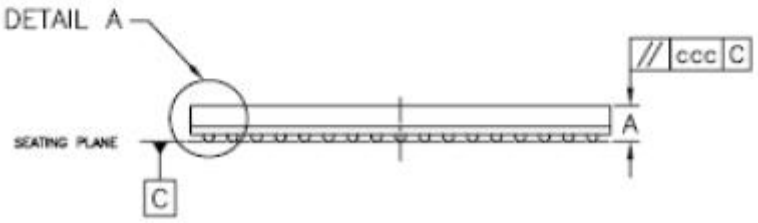
5.2 Package Information

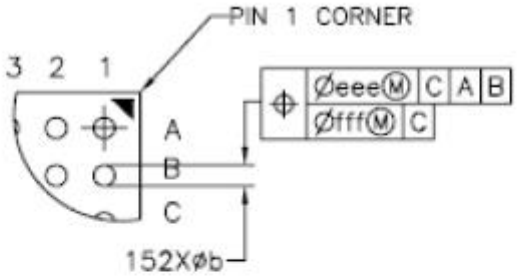


TOP VIEW

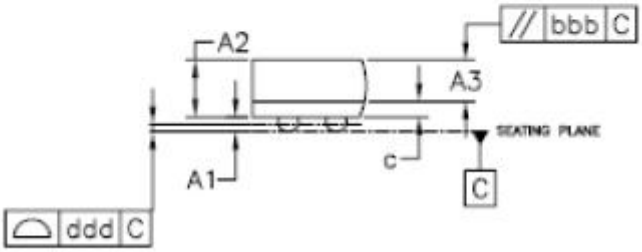


BOTTOM VIEW





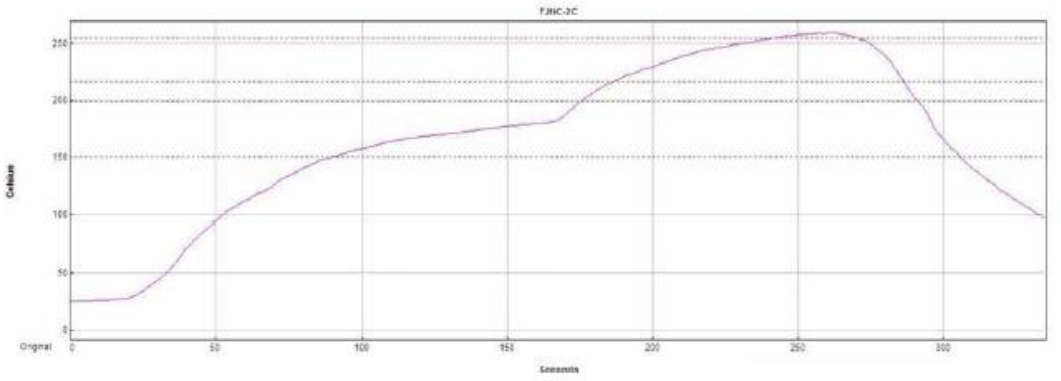
DETAIL B(2:1)



DETAIL A(2:1)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.28
A1	0.20	0.25	0.30
A2	0.91	0.96	1.01
A3		0.70 BASIC	
c	0.22	0.26	0.30
D	9.90	10.00	10.10
D1		8.80 BASIC	
E	13.90	14.00	14.10
E1		12.80 BASIC	
e		0.80 BASIC	
b	0.30	0.35	0.40
aaa		0.10	
bbb		0.10	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

6 Reflow Profile



(Figure 6-1 Recommended Reflow Profile)

(Table 6-1 Reflow Profile Condition)

Max rising slope	2.59	73%
Max falling slope	-3.69	-8%
Preheat 150 – 200C	85.65	-57%
Reflow time /255C	29.24	-8%
Peak temperature	259.66	86%
Total time /217	99.81	-12%