High Speed System Applications

1. High Speed Data Conversion Overview
2. Optimizing Data Converter Interfaces
3. DACs, DDSs, PLLs, and Clock Distribution
4. **PC Board Layout and Design Tools**

SECTION 4
PC BOARD LAYOUT AND DESIGN TOOLS

Grounding and Layout

One of the biggest problems in system design is how to handle grounding. There are several competing requirements that are dependent on the frequency and system complexity.

Unfortunately, there is no magic "cookbook" approach to grounding that will always guarantee success. What we will do here is present some of the effects that must be considered when designing the system.

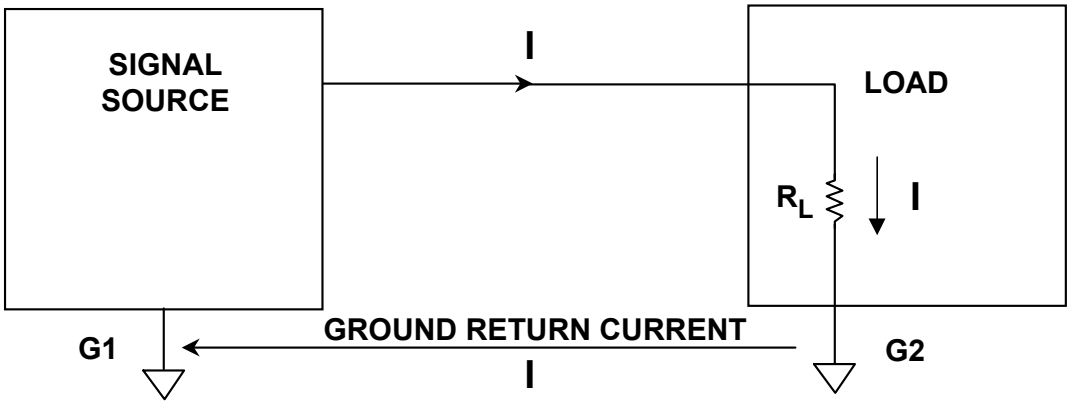
The main thing is to look at how and where the dc and ac currents flow in a PCB.

More information on PC board design techniques can be found in the following two references:

Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 9. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2004, ISBN: 0750678410, Chapter 9.

Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5, Chapter 7. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5, Chapter 7.

Kirchoff's Law Helps Analyze Voltage Drops Around a Complete Circuit

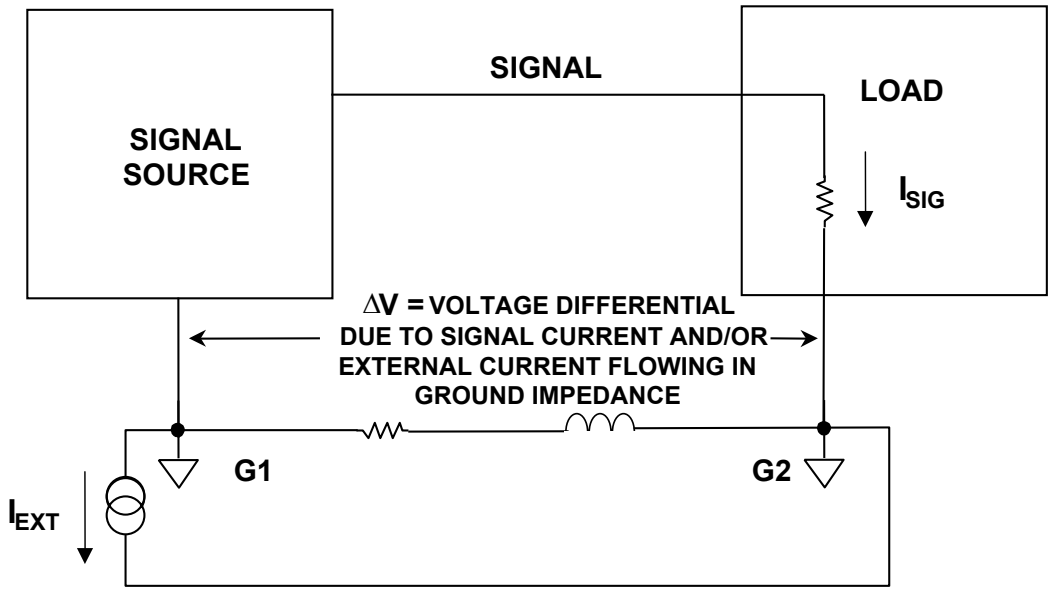


AT ANY POINT IN A CIRCUIT
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO
OR
WHAT GOES OUT MUST COME BACK
WHICH LEADS TO THE CONCLUSION THAT
ALL VOLTAGES ARE DIFFERENTIAL
(EVEN IF THEY'RE GROUNDED)

When we draw the ground symbol on a schematic, we assume that all ground points are at the same potential. This is rarely the case, unfortunately. Historically, ground was the reference level with which we measured various voltage levels in the circuit. However, ground has also become the power return not only for digital signals but for analog signals as well.

All signals that flow in a circuit must have a return path to complete the loop. Often we consider the forward path only, but there always must be a return to close the loop or current can not flow. This return path is often through the ground plane.

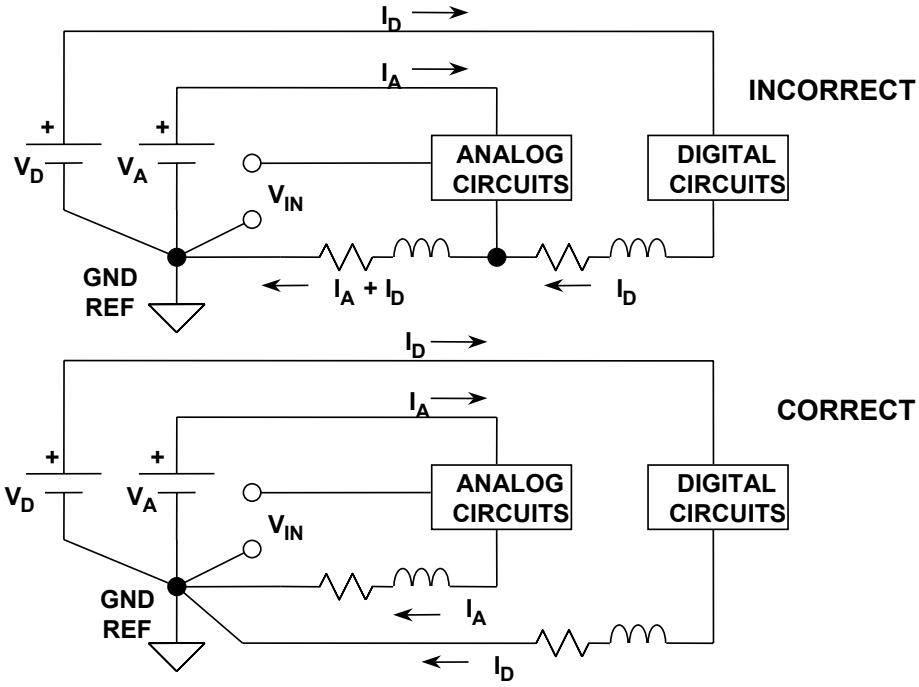
A More Realistic View of the Impedance Between Grounds



A ground is never zero impedance. There is always some resistance and inductance, even in a large area heavy ground plane. The magnitude of the impedance may be small, but it is not zero. And a current flowing through an impedance causes a voltage drop. This means that the two grounds in the diagram above will not be at the same potential.

It is important to consider the inductance of the ground as well as the resistance, especially as the frequency increases.

Digital Currents Flowing in Analog Return Path Create Error Voltages



Because ground is the power return for all digital circuits, as well as many analog circuits, one of the most basic design philosophies is to separate digital ground from analog ground.

If the grounds are not separated, not only does the return from the analog circuitry flow through the analog ground impedance, but the digital ground current also flows through the analog ground, and the digital ground current is typically much greater than the analog ground current.

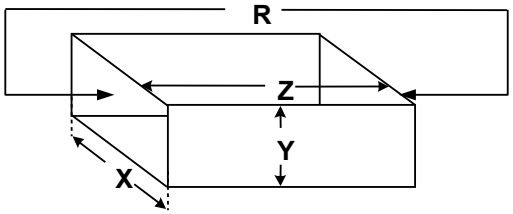
As the frequency of digital circuits increases, the noise generated on the ground increases dramatically. TTL and CMOS logic families are of the saturating types. This means that the logic transitions cause large transient currents on the power supply and ground. CMOS outputs basically connect the power to ground through a low impedance during the logic transitions.

And it's not just the basic clock rate that is a problem. Digital logic waveforms are basically rectangular waves, which implies many higher frequency harmonic components.

Calculation of Sheet Resistance and Linear Resistance

$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY



SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

$\rho = 1.724 \times 10^{-6}\ \Omega$ cm, Y = 0.0036cm

$$R = 0.48 \frac{Z}{X}\ m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

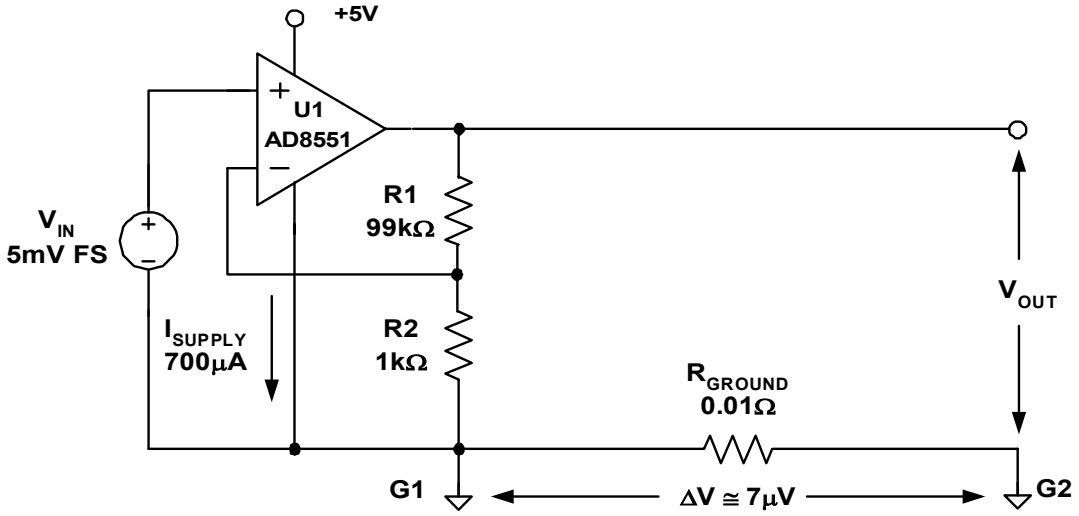
R = SHEET RESISTANCE OF 1 SQUARE (Z = X)
= 0.48mΩ/SQUARE

Resistance is the first ground component we will consider. All conductors have some resistance (at least when operating above 0°K). Using large area ground planes decreases the resistance, but cannot eliminate it. And from Ohm's law we know that a current flowing through a resistance will cause a voltage drop across the resistance.

The resistance of a trace (or a ground plane) can be calculated by taking the resistivity of the material, which will typically be given in a resistance per unit volume (squares) of the conductor material, and multiplying by the number of the squares.

In the above example, the sheet resistance of 1 oz. copper, which is a typical PC board material, is calculated as 0.48mΩ/square.

Even Small Common Ground Currents Can Degrade Precision Amplifier Accuracy

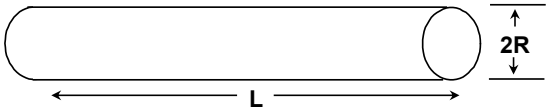


This is an example of how even a small amount of resistance can cause significant error.

Here the quiescent (supply) current of the AD8551 (700µA) flowing through the ground resistance (0.01Ω) causes an error at the point where the signal will be processed (Vout). Although 700µA is a relatively low current, and the ground resistance of 0.01Ω is also a relatively low value, this combination will cause a voltage drop, in this example, of 7µV, also a low value, but much greater than the offset voltage spec of 1µV of the AD8551.

The AD8551 is a chopper stabilized amplifier which, in addition to the voltage offset specification of 1µV, has a offset voltage drift spec of 0.005µV/°C.

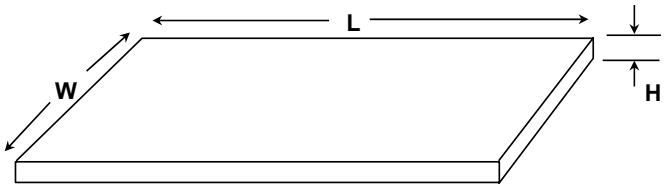
Wire and Strip Inductance Calculations



L, R in mm

$$\text{WIRE INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\ \mu H$$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)



$$\text{STRIP INDUCTANCE} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

In addition to the resistance (basically a dc spec), a trace (wire or ground plane) will have a frequency dependent impedance component (known as inductance). Inductive impedance increases linearly with frequency. This can become significant at higher frequencies.

The inductance of a trace (wire or ground plane) can be calculated from the information in this figure. The inductive impedance can be calculated from:

$$Z_L = j\omega L$$

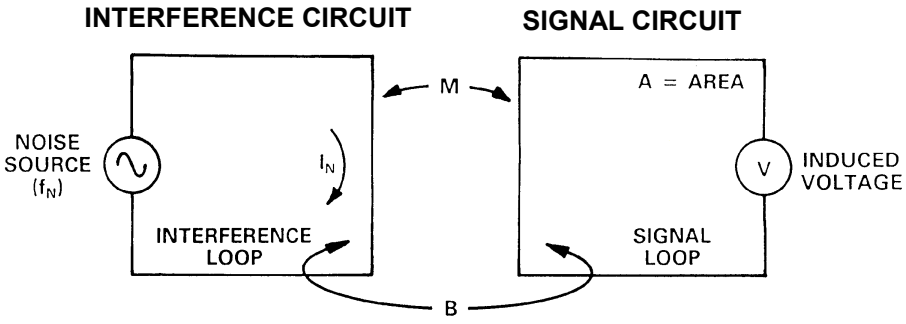
where:

$$j = \sqrt{-1}$$

and

$$\omega = \text{radian frequency} = 2\pi \cdot \text{frequency in Hertz}$$

Basic Principles of Inductive Coupling



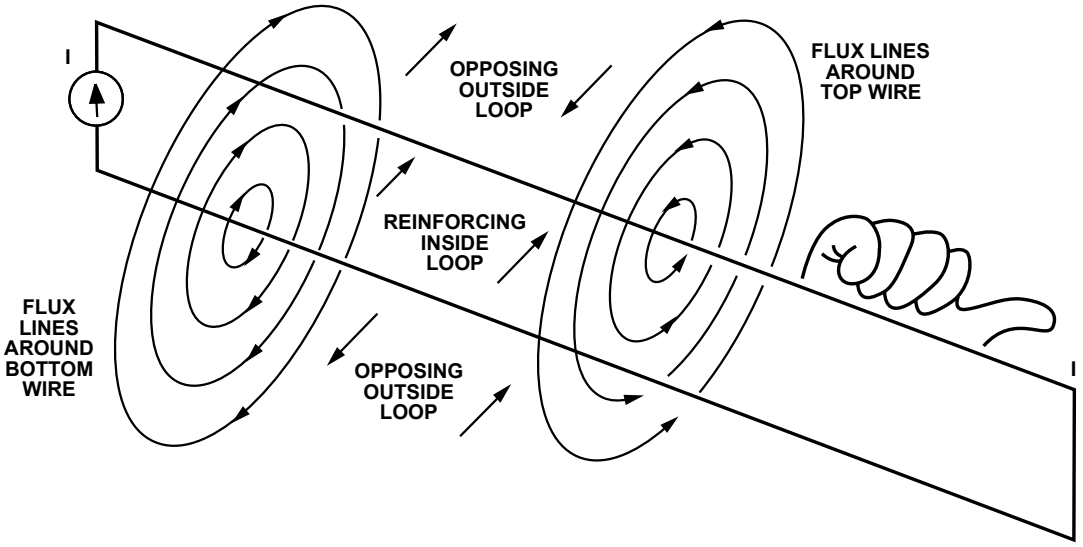
M = MUTUAL INDUCTANCE
B = MAGNETIC REFLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

The increase in impedance with frequency is only one of the issues with inductance. The other potential problem is the coupling of signal from one circuit to another via mutual inductance.

The amount of coupling will depend on the strength of the interference, the mutual inductance, the area enclosed by the signal loop (which is basically an antenna), and the frequency. Also, the mutual inductance will depend primarily on the physical proximity of the loops, as well as the permeability of the material.

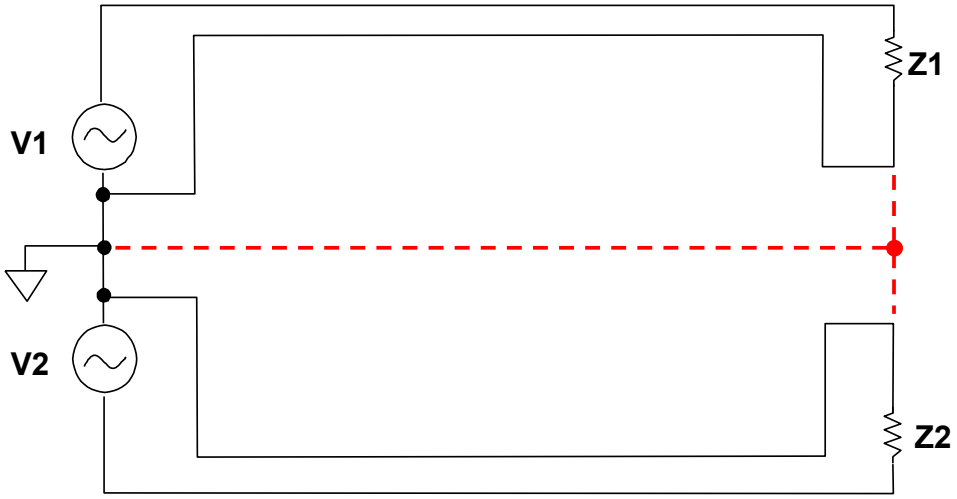
Magnetic Field Lines and Inductive Loop (Right Hand Rule)



The right hand rule is useful in predicting the direction of the magnetic field lines produced by a current flowing in a conductor.

If you point the fingers of your right hand in the direction of the flux density, the induced signal will flow in the direction that your thumb is pointing.

Proper Signal Routing and Layout Can Reduce Inductive Coupling

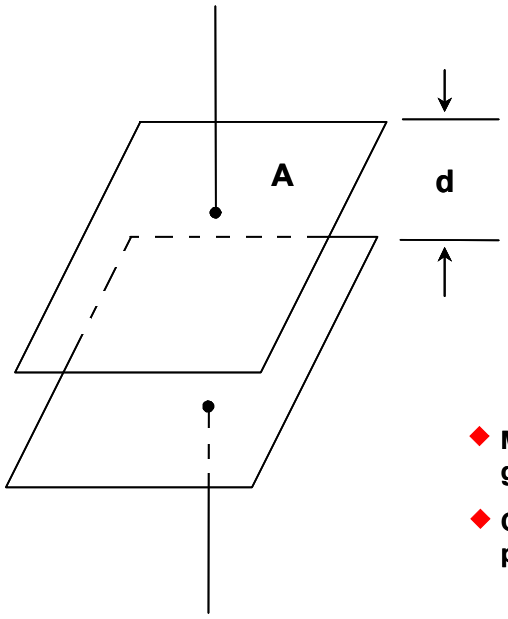


Here is an example of one technique to reduce inductive coupling.

Looking at the above circuit, at first it may seem logical to use a single trace as the return path for the two sources (shown by the dotted lines). However, this will cause the return currents for both signals to flow through the same impedance, which is not desirable. In addition, doing so will maximize the area of the interference loops and increase the mutual inductance by moving the loops close together. This will increase the mutual inductance and the coupling between the circuits.

Routing the traces in the manner shown in this figure minimizes the area enclosed by the loops and separates the return paths, thus separating the circuits and, in turn, minimizing the mutual inductance.

Capacitance of Two Parallel Plates



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

- **Most common PCB type uses 1.5mm glass-fiber epoxy material with E_r = 4.7**
- **Capacitance of PC track over ground plane is roughly 2.8 pF/cm^2**

Another PCB parasitic to be considered is capacitance. While capacitance will not directly affect the impedance of the ground, it can be a major source of coupled interference in a system.

A capacitor consists of two conductors separated by an insulator. This can be as simple as a trace running over a ground, two traces running parallel to each other along a PC board, or two wires running next to each other in a cable bundle.

Capacitive impedance decreases linearly with frequency. This can become significant at higher frequencies.

The capacitance can be calculated from the information in this figure. It is dependant on the dimensions of conductors, the separation of the conductors, and the dielectric constant of the insulator. The capacitive impedance can be calculated from:

$$Z_C = 1/j\omega C$$

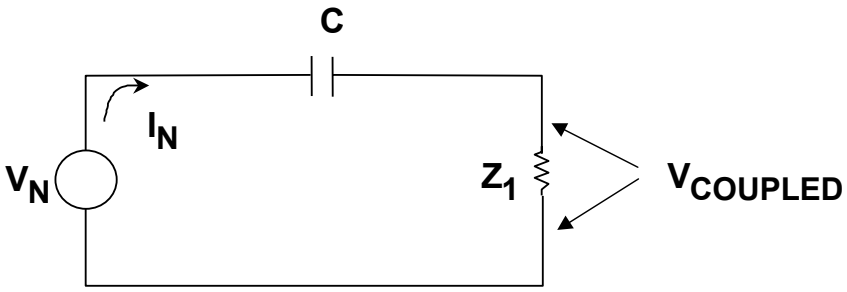
where:

$$j = \sqrt{-1}$$

and

$$\omega = \text{radian frequency} = 2\pi \cdot \text{frequency in Hertz}$$

Capacitive Coupling Equivalent Circuit Model



Z_1 = CIRCUIT IMPEDANCE

$Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left[\frac{Z_1}{Z_1 + Z_2} \right]$$

This illustrates the mechanism of capacitive coupling. The capacitor formed by the traces (C) forms a high pass filter with the impedance of the circuit into which the signal is being coupled (Z_1).

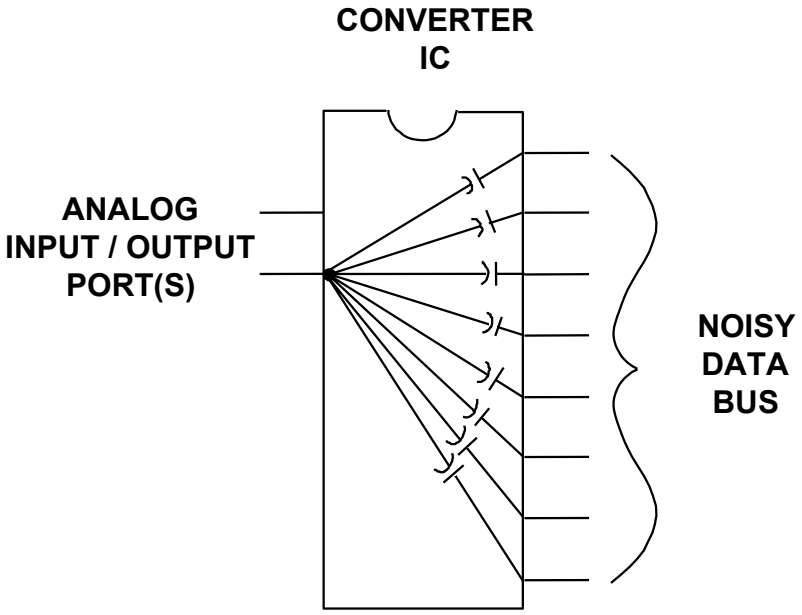
The corner frequency of this filter is:

$$f = 1/2\pi Z_1 C$$

If the impedance of the receiver circuit is low, the corner frequency is moved higher in frequency, This results in less coupling at lower frequencies.

This is one reason that most high frequency circuits tend to use low impedances in their design.

A High Speed Converter Directly Interfacing to a Digital Data Bus Showing Path of Injected Noise



This figure shows how capacitive coupling can degrade the performance of data converters.

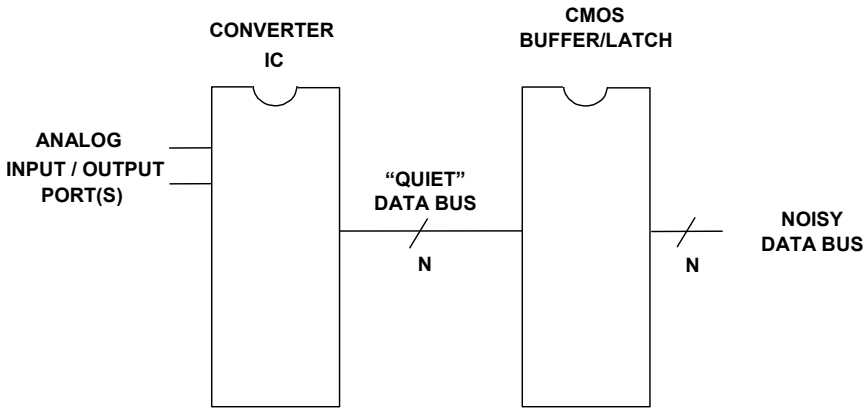
In this example, a converter is connected directly to the data bus. This data bus, in turn, is connected to the CPU (DSP, ASIC, FPGA, etc.), memory and other peripherals. The signals on the bus are generally high speed, with fast edges. This implies a great deal of high frequency energy.

Even if the data bus is not active, these signals still appear on the pins, and the bus presents a capacitive load to the converter data pins. The small capacitors in the diagram represent capacitance between the bond wires. This can typically be on the order of 0.2pF or so. As we have seen before, this is a relatively low value, but it becomes increasingly important as frequency increases.

This applies to DACs as well as ADCs, although it will typically be more of an issue with ADCs.

As a side note, this is not the only mechanism of noise injection into a data converter. The signals on the data bus will also get onto the die, even if there is an input latch (for data input to a DAC) or if the output drivers are tri-stated (for data output of an ADC). In either case, the high speed signals will still couple to the die through the stray capacitance.

Partial Solution to the Noisy Data Bus Issue



- THE OUTPUT BUFFER/LATCH ACTS AS A FARADAY SHIELD BETWEEN "N" LINES OF A FAST, NOISY DATA BUS AND A HIGH PERFORMANCE ADC.
- THIS MEASURE ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY, AND MOST IMPORTANTLY, *IMPROVED PERFORMANCE!*

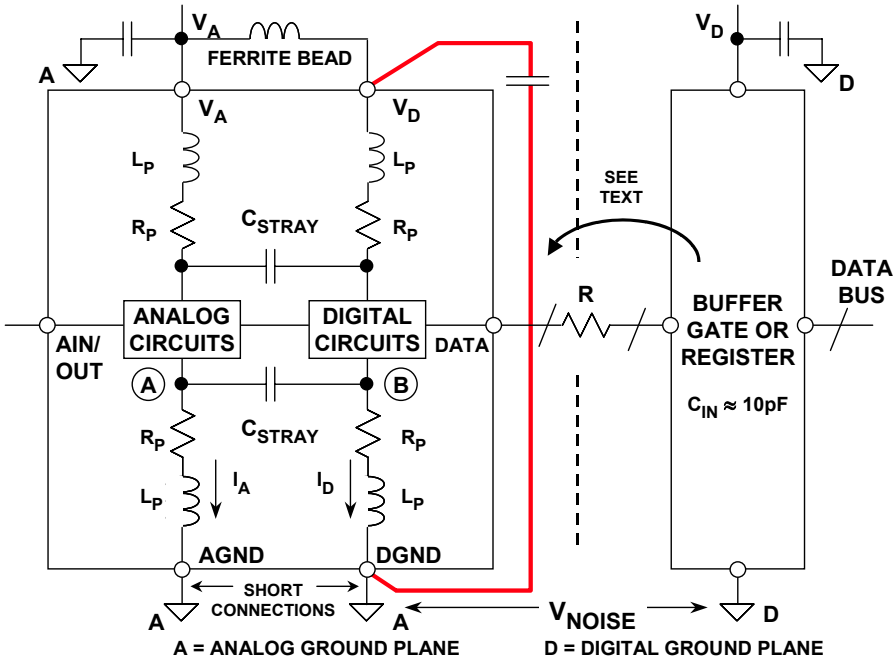
One part of the solution to the capacitively coupled noise issue is to isolate the converter from the data bus. This is accomplished by placing a Faraday shield, in the form of a buffer, between the converter and the data bus. This provides a degree of improvement due to the noise immunity provided by the buffer.

The bus between the buffer and the converter is lower noise since the load provided by these ICs requires less transient drive current (due to lower capacitance ~ 10pF).

The noise rejection of the "quiet" bus can be further enhanced by only making this bus active when actually writing to or reading from the converter. This is accomplished by replacing the buffer with a latch and providing some address decoding.

Further improvement could possible be achieved by connecting pull-up/pull-down resistors to the data lines.

Proper Grounding of Mixed-Signal ICs With Low Internal Digital Currents



A more complete solution is shown here. In addition to the “quiet” bus solution of the previous slide, attention is paid to how the grounds are handled.

Historically converters have had two separate grounds. These were typically designated as “AGND” (for analog ground) and “DGND” (for digital ground). Conventional wisdom said to connect AGND to the system analog ground and DGND to the system digital ground. The "star" point (the point where the two grounds connect) was at the converter.

This worked if there is only one converter in the system. It also worked better with the relatively low speed logic of years ago. As systems have increased in both complexity and speed, this approach is no longer optimum.

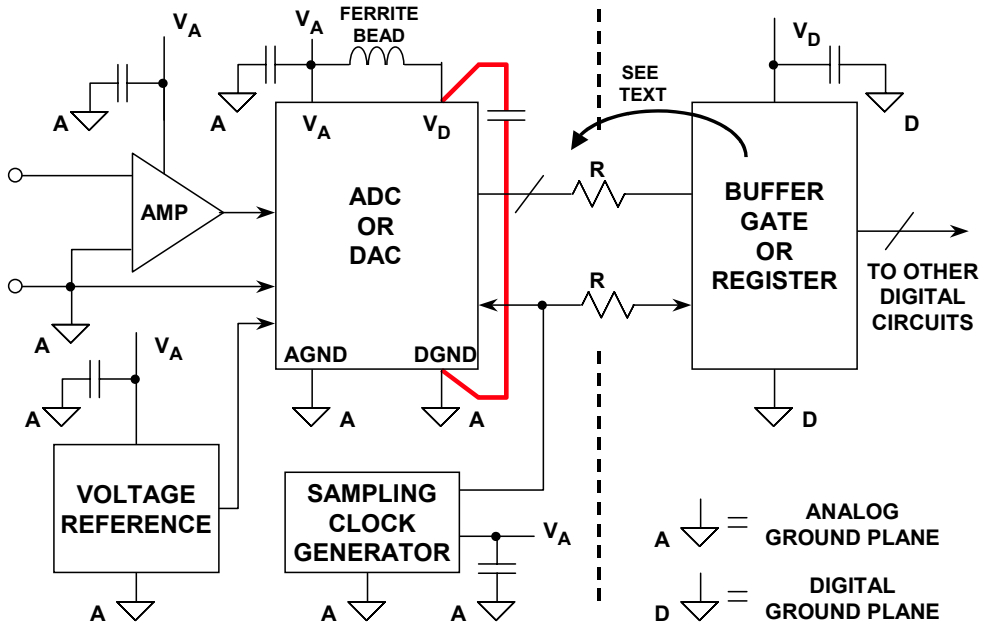
As shown, both grounds of the converter are connected to the system analog ground. This is because it causes less problems for the relatively small amount of digital return current to be returned through the analog ground than it would to connect the converter to the much more noisy digital ground.

It can be seen that, in addition to the separate grounds, there are separate power supply pins. These should be connected to the analog supply as well. Note that even though the power is form the same source, there is a ferrite bead and a decoupling capacitor included in the digital supply pin. The intent here is to prevent the noise generated by the digital section of the converter from feeding back into the analog supply, rather than preventing noise from getting into the converter digital section.

Of course, there are occurrences where the digital power supply is different from the analog supply where this won’t apply. The digital supply should still be developed from the analog source.

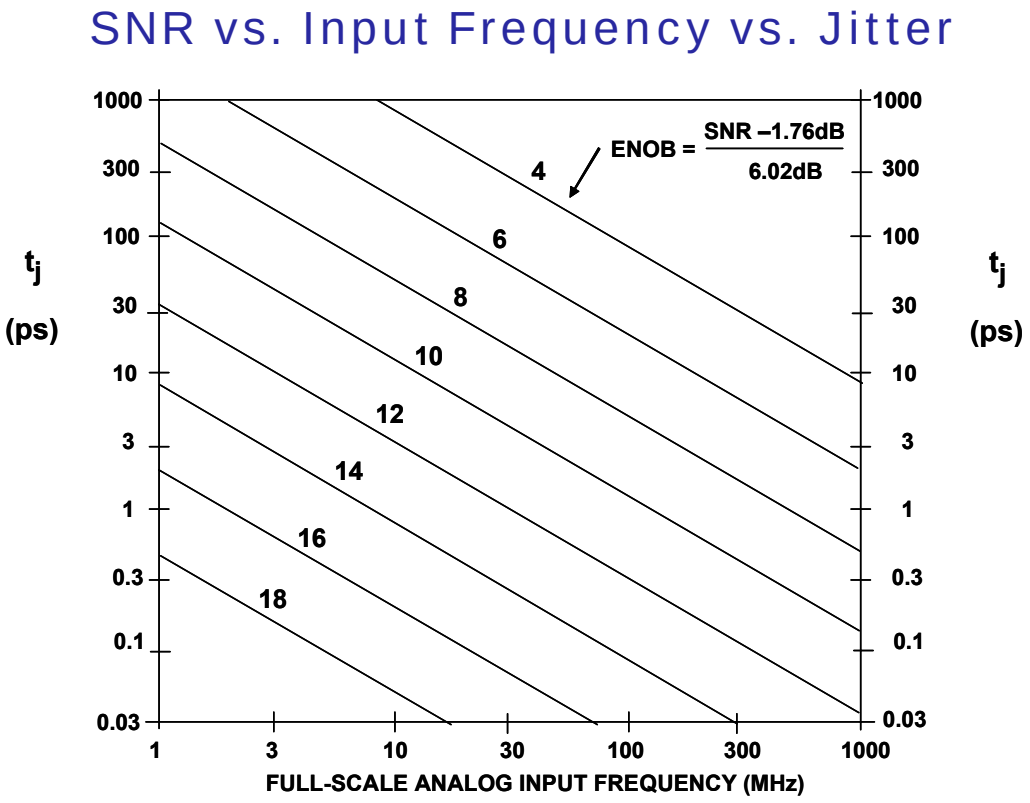
There is one concern here, however. The return path for the digital bus will be through the digital ground and then through the analog ground. This could result in a fairly large enclosed loop, resulting in a interference problem.

Grounding and Decoupling Points



The clock, even though it is typically viewed as a digital signal, should be handled in the analog domain as well. The primary reason for this is to keep the jitter low. This is especially true as frequency goes up. As we have seen previously, high speed, high accuracy converters require a low jitter clock to realize their performance.

If required elsewhere in the system the clock can be distributed the same way as the converter digital input/output.



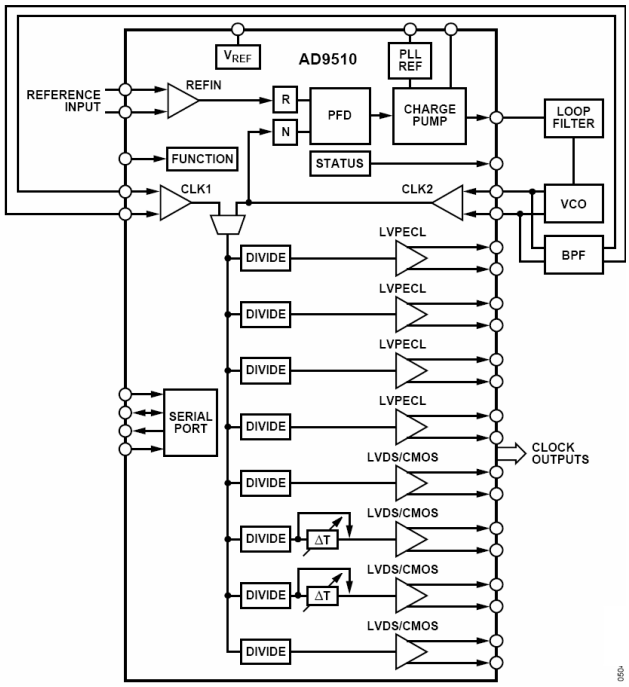
This figure is a reminder of the effect of sampling clock phase jitter on the SNR of an ADC.

This is the maximum signal to noise (SNR) performance possible with a given amount of phase jitter on the clock. Any other signal impairment will only reduce the SNR.

It is obvious that the issue of phase jitter becomes more important as the analog input frequency increases. This is because a given amount of jitter produces a larger error as the slew rate of the input signal increases. SNR is related to the analog input frequency and the clock jitter by the expression:

$$SNR = 20\log[1/2\pi ft_j].$$

AD9510 Clock Generation and Distribution



A good way of generating a low phase noise clock is to use a member of the AD851X clock generation and distribution circuits. These circuits are available as generation only, distribution only, and combination parts, as illustrated by the AD9510 in this figure.

The generation section is based on PLL and/or DDS technology .

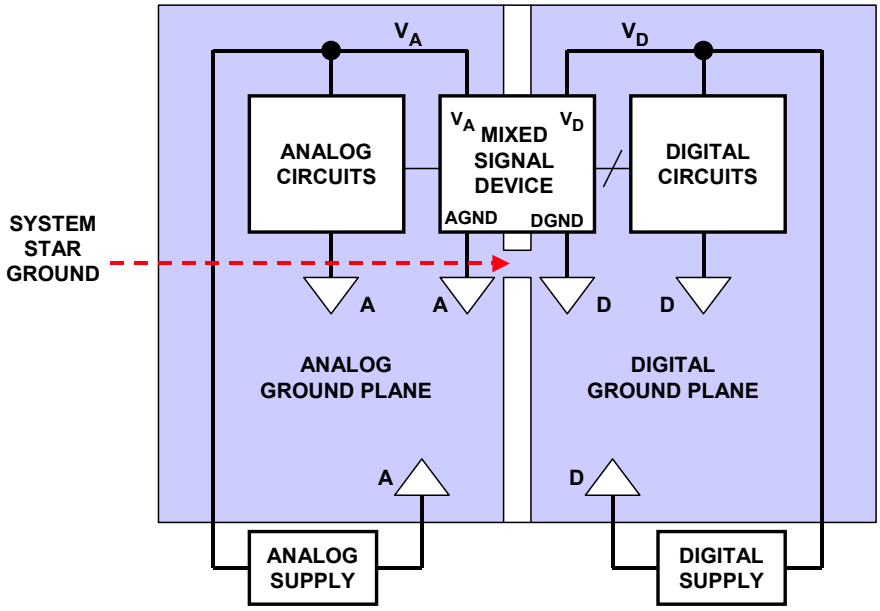
The PLL section consists of a programmable reference divider (R); a low noise phase frequency detector (PFD); a precision charge pump (CP); and a programmable feedback divider (N).

By connecting an external VCXO or VCO to the CLK2/CLK2B pins, frequencies up to 1.6GHz may be synchronized to the input reference.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment. Two of the LVDS/CMOS outputs feature programmable delay elements with full-scale ranges up to 10ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose for each full-scale setting.

An external band-pass filter may be used to try to improve the phase noise and spurious characteristics of the PLL output. This option is most appropriate to optimize cost by choosing a less expensive VCO combined with a moderately priced filter. Note that the BPF is shown outside of the VCO-to-N divider path, with the BP filter outputs routed to CLK1.

Grounding Mixed Signal ICs: Single PC Board (Typical Evaluation/Test Board)

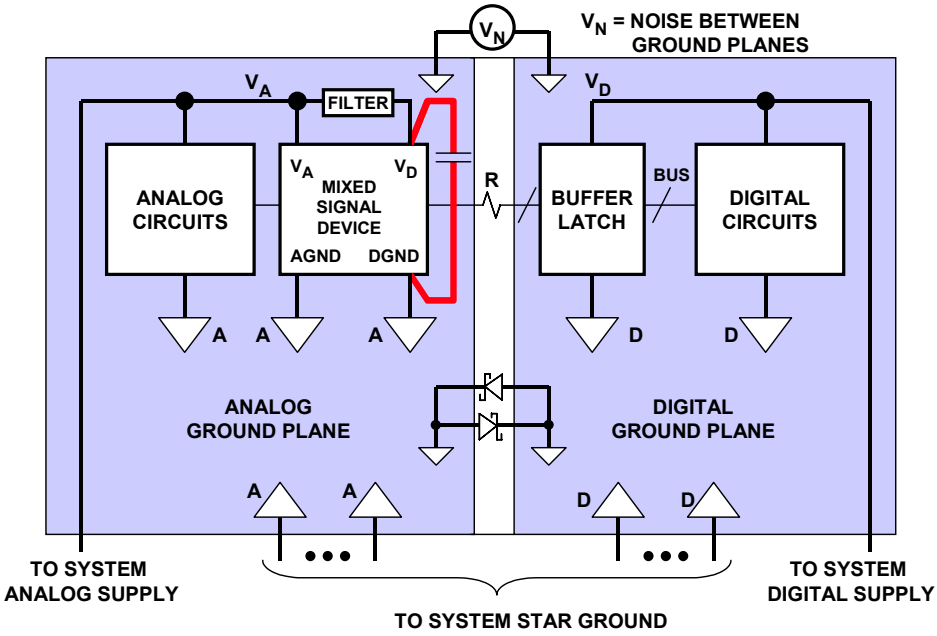


The technique shown in Figure 4.15 assumes a converter with a minimum of digital content. Low digital content implies low digital supply currents.

In some instances the converter will have significantly more digital content. An example of this would be a Sigma-Delta converter, which would include a digital filter as a subsection of the converter architecture. Other examples of high digital content components would be mixed signal parts, codecs, AFEs (analog front ends), and receive signal processors, In the case of higher digital content it may be desirable to keep the digital signals isolated from the analog ground. This is how the evaluation boards for these parts are typically designed. The star point for the system is at the converter.

The problem is that an evaluation board is a fairly small system. What is appropriate for this system may not be appropriate for a larger system containing many data converters. Connecting the ground planes together at each data converter generates multiple "star" points and can introduce ground loops.

Grounding Mixed Signal ICs with High Internal Digital Currents: Multiple PC Boards

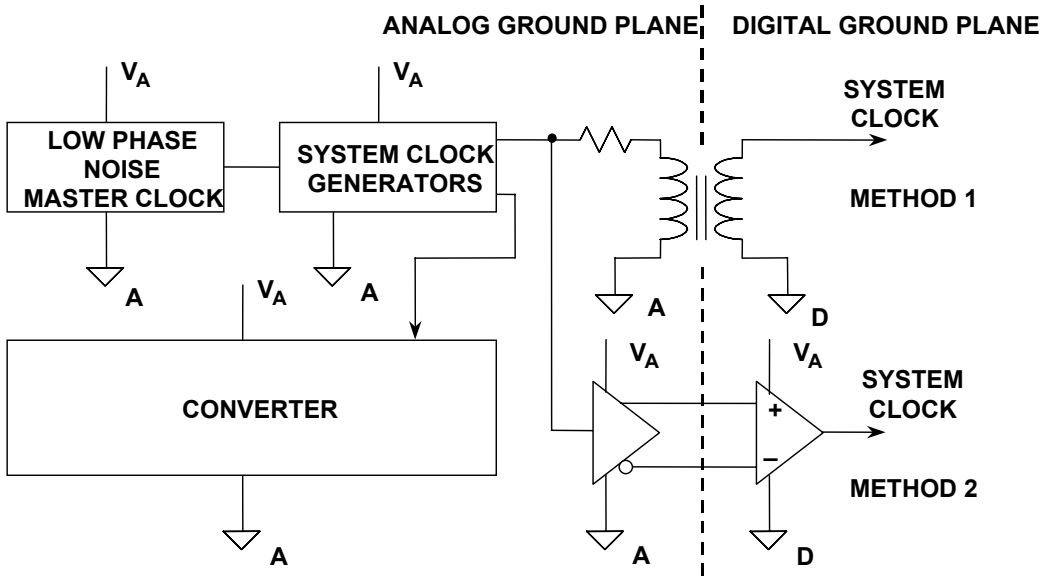


In some cases, even high digital content parts should be connected to the analog ground plane. This is especially true in systems where there are a number of converters, and the star ground point is usually located near the system power supplies.

The caveats noted in Figure 4.19 still apply. The return currents for the digital signals flow through the digital ground and the analog ground and can enclose a large loop.

The back-to-back Schottky diodes are there as protection. They will ensure that the grounds on the board will not drift too far away from each other, should there be a break in the connection between the board and the power supply. A typical specification for the maximum allowable voltage between the analog and digital grounds is ±300mV.

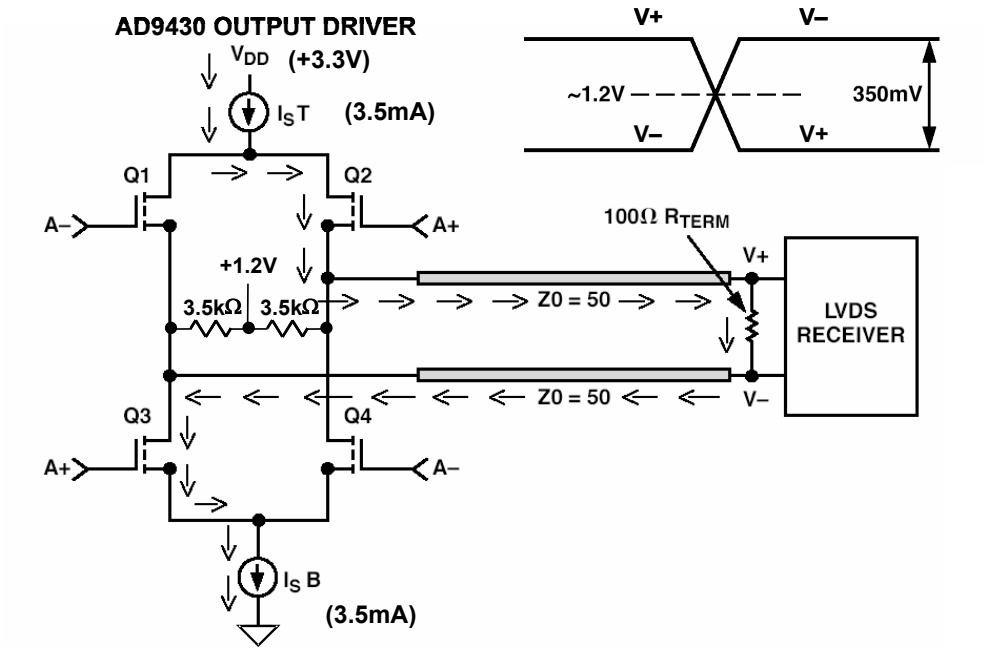
Balanced Sampling Clock or Data Distribution From Analog to Digital Ground Planes



One possible solution to the problem of the return currents enclosing a large loop is to cross the boundary between the analog and digital ground plane with a balanced signal. In this case the return currents will form a very small loop.

This technique works for both clocks and digital signals.

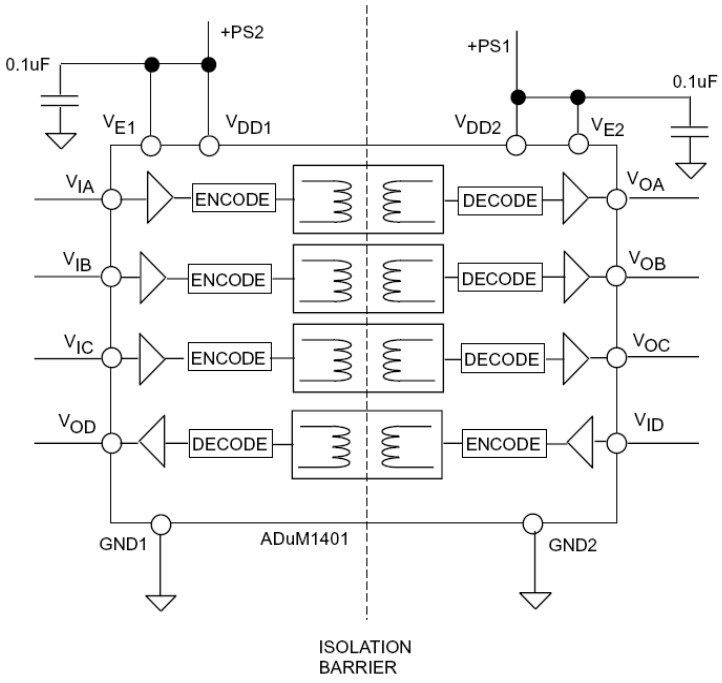
LVDS Driver and Receiver



Another alternative for balanced signals might be the use of LVDS (Low Voltage Differential Signal) components.

LVDS is basically a descendant of emitter-coupled logic (ECL). It generates much less noise, since it is not saturating logic like TTL or CMOS. The current remains the constant, thereby minimizing transient switching noise.

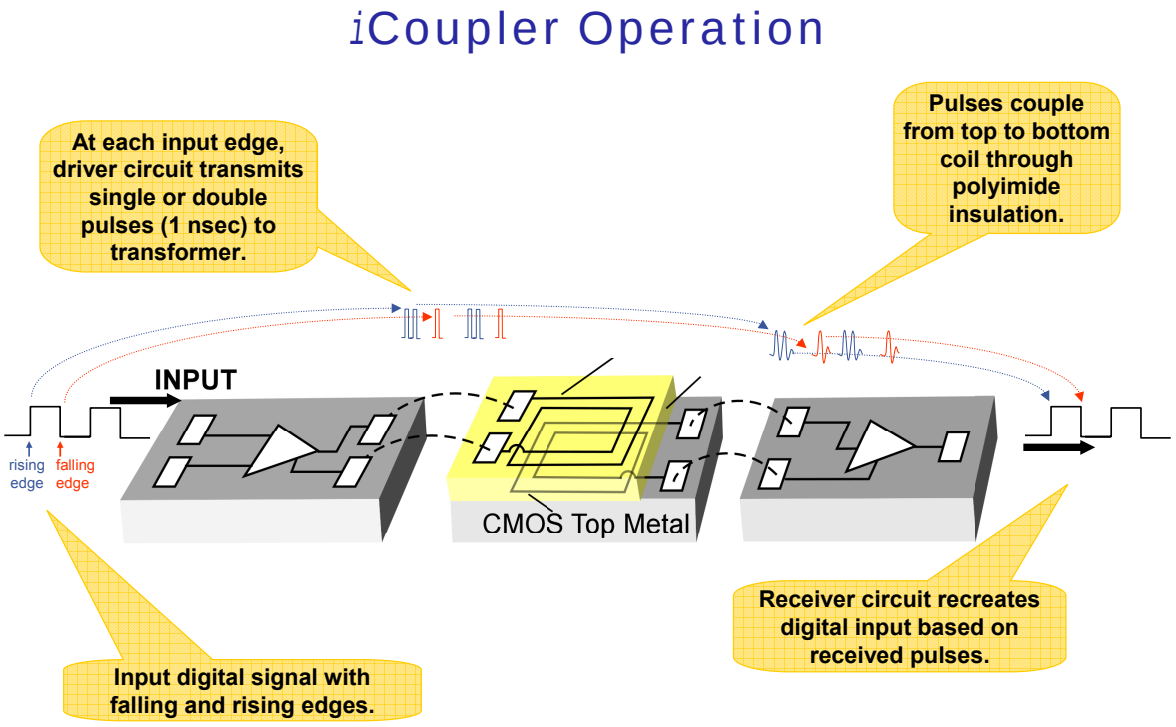
*i*Coupler Block Diagram



Another possibility is to use an isolation device to separate the grounds. This is demonstrated here by the *i*Coupler.

Designed primarily for galvanic isolation in industrial applications, the *i*Coupler isolator can be used to pass signals between ground planes at different potentials. No currents will circulate through the various grounds, since we are using transformers to isolate the grounds. The transfer rate through the *i*Coupler can be as high as 100MB/s.

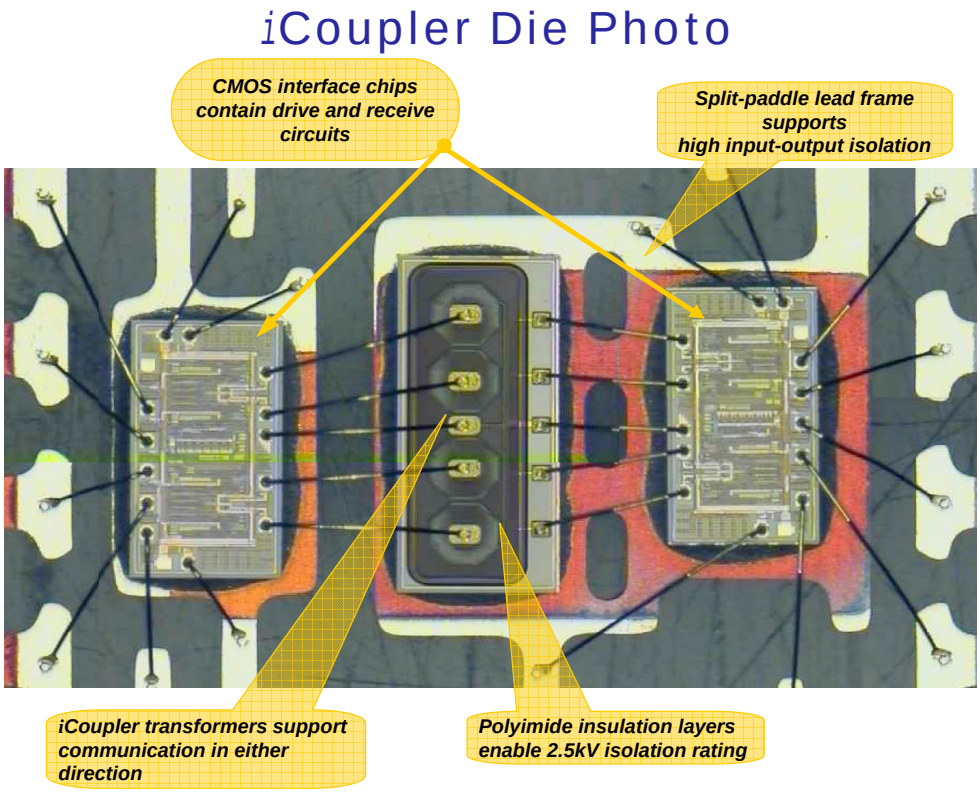
Different models of the *i*Couplers have different configurations of forward and return paths.



This figure illustrates *i*Coupler operation.

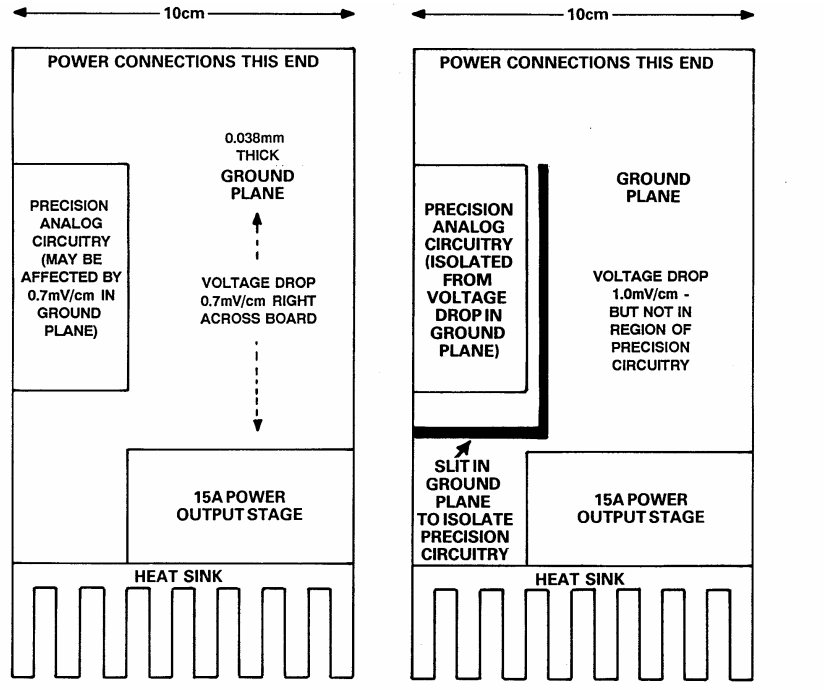
Transformer coupling is used for the isolation. There are separate transmit and receive circuits on either side. The planar transformers use CMOS metal layers, plus a gold layer that is placed on top of the passivation. A high breakdown polyimide layer underneath the gold layer insulates the top transformer coil from the bottom.

*i*Couplers have very good noise immunity since the area enclosed by the loop is very small, making it a very poor antenna, which is a good thing.



This is a die photo to show the three sections of the *i*Coupler inside the package. The internal spacing is needed where high isolation voltage is required. A high isolation voltage is not required for simply isolating grounds.

A Slit in the Ground Plane Can Reconfigure Current Flow for Better Accuracy

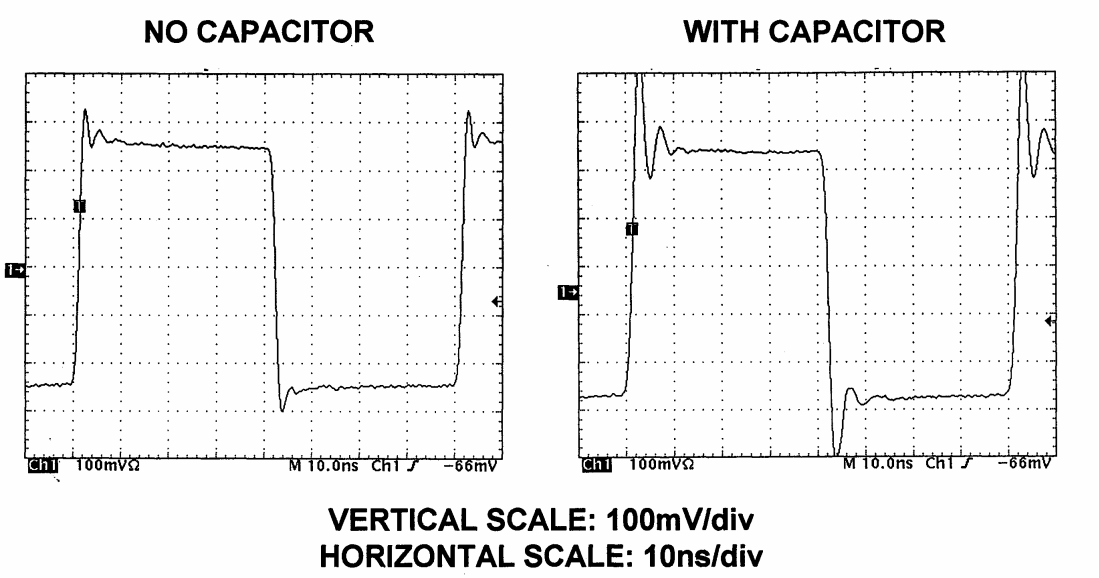


In most cases, a ground plane should be as free from breaks and crossovers as possible. An example of where this is not so is shown in this figure.

As originally designed this board had a solid ground plane. The location of the edge connector and the high current circuit was set by the physical constraints of the system. As originally configured, the relatively large current of the output section flowed through the sensitive precision circuitry. This caused an offset voltage error.

By adding the slit in the ground plane, these currents are forced to flow around the precision circuitry, thereby eliminating the offset error.

Effects of 10pF Stray Capacitance on the Inverting Input on Amplifier Pulse Response



VERTICAL SCALE: 100mV/div
HORIZONTAL SCALE: 10ns/div

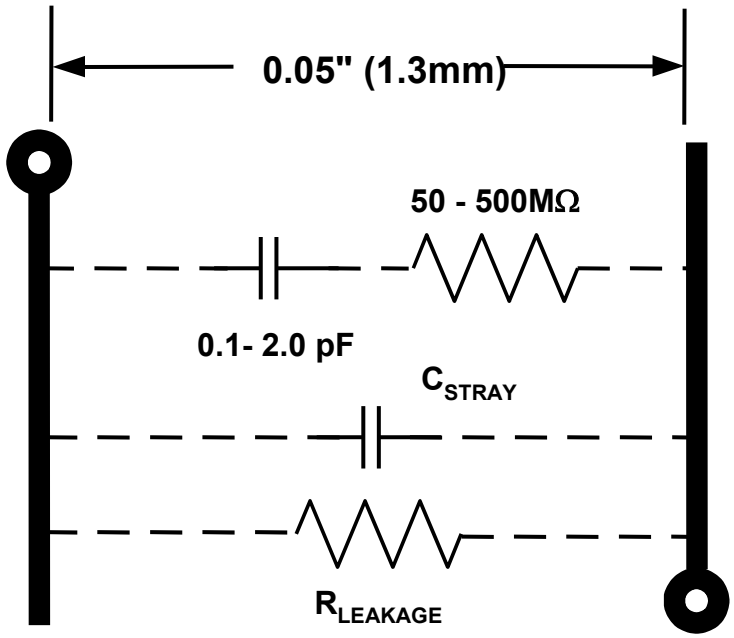
Another example of where less ground plane is better is shown here.

Stray capacitance on the inverting input of current feedback amplifiers causes peaking and instability.

These scope captures show the effect on pulse response of a small (10pF) stray capacitance on the inverting input of a typical current feedback amplifier. This capacitance can be caused by running the ground plane too close to the pin on the amplifier.

In most cases, the ground plane should be etched away directly underneath the inverting input pin so that parasitic capacitance is minimized.

Parasitics Plague Dynamic Response of PCB-Based Circuits



In addition to the parasitics created between a trace and ground, there can also be parasitics between two traces running parallel to each other.

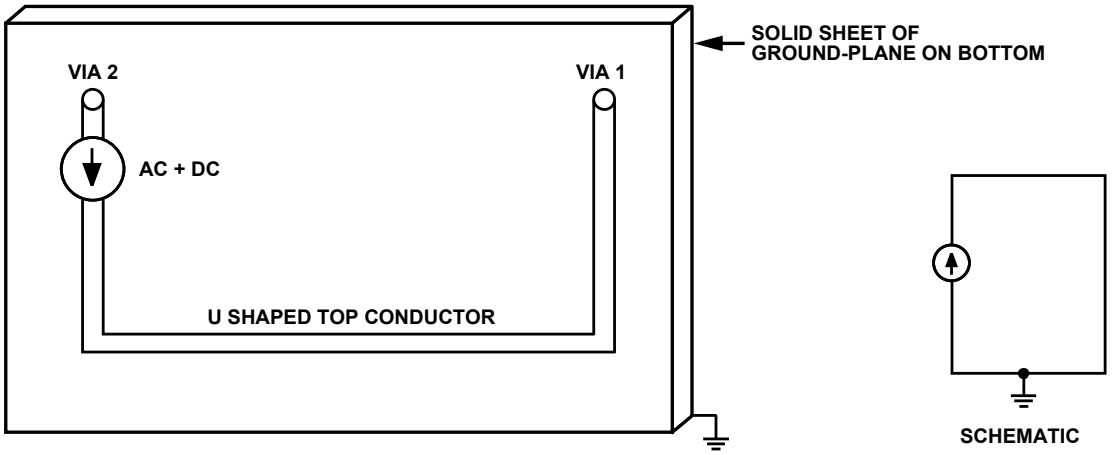
This figure gives an idea of the magnitude of the parasitics between two traces 50 mils apart. Closer spaced traces will have more stray capacitance. In addition, the capacitance will vary with the PC board material and the solder mask used.

Dielectric absorption (DA) represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in this figure, the RC model for this effective capacitance ranges from 0.1 to 2.0pF, with the resistance ranging from 50 to 500MΩ. Values of 0.5pF and 100MΩ are most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

Fortunately, there are solutions to DA. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through-hole components). In addition, low-loss PCB dielectrics are also available.

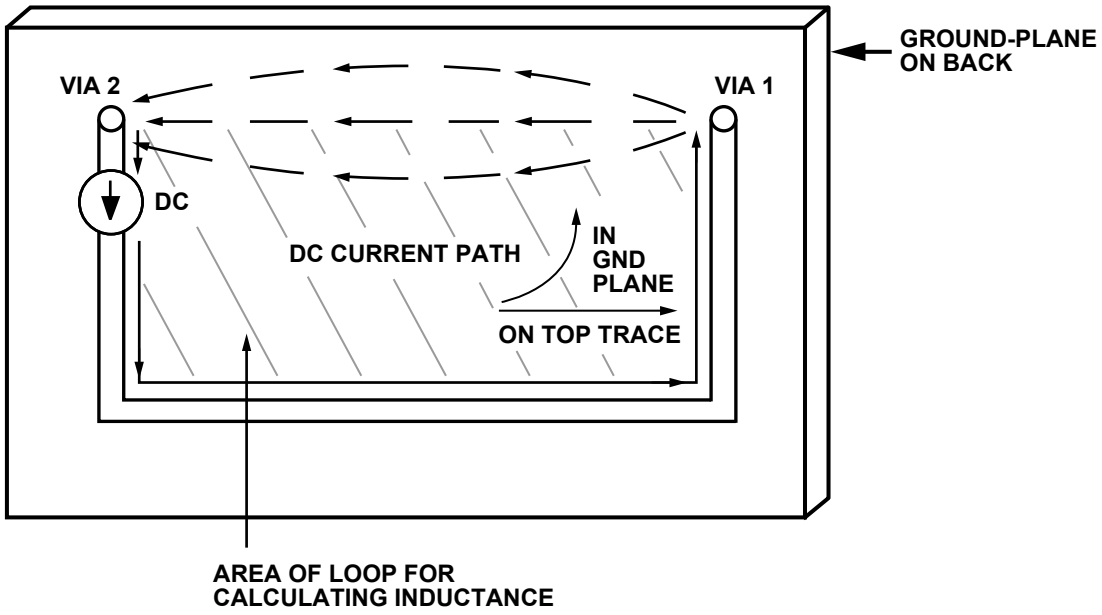
Schematic and Layout of Current Source with U-shaped Trace on PC Board and Return Through Ground Plane



Ground planes are the most effective way to provide a low impedance current return path.

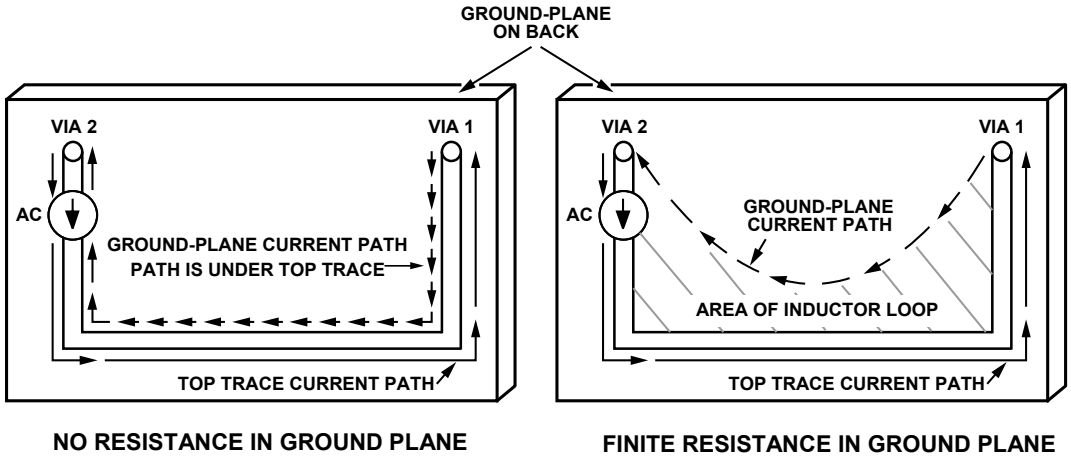
The following several figures investigate the return current flow in a circuit formed by a current source driving a current into a “U”-shaped trace on the top layer of a PC board with a ground plane for the return.

DC Current Flow for Figure 4.29



At dc and low frequencies, the current return path will be the path of least resistance, which will be the most direct path between the two vias. There will be some spreading of the return current path due to the finite resistance in the ground plane, but the return current basically takes the most direct path.

AC Current Path Without (left) and With (right) Resistance in the Ground Plane

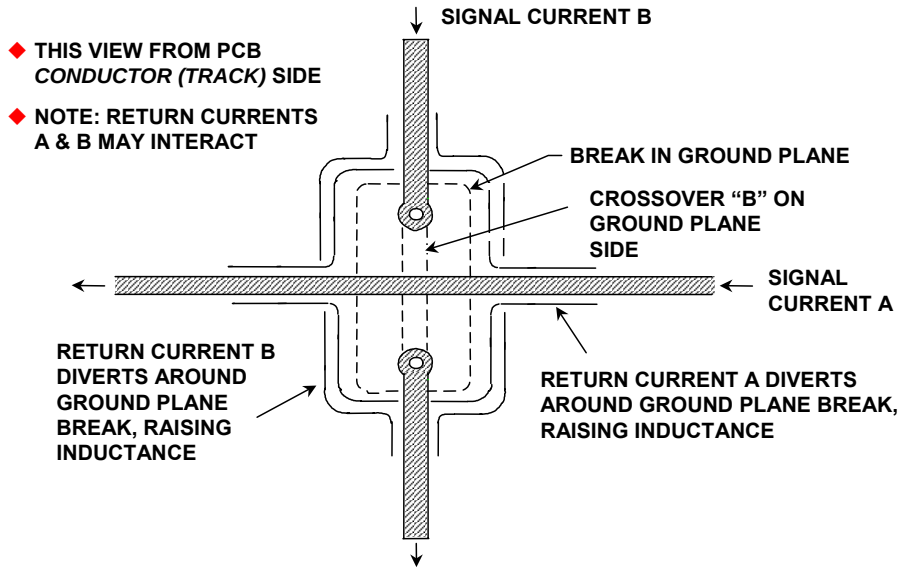


At higher frequencies, however, the return current follows the path of least *impedance* rather than the path of least resistance.

Inductance will be minimized when the enclosed area is reduced as much as possible. This occurs when the enclosed loop is at it's minimum, and that is when the return current flows directly under the forward path. Again, there will be some spreading of the path due to resistance, and there will also be frequency dependence. However, as frequency goes up, the return current will more closely follow the forward path.

The return current flow is nearly completely under the forward trace even at frequencies as low as 1 to 2MHz.

A Ground Plane Break Raises Circuit Inductance and Increases Vulnerability to External Fields



Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in this figure, where conductors A and B must cross one another.

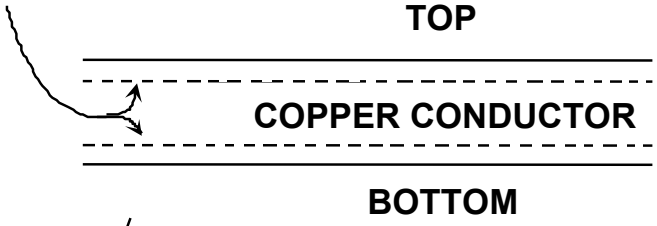
Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

The use of double-sided or multi-layer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

Skin Depth in a PCB Conductor

- **HF Current flows only in thin surface layers**



- **Skin Depth ≈ 6.61 / √f cm, f in Hz**
- **Skin Resistance ≈ 2.6×10^{-7} √f ohms per square, f in Hz**
- **Since skin currents flow in both sides of a PC track, the value of skin resistance in PCBs must take account of this**

At high frequencies, we must also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

The equation for calculating the skin depth is given as:

$$\delta = \sqrt{\frac{2}{\mu\,\omega\,\sigma}} = \sqrt{\frac{\rho}{f\,\pi\,\mu}}$$

where:

μ = permeability ($4\pi \times 10^{-7}$ H/m), note: H = henries = Ω·s

δ = skin depth (m)

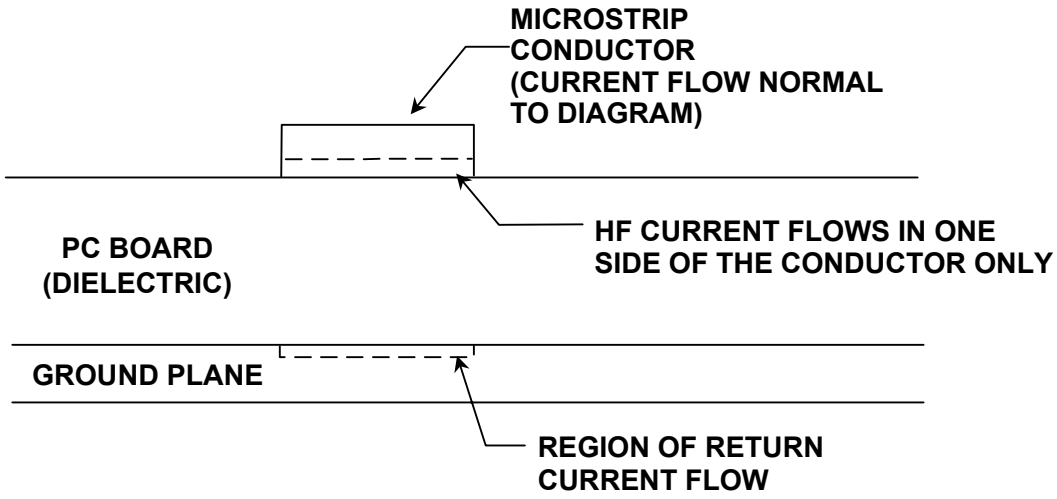
ρ = resistivity (Ω·m)

ω = radian frequency = $2\pi f$ (Hz)

σ = conductivity (mho/m), note: mho [℧] = siemen [S]

Obviously the skin depth calculation breaks down when the skin depth is greater than the conductor thickness (i.e., at lower frequencies).

Skin Effect with PCB Conductor and Ground Plane



This figure shows the regions of current flow for higher frequencies, as it is reduced by the skin effect.

It is important to remember that the current will flow in both sides of the PCB trace. This is not necessarily the case with microstrips, however. These will be covered next.

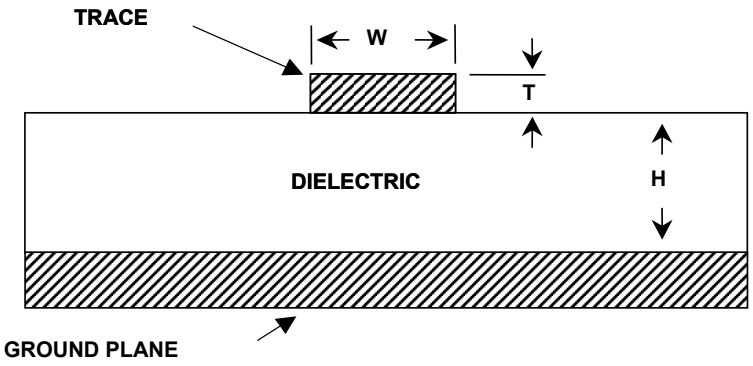
In the case where current does flow in both edges of a trace, the resistivity is halved.

For copper, the equation for skin depth and skin resistance can be approximated by:

Skin Depth $\approx 6.61 / \sqrt{f}$ cm, where f is in Hz.

Skin Resistance $\approx 2.6 \times 10^{-7} \sqrt{f}$ ohms per square, where f is in Hz.

A Microstrip Transmission Line



$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right]$$

The characteristic impedance of a microstrip transmission line will depend on the width and thickness of the trace and the thickness and dielectric constant of the PCB material.

The characteristic impedance is unimportant at lower frequencies, but is important in maintaining proper termination of signal lines as frequency increases.

For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50Ω.

Characteristic Capacitance and Propagation Delay in a Stripline

- **In addition to the characteristic impedance (Z_0). the stripline also has a characteristic capacitance, which can be calculated in terms of pF/in:**

$$C_o(pF/in) = \frac{0.67(\varepsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]}$$

- **The propagation delay of the stripline is shown in slide 4.35**

$$t_{pd}(ns/ft) = 1.017\sqrt{0.475\varepsilon_r + 0.67}$$

- **or, in terms of ps:**

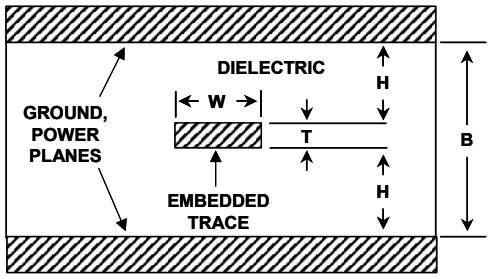
$$t_{pd}(ps/in) = 85\sqrt{0.475\varepsilon_r + 0.67}$$

- **Thus, for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional approximations can be useful in designing the timing of signals across PCB trace runs.**

In addition to the characteristic impedance we should be aware of the characteristic capacitance of the trace. This could become an issue in some applications.

Driving large capacitances requires more drive capability from the op amp. Large capacitive loads may also cause the op amp driver to become unstable.

A Symmetric Stripline Transmission Line



$$Z_o(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right]$$

A microstrip transmission line can also be embedded between two ground or power planes (remembering that a power plane is essentially a ground plane for ac signals).

In this case we must calculate the characteristic impedance including both planes.

Characteristic Capacitance and Propagation Delay in a Symmetrical Stripline

- **The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in:**

$$C_O(pF/in) = \frac{1.41(\varepsilon_r)}{\ln[3.81H/(0.8W+T)]}$$

- **The propagation delay of the symmetric stripline is shown in slide 4.37**

$$t_{pd}(ns/ft) = 1.017\sqrt{\varepsilon_r}$$

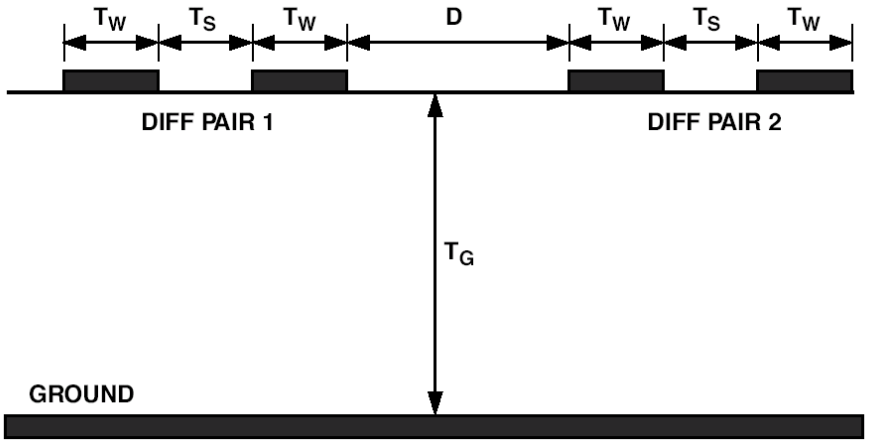
- **or, in terms of ps:**

$$t_{pd}(ps/in) = 85\sqrt{\varepsilon_r}$$

- **For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.**

As in the case of a stripline, in addition to the characteristic impedance of a symmetrical stripline we should be aware of the characteristic capacitance as well. This could become an issue in some applications. Driving larger capacitances requires more drive ability for the output of the driving amplifier. Again, stability may be an issue with the load capacitance affecting the driving op amp.

Microstrip PCB Layout for Two Pairs of LVDS Signals



- **Keep T_W, T_S, and D constant over the trace length**
- **Keep T_S ~ < $2T_W$**
- **Avoid use of vias if possible**
- **Keep D > $2T_S$**
- **Avoid 90° bends if possible**
- **Design T_W and T_G for ~ 50Ω**

Some rules of thumb for laying out LVDS microstrip lines are given here.

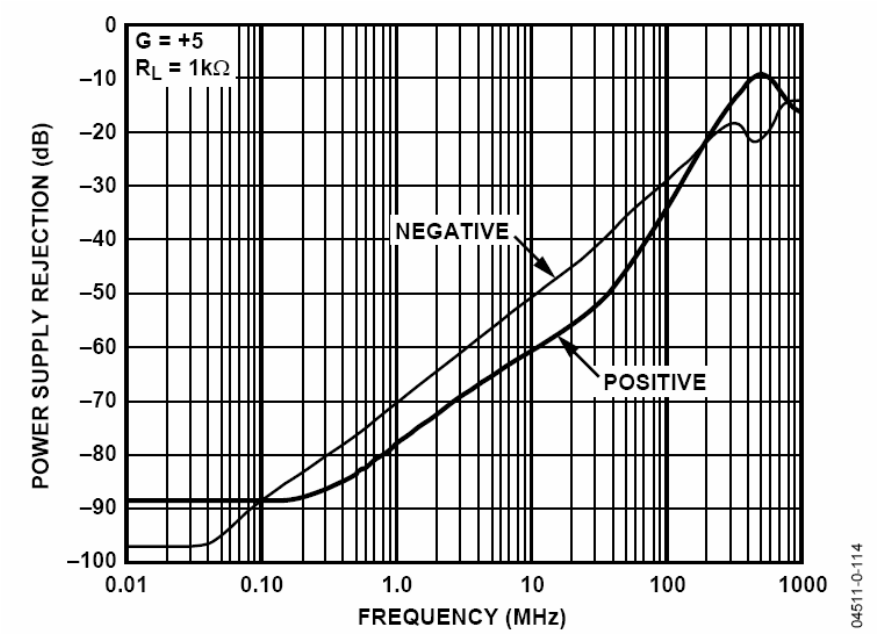
LVDS outputs for high-performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 to 10 meters in high-speed digital applications (dependent on data rate), it is not recommended to let a high-performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs. This also controls the power that the output drivers have to develop to drive the line, which keeps the internal noise of the converter down. The differential output traces should be routed close together, maximizing common-mode rejection, with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew.

The impedance can be determined by the information in Figure 4.35.

Decoupling

Power supply decoupling is important in any precision or high speed circuit. The power supply is part of the circuit and should be handled accordingly. The idea is to develop a low noise environment in which the circuit can operate. Improper decoupling can destroy the performance of an otherwise competent design.

Power Supply Rejection Ratio vs. Frequency for the AD8099



Why is decoupling necessary?

This graph shows how the power supply rejection ratio (PSRR) of an amplifier varies with frequency. The power supply pin is really in series with the output. Therefore, any high frequency energy on the power line will couple to the output directly. So it is necessary to keep this high frequency energy from entering the chip in the first place. This is done by using a small capacitor to short the high frequency signals away from the chip.

Power supply rejection of data converters is typically the same order of magnitude as shown in this figure.

Another aspect to decoupling is the lower frequency interference. Here we use larger electrolytic capacitors as shown in the next figure.

What Is Proper Decoupling?

- **A large electrolytic capacitor (typ. 10 µF – 100 µF) no more than 2 in. away from the chip.**
  - **The purpose of this capacitor is to be a reservoir of charge to supply the instantaneous charge requirements of the circuits locally so the charge need not come through the inductance of the power trace.**
- **A smaller cap (typ. 0.01 µF – 0.1 µF) as physically close to the power pins of the chip as is possible.**
  - **The purpose of this capacitor is to short the high frequency noise away from the chip.**
- **Optionally a small ferrite bead in series with the supply pin.**
  - **Localizes the noise in the system.**
  - **Keeps external high frequency noise from the IC.**
  - **Keeps internally generated noise from propagating to the rest of the system.**

As stated, the electrolytic type large value capacitors are used as local charge reservoirs. This means that the instantaneous current requirements do not have to be met by the power supply, which may be located an appreciable distance away with a considerable amount of inductance in the line.

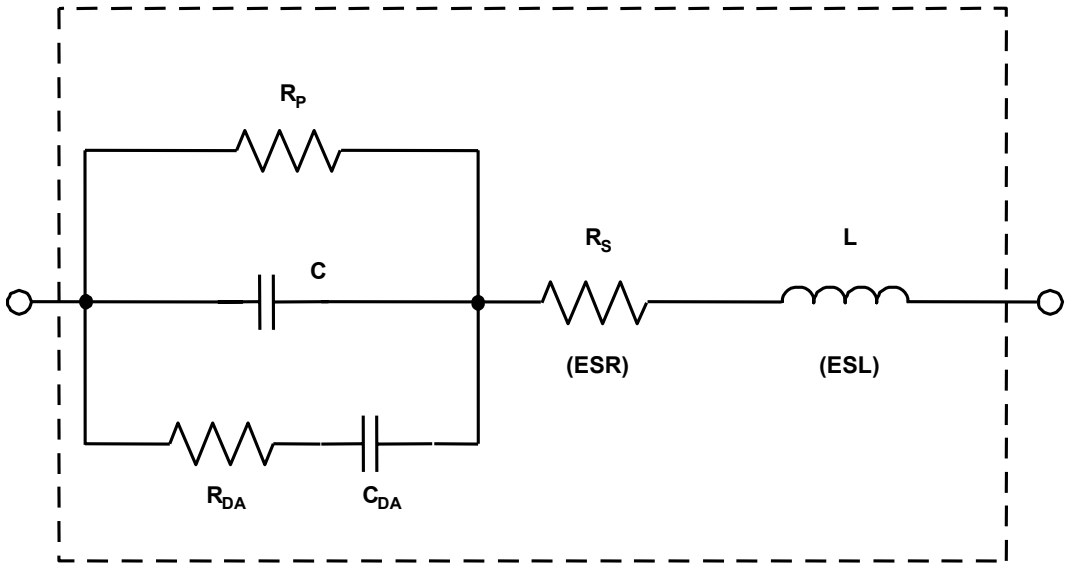
The smaller value capacitors are used to short the high frequency interference away from the chip. Relevant parameters here are low equivalent series inductance (ESL) and equivalent series resistance (ESR). Quite often multilayer ceramics are excellent choices for these applications.

Ferrites (nonconductive ceramics manufactured from the oxides of nickel, zinc, manganese, or other compounds) are useful for decoupling in power supply filters. At low frequencies (<100kHz), ferrites are inductive; thus they are useful in low-pass LC filters. Above 100kHz, ferrites becomes resistive, an important characteristic in high-frequency filter designs. Ferrite impedance is a function of material, operating frequency range, dc bias current, number of turns, size, shape, and temperature.

The ferrite beads may not always be necessary, but they will add extra high frequency noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, especially when op amps are driving high output currents. When a ferrite saturates it becomes nonlinear and loses its filtering properties.

Note that some ferrites, even before full saturation occurs, can be nonlinear; so if a power stage is required to operate with a low distortion output, this should also be checked in a prototype.

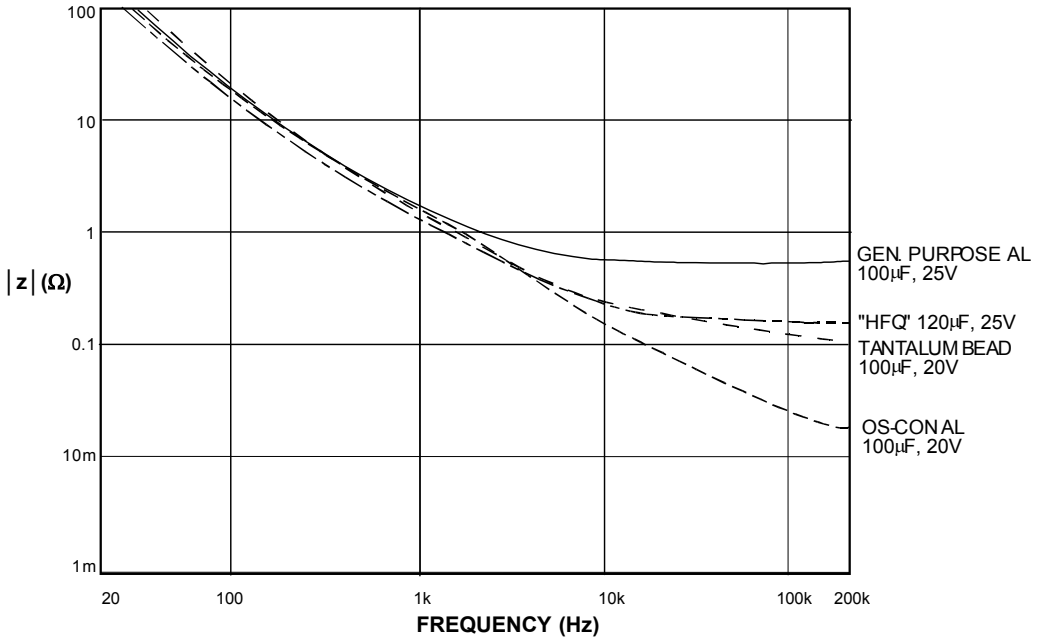
A Nonideal Capacitor Equivalent Circuit Includes Parasitic Elements



This is a workable model of a nonideal capacitor. The nominal capacitance, C, is shunted by a resistance RP, which represents insulation resistance or leakage. A second resistance, RS—equivalent series resistance, or ESR,—appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

Note that capacitor phenomena aren't that easy to separate. The model is for convenience in explanation. Inductance, L—the equivalent series inductance, or ESL,—models the inductance of the leads and plates. Finally, resistance R_{DA} and capacitance C_{DA} together form a simplified model of a phenomenon known as dielectric absorption, or DA. It can ruin fast and slow circuit dynamic performance. In a real capacitor, R_{DA} and C_{DA} may actually consist of multiple parallel sets.

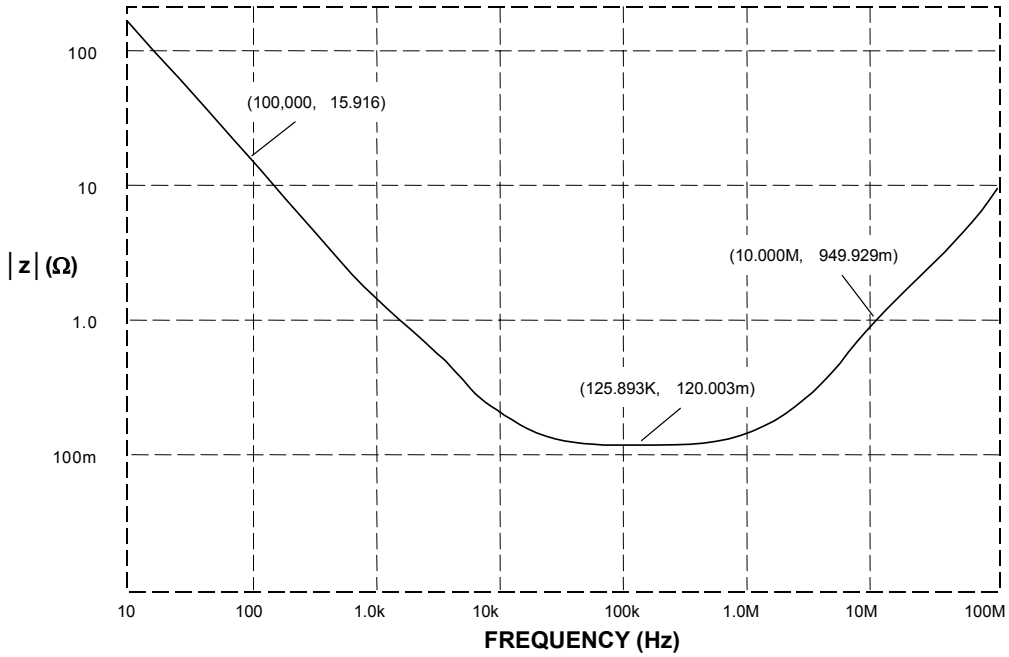
Impedance Z(Ω) vs. Frequency for 100µF Electrolytic Capacitors



This figure illustrates the high frequency impedance characteristics of several electrolytic capacitor types, using nominal 100µF/20V samples. In these plots, the impedance, |Z|, vs. frequency over the 20Hz to 200kHz range is displayed using a high resolution 4-terminal setup.

Shown in this display are performance samples for a 100µF/25V general purpose aluminum unit, a 120µF/25V HFQ unit, a 100µF/20V tantalum bead type, and a 100µF/20V OS-CON unit (lowest curve). While the HFQ and tantalum samples are close in the specified 100kHz impedance, the general purpose unit is about four times worse. The OS-CON unit is nearly an order of magnitude lower in 100kHz impedance than the tantalum and switching electrolytic types.

100µF/20V Tantalum Capacitor Simplified Model Impedance (Ω) vs. Frequency (Hz)



Here we have expanded the frequency range in the previous figure for the 100µF/20V tantalum electrolytic capacitor.

At low frequencies the net impedance is almost purely capacitive, as noted by the 100Hz impedance of 15.9Ω. At the bottom of this "bathtub" curve, the net impedance is determined by ESR, which is shown to be 0.12Ω at 125kHz. Above about 1MHz this capacitor becomes inductive, and impedance is dominated by the effect of ESL.

All electrolytics will display impedance curves which are similar in general shape. The exact values will be different, but the general shape stays the same. The minimum impedance will vary with the ESR, and the inductive region will vary with ESL (which in turn is strongly affected by package style).

Some Capacitor Dielectric Types for Decoupling Applications

Type	Typical DA	Advantages	Disadvantages
NPO Ceramics	< 0.1%	Small case size Inexpensive Many vendors Good stability Low inductance	DA generally low (may not be specified) Low maximum value
Monolithic Ceramic (High K)	>0.2%	Low inductance Wide range of values	Poor stability Poor DA High voltage coefficient
Multilayer Ceramic	< 0.1%	Very low inductance Small case size	

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size and low loss. But the characteristics of ceramic dielectrics varies widely. Some types are better than others for various applications, especially power supply decoupling. Ceramic dielectric capacitors are available in values up to several μF in the high-K dielectric formulations of X7R and Z5U, at voltage ratings up to 200V. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). The NP0 types are limited in available values to 0.1μF or less, with 0.01μF representing a more practical upper limit.

Multilayer ceramic “chip caps” are increasingly popular for bypassing and filtering at 10MHz or more, because their very low inductance design allows near optimum RF bypassing. In smaller values, ceramic chip caps have an operating frequency range to 1GHz. For these and other capacitors for high frequency applications, a useful value can be ensured by selecting a value which has a self-resonant frequency above the highest frequency of interest.

In general, film type capacitors are not useful in power supply decoupling applications. This is due to their construction. They are generally wound, which increases their inductance.

Electrolytic Capacitor Types for Power Supply Applications

Type	Advantages	Disadvantages
Aluminum	Cost Wide variety of values and working voltages	High leakage
Switching type Aluminum	High frequency performance Broader range of values than Tant.	Slightly more expensive than standard Al.
Tantalum	Size Lower ESR Better high frequency performance	Availability Limited range of values Cost
OS-CON	Much lower ESR Much better high frequency performance	Cost Availability

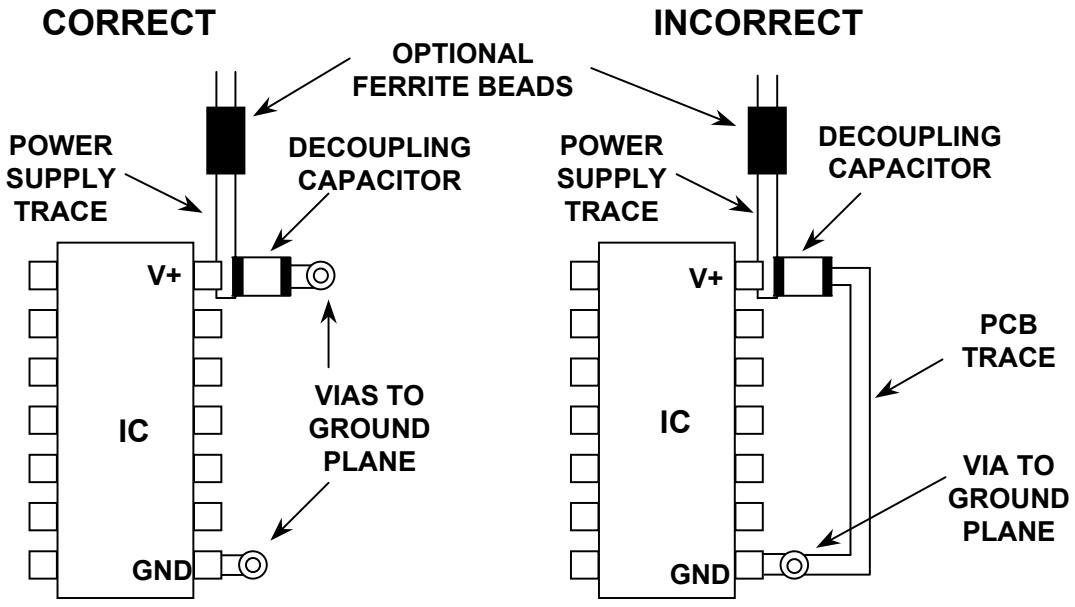
The electrolytic family provides an excellent, cost effective low-frequency filter component because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes general-purpose aluminum electrolytic types, available in working voltages from below 10V up to about 500V, and in size from 1μF to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without damage. They have relatively high leakage currents (this can be tens of μA, but is strongly dependent upon specific family design, electrical size, and voltage rating versus applied voltage). However, this is not likely to be a major factor for basic filtering applications.

A subset of aluminum electrolytic capacitors is the switching type, which is designed and specified for handling high pulse currents at frequencies up to several hundred kHz with low losses. This type of capacitor competes directly with the tantalum type in high frequency filtering applications and has the advantage of a much broader range of available values.

Also included in the electrolytic family are tantalum types, which are generally limited to voltages of 100V or less, with capacitance of 500μF or less. In a given size, tantalums exhibit higher capacitance-to-volume ratios than do the general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics and must be carefully applied with respect to surge and ripple currents.

More recently, high performance aluminum electrolytic capacitors using an organic semiconductor electrolyte have appeared. These OS-CON families of capacitors feature appreciably lower ESR and higher frequency range than do the other electrolytic types, with an additional feature of minimal low-temperature ESR degradation.

High Frequency Supply Filter(s) Require Decoupling via Short Low-Inductance Path (Ground Plane)

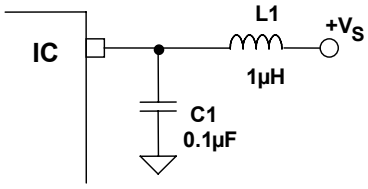


The decoupling capacitor must be as close to the chip as possible. If it is not, the inductance of the connecting trace will have a negative impact on the effectiveness of the decoupling.

In the left figure, the connection to both the power pin and the ground are a short as possible, so this would be the most effective configuration.

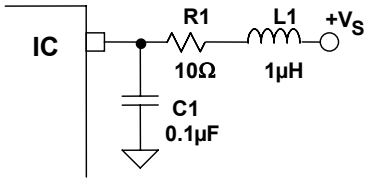
In the figure on the right, however, the extra inductance and resistance in the PCB trace will cause a decrease in the effectiveness of the decoupling scheme and may cause interference problems by increasing the enclosed loop.

Resonant Circuit Formed by Power Line Decoupling



EQUIVALENT DECOUPLED POWER LINE CIRCUIT RESONATES AT:

$$f = \frac{1}{2\pi\sqrt{LC}}$$



SMALL SERIES RESISTANCE CLOSE TO IC REDUCES Q

An inductor in series or parallel with a capacitor forms a resonant, or "tuned," circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q (quality factor) of the tuned circuit. The Q of a resonant circuit is a measure of its reactance to its resistance.

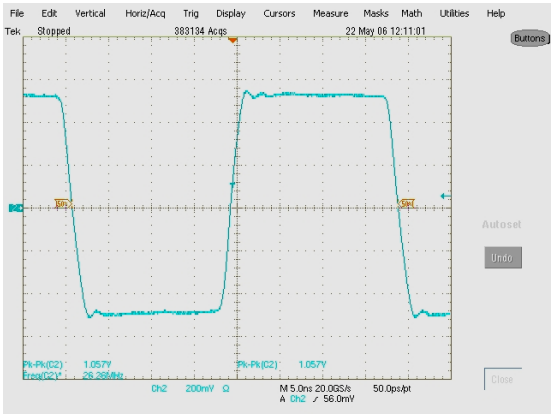
$$Q = 2 \pi f (L/R)$$

If stray inductance and capacitance in a circuit forms a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

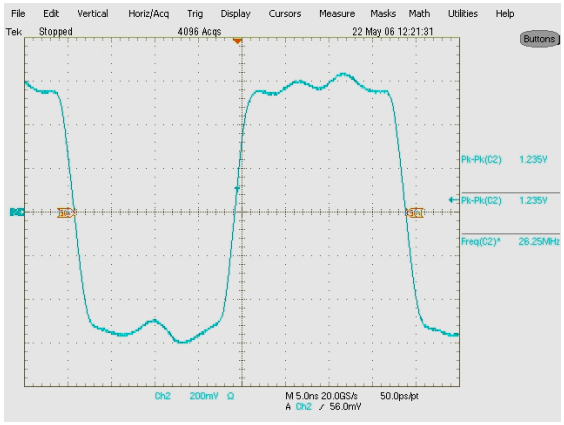
While normal trace inductance and typical decoupling capacitances of 0.01µF to 0.1µF will resonate well above a few MHz, an example 0.1µF capacitor and 1µH of inductance resonates at 500kHz. Left unchecked, this could present a resonance problem, as shown in the left case. Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10Ω) in the power line close to the IC, as shown in the right case.

The resistance should be kept as low as possible to minimize the IR drop across the resistor. The resistor should be as large as needed, but no larger. An alternative to a resistor is a small ferrite bead which looks primarily resistive at the resonant frequency.

Effects of Decoupling on Performance of the AD8000 Op Amp



Proper decoupling



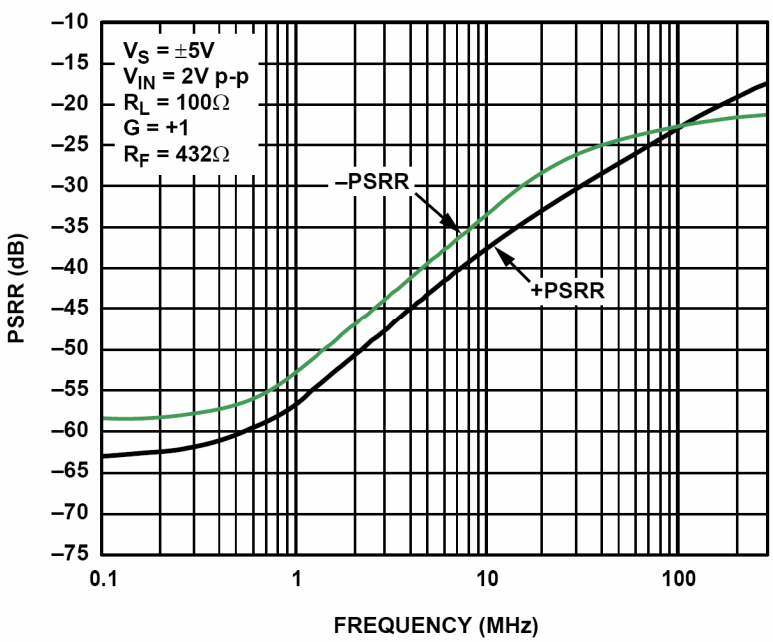
No decoupling

What is the effect of proper and improper decoupling?

Here is an example of what could happen to the response of an op amp with no decoupling.

Both of the oscilloscope graphs were taken on the same board. The difference is that on the right the decoupling caps were removed. Other than that everything remained the same. In this case the device was an AD8000, a 1.5GHz high speed current feedback op amp, but the effect will occur in most any high speed circuit.

AD8000 Power Supply Rejection Ratio (PSRR)

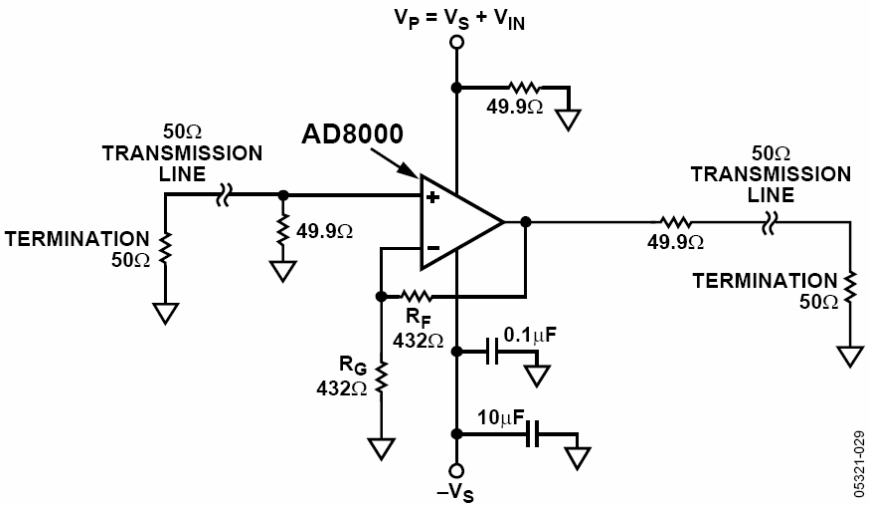


This figure shows the PSRR of the AD8000 as a function of frequency.

Note that the PSRR falls to a relatively low value in its working frequency range. This means that signals on the power line will propagate easily to the output.

As a side note, decoupling keeps signals generated internally in the op amp from propagating through the power lines to other circuits.

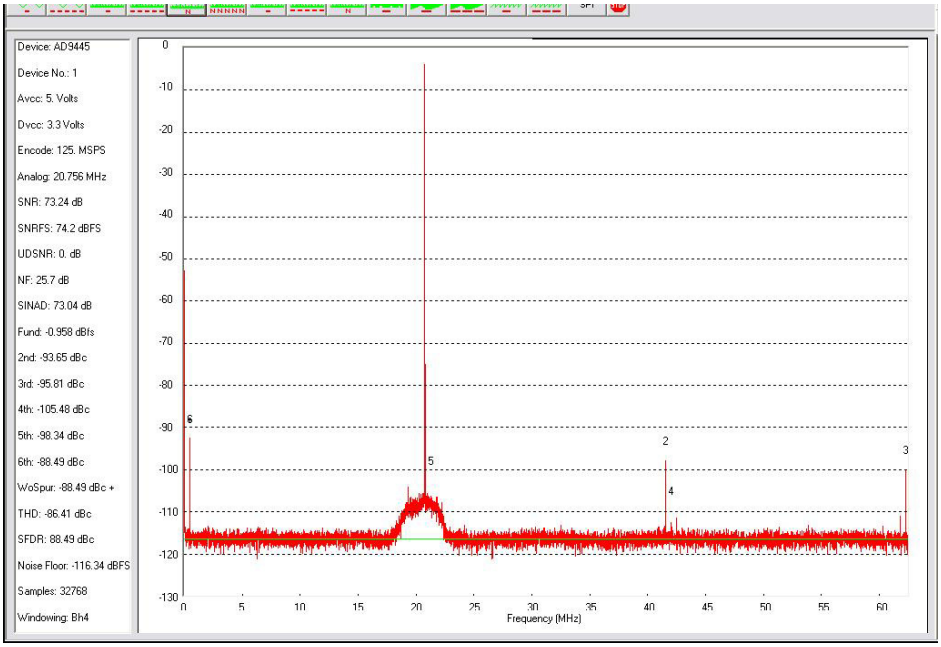
AD8000 Positive PSRR Test Circuit



This figure shows a test circuit with which to measure PSRR. In this instance, we are measuring the positive supply rejection. Note that the negative rail is fully decoupled. Also note that we are operating the input and output into matched lines. The positive rail is driven with the signal generator, V_{IN}, which is terminated in its characteristic impedance (50Ω).

The negative rail test circuit is similar. The positive rail is decoupled, and the negative rail is driven with the signal generator.

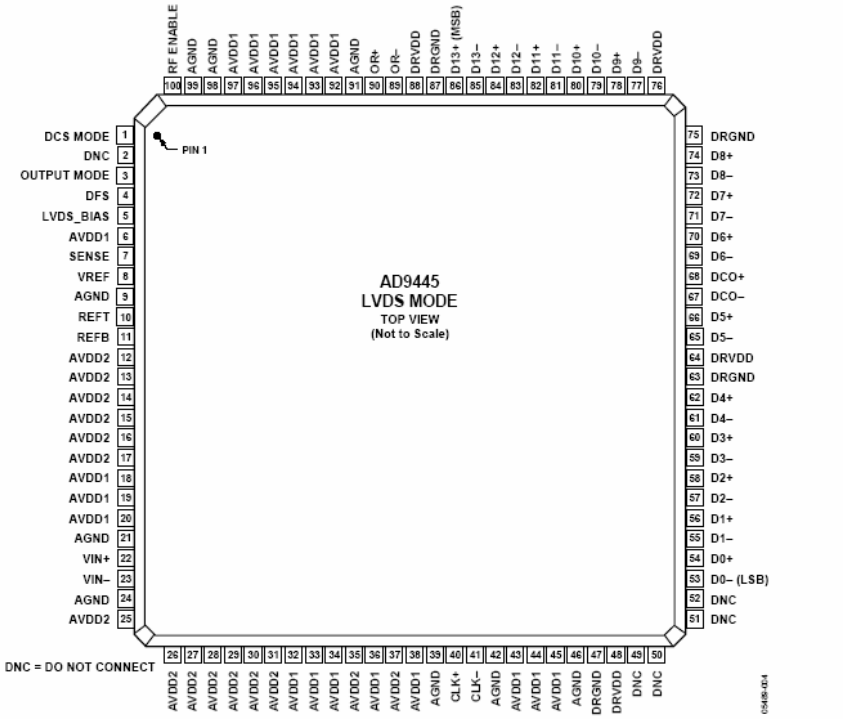
SNR Plot for the AD9445 Evaluation Board with Proper Decoupling



We will now examine the effect of proper and improper decoupling on a high performance data converter, the AD9445 14-bit, 105/125MSPS ADC.

While a converter will typically not have a PSRR specification, proper decoupling is still very important. Here is the FFT output of a properly designed circuit. In this case, we are using the evaluation board for the AD9445. Note the clean spectrum.

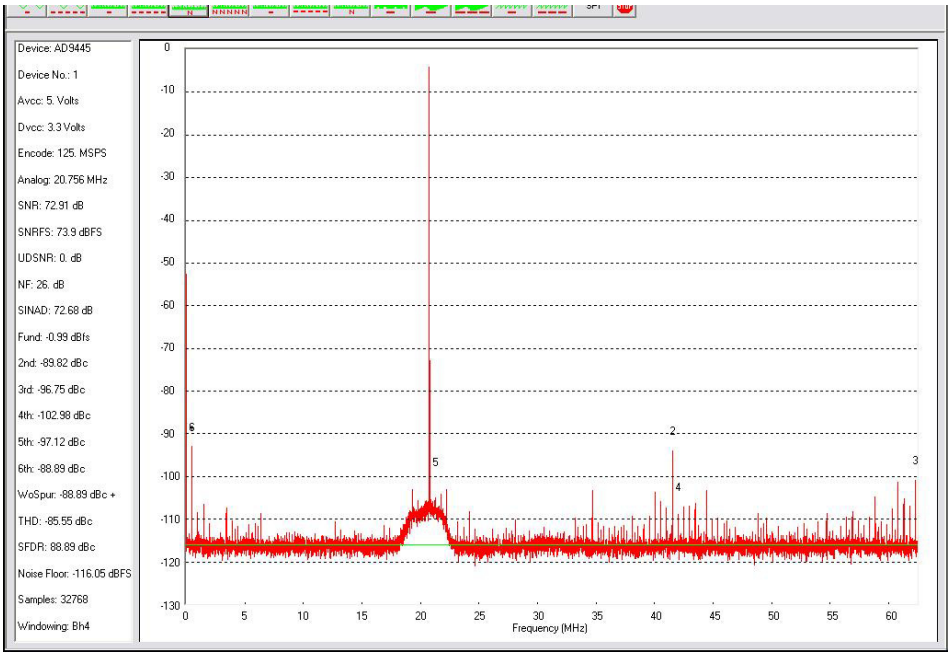
AD9445 Pinout Diagram



This is the pinout of the AD9445. Note that there are multiple power and ground pins. This is done to lower the impedance of the power supply (pins in parallel). There are 33 analog power pins. 18 pins are connected to AVDD1 (which is +3.3V ± 5 %) and 15 pins are connected to AVDD2 (which is +5V ± 5%). There are four DVDD (which is +5V ± 5 %) pins.

On the evaluation board used in this experiment, each pin has a decoupling cap. In addition, there are several 10µF electrolytic capacitors as well.

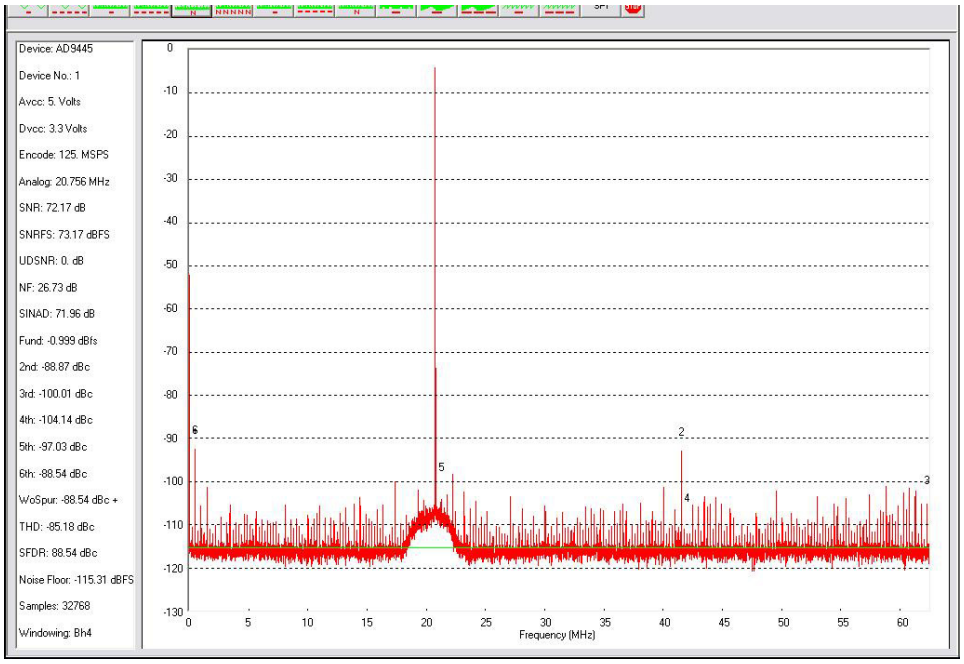
SNR Plot for an AD9445 Evaluation Board with Caps Removed from the Analog Supply



Here is the spectrum with the decoupling caps removed from the analog supply. Note the increase in high frequency spurious signals, as well as some intermodulation products (lower frequency components). The SNR of the signal has obviously degenerated.

The only difference between this figure and the last is removal of the decoupling capacitors. Again we used the AD9445 evaluation board.

SNR Plot for an AD9445 Evaluation Board with Caps Removed from the Digital Supply



Here is the result of removing the decoupling caps from the digital supply. Again note the increase in spurs. Also note the frequency distribution of the spurs. Not only do these spurs occur at high frequencies, but across the spectrum.

This experiment was run with the LVDS version of the converter. We can assume that the CMOS version would be worse because LVDS is less noisy than saturating CMOS logic.

More information on PC board design techniques can be found in the following two references:

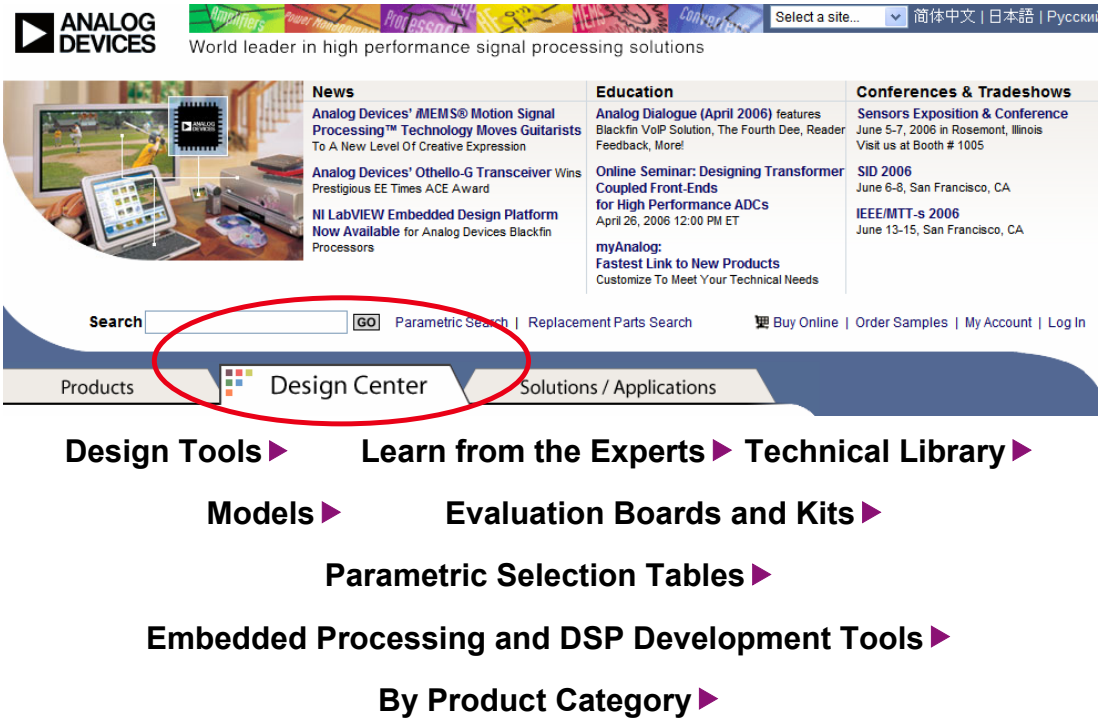
Walt Kester, *Analog-Digital Conversion*, Analog Devices, 2004, ISBN: 0916550273 Chapter 9. Also available as *Data Conversion Handbook*, Elsevier-Newnes, 2005, ISBN: 0750678410, Chapter 9.

Walt Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN: 0-916550-26-5, Chapter 7. Also available as *Op Amp Applications Handbook*, Elsevier-Newnes, 2004, ISBN: 0-7506-7844-5, Chapter 7.

Design Tools

www.analog.com/designcenter

Analog Devices' Online Design Center



Design Tools ▶ **Learn from the Experts ▶** **Technical Library ▶**

Models ▶ **Evaluation Boards and Kits ▶**

Parametric Selection Tables ▶

Embedded Processing and DSP Development Tools ▶

By Product Category ▶

The Design Center tab of the Analog Device Home page is where the design tools reside.

Design Tools Overview

- **ADC Simulation: ADIsimADC**
- **DDS Simulation: ADIsimDDS**
- **PLL Simulation and Design: ADIsimPLL**
- **Clock Circuit Simulation: ADIsimCLK**
- **Amplifier Evaluation Tool: ADIsimOpAmp**
- **Design Assistants:**
  - **Analog Active Filter Design Assistant**
  - **ADC Aliasing Suppression**
  - **DAC Harmonic and Image Locator**
  - **Error Budget Calculation**
  - **Differential Amplifier Gain and Level Calculator**
  - **Analog Bridge Design Assistant**
  - **Analog Photodiode Preamp Design Assistant**
  - **Voltage Reference Wizard**
- **Register Configuration Assistants**
  - **Sigma-Delta ADCs, TxDACs, DDS, etc.**
- **Useful Calculators**
  - **SNR/THD/SINAD/ENOB, dBm/dBV/dBu, Die Temperature, etc.**

This is a partial list of the design tools available from Analog Devices.

More tools are being added all the time.

We have discussed the ADIsimADC, ADIsimDAC, ADIsimPLL and ADIsimCLK programs previously in this book.

ADIsimOpAmp

- **An On-Line tool to help with the selection, evaluation and troubleshooting of voltage feedback operational amplifiers (Op-Amps). Allows for two modes of Evaluation:**
  - **APET Mode Uses National Instruments LabVIEW® along with typical parametric data to mathematically model the general behavior of a selected amplifier. It allows a user to choose an amplifier, quickly configure a circuit, apply a signal, and evaluate its general performance.**
  - **SPICE Mode Uses the MultiSIM9® SPICE simulation engine allowing the user to perform additional testing in the SPICE environment.**
- **The tool is useful for quickly selecting and checking an amplifier's parametric performance such as Gain Bandwidth, Slew Rate, Input/Output Range, Differential Voltages, Gain Error, Load Current, Possible Stability Issues and dc Errors. The APET mode is limited to first-order approximations and additional evaluation should be performed using SPICE simulation and hardware testing.**

The ADIsimOpAmp is an on-line aid to help engineers find and evaluate an amplifier for their application. It can quickly search through hundreds of amplifiers to find the right one for the application. ADIsimOpAmp can be used in either the Amplifier Parametric Evaluation mode, which uses the National Instrument's LabVIEW environment, or the SPICE simulation mode.

The LabVIEW environment uses a mathematical model to evaluate the circuit. The spice mode uses a more traditional spice simulation engine.

How ADIsimOpAmp Is Used

- **Select the Circuit**
- **Enter the Circuit Component Values**
- **Select and Enter the Input Signal Parameters**
- **Select the Amplifier to be Evaluated**
  - **Parametric Search**
  - **Amplifier Wizard**
  - **Suggest Amplifier (Reverse Search-See Below)**
- **Analyze the Amplifier's Response**
  - **Run Model**
  - **View Results**
- **Suggest Amplifier uses the entered circuit requirements to perform parametric calculations on all amplifiers located in the data base. Once the calculations are complete a list of parts from best to least is generated. If an amplifier that meets all requirements can't be found, the search will suggest components that are close.**

Choose an Amplifier to be evaluated from the pull down, labelled "Select Amplifier," located at the top of the tool. Additional amplifiers can be added to the list by using one of the options below:

Parametric Search - If you know the required op-amp parameters the Parametric Search Engine can be used to find and suggest amplifiers for evaluation. To perform a search enter the values for the desired parameters in the input blocks provided and press search. The tool will display results that best meet the input criteria. Additional search parameters can be added by checking the desired box under "Add Searchable Parameters." If desired, amplifiers can be selected for further evaluation by selecting the "Add Part(s) to Amplifier Parametric Evaluation Tool," selecting the checkbox next to the desired part(s), then clicking the "Add to Tool" button at the bottom of the page.

Amplifier Wizard - If you're not sure of how to select an amplifier, let the Amplifier Wizard help suggest one. The Amplifier Selection Wizard will lead you through a few generic questions and based on the response information will search for and sugest amplifiers for further evaluation.

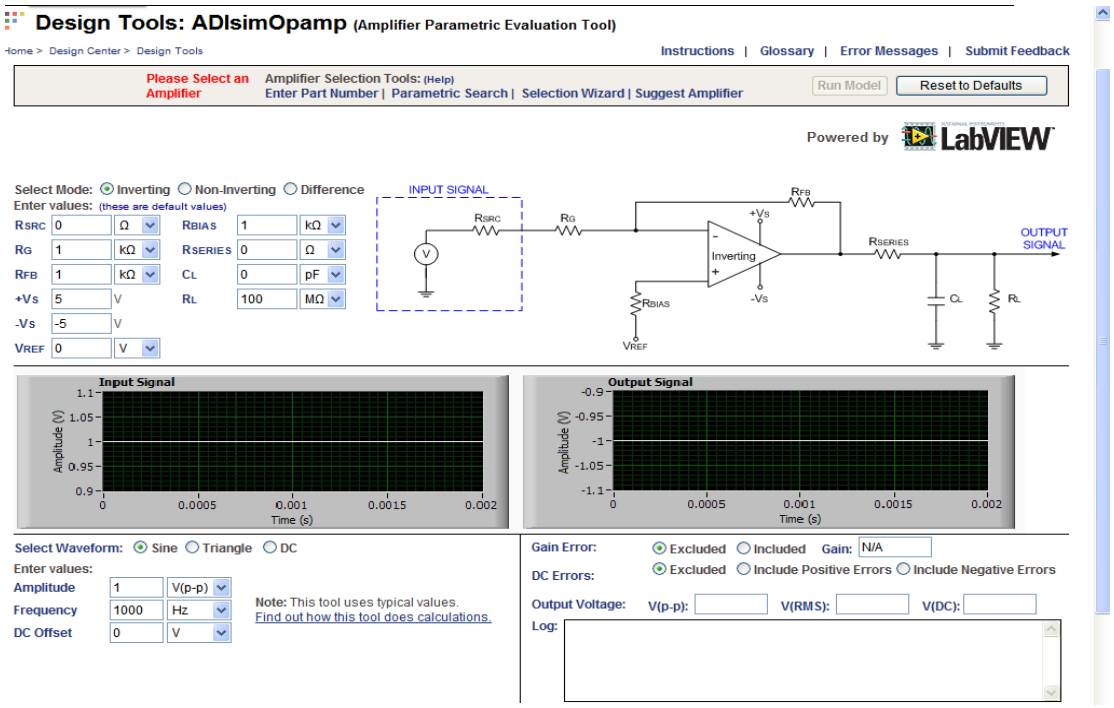
Reverse Search - Data derived from the configured circuit can be used to automatically load the parametric search engine. This allows the parametric search to look for an amplifier that will work in the circuit. If an amplifier that meets all requirements can't be found, the search will suggest components that are close.

Select the Circuit

Choose the a circuit from the pull down, labelled "Select Mode," located at the top of the tool. The selections are Inverting amp, Non-Inverting amp or Difference amp configurations.

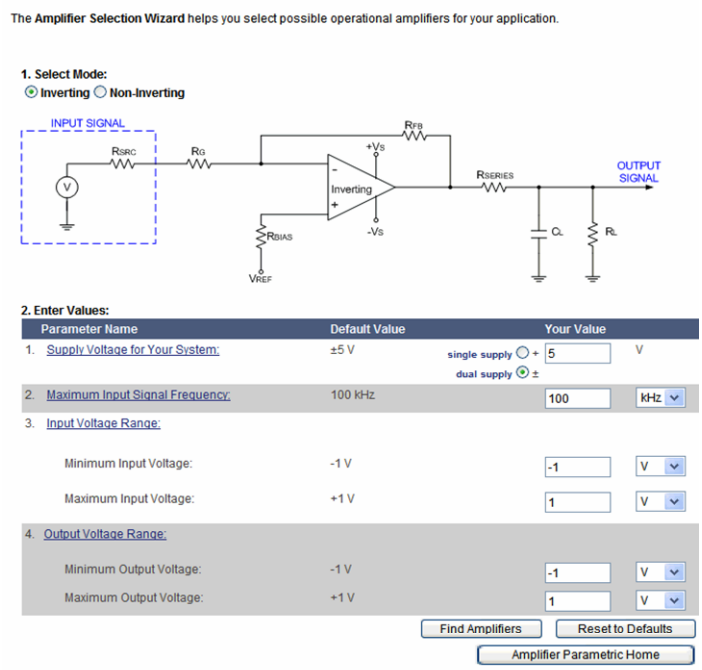
Configure the Circuit, Set Signal Parameters, Run the Model, View Results

ADIsimOpAmp (Opening Screen)



When first opened the ADIsimOpAmp will appear as shown above. This screen allows the user to configure a circuit, enter component values, and select the input signal type (square wave or sine wave), frequency, and amplitude. It also offers the option of either entering a desired part number or using the selection features to help find a part that will be suitable for the circuit.

ADIsimOpAmp: Selection Wizard



If assistance is needed with determining a circuit configuration or level shifting, the Selection Wizard offers the user additional help. By selecting the desired function and entering values in the blocks provided the Wizard can suggest a circuit and amplifiers for the application.

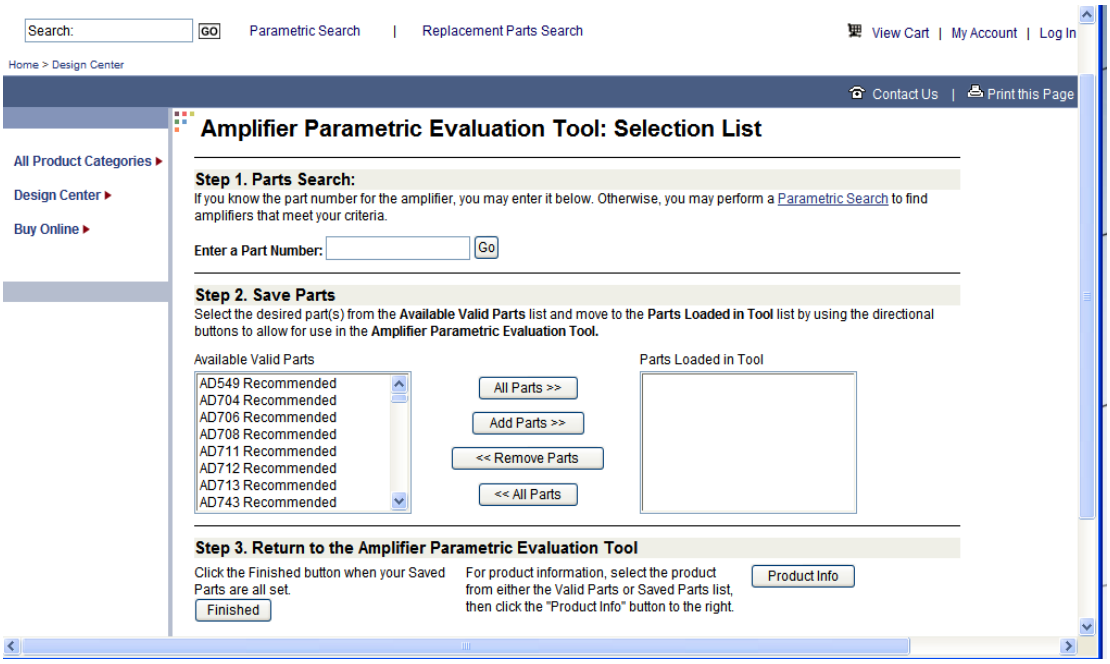
This shows the opening screen of the "Selection Wizard" portion of the Amplifier Evaluation tool.

First select the mode of operation: inverting or non-inverting.

Then select the power supply values, the maximum input frequency, minimum and maximum input voltage range, and minimum and maximum output voltage range.

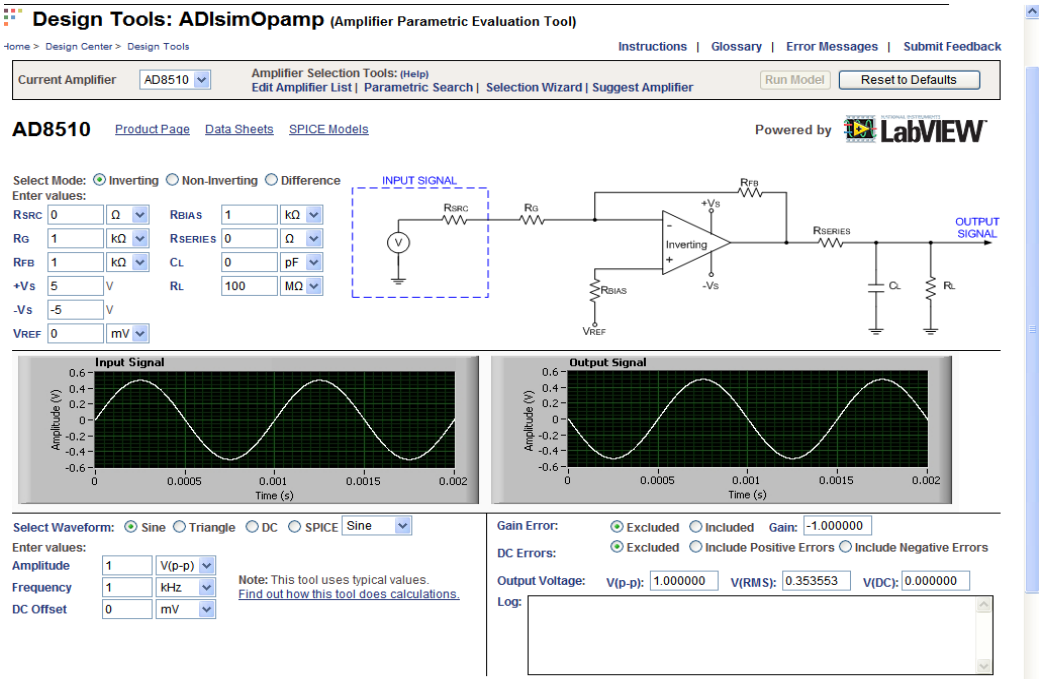
Next, click on the button "Find Amplifiers."

ADIsimOpAmp: Selection List



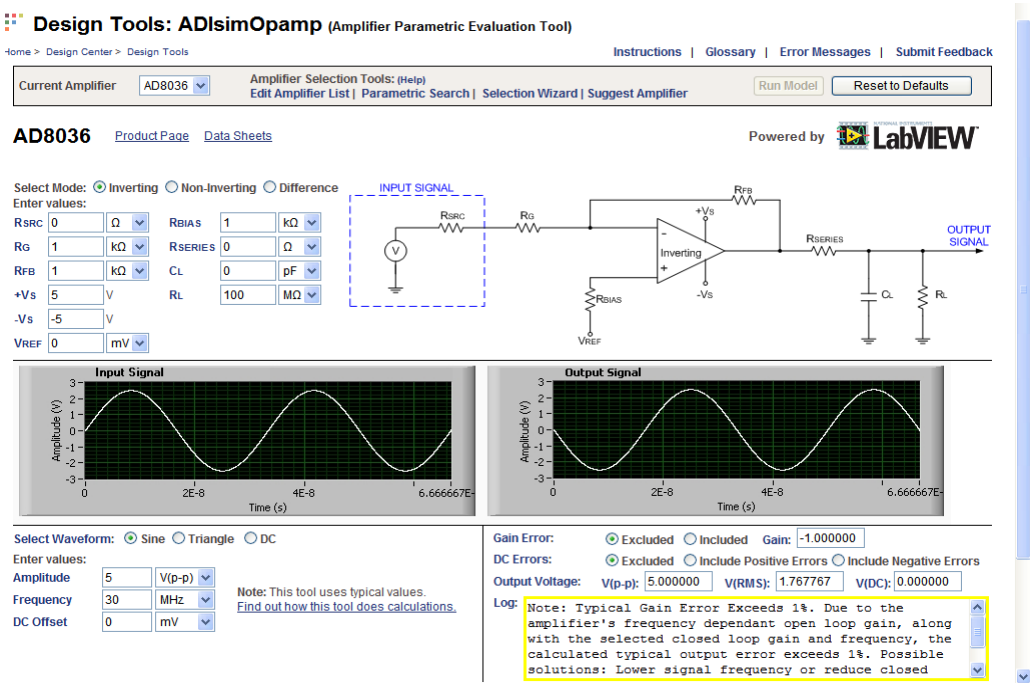
Shown above are the results of a Suggest Amplifier (reverse search) List. Note that the part numbers listed are "Recommended." Recommended means that the device will work in that application as defined earlier. Desired parts can be selected from the list and loaded into the tool for evaluation.

ADIsimOpAmp Screen – Normal Results



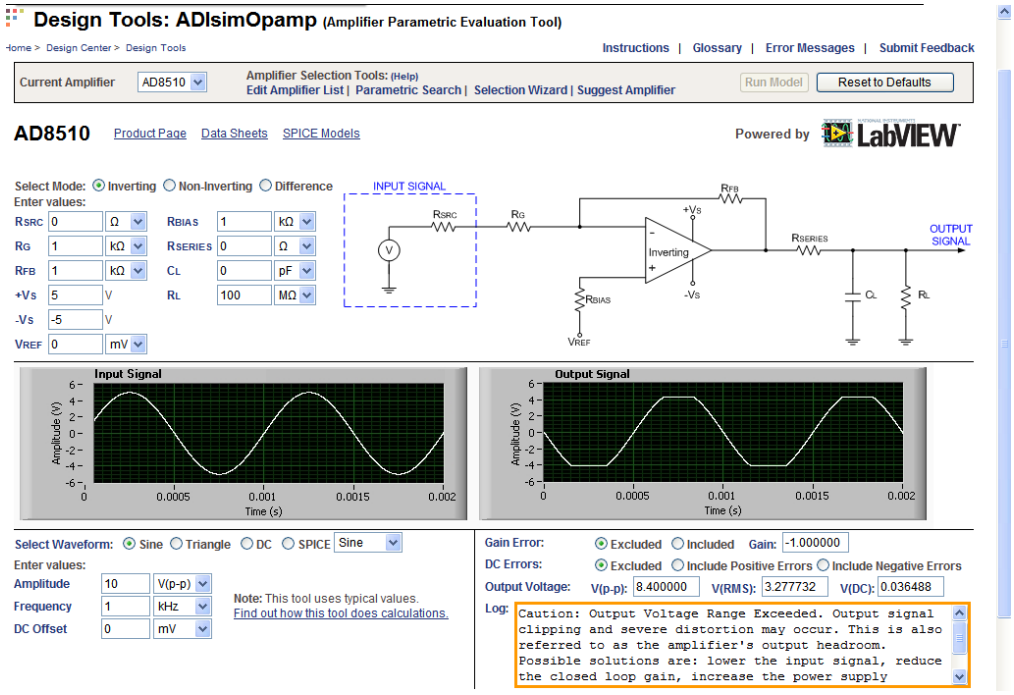
This figure shows the result of a circuit simulation using the AD8510, in the APET mode. No failures were detected. At this point the user could then perform further evaluation of the AD8510 in SPICE mode by clicking the SPICE radio button and then selecting a Sine or Square wave for the input signal.

ADIsimOpAmp Screen - Warning



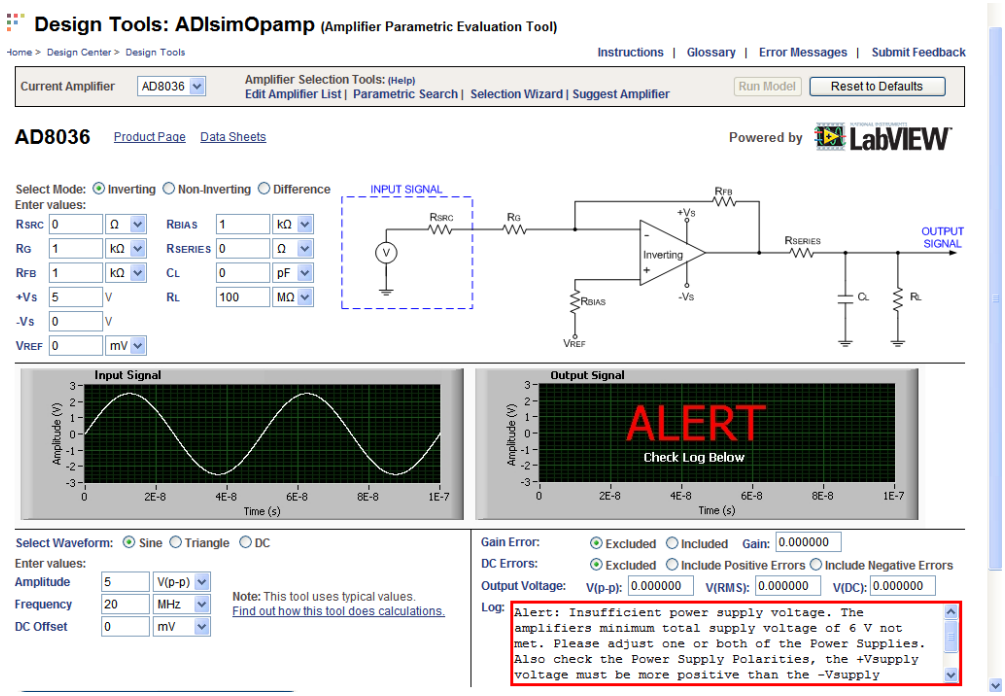
In this slide the amplifier gain error exceeds a set limit and so the tool returns a warning. This warning is in the log. Note that the log box is framed in yellow to emphasize the warning. It is then left to the designer to determine if this warning is a problem that needs correcting. Note that several corrective actions are suggested.

ADIsimOpAmp Screen – Warning (Cont.)



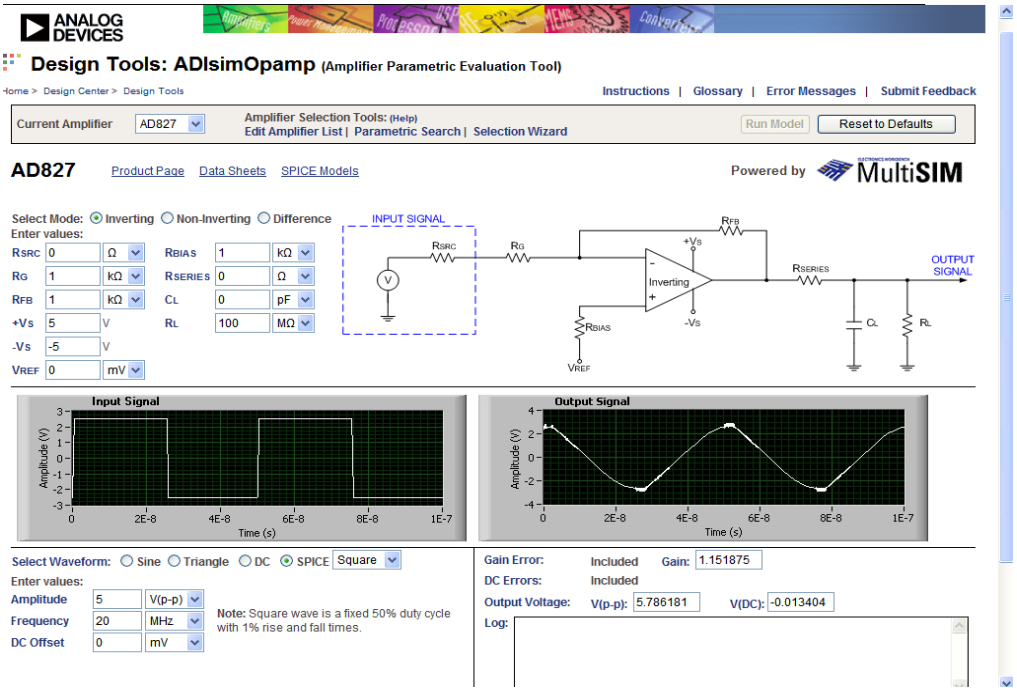
This slide demonstrates another level of warning. Note that the log box in this case is framed in orange. The issue here is that the amplifier is clipping. Again, note that several corrective actions are suggested.

ADIsimOpAmp Screen – Error

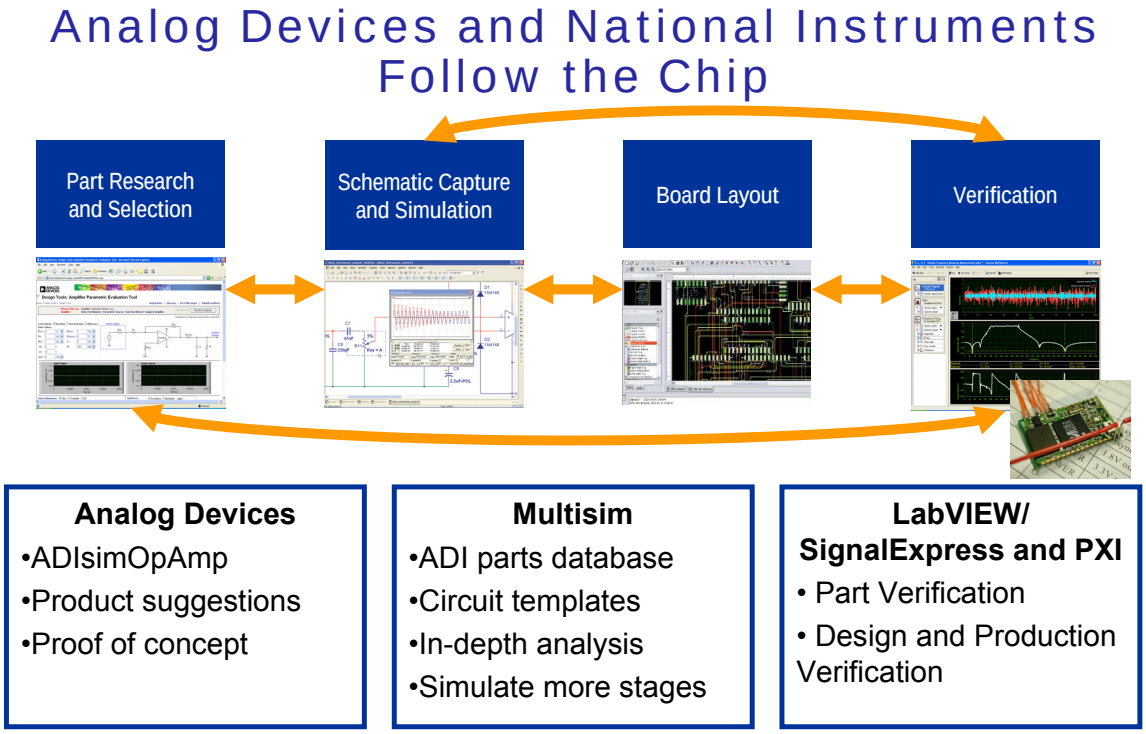


A more serious error is detected here. The minimum power supply requirements have not been met. Note that the log box is framed in red this time. Once more, corrective actions are suggested.

ADIsimOpAmp Screen – Spice Mode



In this case the spice mode has been selected. In the spice mode, some of the error checking is not used, since this is a function of the LabVIEW environment. In the spice mode the only error that will be reported is if the circuit fails to converge. The output is whatever it would be. In this case the amplifier is slew limited. The amplifier is a 50MHz part and the input is a 20MHz square wave. Being a square wave, the harmonic content is largely outside the range of the op amp. Also the amplitude of the input is in excess of the slew rate of the amplifier.



Any design has four major stages

Part Research and Selection

Schematic Capture and sometime simulation

Board Layout and

Verification

Traditionally many of these stages were done in isolation with little automation or connection between the tools used for each stage – now ADI and National Instruments are working to integrate these steps.

Tools like the ADIsimOpamp help you find and select parts far better than just data sheets.

Multisim supports the ADIsimOpamp and gives you an easy transition to working in Multisim by providing circuit templates that complement the ADI tool.

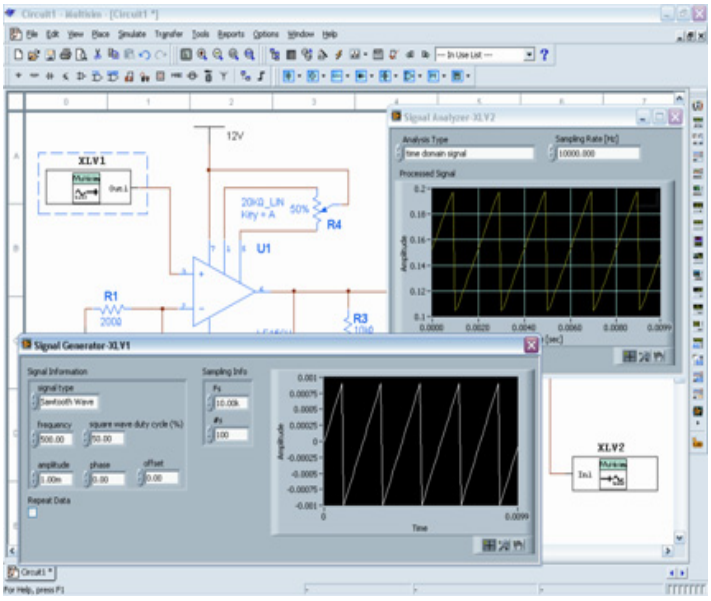
You can also find a complete database of all available ADI op amp models for Multisim. Information on how to obtain these models for the Freeware edition of Multisim are included in the CD package.

Multisim lets you evaluate your components in more detail as well as simulate your complete designs.

You can also use LabVIEW and SignalExpress in conjunction with test equipment to verify component or design operation. Once you set up a project, you can save and reuse it; this helps to automate your evaluation process.

Multisim Product Overview

- **Integrated schematic capture and simulation**
- **Interactive simulation**
- **Advanced analyses**
- **Useful for SPICE and VHDL* simulation and co-simulation**
- **Tight integration with real-world measurements**
- **Analog Devices circuit templates**



Multisim provides you with an integrated schematic capture and simulation environment. You can simulate right from the schematic environment. You can also immediately run simulations without going through complicated set-up procedures.

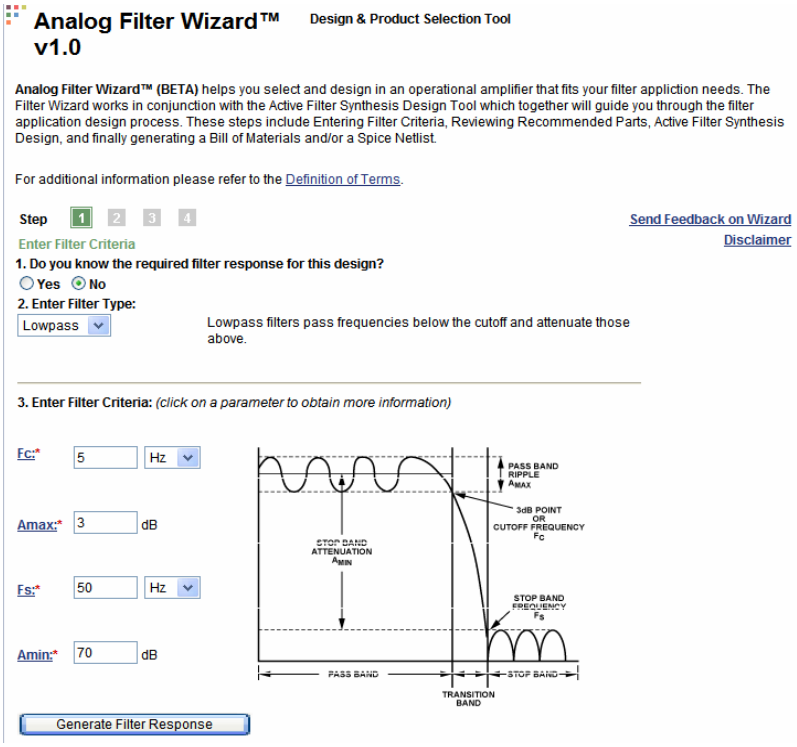
You can make use of Virtual Instruments, like oscilloscopes and function generators, to simulate your designs. These instruments connect to your schematic like real instruments connect to test circuits. You can even create your own custom sources and instruments with NI LabVIEW and use them in Multisim.

Virtual instruments, together with interactive components like potentiometers, enable an interactive simulation environment that closely matches the lab experience. Available analyses range from ac and dc sweeps to noise analysis and worst case analysis. If you have data acquisition devices or want to import scope data, you can make use of a wide range a data import functions. You can also export your results to NI SignalExpress and compare your simulations to measurements from your prototypes.

To help you get started, you can use some of the circuit templates that complement the ADIsimOpAmp tool.

You will receive a freeware edition of Electronics Workbench software. This edition limits your design size to 50 components and 2-layer boards. The simulation capabilities will run for 45 days after you run Multisim for the first time.

Active Filter Design Using Filter Wizard

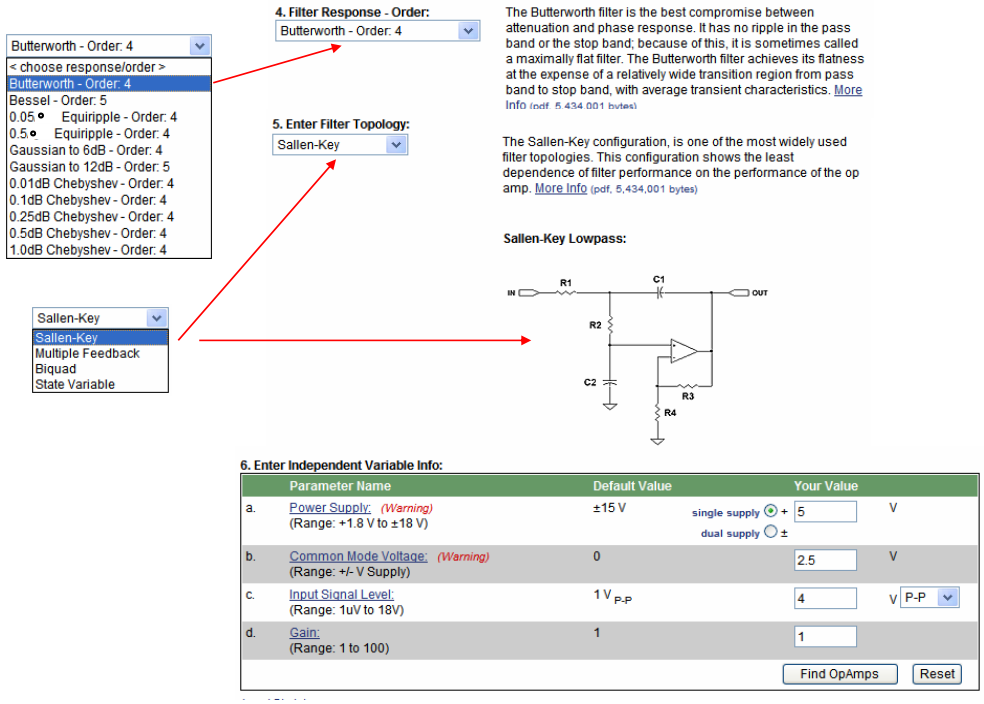


The Filter Design Wizard is designed to assist in the design and part selection for active filters.

There are two modes of operation for the Filter Wizard. The first is the “expert” mode. In this mode the designer knows the type of filter to be designed. That is he knows that he needs, for instance, a fifth-order 0.5dB Chebyshev.

Otherwise, you must describe the response of the filter in terms of the passband ripple, corner frequency, stopband frequency, and minimum attenuation. Then you will be asked to choose between the various filter types.

Selecting the Filter Response, Topology, Power Supply, CM Voltage, and Gain



The wizard will then come back with several possible filters that will satisfy the requirements in a pull down menu. Beside the filter response pull down is a discussion that gives a brief description of the tradeoffs of each of the possible choices. There is also a link to the filter section which will give a much more detailed description of each filter type.

Designing a filter is a two step process. The first is to decide what it is you want to build. This means to determine the response characteristics and order of the filter, which is what we have just done. The next step is to determine how to build it. What this means is to determine the circuit topology. Again, several choices are available in a pull down box. Next to the pull down, again, is a brief description of the circuit, with a link to a more detailed description. A schematic is also included.

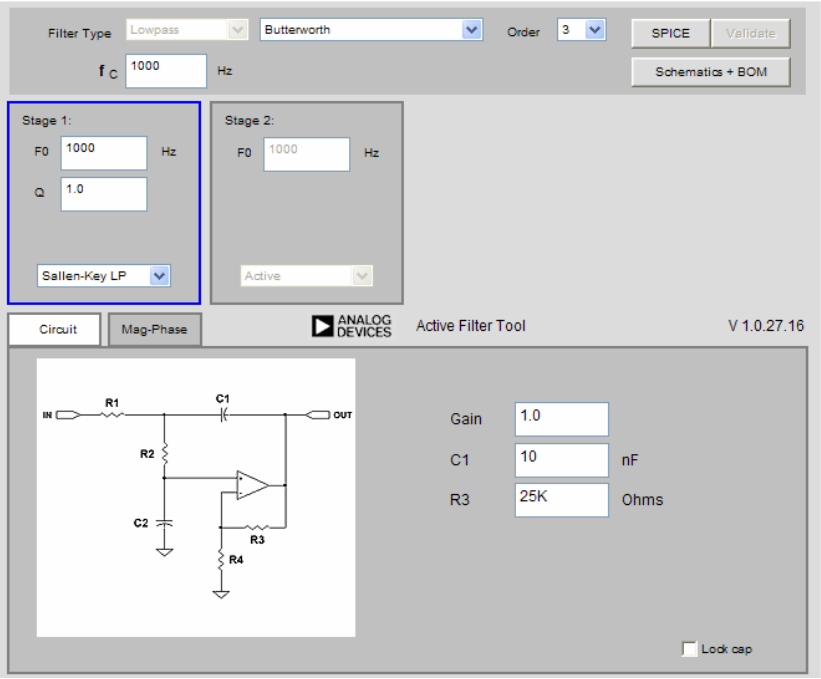
The Wizard then suggests op amps that best fit the application performance values you entered. “Best-fit” is determined by the results of a parametric search of Analog Devices' product database. The order of parametric preference is: input bias current, voltage noise density, current noise density, input offset voltage, open-loop gain, and power supply voltage.

Each product number is a link to the product page. The product page provides links to the product description, data sheet, package/price, samples, and purchasing information.

Once the selection of circuit topology has been made, the designer enters information on a few more variables, such as supply voltages and signal levels, and the wizard then returns a selection of op amps that will work in the circuit.

Since the open loop response of an op amp is, in itself, a low pass filter, the op amps are chosen so that the open loop gain is large enough that the op amp response will not materially affect the response of the filter.

Filter Wizard Stage Design (top)

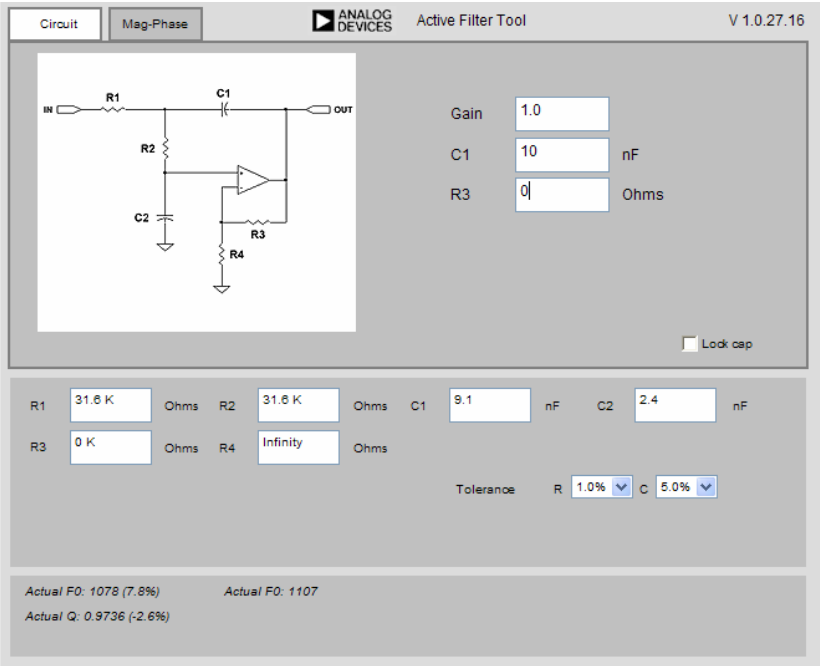


Once the op amp is chosen from the list provided, the designer enters the third page. Here, the component values for the filter are determined.

Multipole filters are made up of cascaded first-order and second-order sections. While it is possible to design a third-order section with only one active element, the circuit value sensitivities increase, so we have limited the choices here to first- and second-order sections.

The pertinent parameters (Fo and Q) for each of the filter section are loaded into the wizard. Since all of the component values are ratiometric, one value has to be chosen to set the rest of the variables. We typically choose a capacitor first, since there are fewer choices of values for capacitors than there are for resistors.

Filter Wizard Stage Design (bottom)

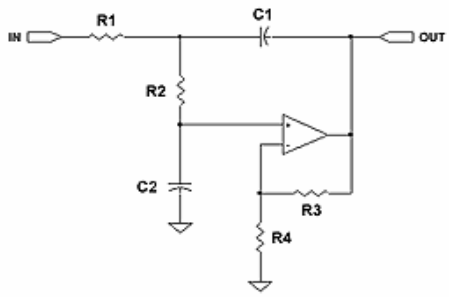


The values returned for the component values are exact values. There is the option to choose standard values (0.5% to 2% for resistors and 2% to 5% for capacitors). The designer has the ability to overwrite these values as well. Since changing the resistor and capacitor values will cause a small change in the Fo and Q of the filter, the wizard will recalculate these values and return the error introduced by going to standard values.

Once this process is completed for each section of the filter, the design is finished.

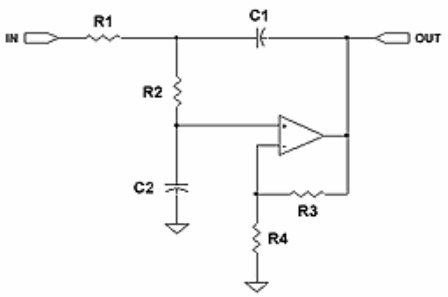
Filter Design with Component List

Stage 1: AD820 Sallen-Key LP



AD820
R1 3.445e4
C1 1.000e-6
R2 3.445e4
C2 8.535e-7
R3 2.500e4
R4 Inf.

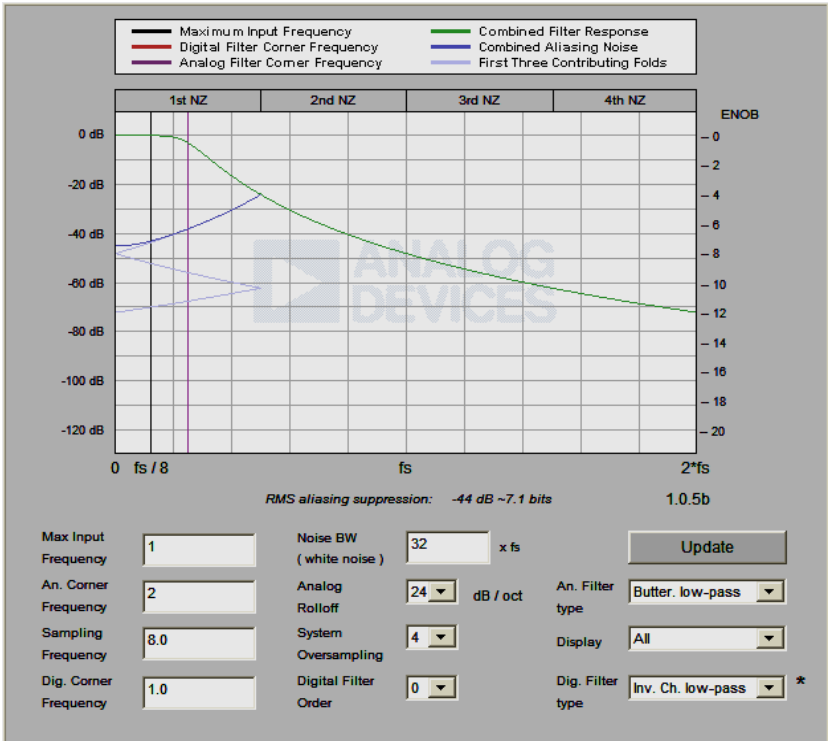
Stage 2: AD820 Sallen-Key LP



AD820
R1 8.321e4
C1 1.000e-6
R2 8.321e4
C2 1.463e-7
R3 2.500e4
R4 Inf.

The possible outputs of the wizard include magnitude and phase plots, a schematic page with component values list, and a Spice deck. With the Spice deck, further characterization of the filter is possible. This includes Monte-Carlo analysis of the component values and possibly including the op amp response with the filter response.

ADC Anti-Aliasing Suppression Assistant

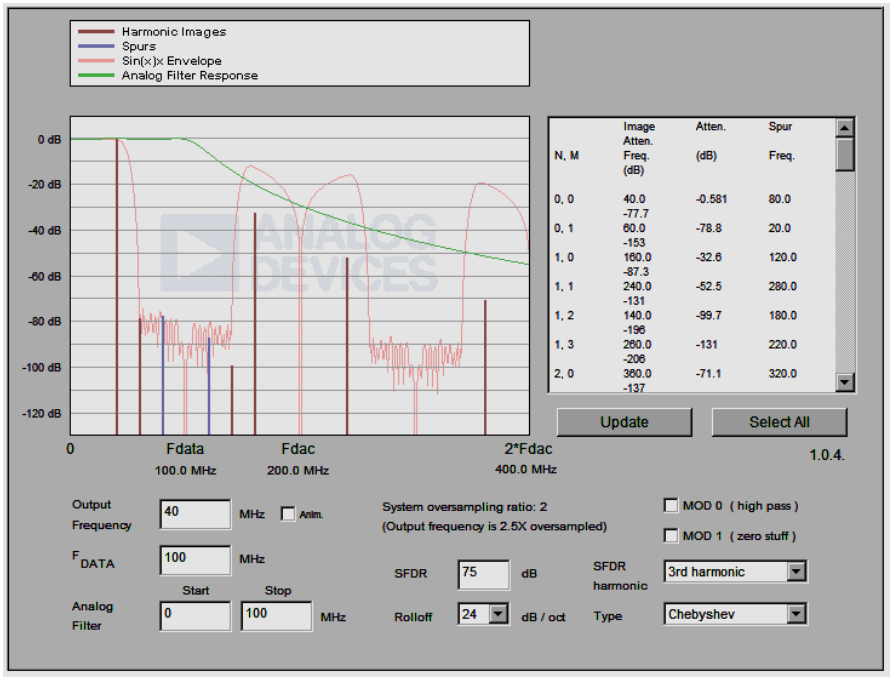


A design assistant is available to help in designing the anti-aliasing filter of an ADC system. This applet illustrates aliasing and its suppression through filtering and oversampling in a classic (non-sigma-delta) A/D converter. An ideal ADC is assumed – distortion free, unlimited bandwidth, etc. – in order to focus solely on aliasing effects. The input signal is also assumed to be noise free, but the most practical use of this applet is to find a combination of filtering and oversampling that pushes the aliased terms below the noise floor of the input, or the overall system .

The finite rolloff of practical analog filters means there are always some undersampled high frequency components that fold into the passband, or "Nyquist Zone" (NZ), and appear in the sampled signal as noise. For the simple case of an input composed of bandlimited white noise, this applet gives an estimate of how much out-of-band signal will be folded into the baseband (1st NZ). In many real-world situations, the out-of-band signal is of lesser amplitude and so this estimate is too conservative; in other cases it might not be conservative enough – it depends on the out-of-band signal level. The bandwidth limit for the input white noise signal is a multiple of the sampling frequency. By default, that multiple is 32×; the maximum is 256×.

Aliasing suppression in oversampled systems is achieved through a combination of analog and digital filtering, but digital filtering cannot replace a high-quality analog filter, because it cannot remove aliasing noise after it's been folded into the passband by the sampling process. Instead, oversampling must be used to put enough octaves and attenuation between the Nyquist frequency and the highest passband frequency of interest. Digital filtering can then be used on the sampled signal to eliminate frequencies between passband and Nyquist. For simplicity, the additional aliasing noise that results from downsampling the sampled signal is not shown.

Harmonic Image DAC Design Tool



The DAC image applet shows the harmonic images and spurs for single frequency output from an DAC, an AD9772 in this example. The model of the AD9772 is simplified and idealized – only SFDR is modeled, and it is assumed frequency-independent. The response characteristics of the internal digital filter have been approximated. See the data sheet for actual performance data.

For an ordinary DAC, images are located at N·FDAC ± FOUT. The AD9772 contains an integral interpolator which doubles the input data rate creating an image of the output frequency mirrored about FDATA/2. An interpolation filter suppresses the upper image in low-pass mode (MOD0=0), or suppresses the fundamental when in high-pass mode (MOD0=1). Both the filtered and unfiltered images then create further images and spurs at the DAC data rate, according to the N·FDAC ± FOUT rule.

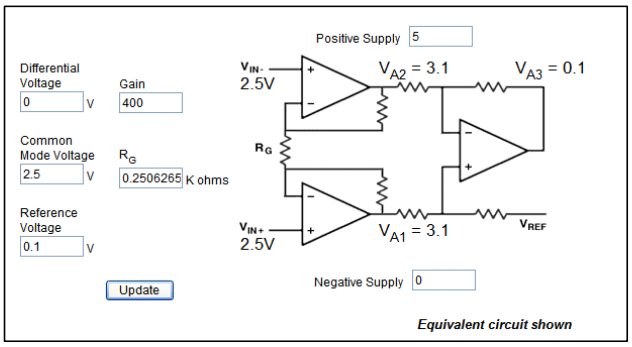
The AD9772 also has a "zero-stuffing" mode (MOD1=1) which allows the data stream to be doubled a second time by inserting zeroes between each sample. Zero-stuffing doubles again the number of images per FDAC harmonic, but FDAC is twice what it would be without zero-stuffing and the mathematics work so that the location of the images is the same as without zero-stuffing – only the amplitudes change. These new images are not filtered internally, so the upper image can be used for direct IF synthesis. MOD0 and MOD1 are often used together for this purpose.

Spurious 2nd or 3rd harmonics of each image are assumed to result from D/A nonlinearities and so are folded within the first Nyquist Zone (NZ) of FDAC. These spurs then have their own harmonic images that roll off as sin(x)/x (where x = π·FSPUR / FDAC). The magnitude response of the AD9772, combining its internal interpolation with the sin(x)/x envelope, is shown.

To show external selection/suppression of desired/undesired images and spurs, the applet can apply a simulated post-DAC analog filter.

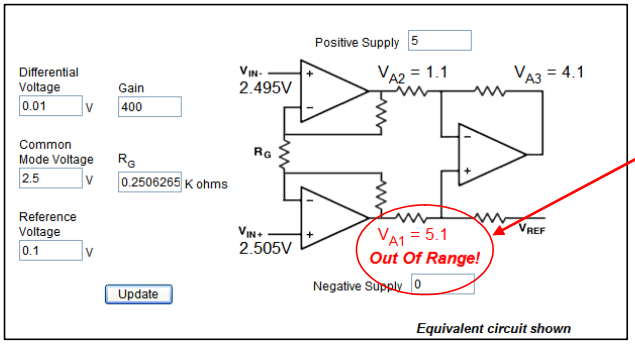
In Amp Gain and Level Calculator—AD623

(A) Differential Input Voltage = 0V



All Nodes Within Allowable Range

(B) Differential Input Voltage = +10mV



Out of Range Error at Node V_{A1}

The Instrumentation Amplifier Gain Calculator calculates the gain of an in-amp circuit given the gain-setting resistor or conversely gives the value of the resistor need for a particular gain. It also checks to ensure all node, even those internal, are kept in their operational range.

To use the tool, simply enter data in the fields provided. If an input is out of range an alert will appear (in red, along with an “error” message).

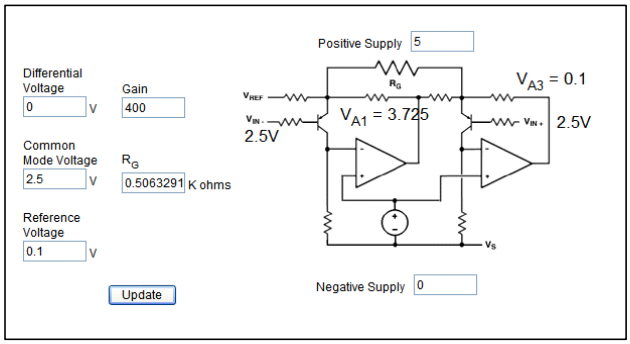
Click "Update" or tab to another field to see node voltages annotate the schematic on the right. Internal node voltages are for the equivalent 3-op amp (or 2-op amp) circuit, assuming a 0.5V level shift. This may not reflect the exact internal implementation, but is instead a simplified schematic.

If the combination of inputs causes internal or external limits to be exceeded, the problem node value will be highlighted in red and an "Out of Range!" message will appear. When this message is present, all node values should be considered invalid. These input conditions could include such things as overranging the output or, especially in single-supply applications, putting an internal node out of range. The fact that the tool will show the conditions of internal nodes is useful, since you cannot probe those nodes directly and may be mislead into believing the circuit is working when, in fact, it is not.

Only one of "Gain" or "RG" can be specified - the other is computed automatically.

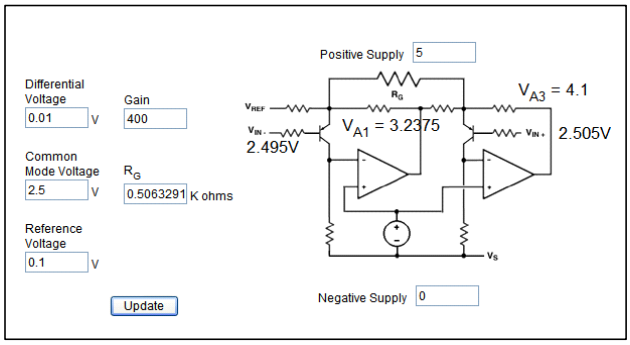
In Amp Gain and Level Calculator—AD627

(A) Differential Input Voltage = 0V



All Nodes Within Allowable Range

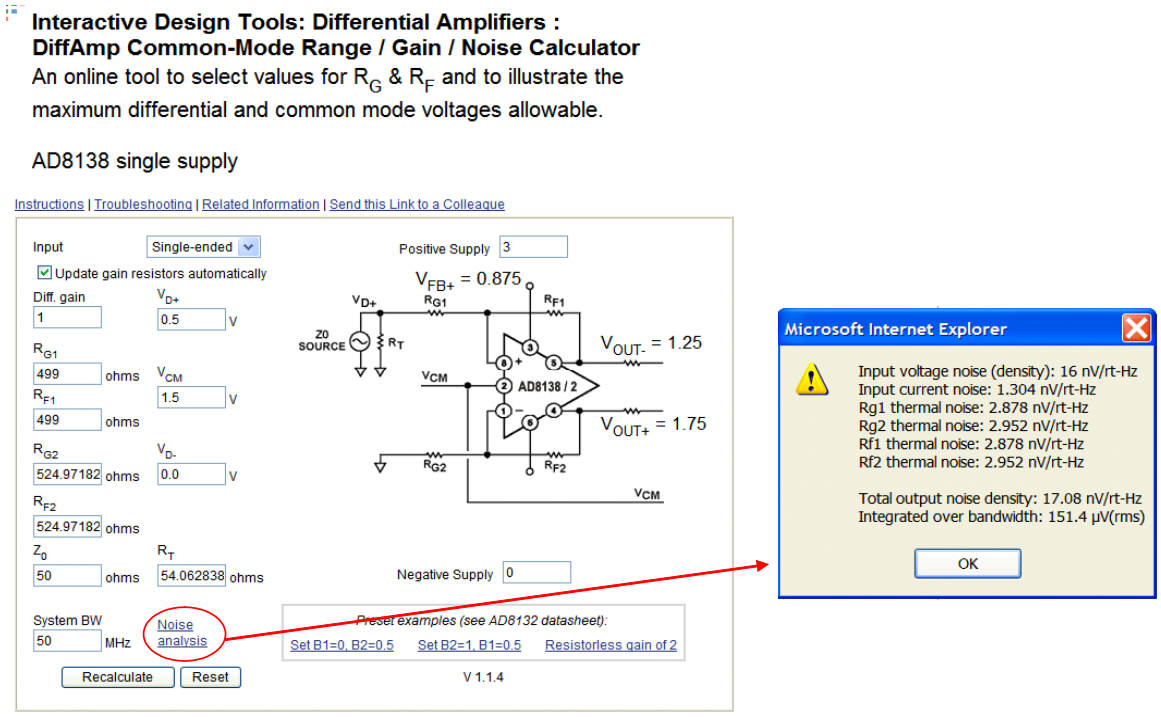
(B) Differential Input Voltage = +10mV



All Nodes Within Allowable Range

The same basic tool exists for the two amplifier configuration instrumentation amps. Special care is needed here to make sure that internal nodes are within their operational range. The tool will detect these conditions and flag them.

Differential Amplifier Interactive Tool



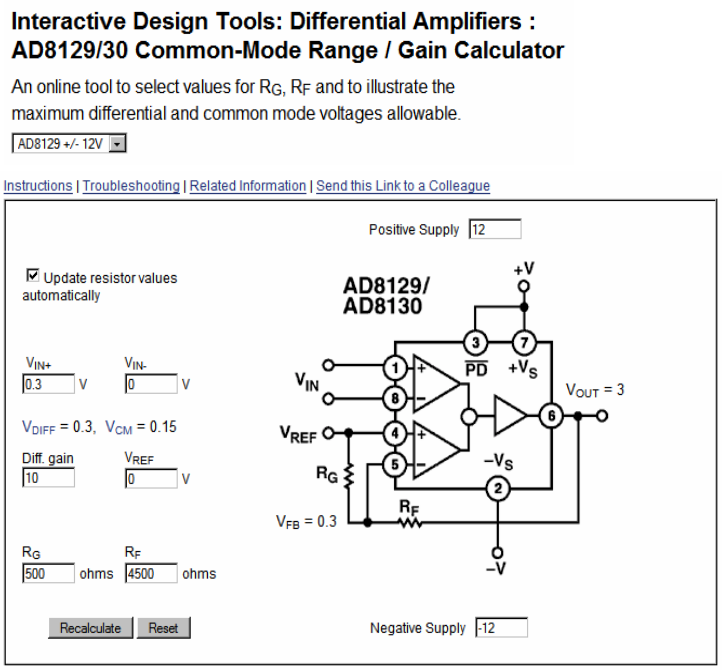
The Differential Amplifier Calculator has two basic modes: manual and automatic. The default is automatic in which it is assumed you want to calculate resistor values (incl. termination) to match a source impedance. In the automatic mode, RF is computed from RG and Gain: changing either of the latter will affect the former. Changing ZO affects all the gain resistors (which should always be a minimum of 10 × ZO), as well as RT. RT is the value for the termination resistor taking into account the impedance of the differential amplifier's gain network and is recalculated when either of RF or RG are changed (changing RT, however, affects nothing). Single-ended termination resistances are calculated assuming VCM = 0. For other fixed voltages, the input impedance is nonlinear.

By unchecking "Update resistor values automatically," the calculator is placed in the manual mode where each resistor can be set independently. Gain and the node voltages are the only thing computed when "Recalculate" is clicked or a new field is entered. For open circuits or "infinite" resistors use a large number instead, such as 1e99. Do not leave any fields blank.

The schematic shows a matched Thevenin source driving a terminated line, however, input voltages are actually set independently for each value of RG. Consequently ZO and RT don't affect the calculation of node voltages. For unterminated calculations set ZO to zero.

Note: For clarity, this calculator shows ideal behavior and does not show the effects of input offset currents and voltages.

Active Feedback Amplifier Common Mode Range/ Gain Calculator



There is a novel amplifier topology called active feedback.

These amplifiers have two sets of fully differential inputs, VX1(1) - VX2(2) and VY1(4)- VY2(5). Internally, the outputs of the two GM stages are summed and drive a buffer output stage.

In this device the overall feedback loop forces the internal currents IX and IY to be equal. These currents are the outputs of the input pin summing amps. This condition forces the differential voltages VX1 - VX2 and VY1 - VY2 to be equal and opposite in polarity. Feedback is taken from the output back to one input differential pair, while the other pair is driven directly by an input differential input signal.

An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so CMR is not dependent on resistor bridges and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100dB at dc.

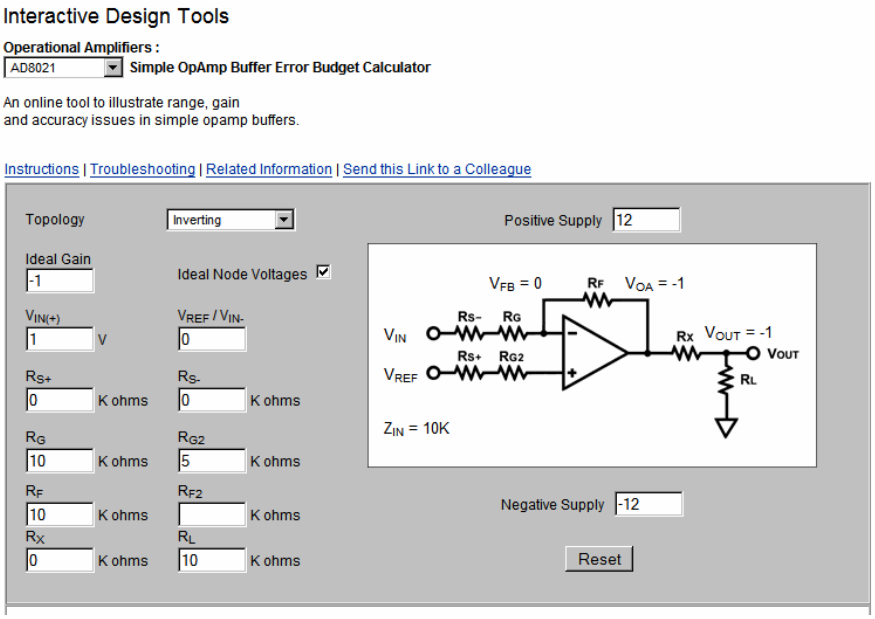
One way to view this topology is as a standard op amp in a non-inverting mode with a pair of differential inputs in place of the op amps standard inverting and non-inverting inputs. The general expression for the stage's gain "G" is like a non-inverting op amp, or:

$$G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1}$$

As should be noted, this expression is identical to the gain of a non-inverting op amp stage, with R2 and R1 in analogous positions.

This tool calculates the common mode and differential mode gain and makes sure all internal nodes are within allowable ranges.

Op Amp Error Budget Calculator -1



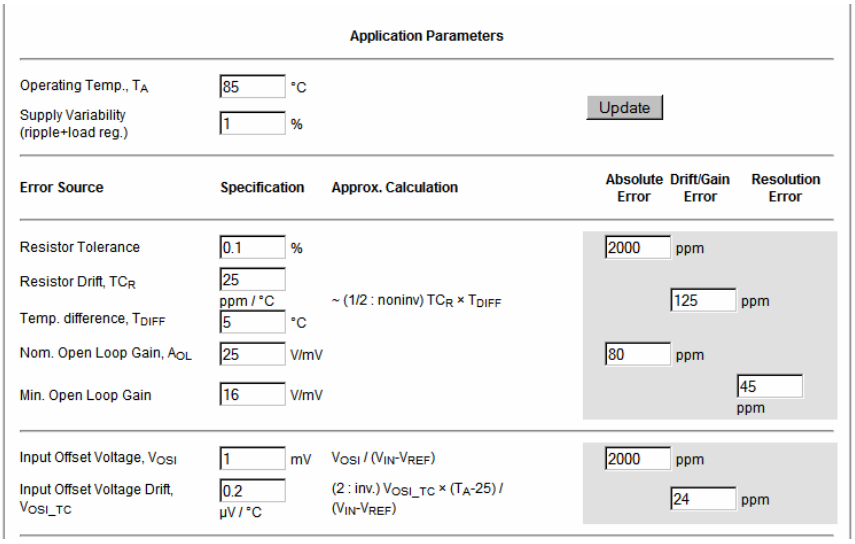
There are a number of sources of potential error in an op amp design. The Error Budget Calculator has two parts: an annotated schematic at top and a table of contributing error sources at bottom. Op amp parametric data is automatically entered in the appropriate fields of the bottom table, and default values for the application parameters have been assigned to the application-specific fields at the top. All input data can be manually overridden, however, output fields (surrounded by light gray) cannot be changed. This is a great time savings from having to enter all the data by hand.

After entering data in a field, hit tab or click "Update" to compute derived values and see node voltages updated on the schematic. If the inputs are out of range an alert will appear. If the combination of inputs causes internal or external output limits to be exceeded, the problem node value will be highlighted in red and an "Out of Range!" message will appear. When this message is present, all node values should be considered invalid. Do not leave fields blank: if you see “NaN” (Not a Number), this means that insufficient data was entered to compute a value.

"Gain" and "RF" are computed automatically from one another, based on the value of "RG." The calculation is ideal and doesn't reflect RS, RX and RL, for example.

Equations listed in the "Calculation" column are approximate and reflect the worst case between the three amplifier configuration choices. Modifications to the equation for particular configuration types are indicated in ( ). For example (1/2 : noninv) means an additional factor of 1/2 should be used to compute this quantity for the noninverting configuration.

Op Amp Error Budget Calculator -2



Application Parameters

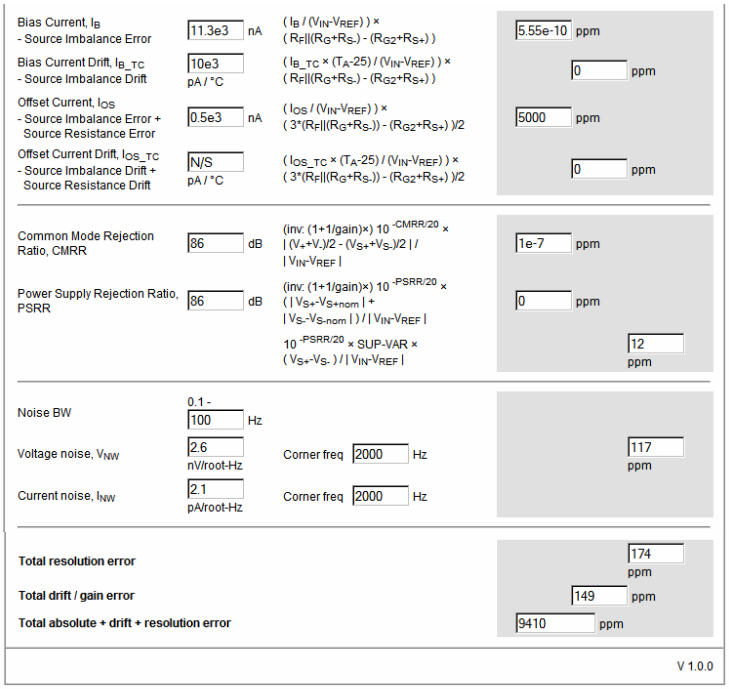
Operating Temp., T_A	85 °C				
Supply Variability (ripple+load reg.)	1 %		Update		

Error Source	Specification	Approx. Calculation	Absolute Error	Drift/Gain Error	Resolution Error
Resistor Tolerance	0.1 %		2000 ppm		
Resistor Drift, TC_R	25 ppm / °C	~ (1/2 : noninv) $TC_R \times T_{DIFF}$		125 ppm	
Temp. difference, T_{DIFF}	5 °C				
Nom. Open Loop Gain, A_{OL}	25 V/mV		80 ppm		
Min. Open Loop Gain	16 V/mV				45 ppm
Input Offset Voltage, V_{OSI}	1 mV	$V_{OSI} / (V_{IN}-V_{REF})$	2000 ppm		
Input Offset Voltage Drift, V_{OSI_TC}	0.2 µV / °C	(2 : inv.) $V_{OSI\_TC} \times (T_A-25) / (V_{IN}-V_{REF})$		24 ppm	

Specs shown are worst-case for the selected part, if available, otherwise typical values are used. If no spec is available, "N/S" will appear in that field and an ideal spec (usually zero) will be used for the calculation. Please note that it is highly unlikely that all worst-case specs would ever be present at the same time in the same part. The designer should always refer to the appropriate data sheet and substitute numbers most appropriate to the application. All calculations are approximations, with errors displayed and summed in absolute PPM, even though in some scenarios the actual values would be negative.

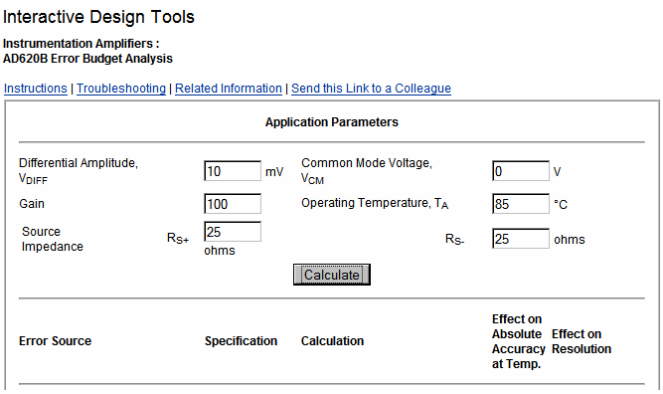
The error calculated is separated into two parts, as discussed in the error source section on op amps. It is separated into “resolution error,” which are errors which cannot be adjusted out of the system, and drift/gain errors, which can be adjusted out with the proper circuitry. Please refer to the op amp section on error sources for more information.

Op Amp Error Budget Calculator -3



This shows the remaining parameters calculated by the Op Amp Error Budget Calculator.

Instrumentation Amp Error Budget Calculator -1


Interactive Design Tools

Instrumentation Amplifiers :
AD620B Error Budget Analysis

Instructions | Troubleshooting | Related Information | Send this Link to a Colleague

Application Parameters

Differential Amplitude, V_{DIFF}	10	mV	Common Mode Voltage, V_{CM}	0	V
Gain	100		Operating Temperature, T_A	85	°C
Source Impedance	R_{S+} 25	ohms		R_{S-} 25	ohms

Calculate

Error Source	Specification	Calculation	Effect on Absolute Accuracy at Temp.	Effect on Resolution

A similar error budget calculator also exists for instrumentation amplifiers. For this tool the pertinent data is entered into the top field of the calculator. The tool automatically enters the specification data for the particular instrumentation amplifier selected and then calculates the error. Again, the error is separated into “resolution error,” which is the non-reducible part and the drift/gain error.

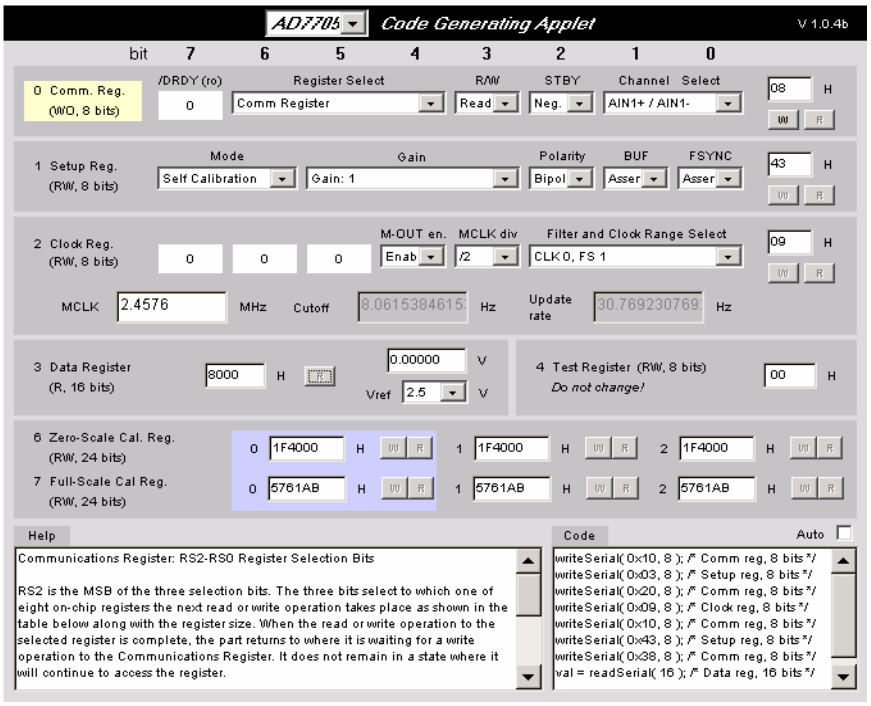
Instrumentation Amp Error Budget Calculator -2

Gain Error	0.5	%		5000	ppm
Gain Drift, G_{TC}	-50	ppm / °C	G_{TC} * (T_A-25)	3000	ppm
Gain Nonlinearity	0.0095	%		95	ppm
Input Offset Voltage, V_{OSI}	85	µV	V_{OSI} / V_{DIFF}	8500	ppm
Input Offset Voltage Drift, V_{OSI_TC}	0.6	µV / °C	(V_{OSI_TC} / V_{DIFF}) * (T_A-25)	3600	ppm
Output Offset Voltage, V_{OSO}	1	mV	V_{OSO} / (GAIN * V_{DIFF})	1000	ppm
Output Offset Voltage Drift, V_{OSO_TC}	7	µV / °C	(V_{OSO_TC} / (GAIN * V_{DIFF})) * (T_A-25)	420	ppm
Bias Current, I_B - Source Imbalance Error	1.5	nA	I_B * (R_{S+} - R_{S-}) / V_{DIFF}	0	ppm
Bias Current Drift, I_{B_TC} - Source Imbalance Drift	3.0	pA / °C	I_{B_TC} * (R_{S+} - R_{S-}) * (T_A-25) / V_{DIFF}	0	ppm
Offset Current, I_{OS} - Source Resistance + Imbalance Error	0.75	nA	I_{OS} * MAX(R_{S+}, R_{S-}) / V_{DIFF}	0	ppm
Offset Current Drift, I_{OS_TC} - Source Resistance + Imbalance Drift	1.5	pA / °C	I_{OS_TC} * MAX(R_{S+}, R_{S-}) * (T_A-25) / V_{DIFF}	0	ppm
Common Mode Rejection, CMRR	80	dB	V_{CM} / ($10^{CMRR/20}$ * V_{DIFF})	0	ppm
Noise, RTI (0.1 Hz - 10 Hz)	6	µV p-p		600	ppm
TOTALS				21520	ppm
				695	ppm

V 1.0.6

This shows the various errors calculated by the Instrumentation Amp Error Budget Calculator.

Register Configuration Assistants



Another type of “on line” design assistant are the configuration assistants. Many modern converters are actually small systems, usually with significant digital content. This digital content is used to set operating conditions (which channel of a multi-channel input ADC for instance), While it is possible to take the register descriptions in the data sheets and use them to set the correct bits in the correct registers, it is much easier to use a configuration assistant.

An example is the configuration assistant for the AD7730 Σ-Δ ADC. Each dark gray rectangle shows a single register's content in two different ways. Most of the space is taken up with pull-down menus and a few hex input fields that display bit fields within the register, MSB to LSB. 8 bits are displayed per row, with the bits aligned in numbered columns. At the right is the combined hex code corresponding to values selected for the individual bit fields.

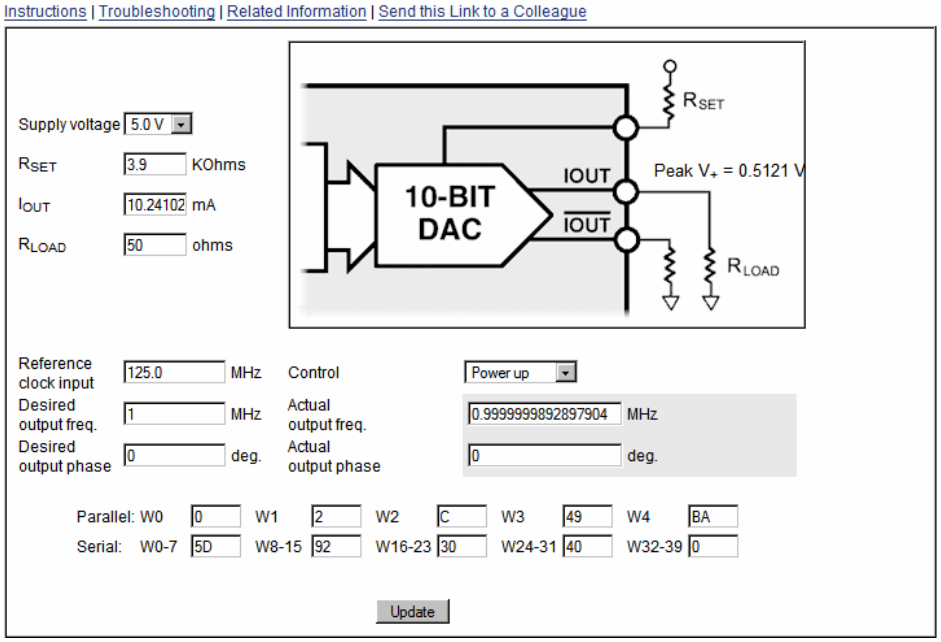
Changing either the hex code or the bit fields updates the other. Registers that can't be broken into separate fields are shown for completeness, even though not much can be done with them.

By default, reading and writing register pseudocode is, like the real AD7730, a two-step process: the Comm register must first be set up to select a target for the next read or write. After a register has been configured to your liking, select it in the Comm register and click "W." The selected register is now highlighted in yellow (and the channel in pink). To complete the cycle, click on the enabled "W" or "R." This will also clear the Register Select bits which must be manually reset for each access. Please note that the multiple read settings are nonfunctional – an ordinary read will be performed instead.

Both operations append pseudo-code instructions to a ticker of instructions at the bottom right of the applet. "writeSerial(val, length)" is an abstract subroutine that takes the quantity "val" and sends "length" bits of it serially to the AD7730, MSB first. The code list can be copied and pasted into another application (on most platforms).

Checking "Auto" above the Code output window puts code generation into a second mode, enabling all registers and automatically prepending the appropriate Comm register write when "W" or "R" for any register is clicked. Please note that in this mode the register select bits in the Comm register are ignored.

Direct Digital Synthesis (DDS) Device Configuration Assistant -1



Another example of a register configuration assistant is the one for an AD9850 Direct Digital Synthesis (DDS) system.

This calculator has several distinct functions. First, it's a tool for selecting a value for RSET, which sets the output current, and checking that the output level remains within limits for a given load.

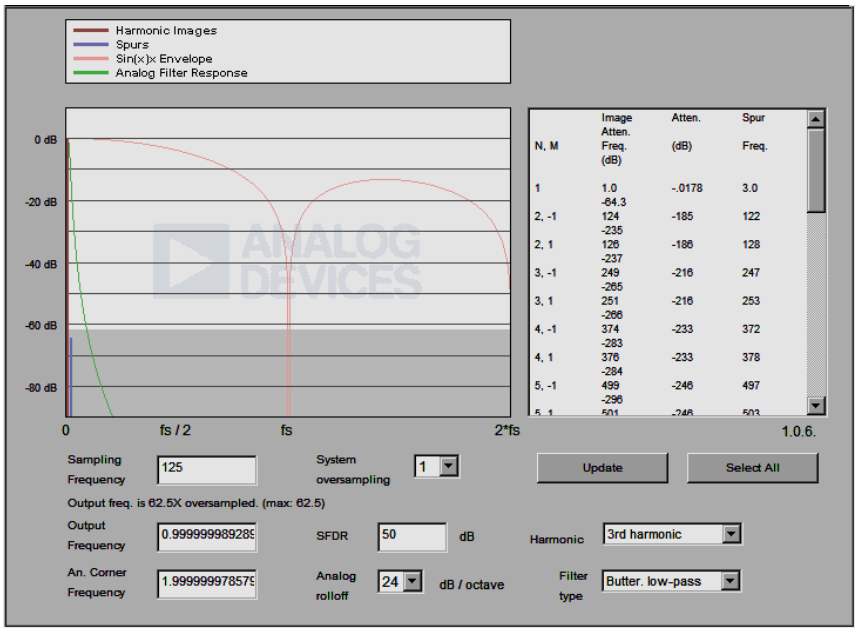
The AD9850 has complementary current output structures which limits the current and voltage that can be supplied and still meet other data sheet specifications. The output current level, IOUT, is set by a single external resistor, RSET, and the two are related by an equation. Changing one of these fields in the calculator updates the other automatically. If too high a current is selected, an error is noted. The IOUT current develops a voltage into the selected RLOAD, shown on the schematic, and is checked against the AD9850's compliance voltage.

Second, it's an assistant for selecting a 32-bit tuning word, given a reference clock and desired output frequency. Third, it shows the tuning word and other configuring bits encoded as a sequence of hex codes for use in programming the AD9850 via its parallel or serial interface.

A tuning word is selected by simply entering the desired REFCLK and output frequency. REFCLK has a maximum frequency that depends on supply voltage, selected at the top of the screen. Because the tuning word is limited to 32 bits there is typically a small deviation between the desired and actual output frequencies, which is shown in a field at right. The actual output frequency is what is encoded as the tuning word and this comprises the last four bytes of the parallel hex codes and the first four of the serial codes. Tuning words greater than 7FFFFFFF H exceed the Nyquist frequency and will cause error messages to appear.

The AD9850 has five bits of programmable phase which is selected in a manner similar to the desired output frequency. The closest available phase setting appears in the field at the right and in the corresponding hex code with the power down bit. The hex code fields are bidirectional, and a known set of hex codes can be entered to retrieve the programmed frequency and phase.

Direct Digital Synthesis (DDS) Device Configuration Assistant -2



Lastly, output harmonics are shown for the selected reference clock and output frequency after an external reconstruction filter has been applied.

Suppression of images and spurs (waveform reconstruction) can be simulated by selecting corner frequency, filter order, and type of a simple analog filter (last line of images calculator; magnitude rolloff). A region corresponding to 10 bits of quantization noise is shaded at the bottom of the graph for reference. This calculator is based on a highly simplified model of the AD9850: check data sheet for parameters appropriate to your application.

Notes: