



SAM9X60 Device

SAM9X60 Device Silicon Errata and Data Sheet Clarification

SAM9X60 Device

The SAM9X60 device that you have received conforms functionally to the current Device Data Sheet (DS60001579), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table. The silicon issues are summarized in [1. Silicon Issue Summary](#).

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [6. Data Sheet Clarifications](#), following the discussion of silicon issues.

The Device and Revision ID values for the SAM9X60 silicon device are shown in the following table.

Table 1. SAM9X60 Silicon Device Identification

Part Number	Device Identification	
	CHIPID_CIDR[31:0]	CHIPID_EXID[31:0]
SAM9X60-V/DWB	0x819B35A1	0x00000000

Note: Refer to the "Chip Identifier" and "Product Identification System" sections in the current device data sheet (DS60001579) for detailed information on chip identification and version for your specific device.

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1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Item/Feature	Summary	Affected Silicon Revisions		
			A		
System Controller	System Controller Write Protection Status Register (SYSC_WPSR) Limitation	Write access violation is not reported by SYSC_WPSR.	X		
OTPC	OTPC Limited Number of Packets	The number of packets is limited to 2.	X		
	OTPC Restricted Operating Range in Write Mode	Write operations cannot be performed over the full temperature and VDDANA ranges.	X		
	OTPC Wrong Default Configuration	The default configuration cannot be used to access the OTP memory in Write mode.	X		
PMC	ULP1 Mode Entry Procedure	Spurious exit from ULP1 mode	X		
Static Memory Controller	Register Write Protection Not Effective on SMC_OCMS Register	The register write protection is not effective on the SMC_OCMS register.	X		

2. System Controller Write Protection (SYSCWP)

2.1 System Controller Write Protection Status Register (SYSC_WPSR) Limitation

The status register SYSC_WPSR does not set the write access violation status flag for write-protected registers of RTC, RTT and WDT peripherals when the bit WPEN is set in SYSC_WPMR for these peripherals. However, the write protection mechanism is active.

Work Around

None

Affected Silicon Revisions

A							
X							

3. OTP Controller (OTPC)

3.1 OTPC Limited Number of Packets

The number of packets allowed to be written in the user area is limited to 2. The maximum size of the payload for each packet is 8192 bits.

Work Around

None

Affected Silicon Revisions

A							
X							

3.2 OTPC Restricted Operating Range in Write Mode

The write operations in the OTPC cannot be performed over the full temperature and VDDANA power supply ranges specified.

Work Around

The write operations in the OTPC are restricted to the following ambient temperature and VDDANA power supply ranges:

- $T_A = [0^{\circ}\text{C to } 50^{\circ}\text{C}]$
- $VDDANA = [3.15\text{V to } 3.45\text{V}]$

Affected Silicon Revisions

A							
X							

3.3 OTPC Wrong Default Configuration

The default configuration of the OTPC cannot be used to access the OTP memory in Write mode.

Work Around

Prior to any write operation in the OTPC, the OTPC must be configured using the following code. This operation needs to be performed only once before the first write operation and whenever the peripheral reset (signal `periph_nreset`) is asserted.

```
#define ARRAY_SIZE(a) (sizeof(a) / sizeof((a)[0]))

/*
 * writing one word lasts 350us
 * the timeout was chosen to be enough for writing 10 words  */ #define TIMEOUT 500000

#define OTPC_0      (0x1u << 0)
#define OTPC_1      16
#define OTPC_2      (0xffffu << OTPC_1)
#define OTPC_3      (0x4391u << OTPC_1)

static void otp_sam9x60_fixup(void)
{
    static const uint32_t fixup0[4] = {0x04194801, 0x01000000, 0x00000008, 0x00000000};
    static const uint32_t fixup1[4] = {0xfb164801, 0x4c017d12, 0x02120e01, 0x00004000};
```

```

__IO uint32_t *OTPC_4 = (__IO uint32_t *)((uint8_t *)OTPC + 0x090);
__IO uint32_t *OTPC_5 = (__IO uint32_t *)((uint8_t *)OTPC + 0x0A0);
__IO uint32_t *OTPC_6 = (__IO uint32_t *)((uint8_t *)OTPC + 0x0B0);
uint32_t timeout;
int i;

timeout = TIMEOUT;
*OTPC_4 = OTPC_0 | OTPC_3;
while (!(OTPC->OTPC_SR & OTPC_SR_UNLOCK) && --timeout > 0);

for (i = 0; i < ARRAY_SIZE(fixup0); i++)
    OTPC_5[i] = fixup0[i];

for (i = 0; i < ARRAY_SIZE(fixup1); i++)
    OTPC_6[i] = fixup1[i];

timeout = TIMEOUT;
*OTPC_4 = OTPC_3;
while ((OTPC->OTPC_SR & OTPC_SR_UNLOCK) && --timeout > 0); }

```

Affected Silicon Revisions

A							
X							

4. Power Management Controller (PMC)

4.1 ULP1 Mode Entry Procedure

If one or more read or write accesses to the PMC user interface follow the last instruction to enter ULP1 mode (set CKGR_MOR.ULP1), the ULP1 mode may be exited immediately after the entry.

Work Around

Add two dummy read accesses outside of the PMC user interface just after setting the CKGR_MOR.ULP1 bit.

Affected Silicon Revisions

A							
X							

5. Static Memory Controller (SMC)

5.1 Register Write Protection Not Effective on SMC_OCMS Register

The register SMC_OCMS is not write-protected when the bit WPEN is set in SMC_WPMR.

Work Around

None

Affected Silicon Revisions

A							
X							

6. Data Sheet Clarifications

6.1 EBI Controls in Special Function Registers (SFR)

6.1.1 Use of DDR_MP_EN and NFD0_ON_D16 bits in SFR_CCFG_EBICSA

When:

- a NAND Flash memory is connected to D16-D23 and
- a DDR2-SDRAM or LPDDR-SDRAM is connected to D0-D15,

the bits SFR_CCFG_EBICSA.DDR_MP_EN and SFR_CCFG_EBICSA.NFD0_ON_D16 must both be set before performing the SDRAM initialization.

7. Revision History

7.1 DS80000846A - 10/2019

First issue.

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