Active Cell Balancing Methods for Li-Ion Battery Management ICs using the ATA6870

ATA6870

Application Note

1. Scope

This application note describes methods of active battery cell balancing with the ATA6870.

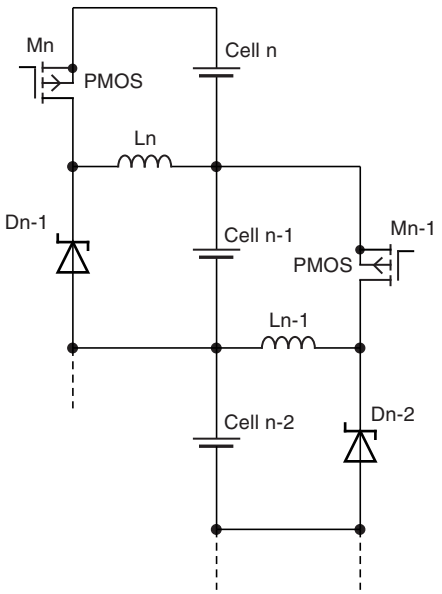
2. Cell Balancing

In a multi-cell battery pack, no two cells are identical. There are always slight differences in the state of charge, capacity, impedance and temperature characteristics — even between cells from the same manufacturer and production lot. Furthermore, these differences generally increase over battery lifetime.

Cell balancing circuits can significantly eliminate these mismatches, resulting in improved efficiency as well as increased overall capacity and lifetime of the battery cell stack.

There are usually two types of balancing: active and passive. With the passive method, the current is bypassed through balancing resistors and the discharged energy is dissipated as heat. The active balancing method, which is significantly more efficient, uses inductors or capacitors for virtually lossless energy transfer between battery cells. Capacitors are used for balancing currents lower than 50 mA, inductors can be used for balancing currents up to 1A and more.

Figure 2-1. Active Balancing Concept with Inductors



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3. Active Cell Balancing with the ATA6870

3.1 ATA6870 Internal DISCHn Control

Figure 3-1. ATA6870 Internal DISCHn Control

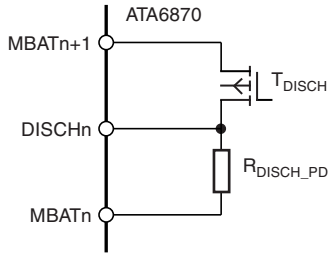


Figure 3-1 shows the internal circuitry of the ATA6870 that controls the DISCHn pin. A PMOS transistor is implemented to pull the DISCHn pin to high. The gates of the external PMOS and NMOS transistors are switched to high via a typical output current of 1 mA. For safety reasons, an integrated pull-down resistor is used for the DISCHn pins instead of a pull-down transistor. This ensures that the balancing process is stopped even when the ATA6870 is switched off and no parasitic cross conduction current can be caused by floating gates. Due to SPI control of the DISCHn pins, the maximum switching frequency is 3 kHz. An additional external resistor R_{PD} is recommended in parallel to R_{DISCH_PD} to achieve adequate switching times.

3.2 Inductive Balancing Method

This method has the advantage of high balancing currents (>100 mA, up to 1A) plus the fact that balancing is independent of the cell voltages.

With the ATA6870, one discharge control signal DISCHn is available for each battery cell. The discharge pins DISCHn are switched on and off via the SPI interface.

The concept for transferring the energy from a battery cell to its lower neighbor cells is shown in Figure 3-2 on page 3. In principle, this is a modular concept that can be used for all cells in a stack. A module generally consists of one switching transistor (PMOS), one diode and one inductor. For a battery stack of n cells, n-1 modules are needed.

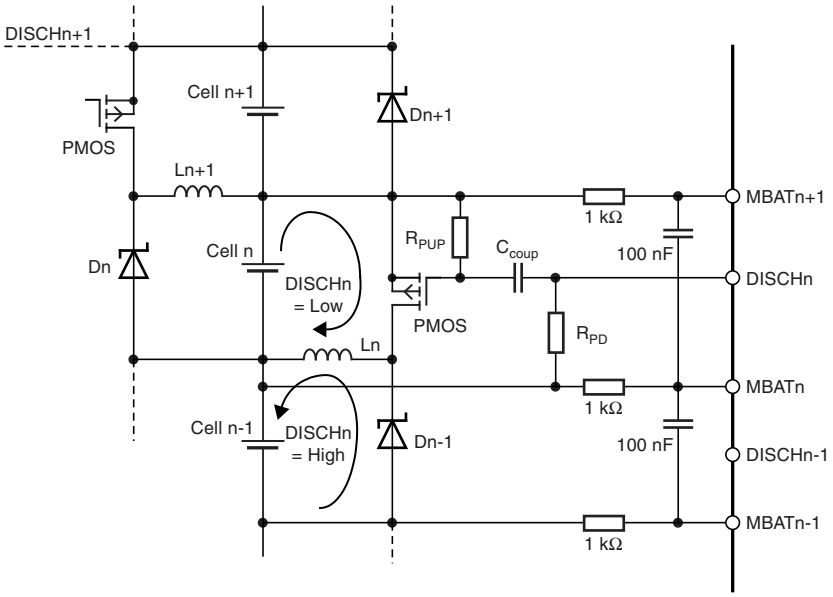
3.2.1 Description of Energy Transfer to Lower Neighbor Cells with ATA6870

After defining the cell to be discharged (cell n), the corresponding DISCHn output is switched on/off via the SPI control, thereby generating a switching frequency of maximum 3 kHz.

When the DISCHn control signal is switched to low, the PMOS transistor of cell n is switched ON and energy is transferred from cell n to inductor Ln (see Figure 3-2 on page 3).

When the DISCHn control signal is switched to high, the switching transistor is OFF and the continuous flow of the inductor current through diode Dn-1 transfers the energy stored in inductor Ln to the lower battery cell. The energy transfer is completed with only slight losses caused by the inductor's series resistor, the ON resistance of the transistor and power dissipation through the diode.

Figure 3-2. Description of Energy Transfer to Lower Neighbor Cell



With the described concept, it is possible to transfer the charge from all cells of a stack to their lower neighbor cells. However, if it is the lowest cell of a battery stack that needs to be discharged, a transformer concept applies, as shown in Figure 3-3. The energy transferred from cell 1 charges the top cell in the battery stack (cell n).

Inductive charge balancing between two stacked ATA6870s is also possible. Figure 3-4 on page 4 depicts the balancing circuit of two stacked ICs and shows how energy can easily be transferred from cell 7 to cell 6, if required.

Figure 3-3. Transformer Concept to Transfer Energy from the Lowest Cell in a Stack to the Top-level Cell

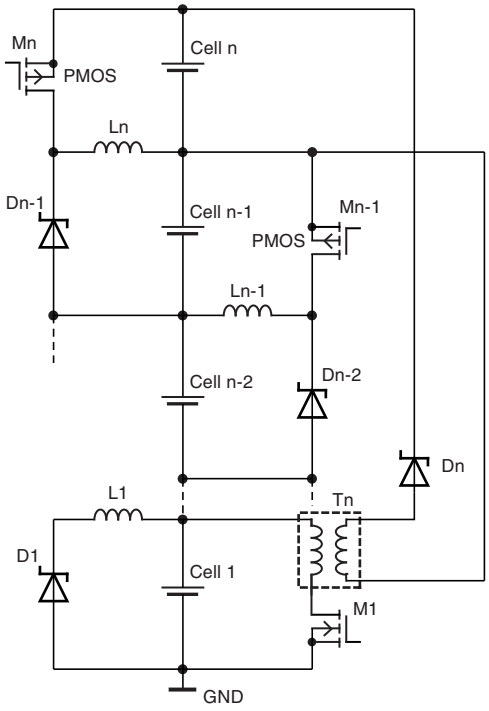
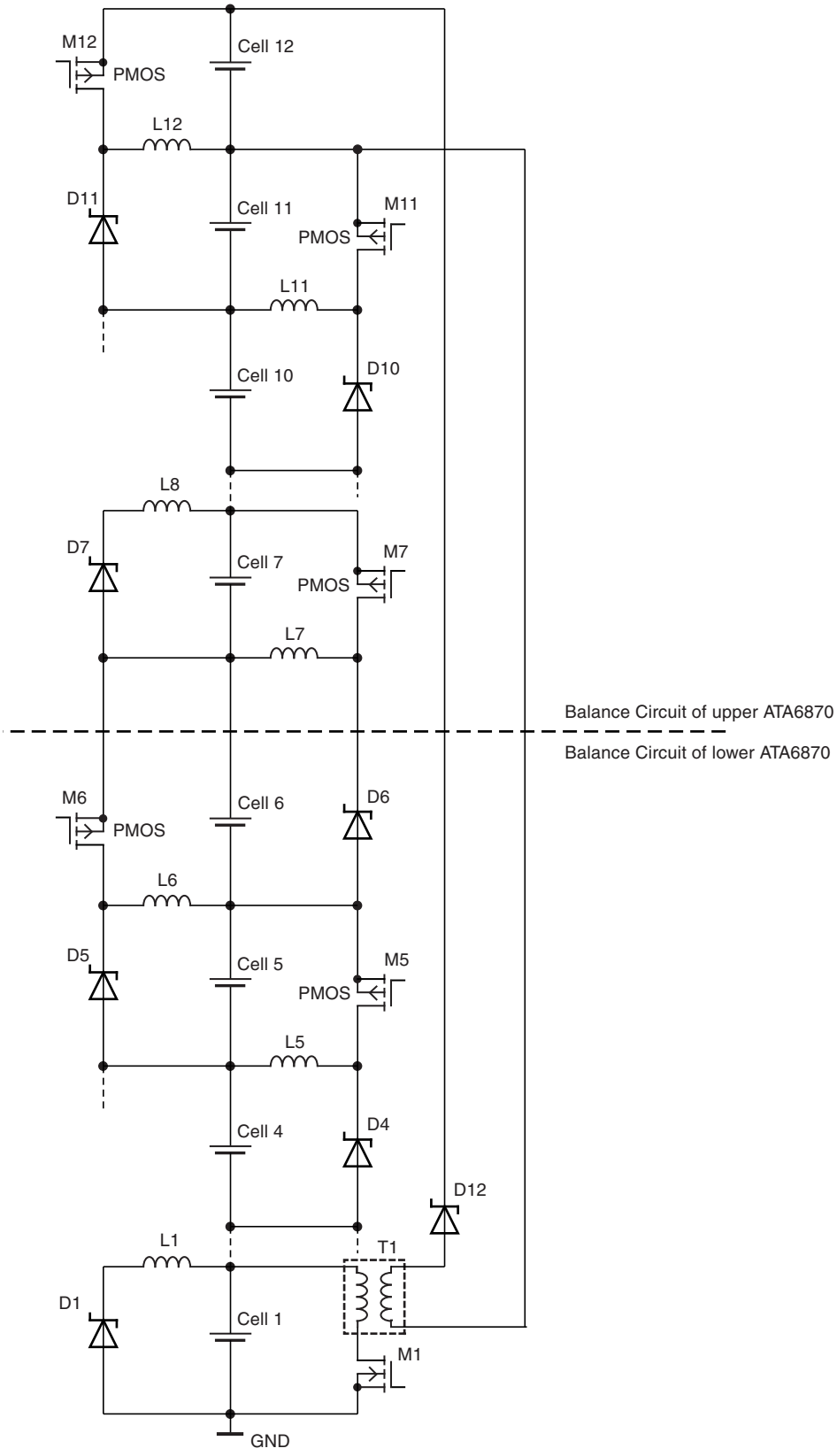


Figure 3-4. Inductive Charge Balancing Between Two Stacked ATA6870s



3.2.2 Circuit Considerations

To ensure that external switching transistors are only switched on with a short pulse, AC coupling between the DISCHn pin and the transistor is strongly recommended. This can be achieved with a capacitor (Ccoup). An additional gate source resistor (R_{PUP}) is necessary to guarantee that transistors are switched off safely where this cannot be done by the microcontroller. Recommended values are Ccoup = 100 nF and R_{PUP} = 100 kΩ. Due to the AC coupling, transistors with a low threshold voltage are recommended, e.g., Vishay® Si5515CDC or Si5935CDC (see Figure 3-2 on page 3).

As mentioned above, an additional external resistor R_{PD} is recommended in parallel to DISCHn to achieve adequate switching times.

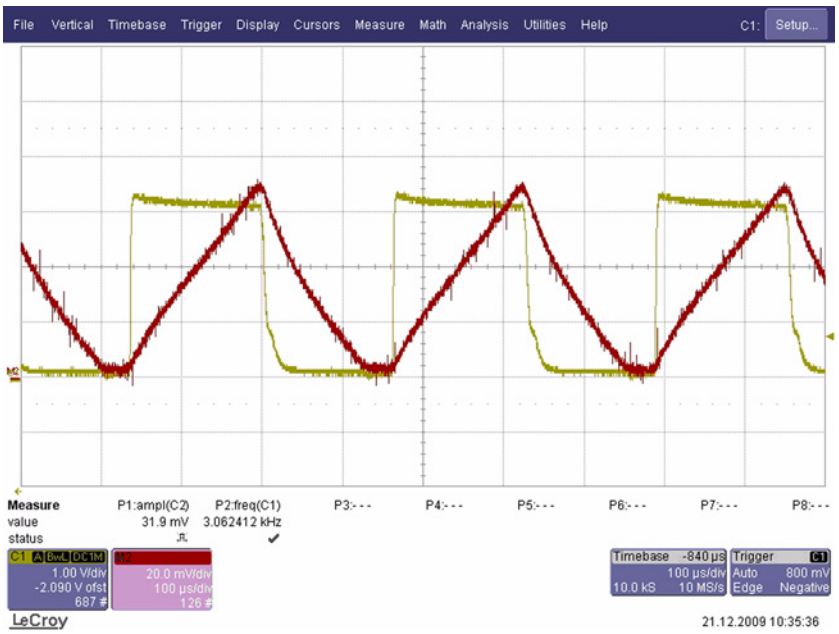
Switching transistors with a low $R_{DS(ON)}$ and inductors with a very low serial resistor R_{DC} are necessary to minimize transfer losses. Also, Schottky diodes are recommended due to their very low forward-bias voltage.

3.2.3 Example of Inductive Balancing

Figure 3-5 shows the current through inductor Ln for a balancing setup with a 470 µH inductor and a switching frequency of 3 kHz. Cell balancing from cell n to its lower neighbor, cell n-1 was achieved with an average cell balancing current of approximately 280 mA. The voltage of cell n was 4.0V.

Channel 1 shows the switching signal coming from the DISCHn pin. Channel 2 shows the balancing current, with a peak value of approximately 790 mA.

Figure 3-5. Cell Balancing to Lower Cell



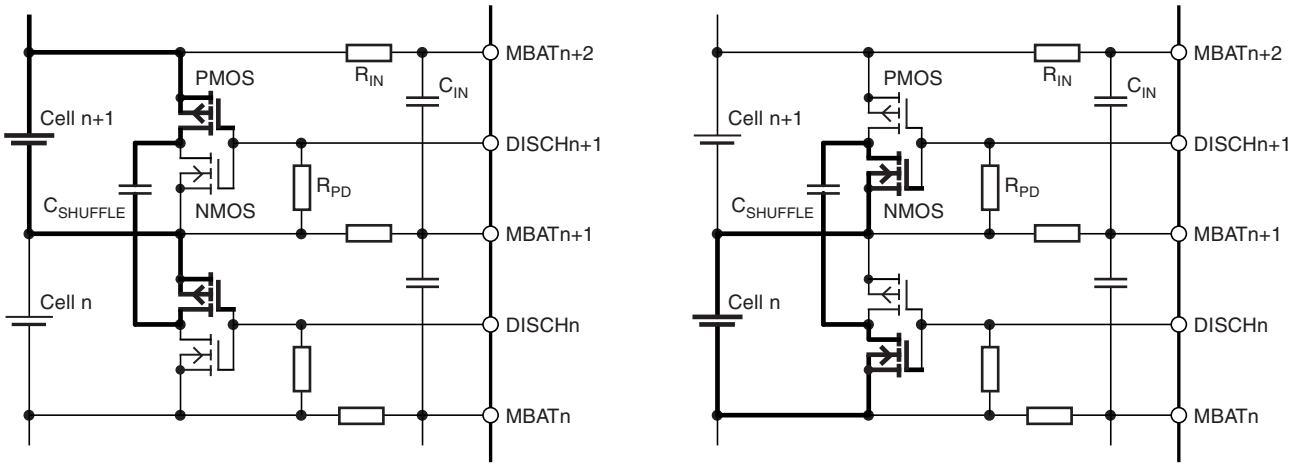
3.2.4 Comparison of Inductor Types

Table 3-1. The Balancing Currents That Can Be Achieved With Different Inductors

f (kHz)	Inductor Type	Inductance (µH)	Resistor of Inductor (mΩ)	Peak Balancing Current (mA)	Average Balancing Current (mA)
3	Toroidal	300	130	1240	470
3	Toroidal	470	135	790	280
3	SMD	220	380	2280	890
3	SMD	330	430	1620	610
3	SMD	470	560	1240	430

3.3 Capacitive Balancing Method

Figure 3-6. Active Balancing Using Capacitors



1. DISCHx = low - both PMOS activated

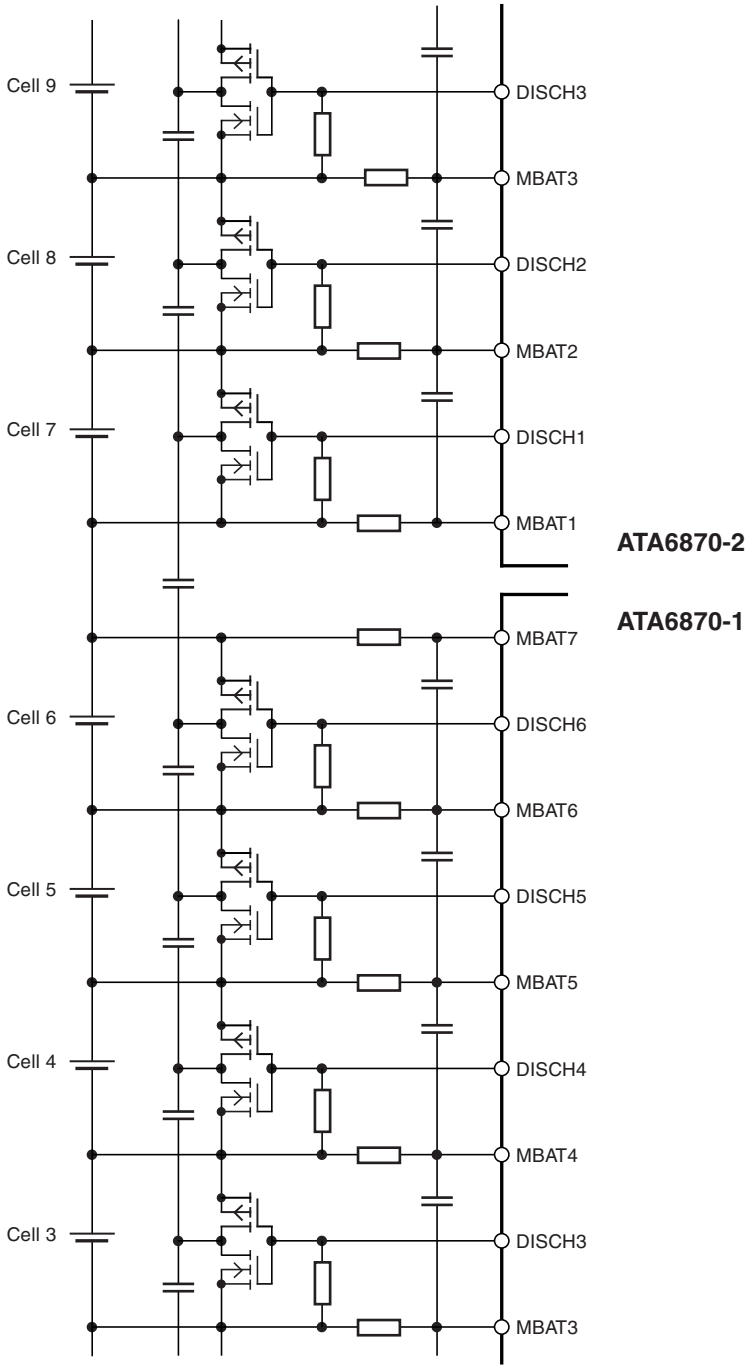
2. DISCHx = high - both NMOS activated

This is an inexpensive active balancing method suitable for average balancing currents up to 50 mA. The discharge pins DISCHn are switched on and off via the SPI interface of the ATA6870. The maximum possible switching frequency is 3 kHz. Figure 3-6 shows how the charge is transferred with capacitors.

First, the shuffle capacitor is switched in parallel to the cell with the higher voltage. The capacitor is charged to this voltage level and then switched in parallel to the cell with the lower voltage. Next, the capacitor charges this cell until its voltage is equal to that of the charged cell. Switching the shuffle capacitor between the two cells transfers the charge from the cell with the higher voltage to that with the lower voltage. The higher the difference in voltage between the cells, the greater the charge transferred in one step.

There are two pairs of NMOS and PMOS transistors to transfer charge between the two cells. The PMOS transistors connect the shuffle capacitor to the upper cell, while the NMOS transistors connect it to the lower cell. The direction of charge transfer is always from higher to lower voltage, irrespective of the cell's position. This type of charge transfer also works between stacked ICs (see Figure 3-7).

Figure 3-7. Active Charge Balancing Between Two Stacked ATA6870s



3.3.1 Example of Capacitive Balancing

External transistors with low gate-source capacity, e.g., the Vishay SI5504BDC are recommended to limit switching losses caused by charging the gate-source capacitors of the PMOS/NMOS channels. To ensure proper switch on/off times for these transistors, a 10 kΩ pull-down resistor is required between the DISCHn and MBATn pins. Figure 3-8 shows the circuit behavior with a 100 µF tantalum capacitor and 3 kHz switching frequency. The upper cell in the string had a voltage of 3.8V, and the voltage of the lower cell in the string was 30 mV higher than that of the upper cell. The charge was balanced, transferring from the lower to the higher cell. In this case, the average balancing current from the lower to the upper cell was 12 mA. Channel 1 shows the voltage level of the negative point of the capacitor, channels 3 and 4 show the balancing currents of the cells being balanced (10 mA/Div).

Figure 3-8. Charge/Discharge Current

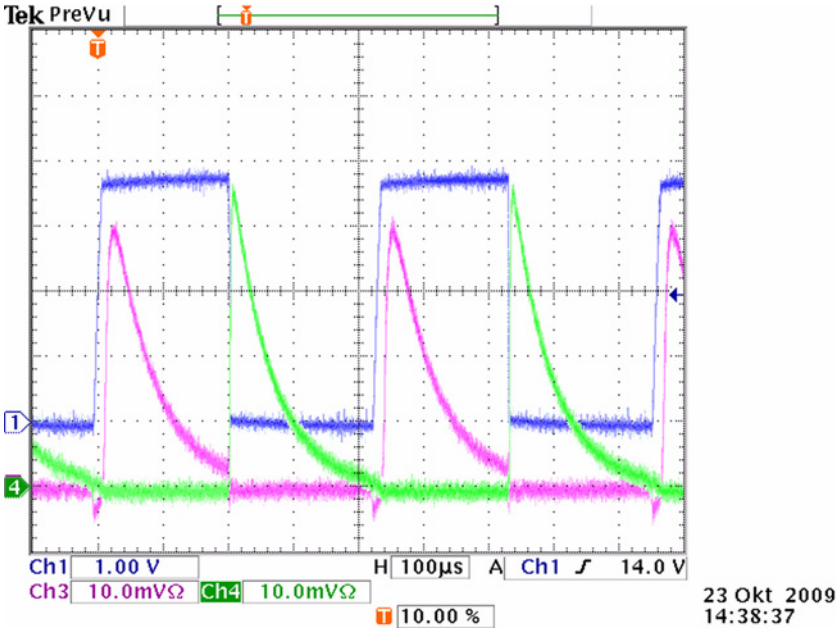


Table 3-2 shows the balancing currents that can be achieved with different frequencies and capacitors.

Table 3-2. Achievable Cell Balancing Current

f (kHz)	Capacitor	Capacity (µF)	Cell Voltage Difference (mV)	Balance Current (mA)
2.3	Electrolytic	33	110	15
3	Electrolytic	100	70	18
1	Electrolytic	470	70	20
3	Electrolytic	470	70	28

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