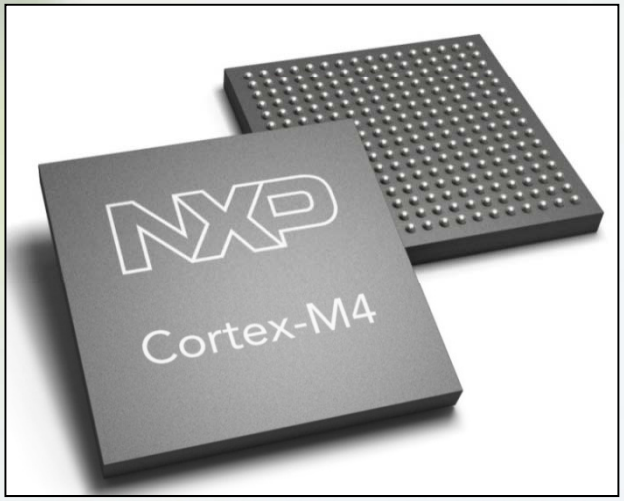
ARM Cortex-M4 based LPC4000 Family



October/November 2010

Presenter's Name

Agenda

- Introduction
- Introducing the Cortex-M4 LPC4300
- NXP’s advanced peripherals
- Demo
- Tools / Getting started

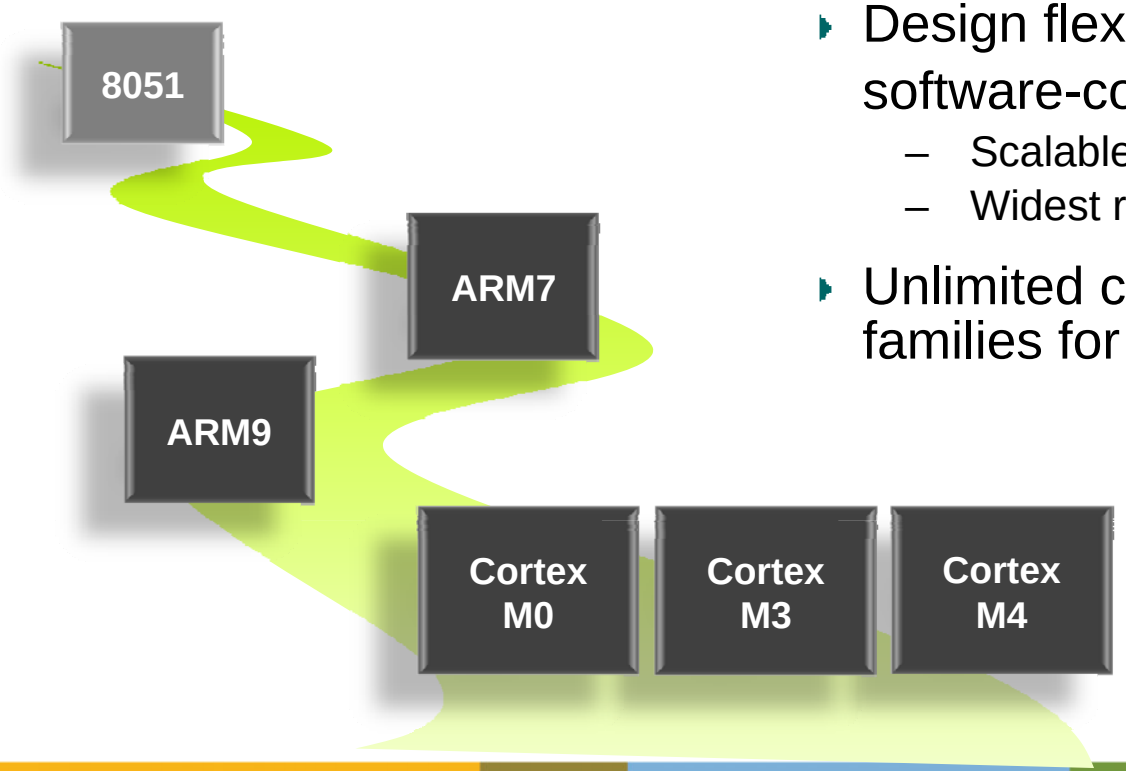
Introduction

NXP Semiconductors

- **Headquarters**: Eindhoven, The Netherlands
- **Employee base:** about 28,000 employees working in more than 25 countries
- **Net sales**: $3.8 billion in 2009
- **Patents:** ~14,000 issued and pending
- **R&D:** Over $600 million investment per year
- **Innovation track record dating 50+ years**

founded by Philips

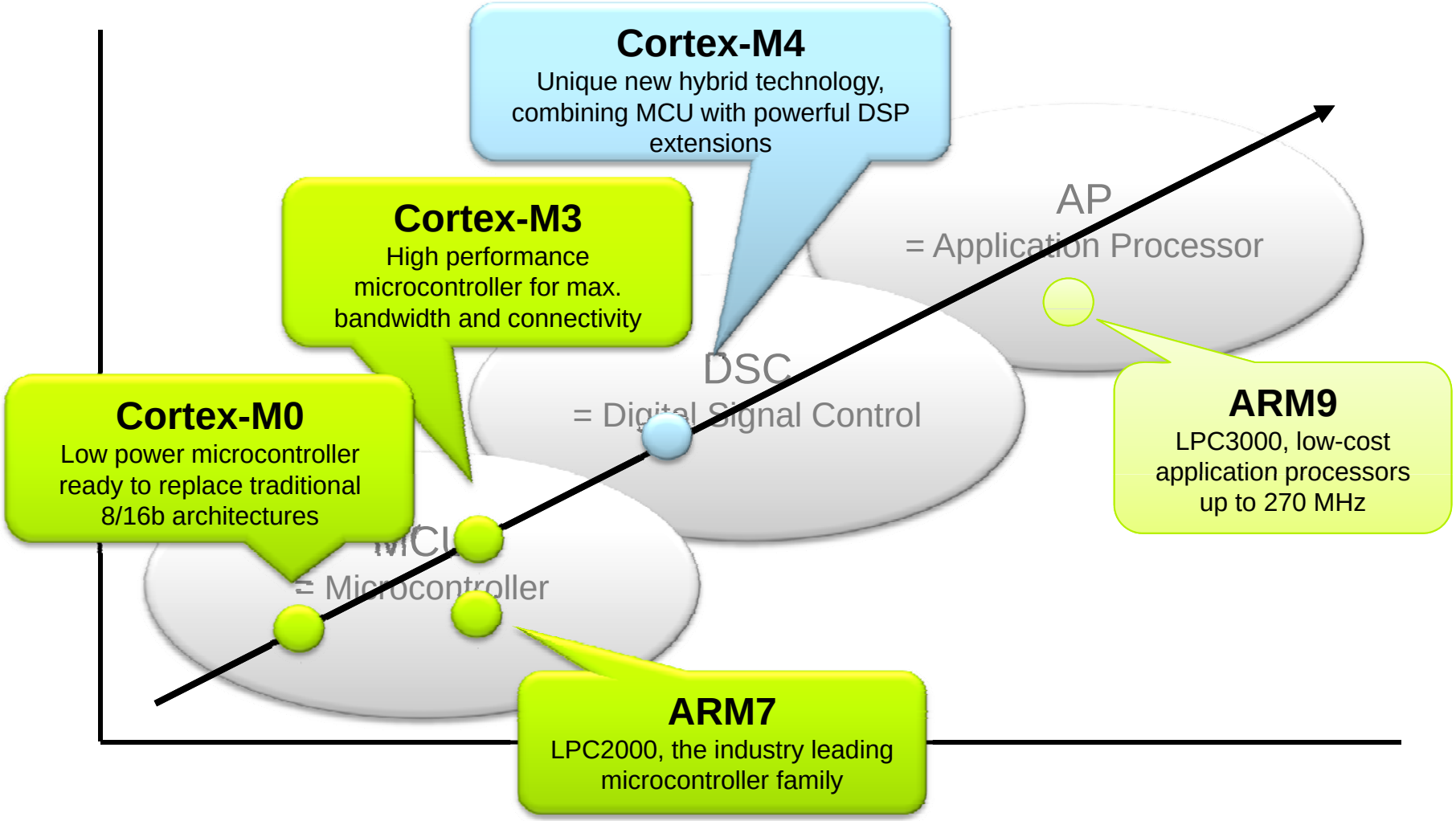
NXP is a leader in ARM Flash MCUs



- Clear strategy: 100% focus on ARM
- Top performance through leading technology & architecture
- Design flexibility through pin- and software-compatible solutions
  - Scalable memory sizes
  - Widest range of peripherals
- Unlimited choice through complete families for multiple cores

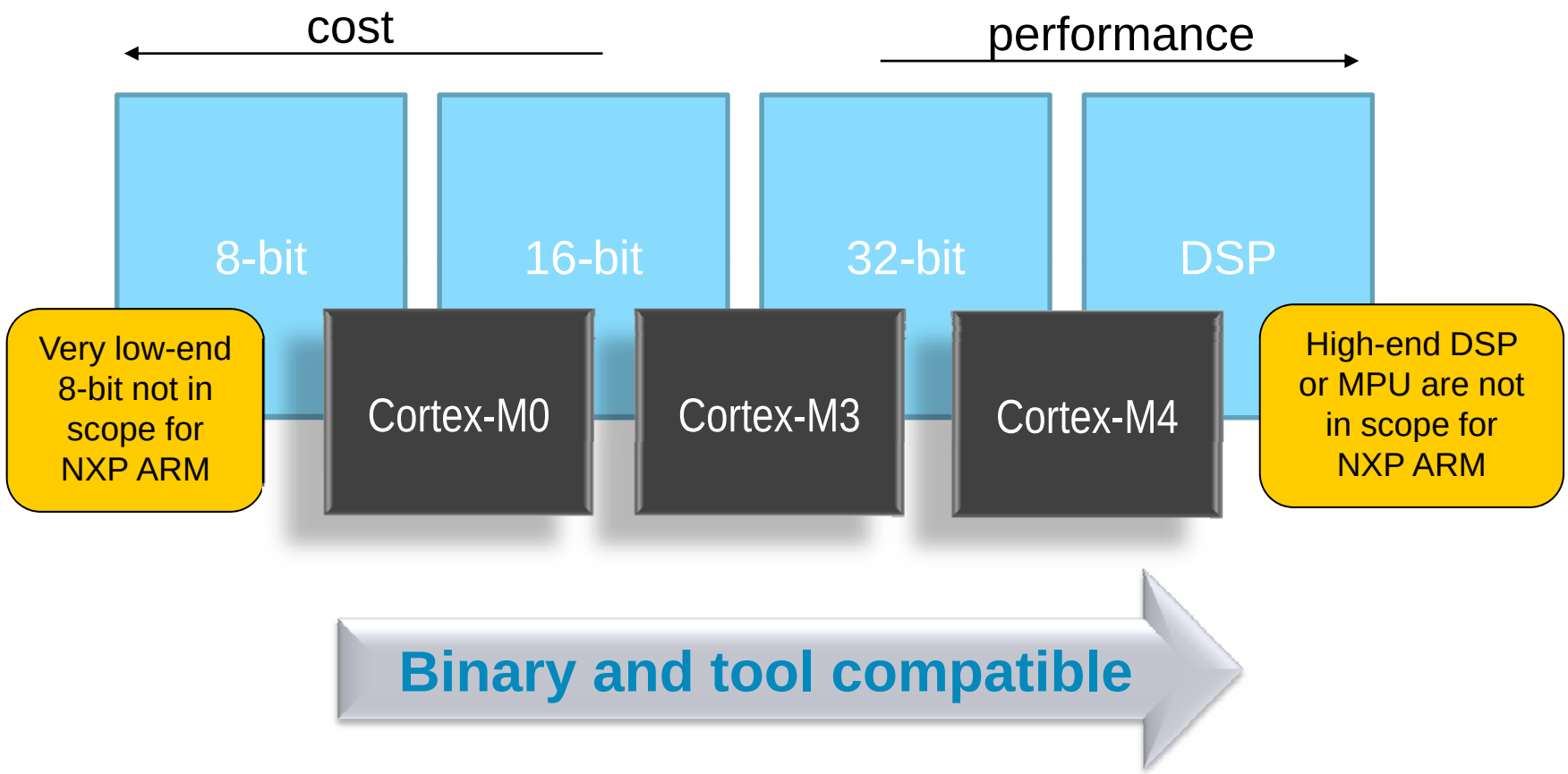
NXP microcontrollers = One continuum

➔ ***Five MCU cores lined up to serve a full range of application requirements***

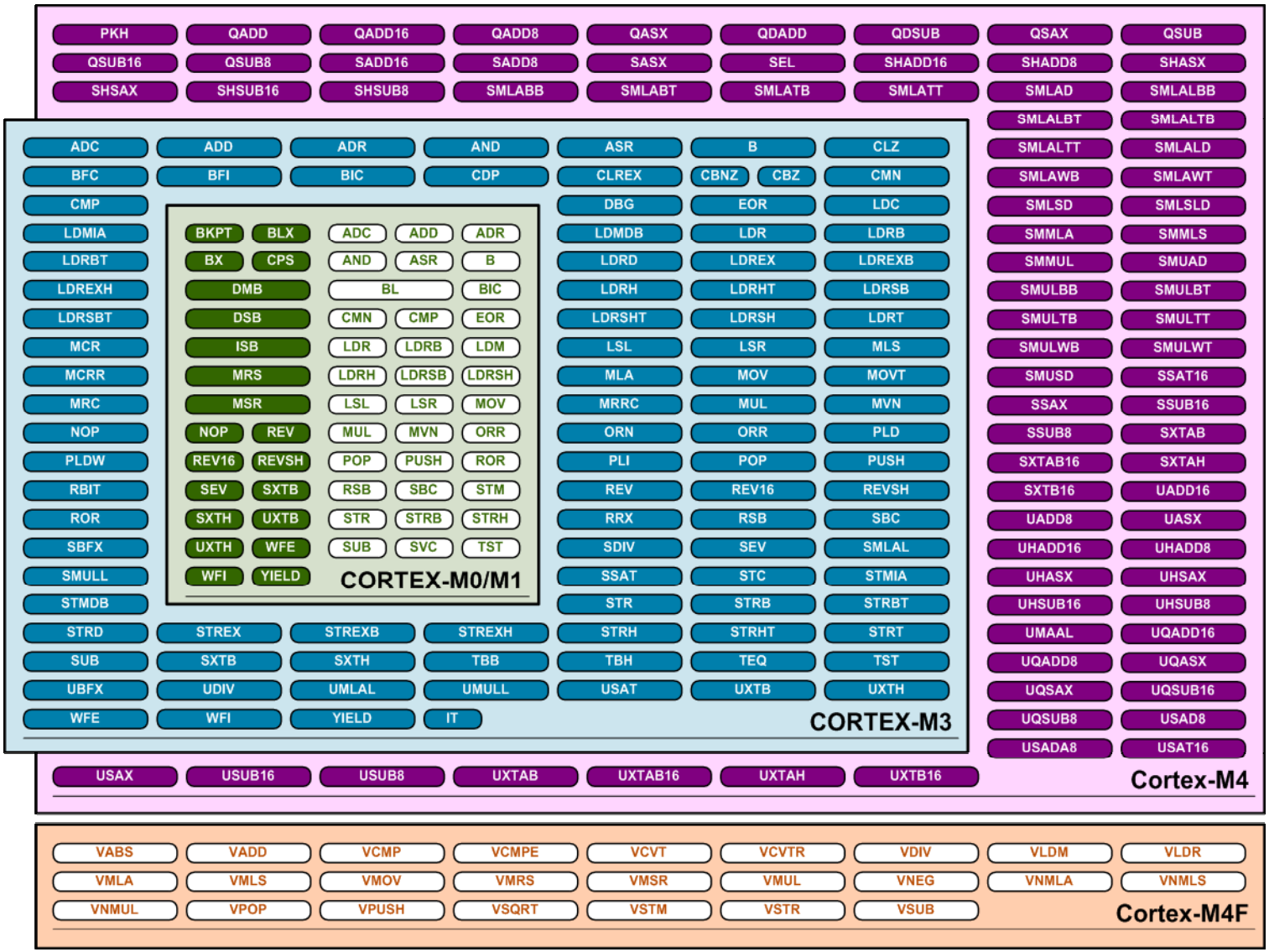


NXP changing the industry MCU landscape

➔ ***Breaking through traditional boundaries of 8b, 16b, 32b and DSP***



Powerful Cortex-M instruction set



ARM Cortex™-M0 based parts

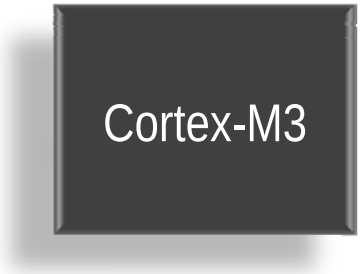
Cortex-M0

- Low Power
- Superior Code Density
- 32-bit performance
- Low Cost



Pin compatible options from M0 to M3

ARM Cortex™-M3 based parts



- General purpose, 32-bit microprocessor
- High performance
- Very low power consumption.

Pin compatible options from M0 to M3

ARM Cortex™-M4 based parts

- Adds DSP extensions and a Floating Point Unit

Rapidly growing family of Cortex-M microcontrollers

➔ ***Check pin- and software compatible options: www.nxp.com/microcontrollers***

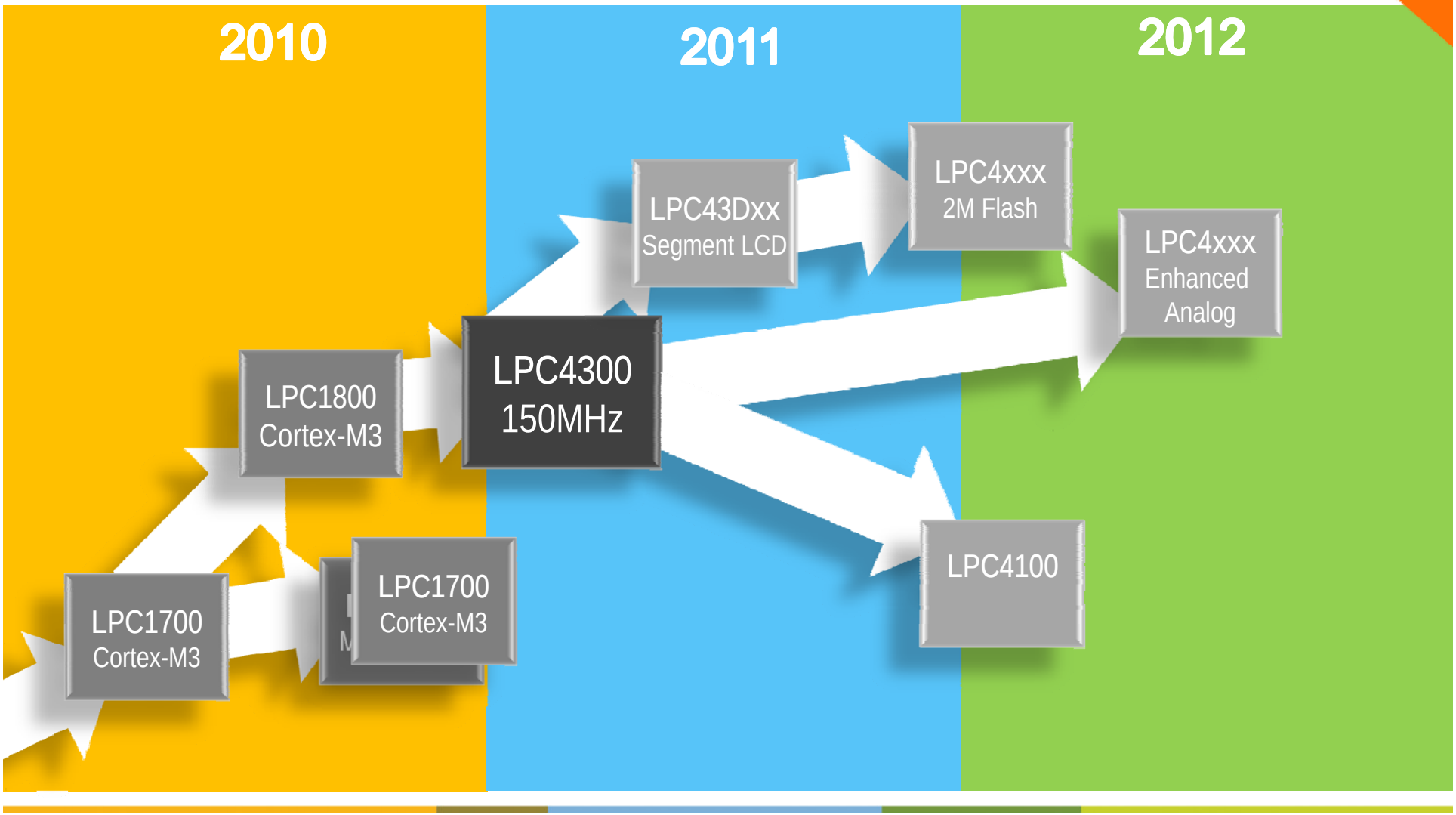
Cortex-M4 *+150MHz*	LPC4300	**MCU with powerful DSP extensions**
Cortex-M3 *Up to 150MHz*	LPC1800	**Memory options up to 1MB flash, 200k SRAM**
	LPC1700	**High-performance with USB, Ethernet, LCD, and more**
	LPC1300	**USB solution, incl. on-chip USB drivers**
Cortex-M0 *Up to 50MHz*	LPC1200	**Memory options up to 128k flash**
	LPC1100	**Best-in-class dynamic power consumption**
	LPC11A00	**Mixed-signal, incl. DAC, Temp Sensor, Comparators**
	LPC11U00	**USB solution, incl. on-chip USB drivers**
	LPC11C00	**CAN solution, incl. on-chip CAN drivers**

LPC4000

Cortex-M4 Introduction

- **Feb 22**, ARM Launches Class-Leading Cortex-M4 Processor For High Performance Digital Signal Control
  - combination of high-efficiency signal processing and MCU technology
- **Feb 22**, NXP Licenses ARM Cortex-M4 Processor for 32-bit Microcontroller Signal Processing Applications
  - **complements NXP's Cortex-M3 and Cortex-M0** processor-based devices and enables us to provide an end-to-end solution to the MCU community
- **April 12**, NXP Demonstrates New Class of DSC Based on ARM Cortex-M4
  - **first working silicon** of newest NXP microcontrollers based on the ARM Cortex-M4
  - the DSP extensions of the Cortex-M4 offer significant advantages, for example, offering 5 to 10 times improvement in complex DSP algorithms
- **Now**, Close cooperation with lead customers and DSP algorithm developers

NXP Cortex-M4 Roadmap

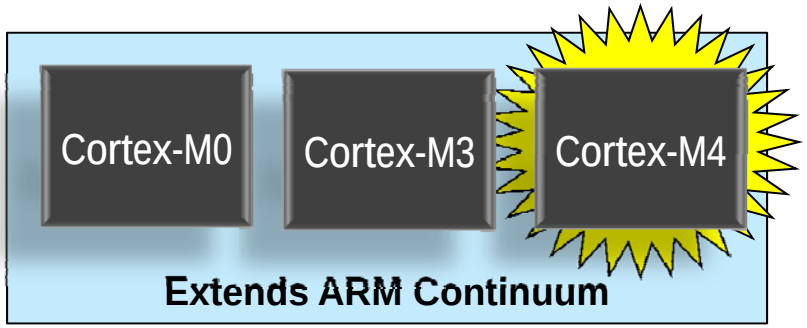


Introducing the LPC4300 Family

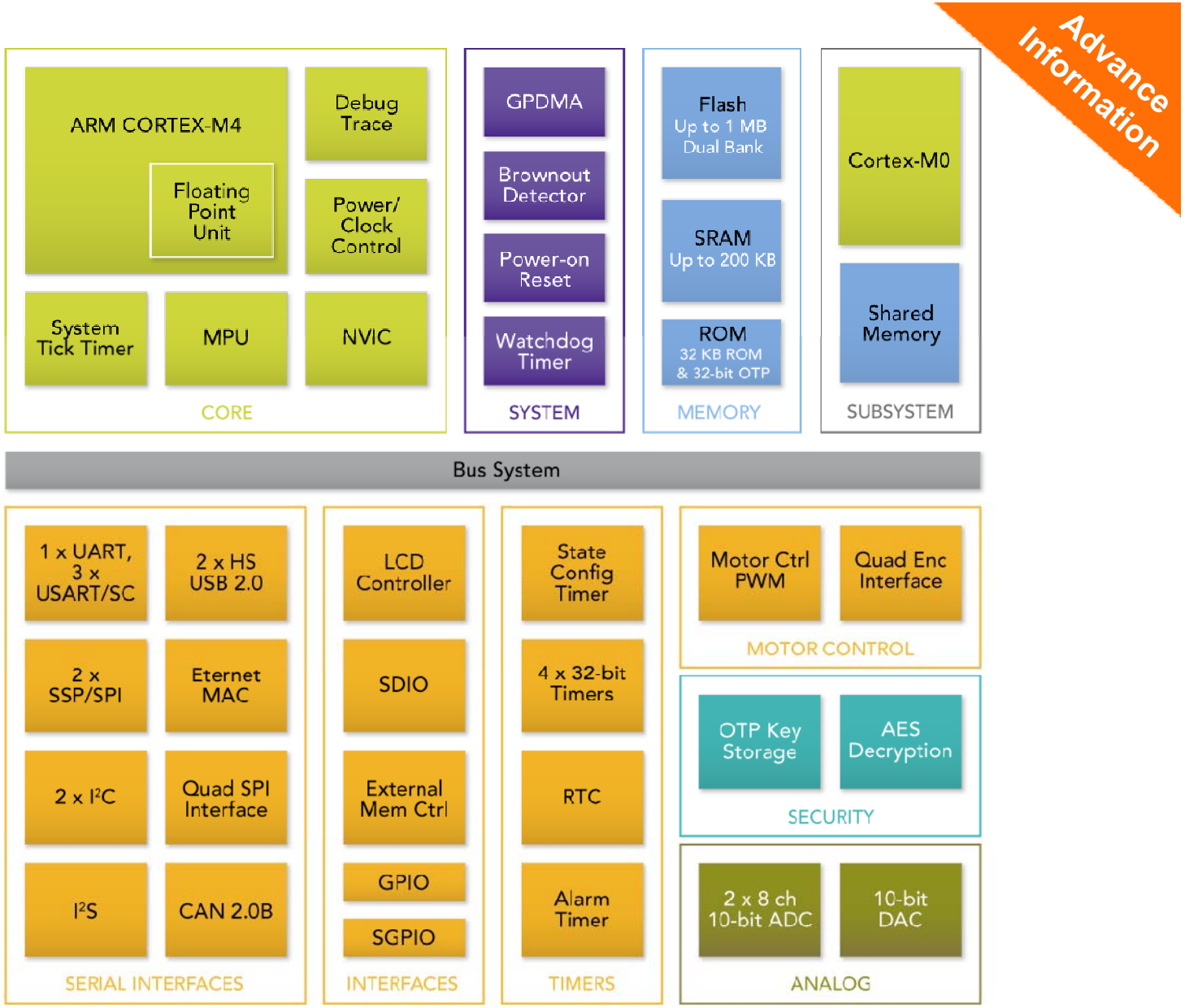
Advance Information

- Cortex-M4 based Digital Signal Controller
- Cortex-M0 Subsystem
- Up to **1 MB Flash**
  - Dual-Bank Flash provides safe in-application programming (IAP)
- Large SRAM: up to **200 KB SRAM**
- SPI Flash Interface with four lanes and up to 80 Mbps/lane
- State Configurable Timer Subsystem
- SGPIO
- Two **High-speed USB 2.0** interfaces. An on-chip High-speed PHY
- Pin compatibility with Cortex-M3 parts

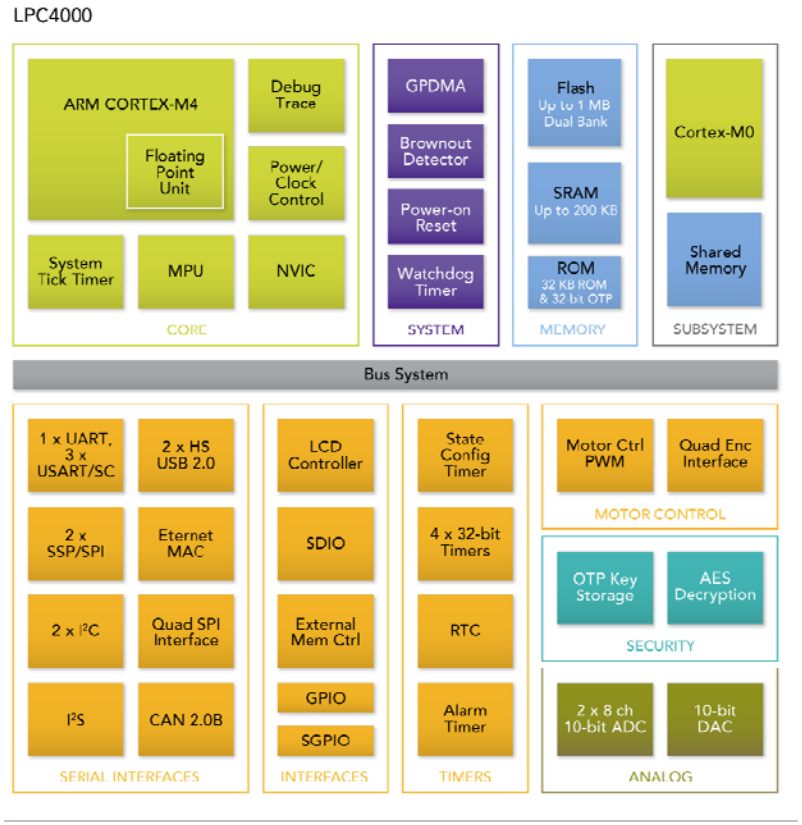
- Additional Features
  - 10/100 Ethernet MAC
  - LCD panel controller (up to 1024H × 768V)
  - Two 10-bit ADCs and 10-bit DAC at 400ksps
  - Eight-channel General-Purpose DMA (GPDMA) controller
  - Motor Control PWM
  - Quadrature Encoder Interface
  - 4x UARTs, 2x I2C, I2S, CAN 2.0B, 2x SSP/SPI
  - Smart card interface
  - Up to 80 general purpose I/O pins



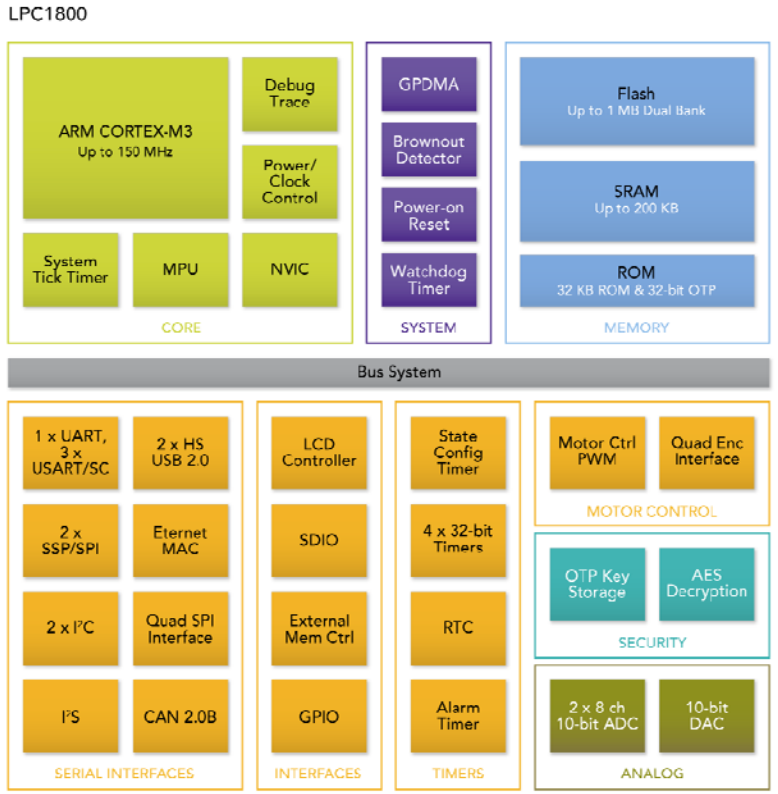
LPC4300


Advance Information
ARM CORTEX-M4
Floating Point Unit
Debug Trace
Power/ Clock Control
System Tick Timer
MPU
NVIC
CORE
GPDMA
Brownout Detector
Power-on Reset
Watchdog Timer
SYSTEM
Flash
Up to 1 MB Dual Bank
SRAM
Up to 200 KB
ROM
32 KB ROM & 32-bit OTP
MEMORY
Cortex-M0
Shared Memory
SUBSYSTEM
Bus System
1 x UART, 3 x USART/SC
2 x HS USB 2.0
2 x SSP/SPI
Eternet MAC
2 x I²C
Quad SPI Interface
I²S
CAN 2.0B
SERIAL INTERFACES
LCD Controller
SDIO
External Mem Ctrl
GPIO
SGPIO
INTERFACES
State Config Timer
4 x 32-bit Timers
RTC
Alarm Timer
TIMERS
Motor Ctrl PWM
Quad Enc Interface
MOTOR CONTROL
OTP Key Storage
AES Decryption
SECURITY
2 x 8 ch 10-bit ADC
10-bit DAC
ANALOG

Code Compatible



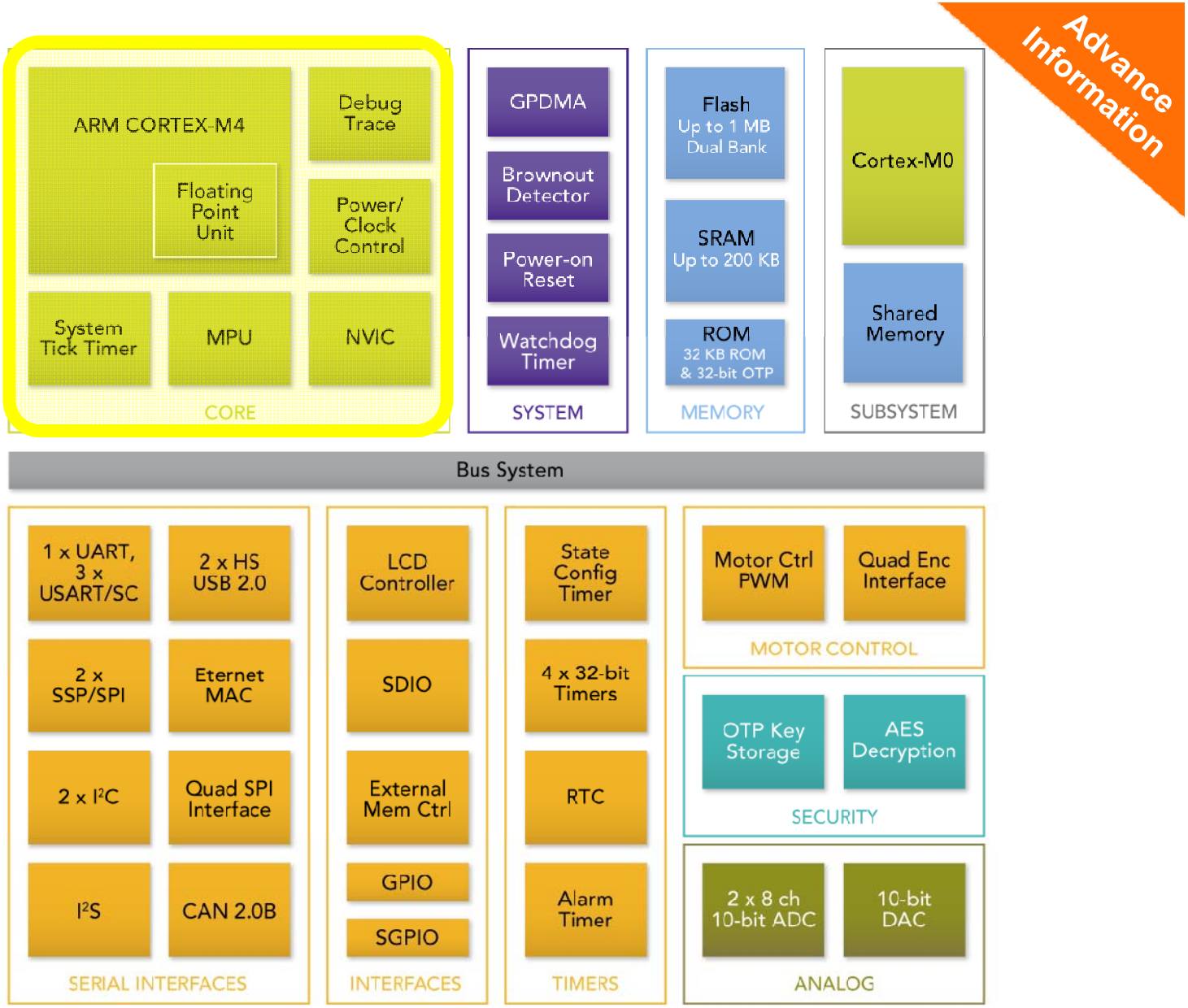
LPC4300 Cortex-M4



LPC1800 Cortex-M3

LPC4300

Cortex-M4

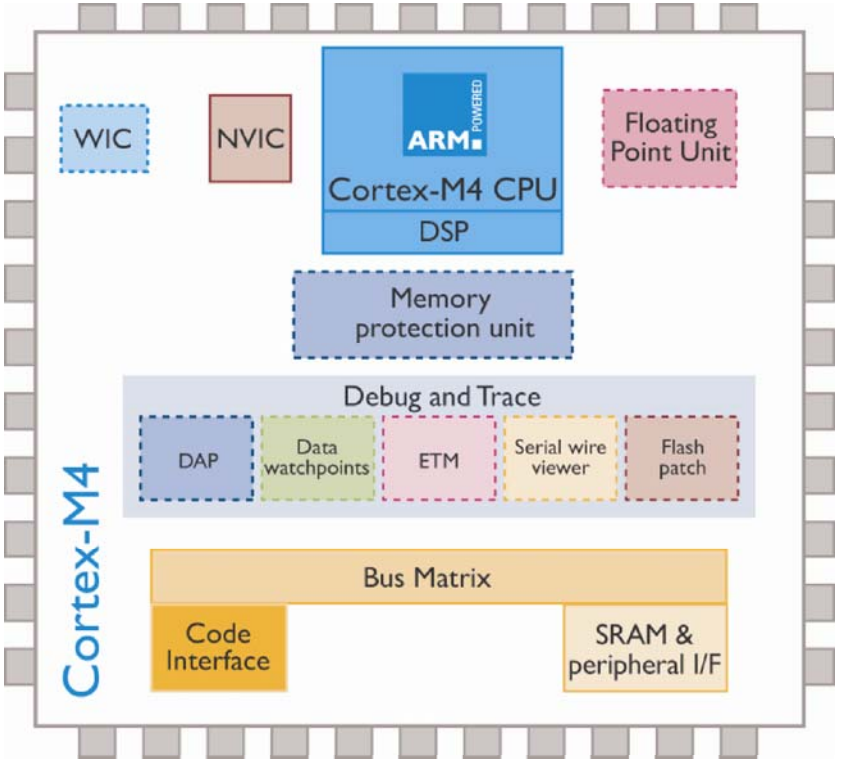


Microcontroller Core – CPU

Advance Information

LPC4000 Family Cortex-M4 Features:

- NVIC & WIC
  - Supports peripheral interrupts
- MPU (Memory Protection Unit)
  - Supports up to 8 regions
- FPU (Floating Point Unit)
  - IEEE 754 compliant
- Full Debug Options:
  - JTAG/SWD
  - ETM
  - Flash Patch
- 150MHz Execution
  - Flash or SRAM

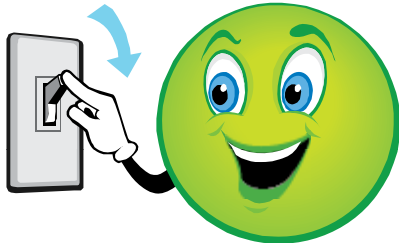


NXP's low-leakage 90nm process technology allows operation at up to 150MHz

Microcontroller Core – Power Control

Advance Information

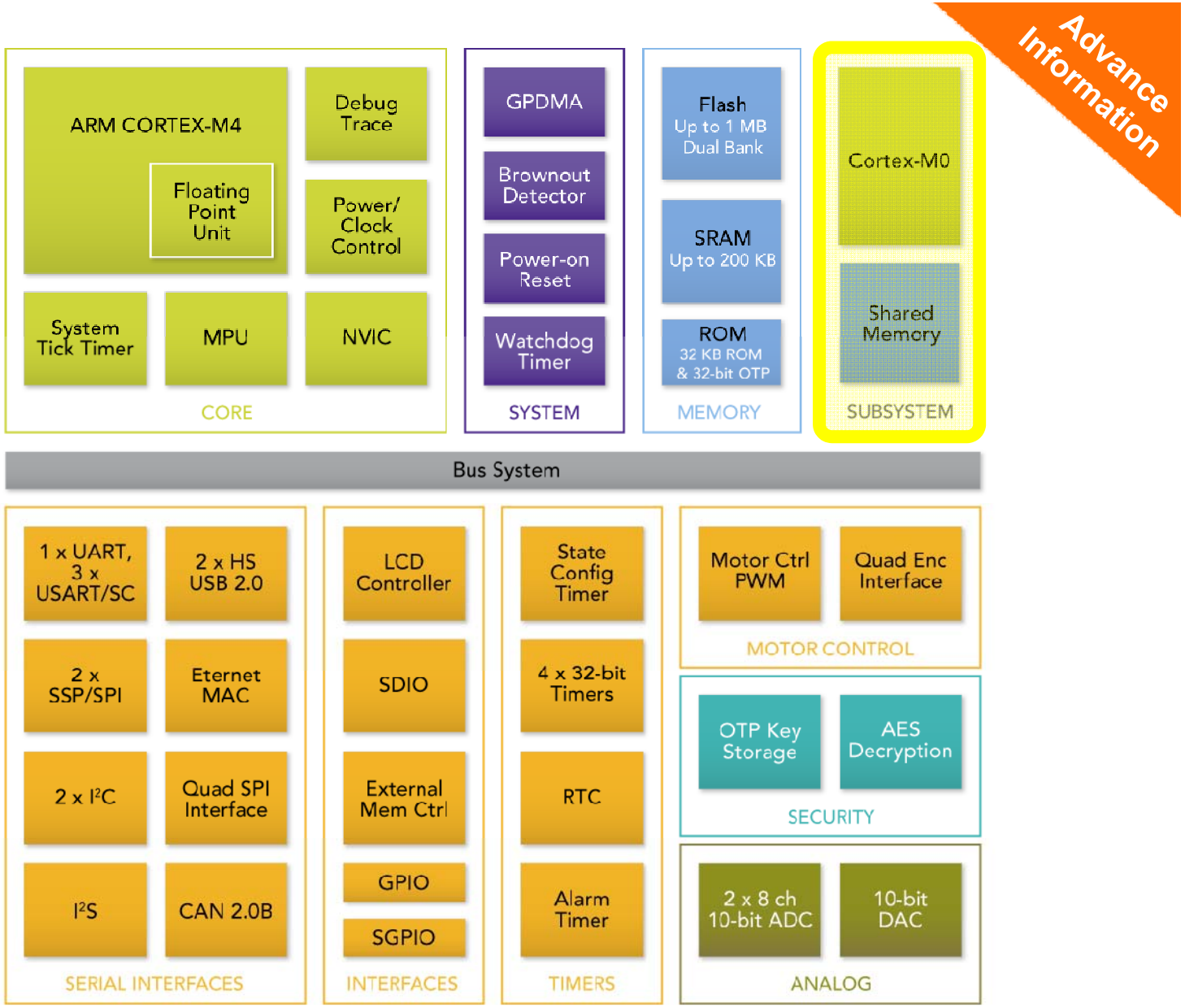
- **Flexible clock generation unit:**
  - Allows clock to each peripheral to be configured independently.
    - Can use different source and create different frequencies.
    - Unused peripherals can be turned off by disabling the clock.
- **Low power modes:**
  - **Sleep:**
    - CPU execution is suspended but peripherals continue



  - **Deep-Sleep**
    - Main oscillator and all internal clocks except the IRC are stopped Flash memory is in standby, ready for immediate use
  - **Power-down**
    - Same as Deep-Sleep mode except Flash and IRC are shut down, state is preserved
  - **Deep power-down**
    - All clocks including IRC are stopped. Internal voltage is turned off
    - Complete system state is lost, special registers in the RTC domain are preserved
    - Wake up via reset, external pin, or RTC Alarm

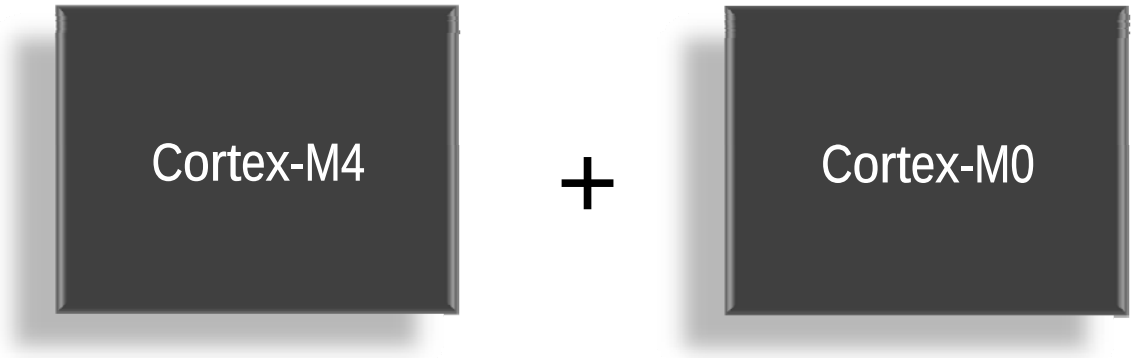
LPC4300

Cortex-M0 Subsystem



Cortex-M0 Subsystem - Overview

Advance Information



= LPC4300

Processing Application

Audio/Image Processing

Control Algorithm

+

Real Time Control

Peripheral Control

Protocol Emulation

= Solution!

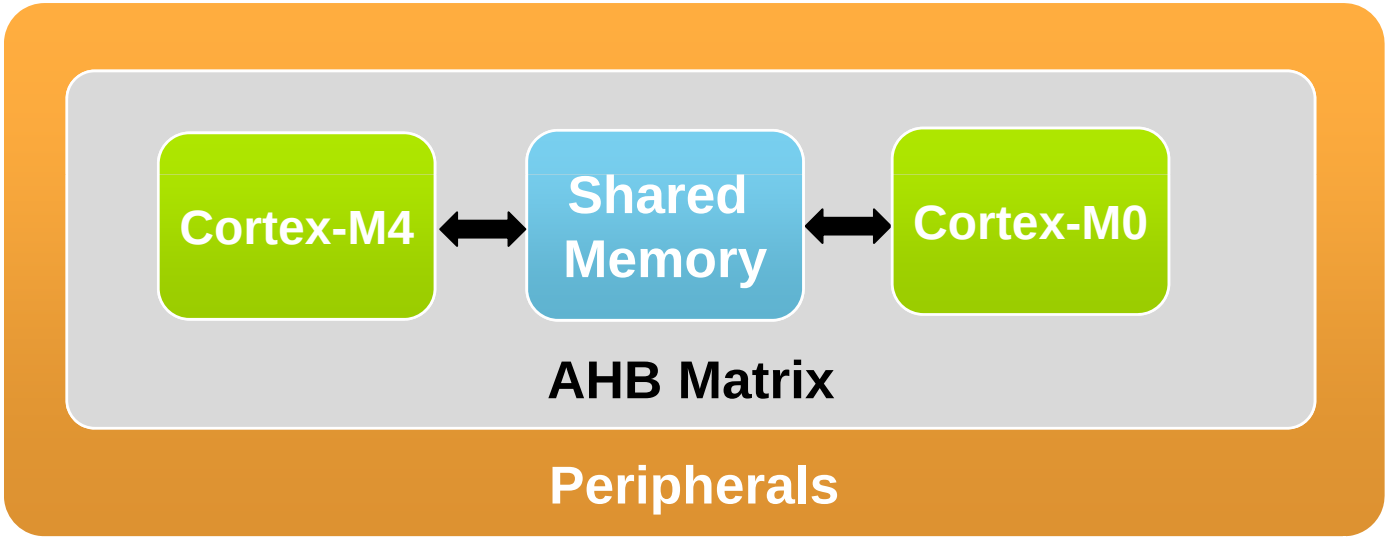
Cortex-M0 subsystem - unburdens the main Cortex-M4 core!

Separates Processing and Real Time Control – in one chip

Cortex-M0 Subsystem - Overview

Advance Information

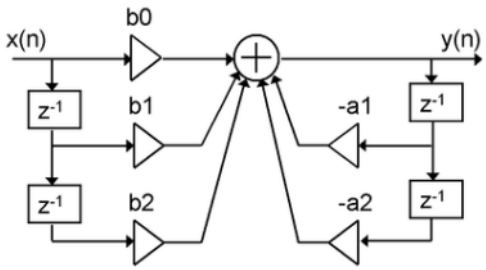
- Highly flexible Cortex-M0 subsystem features
  - Connected to the internal bus matrix giving access to all peripherals.
  - NVIC for dedicated interrupt support.
  - Separate clock and power control
  - Shared memory allows easy inter-processor communication

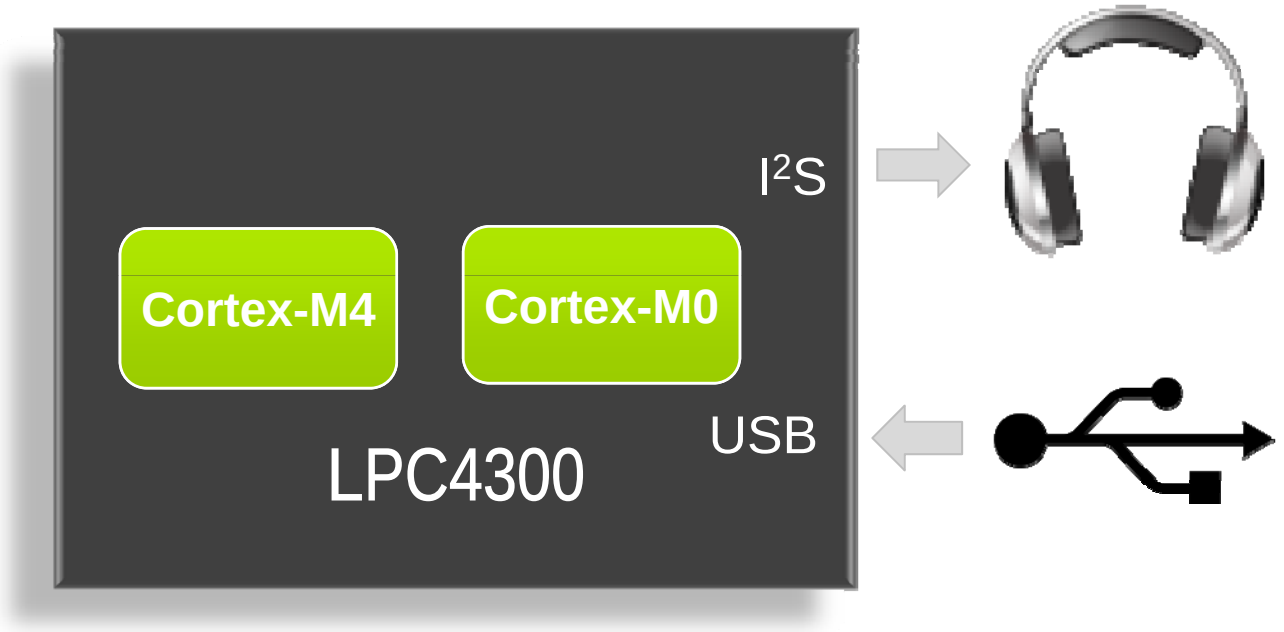


Cortex-M0 Subsystem – Audio Processing

Advance Information

- **Cortex-M4:** Full power devoted to Audio processing
- **Cortex-M0:** Handles the hardware control – I²S & USB

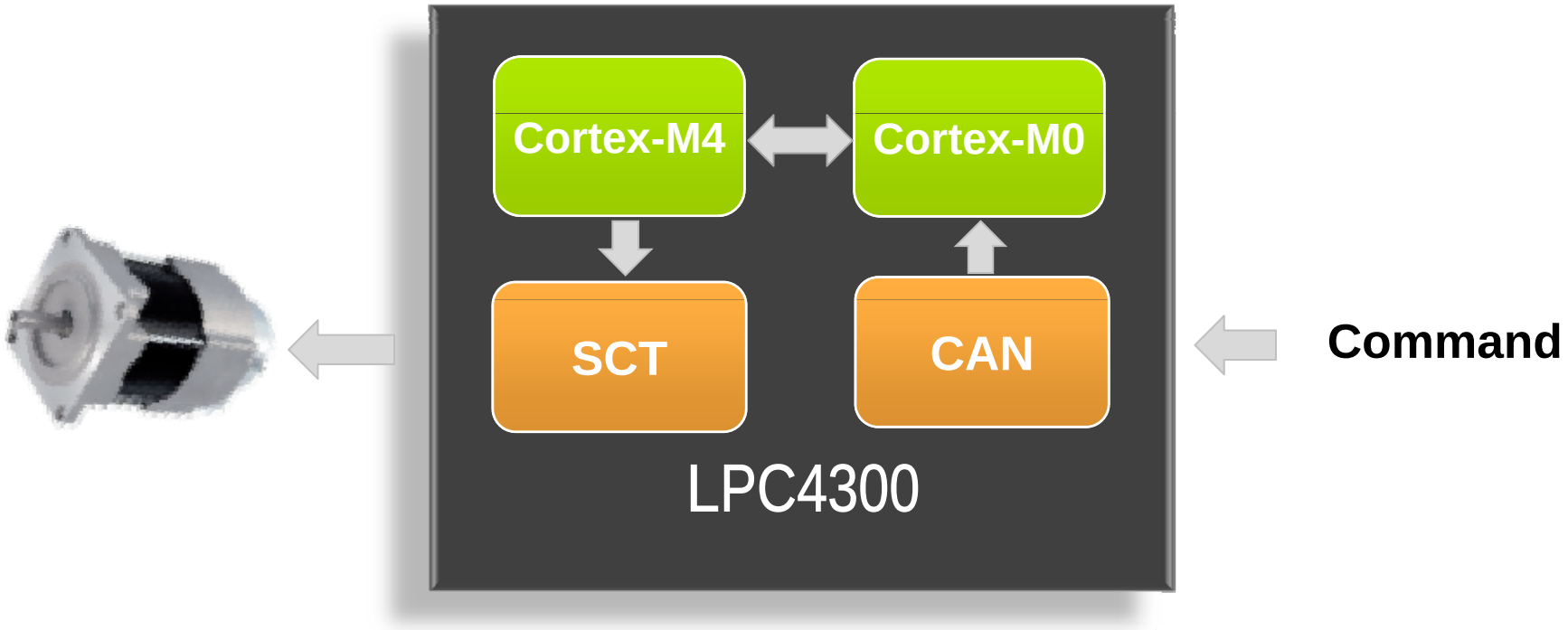




Cortex-M0 Subsystem – Motor Control

Advance Information

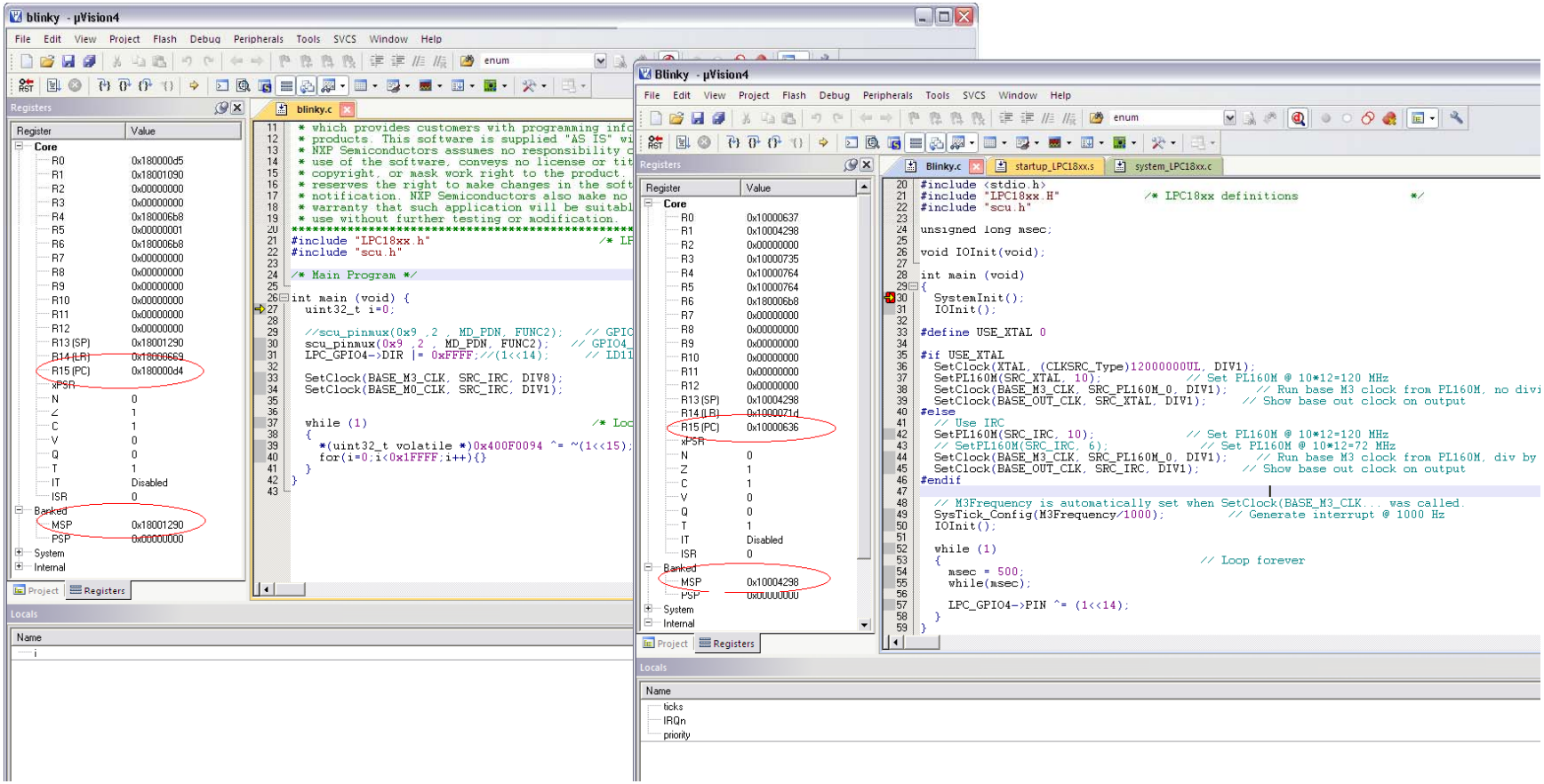
- **Cortex-M4:** Single shunt Field Oriented Control (FOC)
- **Cortex-M0:** Receives control commands via CAN interface



Cortex-M0 Subsystem - Development

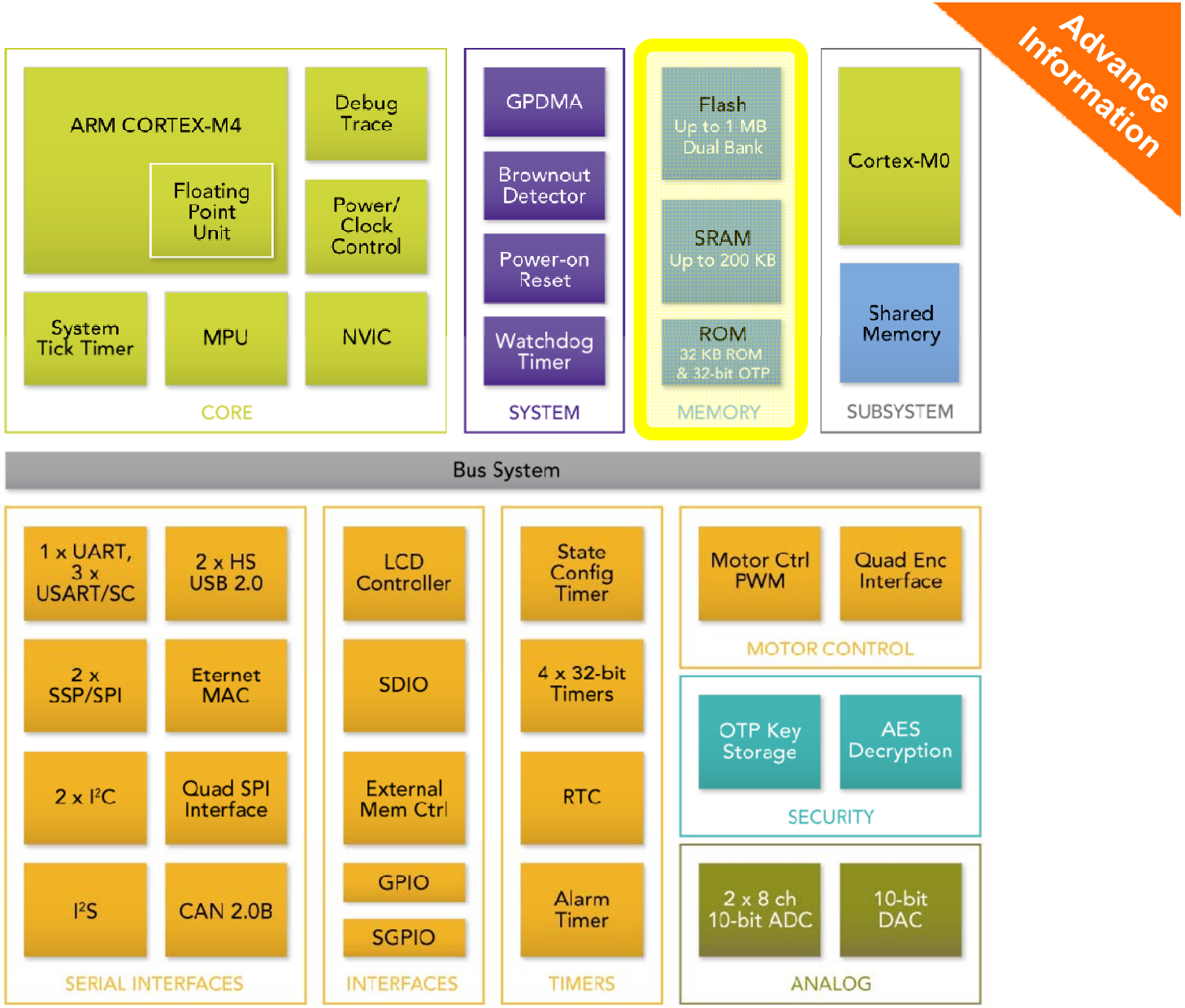
Advance Information

Cortex-M4 and Cortex-M0 share a debug interface allowing a single JTAG/SWD unit to debug both cores



LPC4300

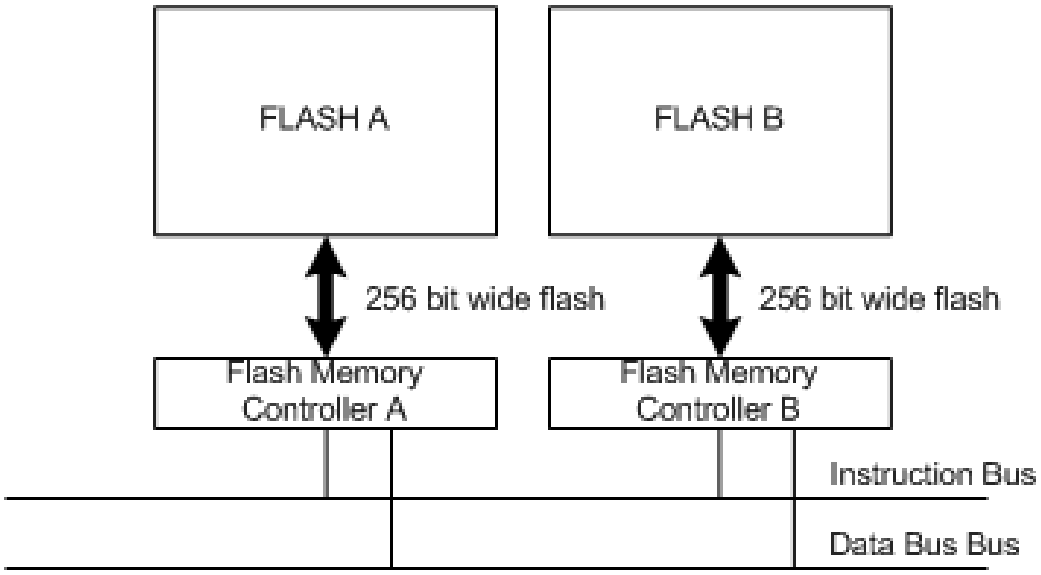
Memory

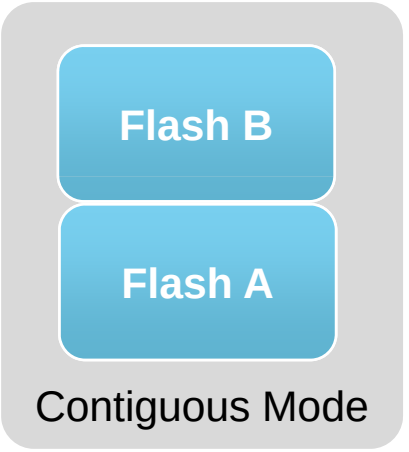


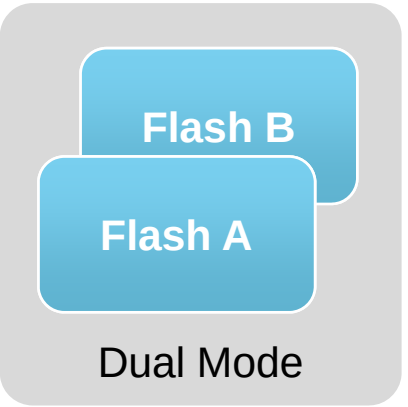
Memory - Dual Bank Flash

Advance Information

- Two 512K byte banks of flash memory.
- Can be used as a single 1M byte memory area.
- Enhanced memory controller and 256-bit wide interface allows operation at up to 150MHz.



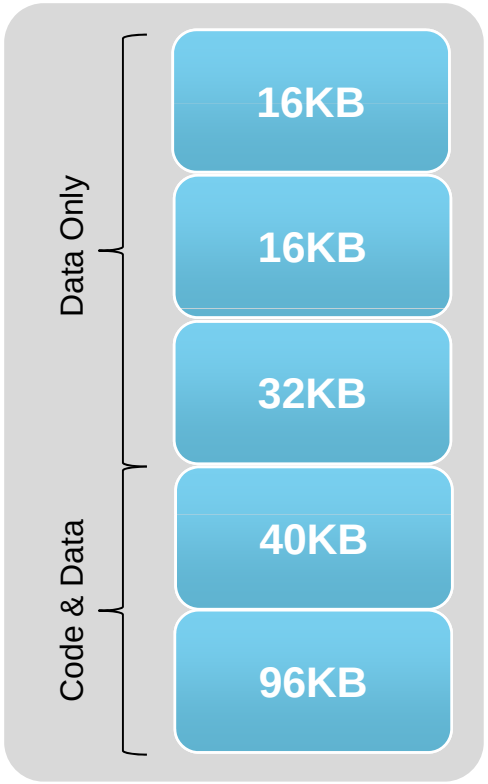




Memory - SRAM

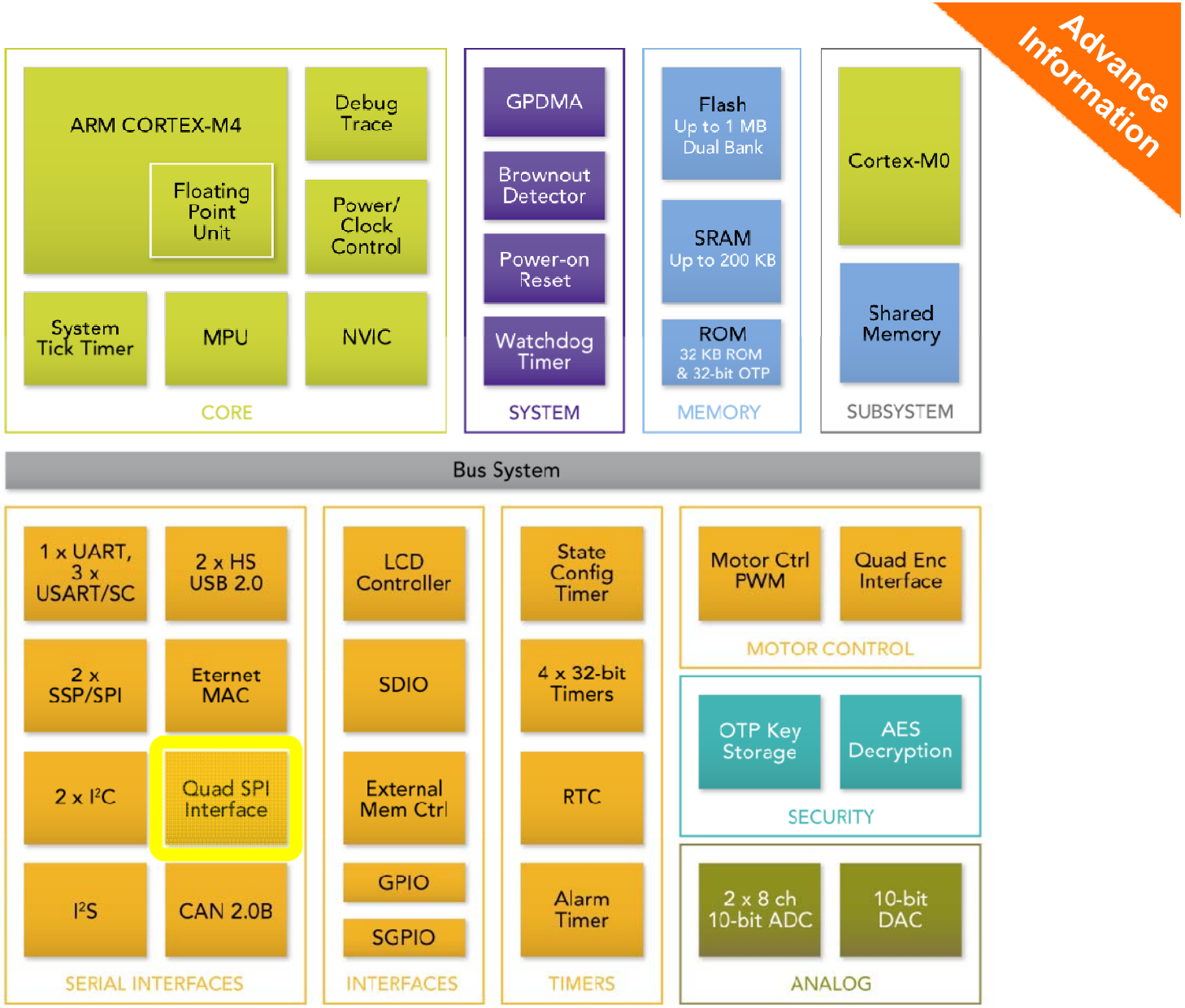
Advance Information

- Up to 200KB static RAM available.
- Optimized for DSP use - 96kB and 40kB SRAM blocks accessible by high speed system bus can be used for code and data storage.
- 32kB and 16kB SRAM blocks with separate bus interfaces.
- Block/bus architecture allows simultaneous CPU and DMA accesses to different SRAM areas.



LPC4300

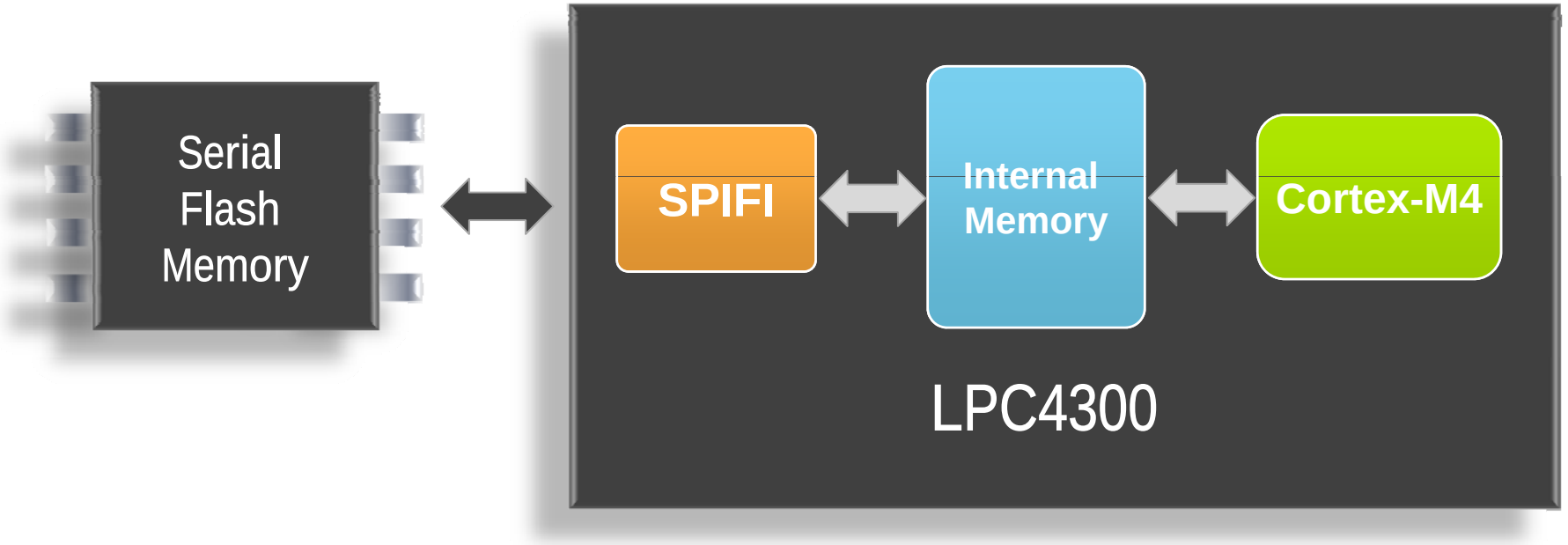
SPI Flash Interface



SPIFI - Overview

Advance Information

SPI Flash Interface



Patented feature that maps low-cost serial flash memories into the internal memory system.

SPIFI - Supported Devices

Advance Information

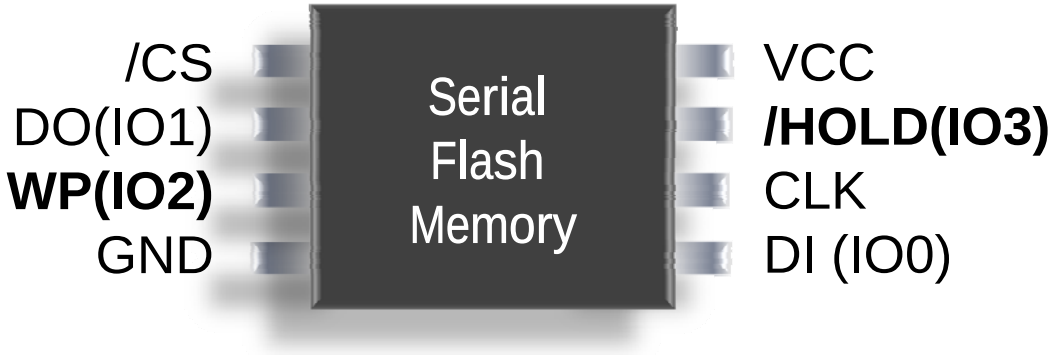
- Compatible with both standard and Quad SPI flash memory devices from a majority of suppliers:
  Atmel, Gigadevice, Macronix Numonyx (now Micron) SST (now Microchip), Winbond

- A couple of years ago, PCs started using Quad-SPI Flash for loading BIOS . The high PC volumes forced prices down to low levels
- Advantages: High speeds, small packages/few pins, low cost
- Disadvantages: Not supported by standard MCUs -- UNTIL NOW!
- NXP's patent-pending SPI Flash Interface (SPIFI) on the LPC4300 series is the first and only MCU to take full advantage of Quad SPI Flash

SPIFI - Quad SPI Flash Interface

Advance Information

- SPI Flash Interface uses either 4 or 6 lines
  - Standard SPI flash uses CLK, CS, MISO and MOSI
  - Quad SPI flash uses CLK, CS IO0, IO1, IO2 and IO3



SPIFI – Image Storage – Problem

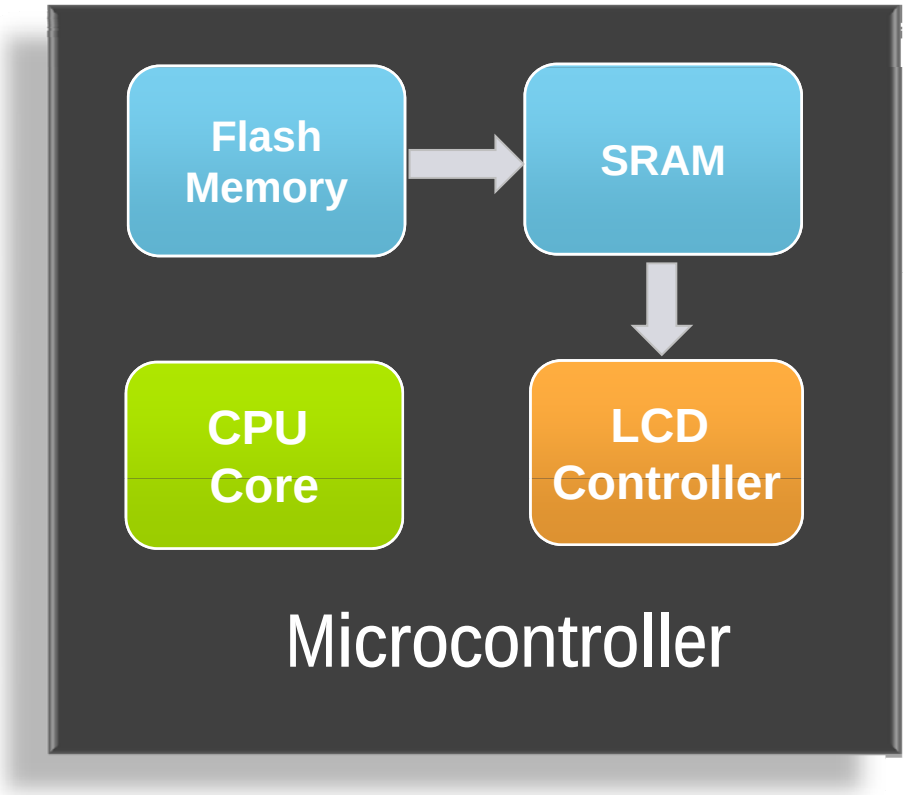


Image Storage: Problem

- Devices with complex user interfaces require storage for images that will be displayed on an LCD.
- Images can be stored in external SPI flash but usually have to be copied into internal SRAM and then sent to LCD controller.
- Problem with this approach is that it uses large amounts of internal SRAM

SPIFI – Image Storage – Solution

Advance Information

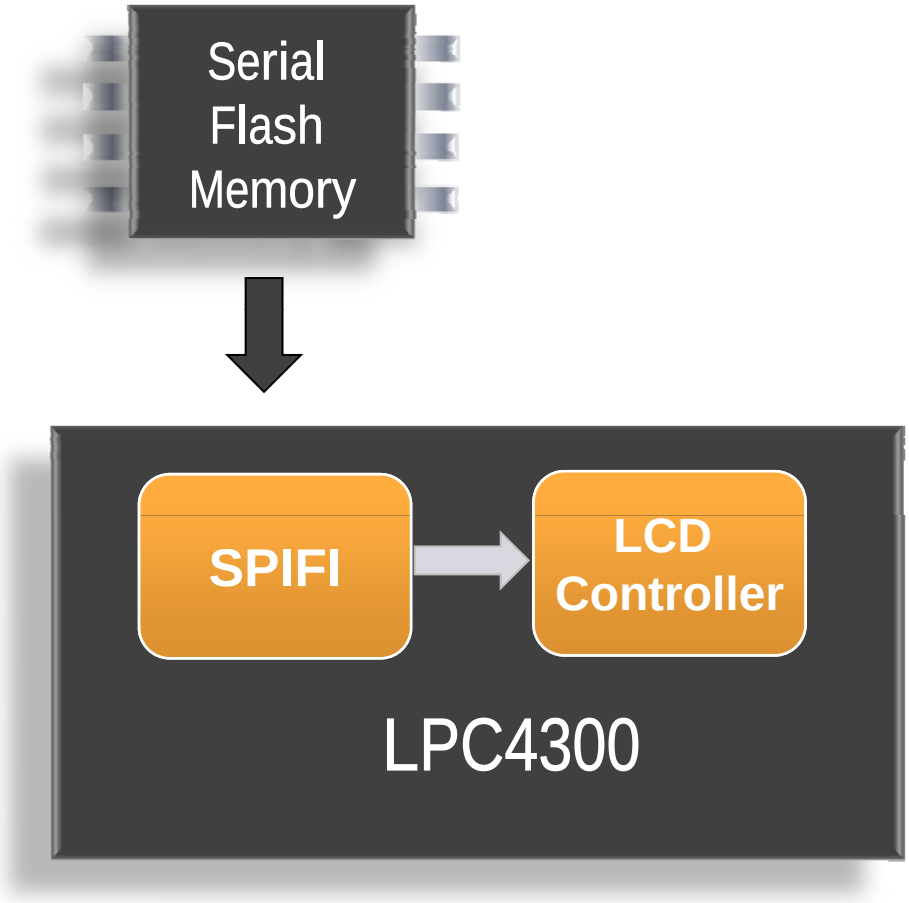
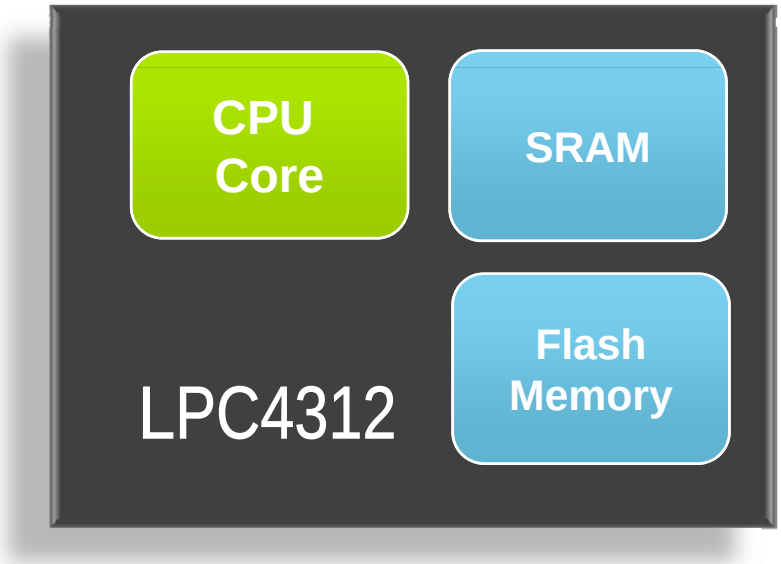


Image Storage: SPIFI Solution

- Image stored within external serial flash memory
- High speed quad SPI interface allows images to be transferred directly to LCD controller using DMA
- **Advantages of a SPIFI based solution:**
  - Does not use precious internal SRAM – available for other uses.

SPIFI - DSP Algorithm: Problem

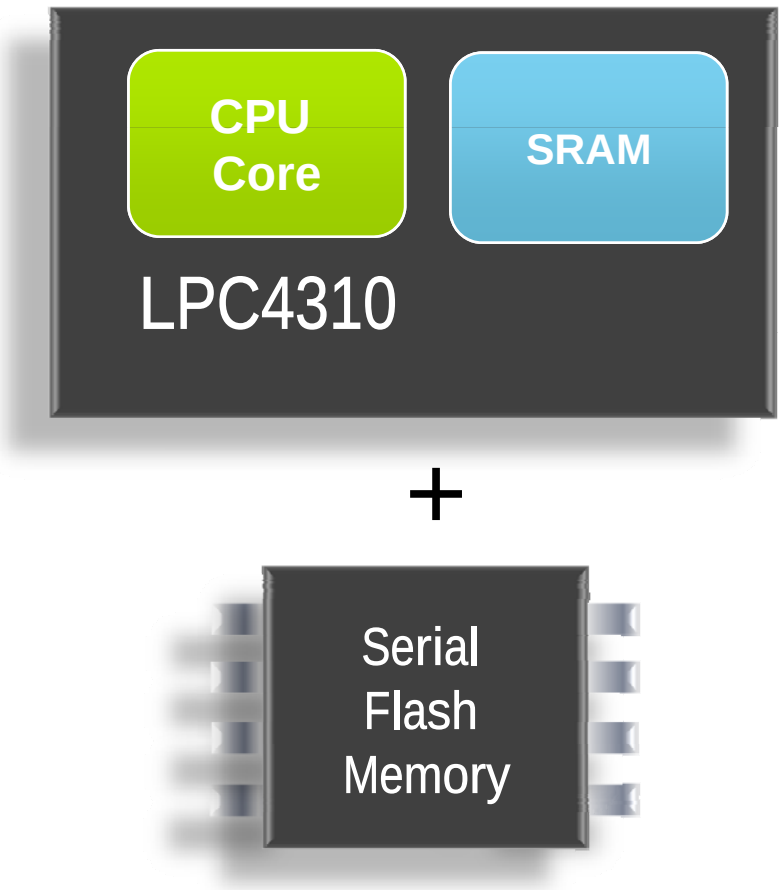
Advance Information



- DSP applications are often loaded from flash into internal SRAM for high performance execution.
- These algorithms are stored within internal or external parallel memory
- **Problems with this approach:**
  - Have to add space consuming external flash memory to board OR
  - Have to sacrifice precious internal flash memory for algorithm storage

SPIFI - DSP Algorithm: Solution

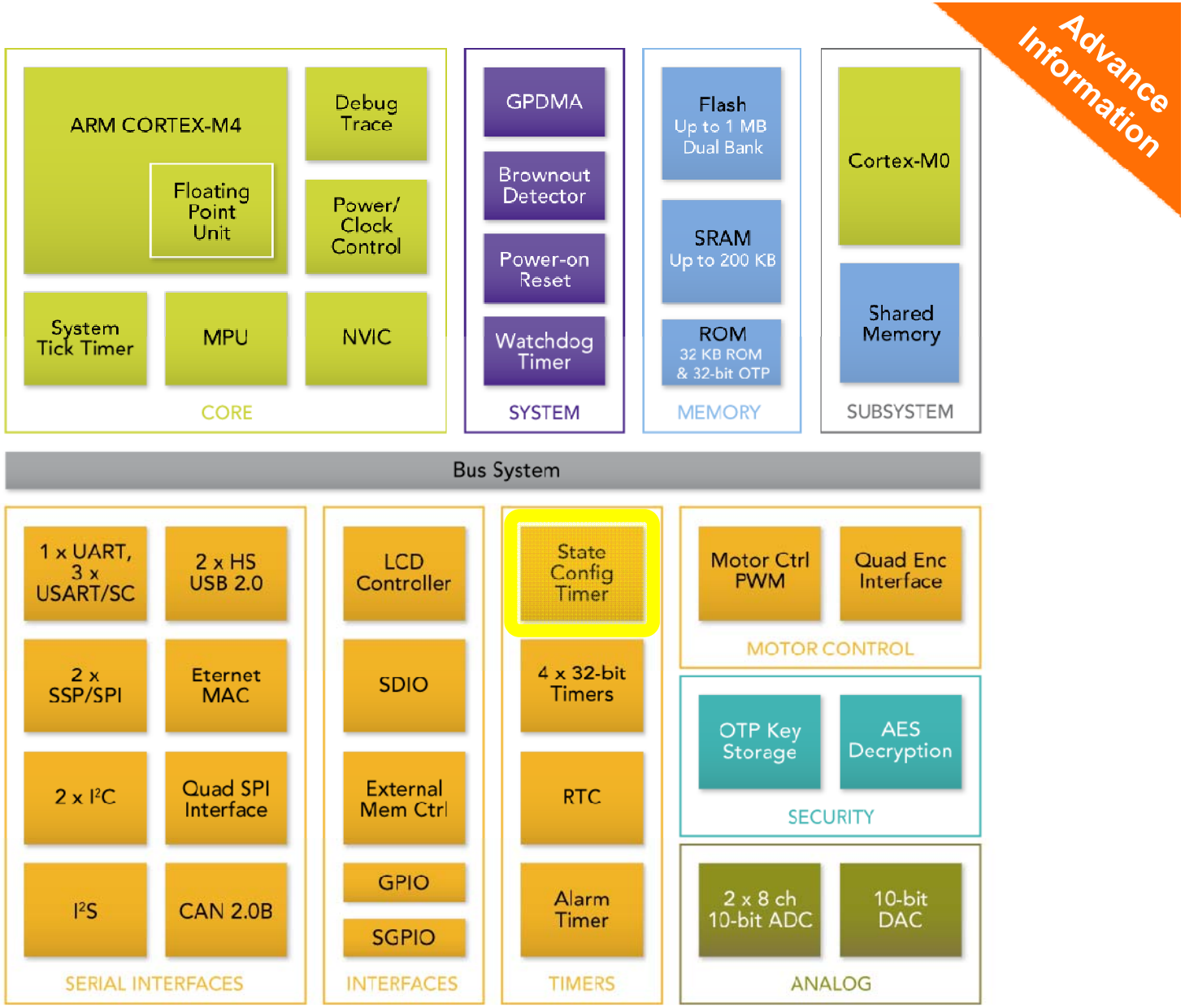
Advance Information



- Store DSP algorithm in low cost external serial flash memory.
- Loaded into dedicated internal SRAM block for high speed execution.
- **Advantages of a SPIFI based solution:**
  - Low cost external SPI flash memory consumes minimal board space.
  - No waste of precious internal flash memory for code that is always executed from SRAM

LPC4300

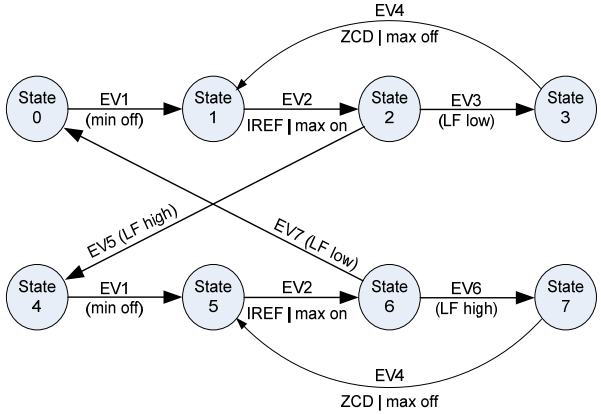
State Configurable Timer Subsystem



SCT - Overview

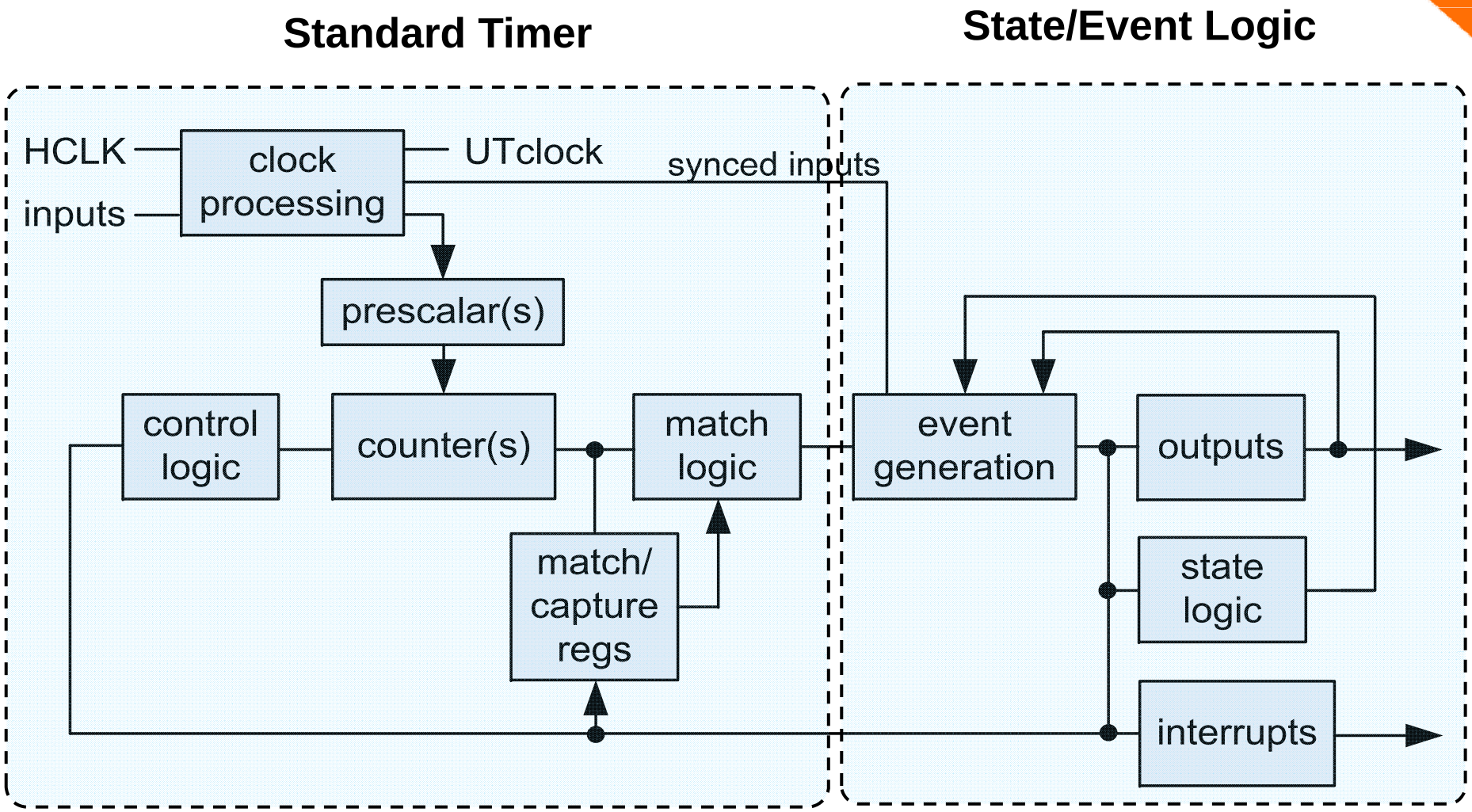
Advance Information

- State Configurable Timer (SCT) is a timer/capture unit coupled with a highly flexible event driven state machine block.
- Allows a wide variety of timing, counting, output modulation, and input capture operations.
- Key Features:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states



SCT - Operation

Advance Information



SCT - Example Application

Advance Information

Simple traffic light:

Car lane red signal

Pedestrian red signal

Car lane yellow signal

Pedestrian green signal

Car lane green signal

Button to request
Car traffic stop

SCT - Example Application

- Four different allowed combinations (states) of the two display entities
- One external input (the button)
- Five outputs

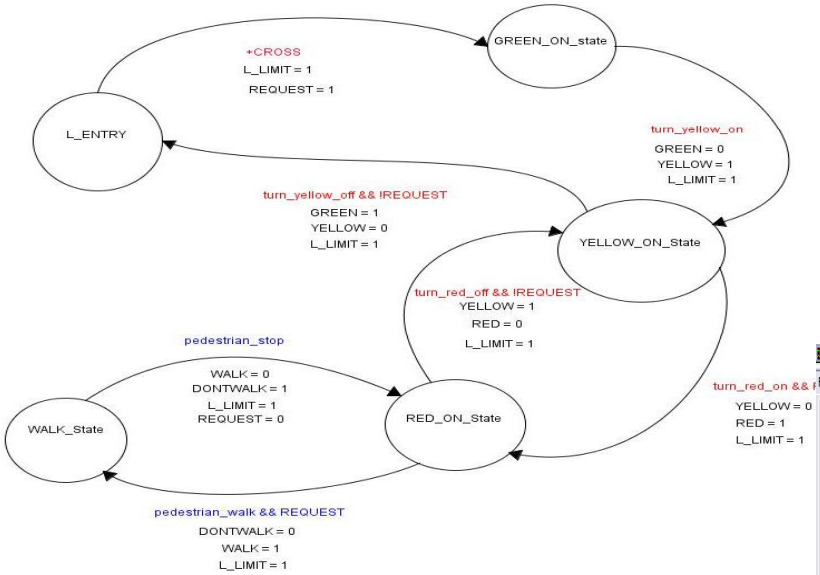
#	Car lane lights	Pedestrian lane lights
1	Green	Red
2	Yellow	Red
3	Red	Red
4	Red	Green

SCT allows a this application to be implemented in hardware!

SCT – Easy to use

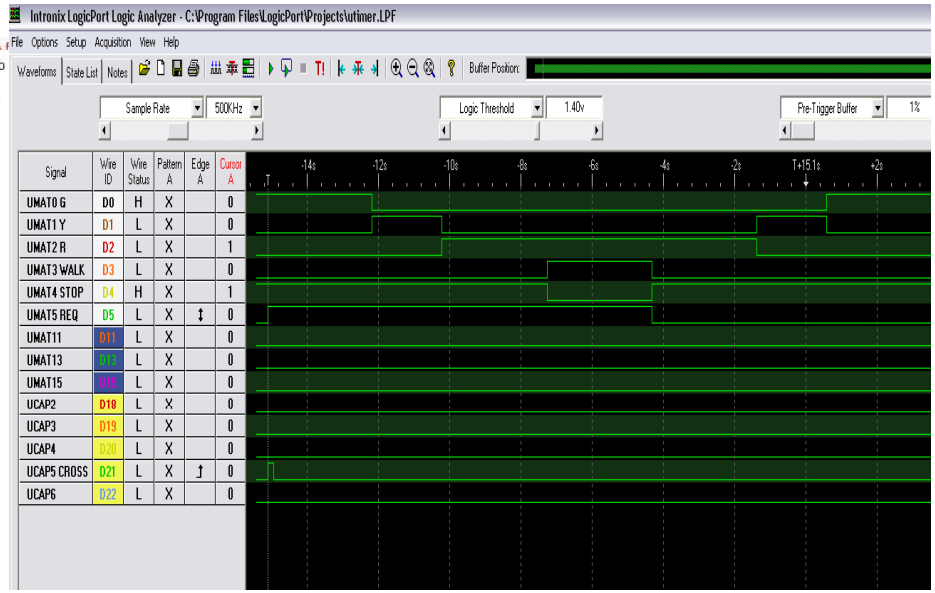
Advance Information

1. Design the state machine



Library of examples will be available!

3. Let the SCT do the work!

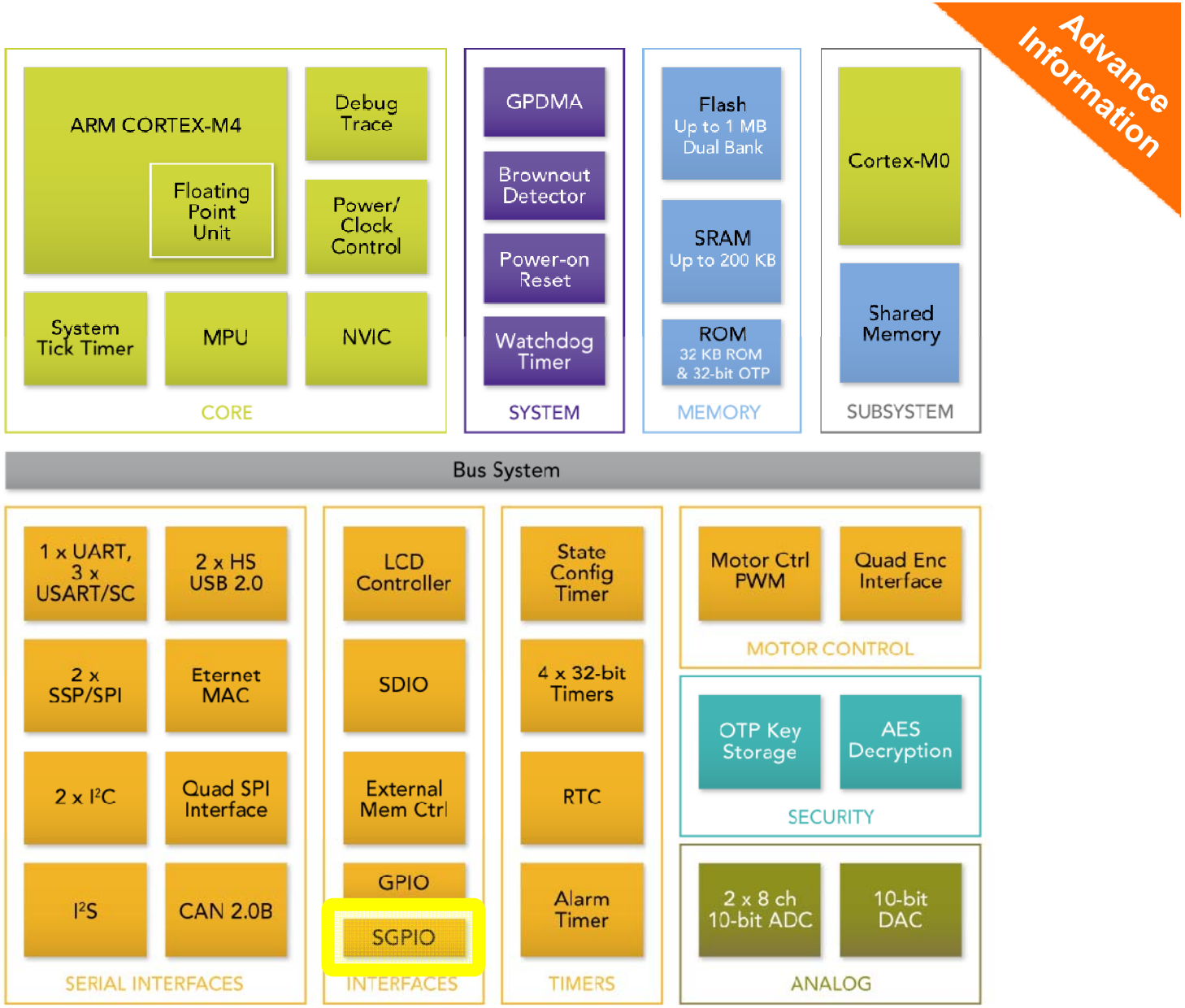


2. Set the registers/timer

```
LPC_SCT->CTRL |= (1UL << 7);
LPC_SCT->TIM   = 0x4534;
LPC_SCT->ENB  &= 0x8001;
```

LPC4300

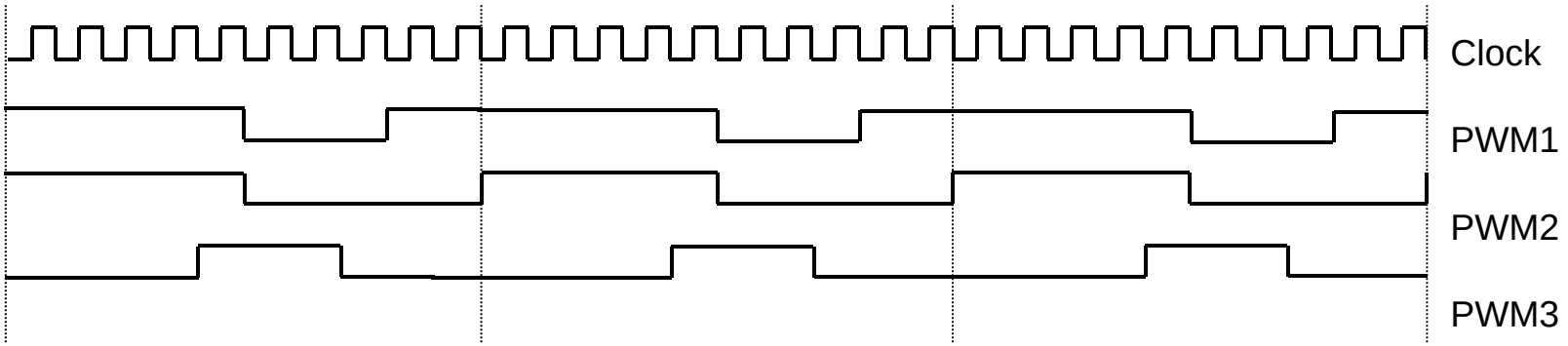
Serial
GPIO



SGPIO - Overview

Advance Information

- Serial GPIO (SGPIO) = GPIO + Timer/Shift Register:
  - Used to create or captures multiple real time serial data streams.
  - No more having to write code loops to manipulate GPIO in real time.
  - Say goodbye to CPU intensive big banging!
- Key Features:
  - Up to 8 inputs/outputs each with their own timer/shift register unit.
  - Counter to control the rate at which data is clocked in/out.
  - Counter to control the number of bits clocked out/in.
  - Output has three states high, low, or high impedance.

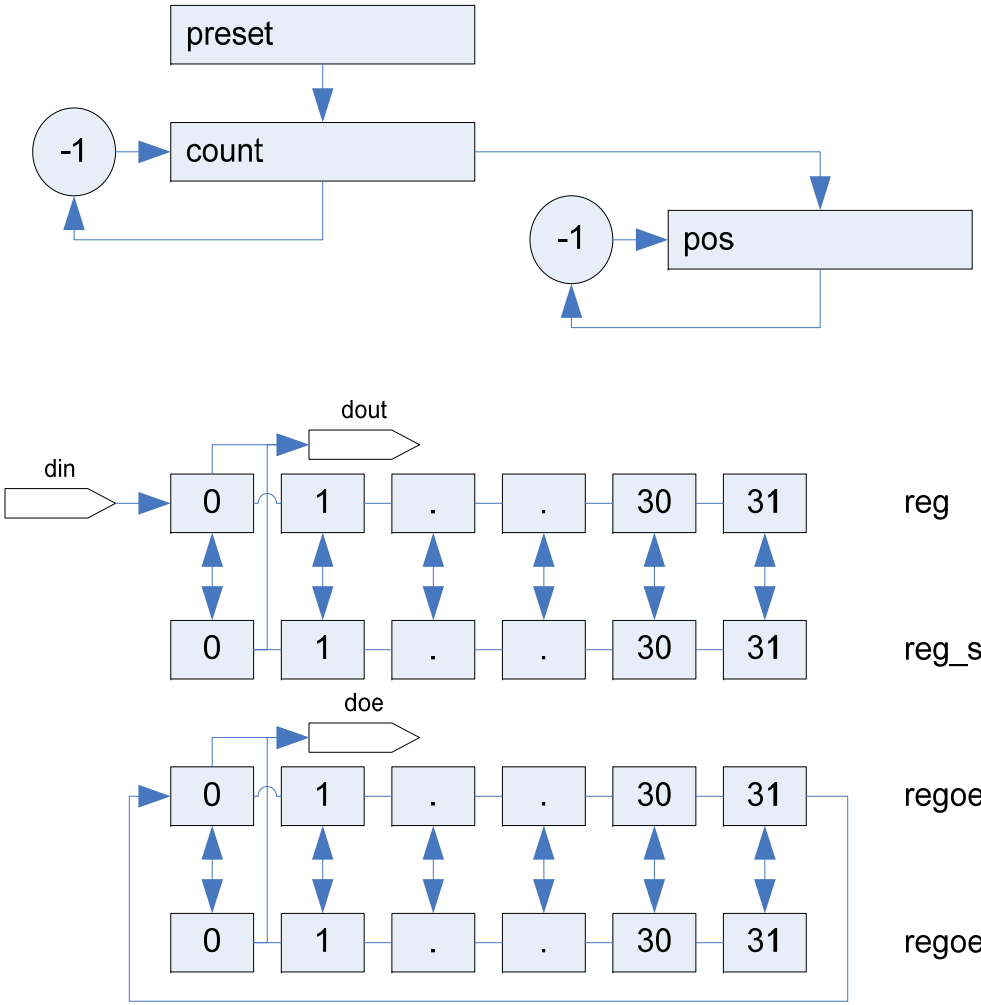


SGPIO - Operation

Advance Information

Each SGPIO unit features:

- Two 32-bit shift registers
- Counter to control bit rate
- Counter to control number of bits clocked out/in
- Register controls the state (enable/disable) of the output for each bit that is clocked out.



SGPIO = Proprietary Serial Interface

Advance Information

SGPIO can be used to emulate proprietary serial interfaces

- **Problem:** Lots of peripherals on the market use **non-standard serial interfaces** (LCD drivers, audio codec etc).
- **Standard Microcontroller Solution (no SGPIO):**
  - Application designer has to write CPU intensive loops to create required bit streams – painful bit banging!
  - CPU is 100% occupied while waveform(s) are generated.
- **LPC4300 based Solution:**
  - Configure SGPIO to generate desired waveform(s) with just a few register writes.
  - Interrupt generated when data is clocked out – CPU is not blocked.

SGPIO = Standard Serial Interface

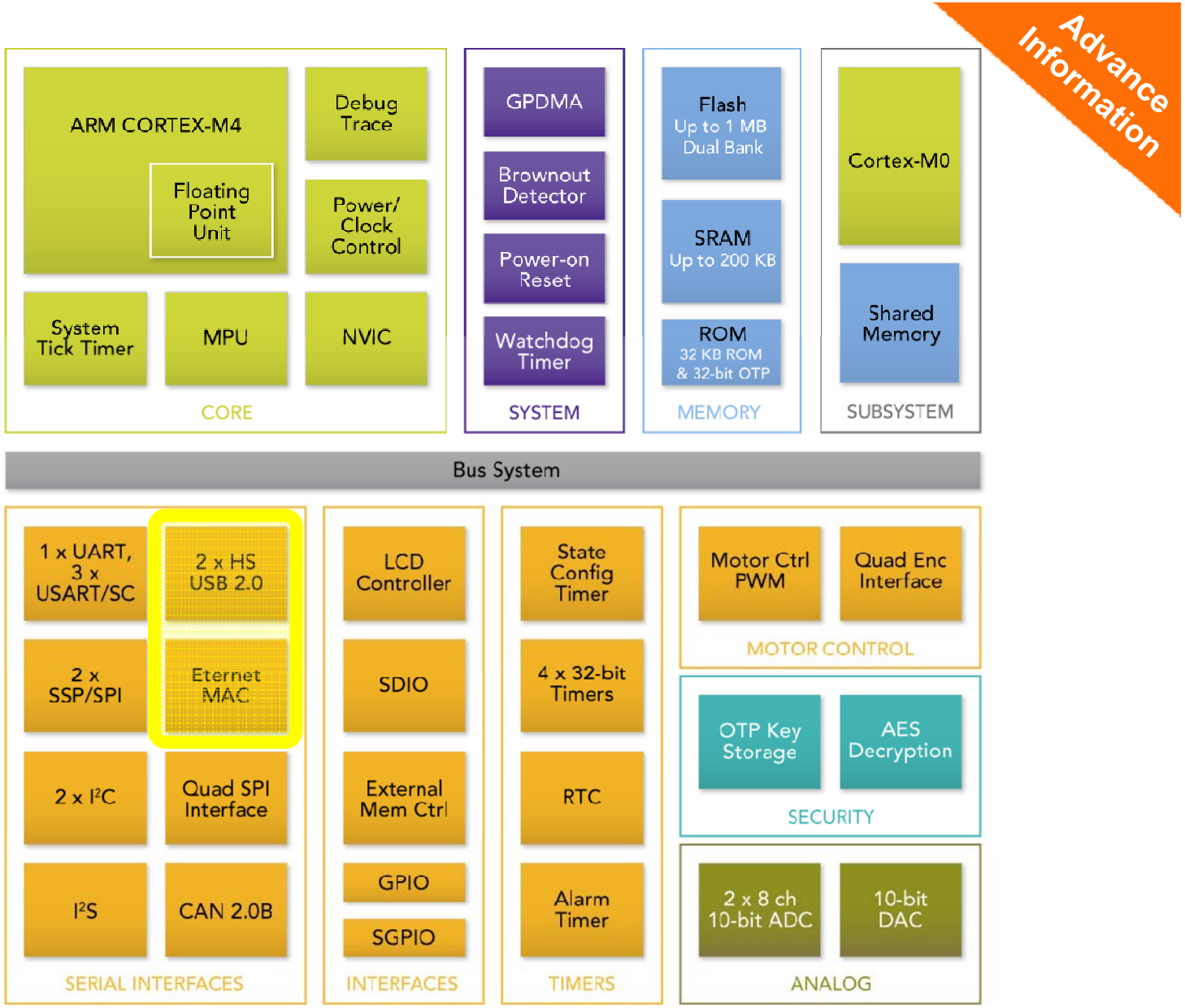
Advance Information

- To create a 7.1 channel I²S output 5 SGPIO units are required:
  - 4x I2S Data for 7.1 channels
  - 1x I2S WS
- Data is shifted out at 2M.fs, M=data word length, fs=sampling rate
- For 32bit data and fs = 96kHz the shift clock = 2.32.96k = 6.144 MHz
- The I²S data shift register should be loaded with the 32b audio samples. The CPU has to read SRAM and load the slices at a rate of 8x96k words/sec.
- The WS shift register should be loaded to create a 96kHz WS waveform.
- The I²S CLK does not need a dedicated shift register, it can be created from a shift counter output.
- CPU load: if an instruction takes 2 clk, SRAM access 2clk, SGPIO access 2clk then the CPU load is 6x8x96kHz, this is 3% load at a 150MHz clk rate

Create **I²S** OR **I²C** OR **SPI** OR…

LPC4300

USB 2.0
Ethernet



Interfaces – USB & Ethernet

Advance Information

- **Two USB 2.0 Interfaces:**
  - USB 2.0 Host/Device/OTG interfaces.
  - One with on-chip high-speed PHY.
  - One with on-chip full-speed PHY and ULPI interface for external high speed PHY

- **Ethernet MAC with RMII and MII interfaces to external transceiver:**
  - Supports 10/100 Mbit/s
  - TCP/IP hardware checksum
  - DMA support allows high throughput at low CPU load
  - IEEE 1588 advanced time stamp support.

Audio Application

Audio Design Example

Real-time Demo

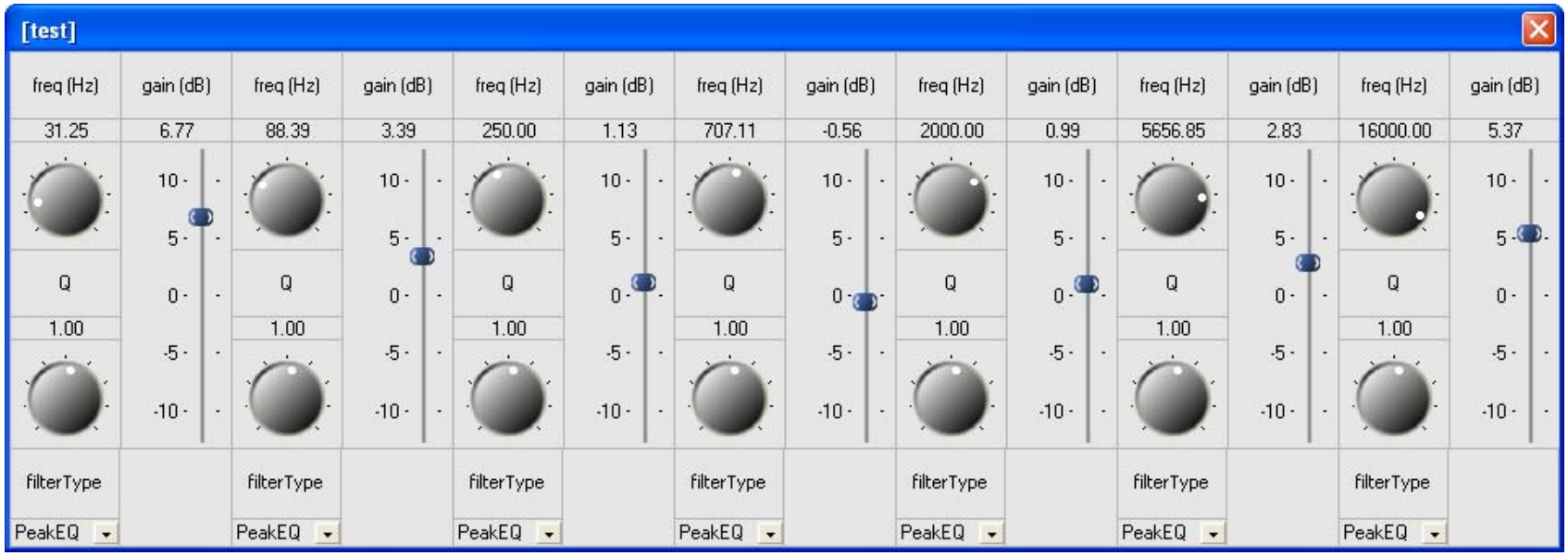
7 band parametric EQ

32-bit precision

Stereo processing

48 kHz sample rate

- 7-band Graphic Equalizer
  - Cortex-M3 LPC1768 running at 120MHz
  - Cortex-M4 running at 120MHz
- Designed using DSP Concept's Audio Weaver development environment
  - a graphical drag-and-drop design environment and a set of optimized audio processing libraries.



2nd order IIR Filter – AKA “Biquad”

Commonly used for control and audio filtering

Implemented using a difference equation.

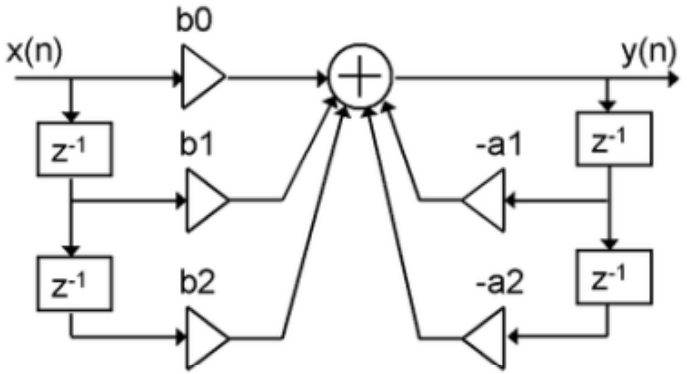
Direct Form 1 structure is the most numerically robust - shown below

Has 5 coefficients and 4 state variables

Coefficients determine the response of the filter (lowpass, highpass, etc.) and may be computed in a number of different ways

- Simple design equations running on the MCU
- External tools such as MATLAB

$$y[n] = b_0 x[n] + b_1 x[n-1] + b_2 x[n-2] - a_1 y[n-1] - a_2 y[n-2]$$



Cortex-M Biquad implementation

	Cortex-M3	Cortex-M4
`xN = *x++;`	2	2
`yN = xN * b0;`	3-7	1
`yN += xNm1 * b1;`	3-7	1
`yN += xNm2 * b2;`	3-7	1
`yN -= yNm1 * a1;`	3-7	1
`yN -= yNm2 * a2;`	3-7	1
`*y++ = yN;`	2	2
`xNm2 = xNm1;`	1	1
`xNm1 = xN;`	1	1
`yNm2 = yNm1;`	1	1
`yNm1 = yN;`	1	1
Decrement loop counter	1	1
Branch	2	2
	27-47 cycles	16 cycles

$$y[n] = b_0 x[n] + b_1 x[n-1] + b_2 x[n-2] - a_1 y[n-1] - a_2 y[n-2]$$

Cortex-M4 40-65% higher performance !

Only looking at the inner loop, making these assumptions

- Function operates on a block of samples
- Coefficients b0, b1, b2, a1, and a2 are in registers
- Previous states, x[n-1], x[n-2], y[n-1], and y[n-2] are in registers

Optimize by unrolling the loop by 3

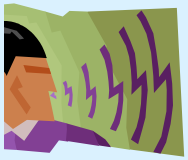
```
x0 = *x++;  (2 cycles)
y0 = x0 * b0;           (1 cycle)
y0 += x1 * b1;          (1 cycle)
y0 += x2 * b2;          (1 cycle)
y0 -= y1 * a1;          (1 cycle)
y0 -= y2 * a2;          (1 cycle)
*y++ = y0;  (2 cycles)

x2 = *x++;  (2 cycles)
y2 = x2 * b0;           (1 cycle)
y2 += x0 * b1;          (1 cycle)
y2 += x1 * b2;          (1 cycle)
y2 -= y0 * a1;          (1 cycle)
y2 -= y1 * a2;          (1 cycle)
*y++ = y2;  (2 cycles)

x1 = *x++;  (2 cycles)
y1 = x1 * b0;           (1 cycle)
y1 += x2 * b1;          (1 cycle)
y1 += x0 * b2;          (1 cycle)
y1 -= y2 * a1;          (1 cycle)
y1 -= y0 * a2;          (1 cycle)
*y++ = y1;  (2 cycles)

Decrement loop counter (1 cycle)
Branch                 (2 cycles)
```

- Reduces loop overhead
- Eliminates the need to shift down state variables
- 30 cycles on Cortex-M4 to for 3 output samples

  → 10 cycles per sample

Sampling / Nyquist

- Nyquist / Shannon Criteria
  - sampling frequency (Fs) must be at least twice the signal bandwidth, or information about the signal will be lost.

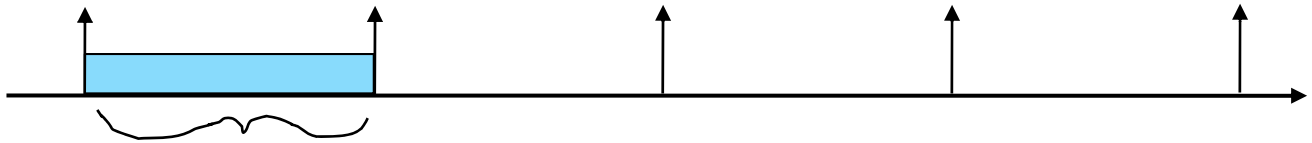
Type	Signal bandwidth	Typical Fs
Voice frequencies 	300 Hz to 3400 Hz	8 kHz
Audible frequencies 	20 to 20,000 Hz*	44.1 kHz 48 kHz

* < 20 Hz often felt rather than heard
>20,000 Hz sometimes sensed by younger people

Real Time Processing

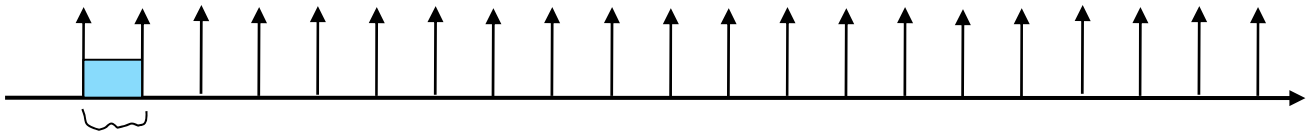
- DSC bandwidth limited by sampling rate
  - Available clock cycles = processor speed / sampling rate

Telephony
Fs = 8kHz



125 μsec => 120 MHz / 8 kHz => 15,000 clock cycles

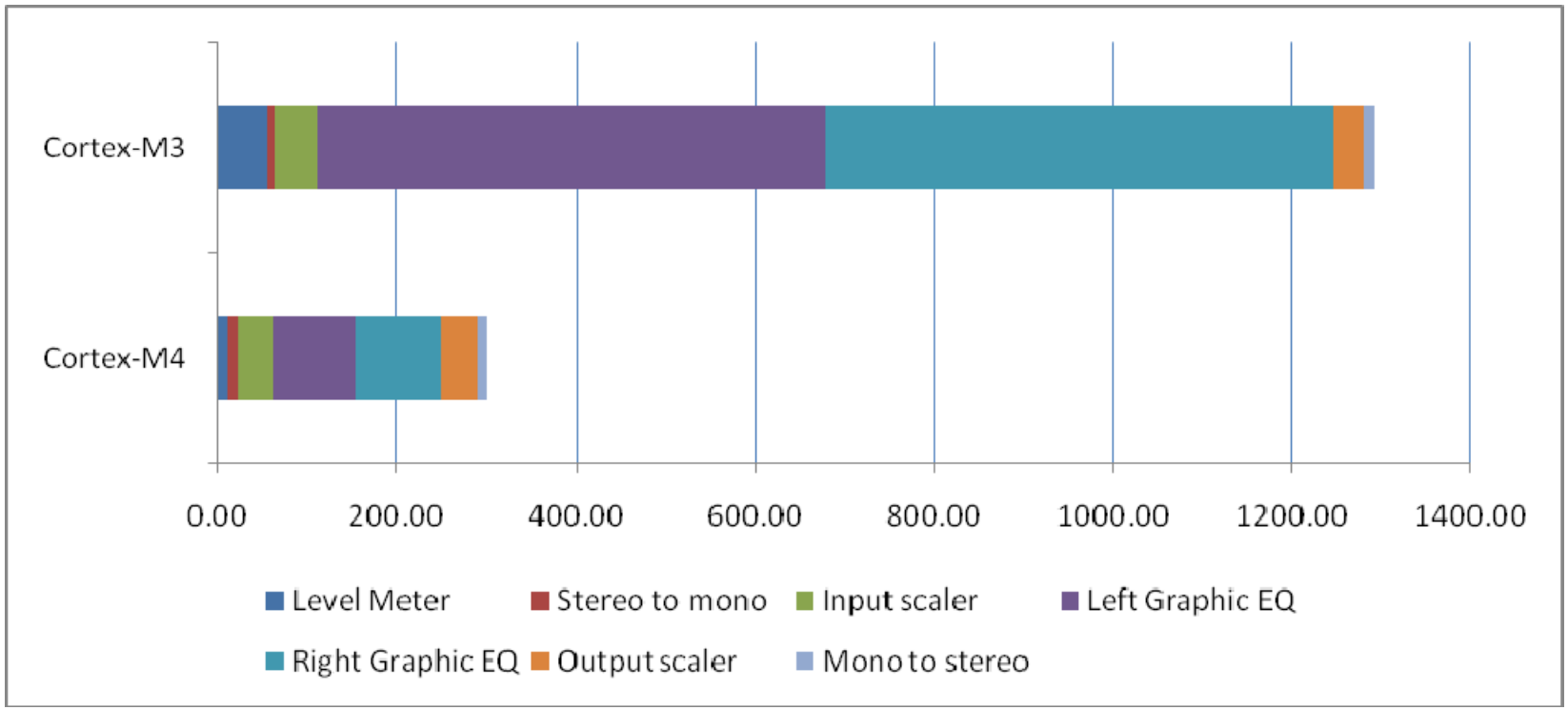
Audio
Fs = 44.1kHz



22.7 μsec => 120MHz / 48kHz => 2,500 clock cycles

Filtering examples. FFTs use block processing. (Processing time = sample interval x N)

Results



Performance

Cortex-M3 needed 1291 cycles (51.6% processor loading)

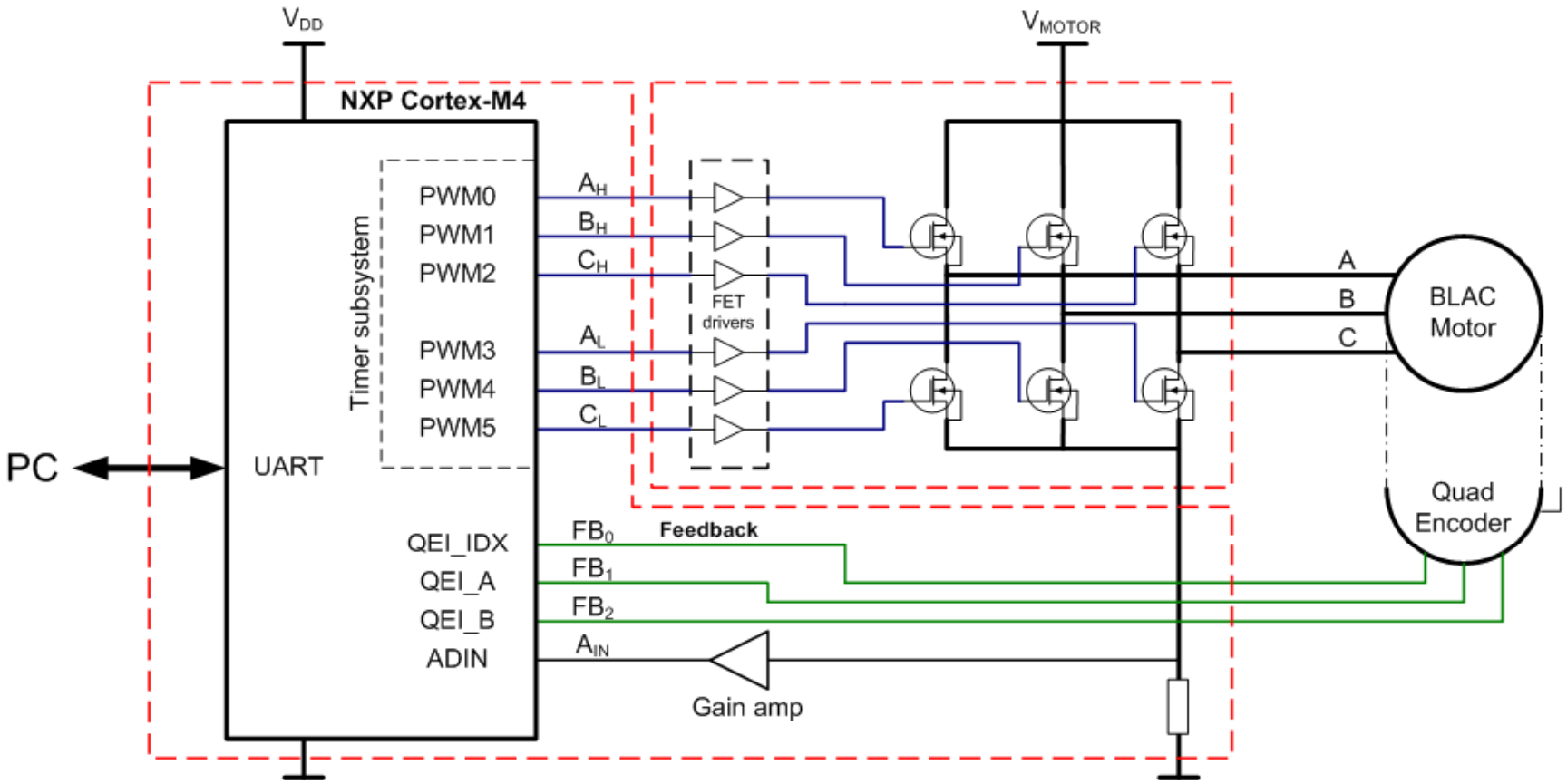
Cortex-M4 needed only 299 cycles (12% processor loading).

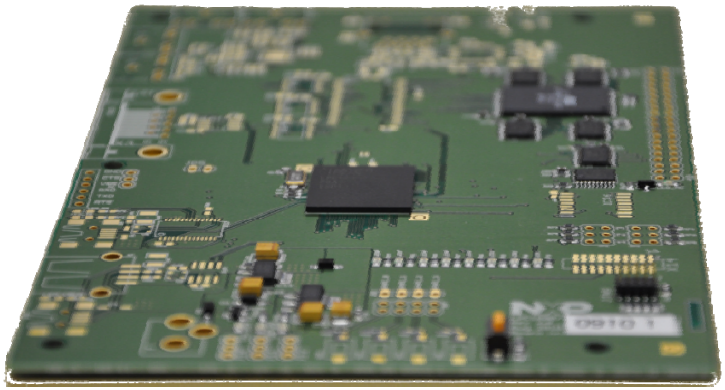
Motor Control Application

NXP's Cortex M4 Motor control EXAMPLE

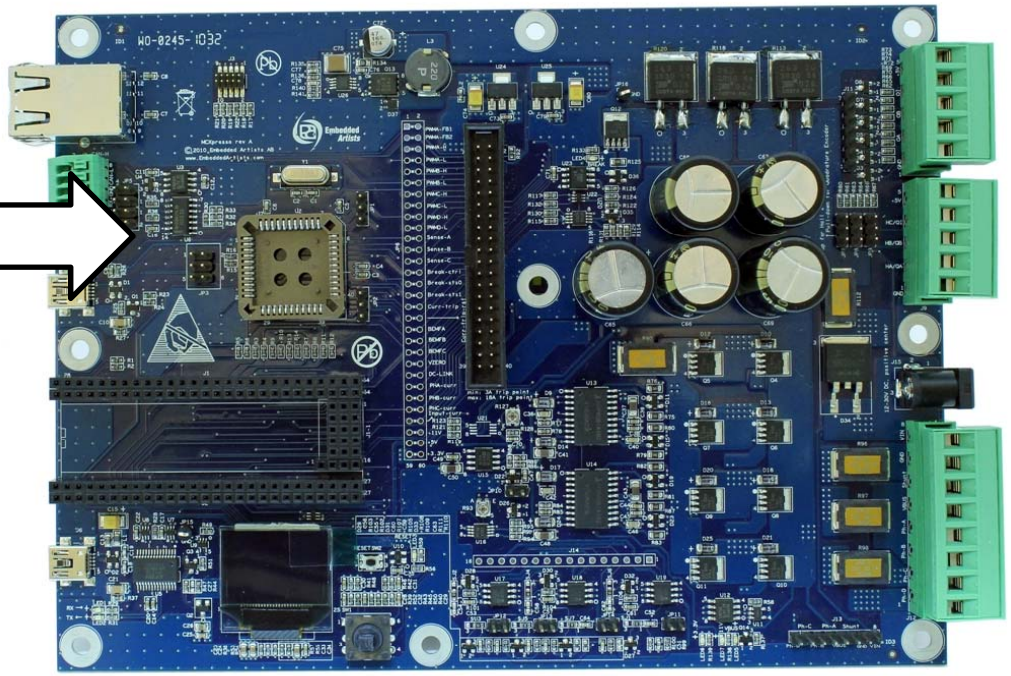
- NXP's first Cortex-M4 based DSC
- Running Single shunt Field Oriented Control (FOC)
- Uses new State Configurable Timer Subsystem
  - Makes 6 independent PWM signals with dual edge control
  - Triggers ADC conversion at an exact determined moment

System overview

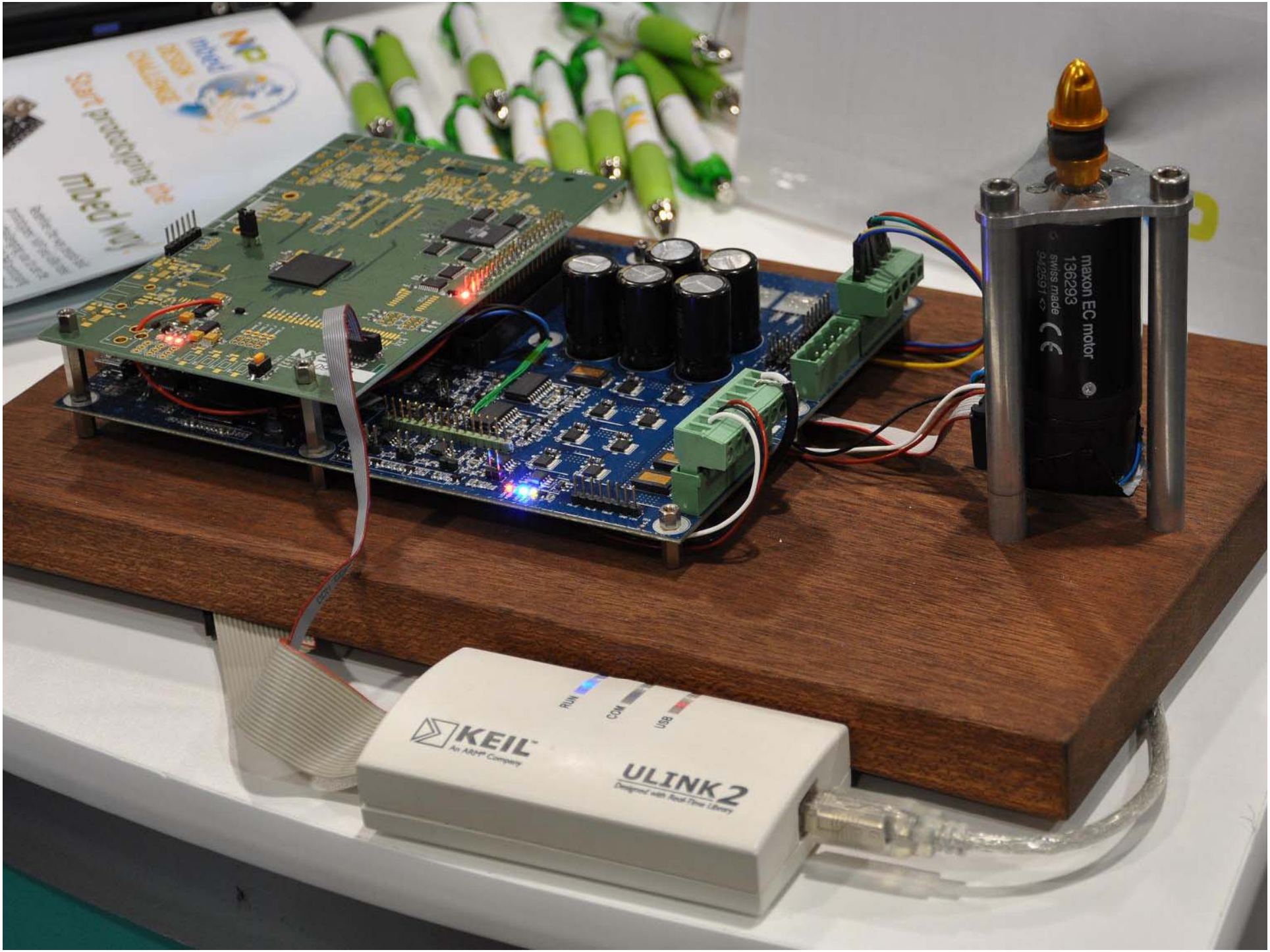




NXP Cortex-M4 Eval board



LPCXpresso Motor Control board


maxon EC motor
136293
swiss made
RUN
COM
USB
KEIL
An ARM Company
ULINK2

Tools/Getting Started

Cortex Microcontroller Software Interface Standard

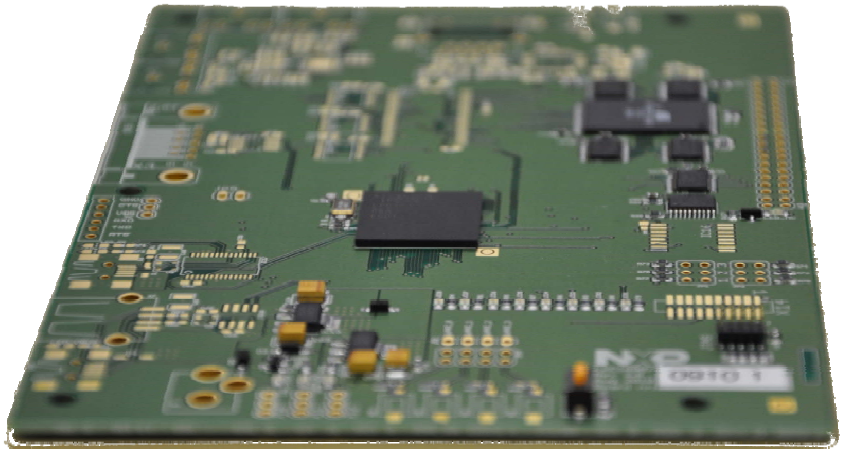
- CMSIS defines for a Cortex-Mx Microcontroller System:
  - A common way to access peripheral registers and a common way to define exception vectors
  - The register names of the Core Peripherals and the names of the Core Exception Vectors
  - A device independent interface for RTOS Kernels including a debug channel
  - Interfaces for middleware components (TCP/IP Stack, Flash File System)
- By using CMSIS compliant software components, the user can easily re-use template code. CMSIS is intended to enable the combination of software components from multiple middleware vendors.

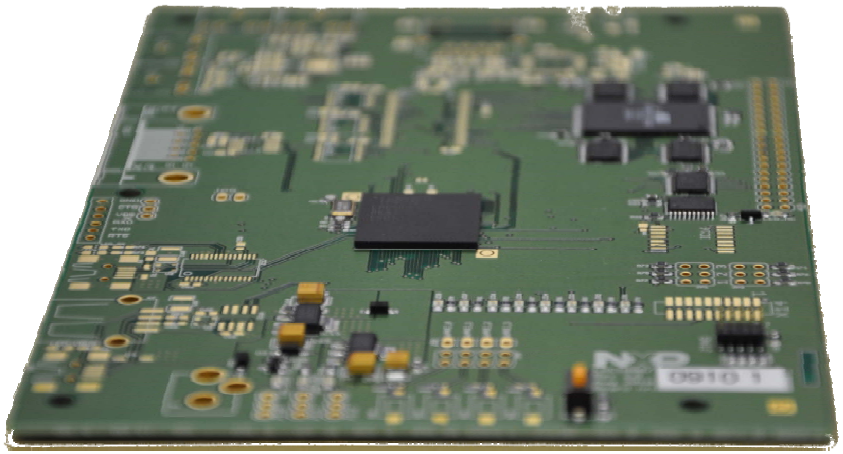
The CMSIS Partnership

DSP Libraries for Cortex™-M3

- C Library of Optimized DSP Algorithms
  - FFT
    - Supports both 32 and 16 bit data lengths
    - Block sizes of 64, 256 and 1024
  - FIR and IIR filters
    - 16-bit single stage Biquad
    - 32-bit single stage Biquad
  - PID controller
  - Resonator function
  - Random number generator
  - Dot Product
  - Cross product of vectors

M3 and M4 pin compatible boards





MCU Tool Solutions

LPC X PRESSO — *NXP's Low cost Development Tool Chain*

mbed — *Rapid Prototyping Online Tool*

IAR SYSTEMS, hitex, KEIL™ An ARM® Company — *Traditional Feature Rich Tools (third party)*

Circuit Cellar/Elektor "NXP mbed Design Challenge"

Succeed and you could walk away with a share of $10,000 in cash prizes!

- Launched Sept 21, 2010
- mbed microcontroller
  - Based on NXP LPC1768
  - Made for prototyping
  - Comes in a 40-pin 0.1" pitch DIP form-fact so it's ideal for experimenting on breadboard, stripboard and PCBs
- Combined with mbed "Cloud" compiler at http://mbed.org
- Already more than 10,000 boards shipped!
- For complete rules, or to request your complimentary contest kit, please visit: www.circuitcellar.com/nxpmbeddesignchallenge.