NUC972 Development Board
User's Manual

Rev. A1.0

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1 General Description

The user's guide describes the operation and use of the NHS-972DF62Y development board, NHS-972-1-YA-1M51. The board places NUC972DF62Y's almost of the functions, which includes the peripheral interfaces as memory (NAND flash, SPI flash, SD x 2), UART x5, IIS, 2 x 3 Key matrix, 24-bit LCD interface, Ethernet, USB host/device, CMOS sensor, SIM card, and reserve EBI port.

In order to easier-check for user, the description is based on the functional block with the sheet of schematic. User can check out what the function port is they would like to design on their system. The schematic is attached for the system reference design.

On the NUC972DF6Y development board, almost of the GPIO pin headers are traced to peripheral device via the dip switches. In which the system designer can easier to verify their module circuit by wire out from the pin header if the corresponding peripheral devices are turned off.

Meanwhile, the board reserves a JTAG ICE port for program development and a UART 0 for debugging message. In which is convenient for the designer to develop their system.

2 Peripheral Device

Block out the development board as several of the area with the difference line color and style. According to the block function, user is easier to search out which one of the function they want to use, and clear the corresponding GPIO has to be setting correctly; the board outline is attached as below:

Boarder color and line-style	Functional Block
	Power Block.
	JTAG ICE port.
	Peripheral Device 2.
	Peripheral Device 1.
	Peripheral Device 3.
	Peripheral Device 4.

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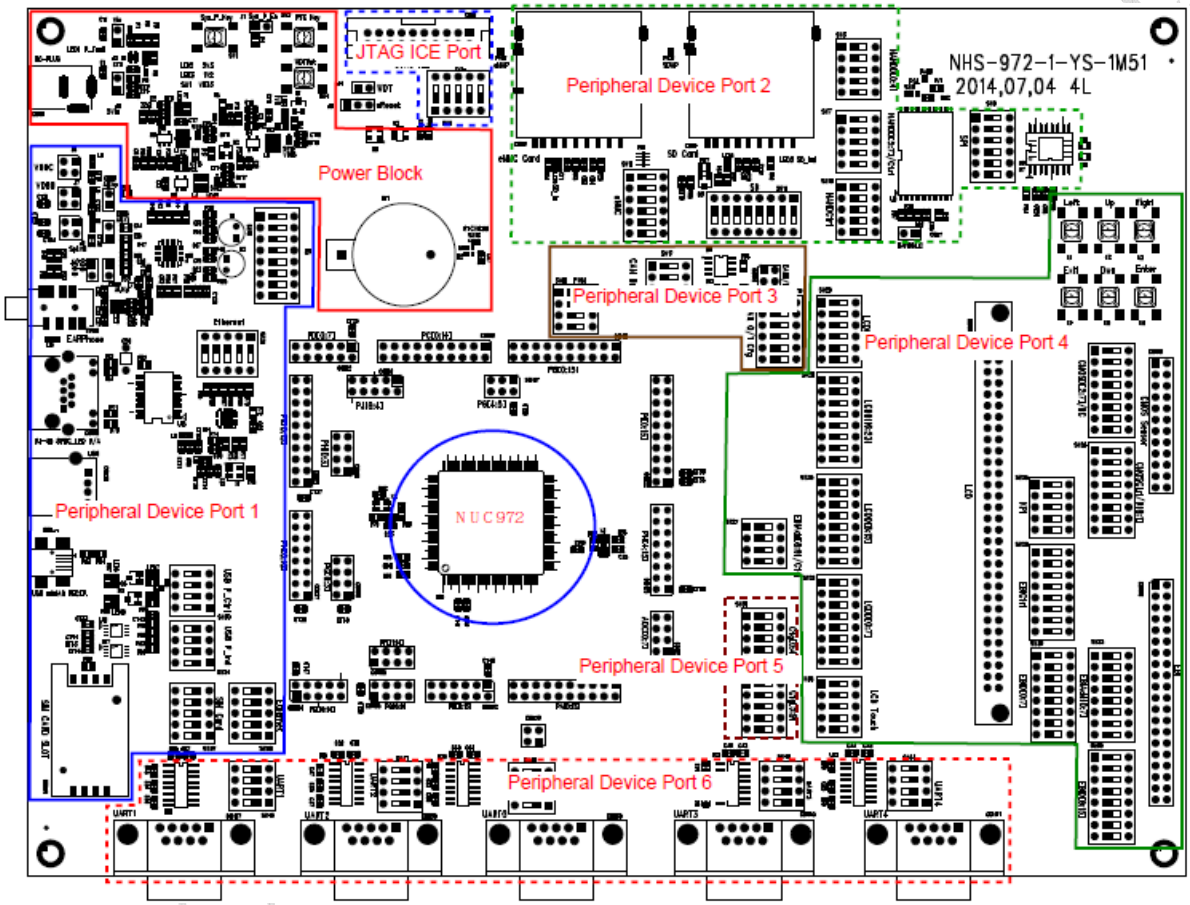
	CPU.
	Peripheral Device 5.
	Peripheral Device 6.

2.1 Partitioned Block –



3 Board Description

3.1 Power Block –

GPIO: SysWkUp, SysPWREn

CON2 is 5VDC power adaptor input jack terminal which provides the system power for the DC/DC converters, 3.3V is for system I/O and peripheral devices, 1.2V is for

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CPU's core power, 1.8V is for CPU's internal RAM.

Plug the 5Vdc adaptor into the CON2, in which will supply RTC power and system power DC/DC convertors input. Toggle the RTC key; system power control key, the RTCWkUp will go low, and then the RTCPWREn output Hi to enable DC/DC convertor U3 (3.3V for IO power), U8 (1.2V for core power), U4 (1.8V for DDR power). Mine while, the power LED2 (3.3V), LED8 (1.2V) and LED3 (1.8V) are light, too.

To prevent the input power is over the development board specification, the system board adds a power protection device U2 (APL3203A). The system power will be terminated and LED1 lighting when the input voltage is over 5.85V (APL3203A) or the current is over 1A.

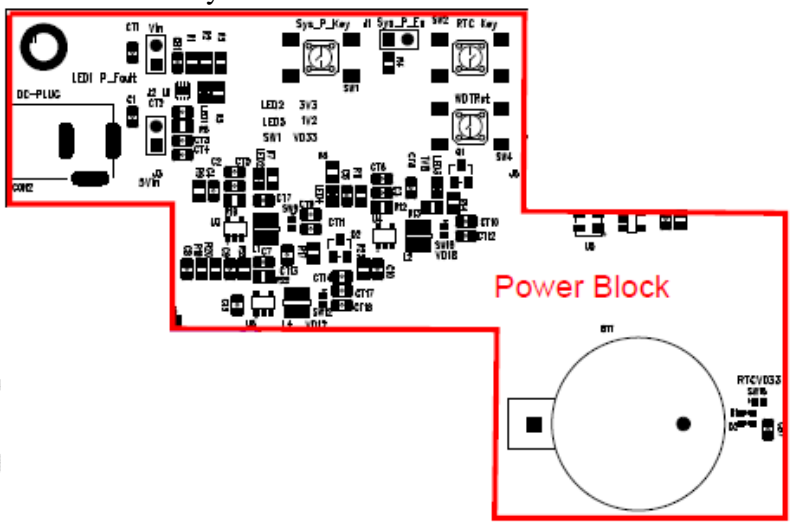
For the over current protection defines formula is as below:

$$I_{OCP} = \frac{K_{ILim}}{R_{ILim}} \qquad K_{ILim} = 25000AK \quad , \quad R_{ILim} = 24K\Omega$$

CON2, 5V power adaptor input terminal, polarity as below:

1: Center hole is positive for 5V+
2: External ring is negative for ground.

SW2 RTC key for system power control on/off.
SW4 Reset key.
BAT1 Battery socket is for CR2032.



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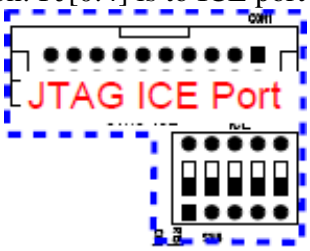
3.2 JTAG ICE port –

CON1 is a connector for JATG ICE port which function has to turn on SW6.

ICE port	PJ[0:4]	SW6	CON1
Note:	SW6 on: PJ[0:4] is to ICE port		



3.3 Peripheral Device 2 –

Memory block includes eMMC socket, SD socket, NAND flash and SPI flash.

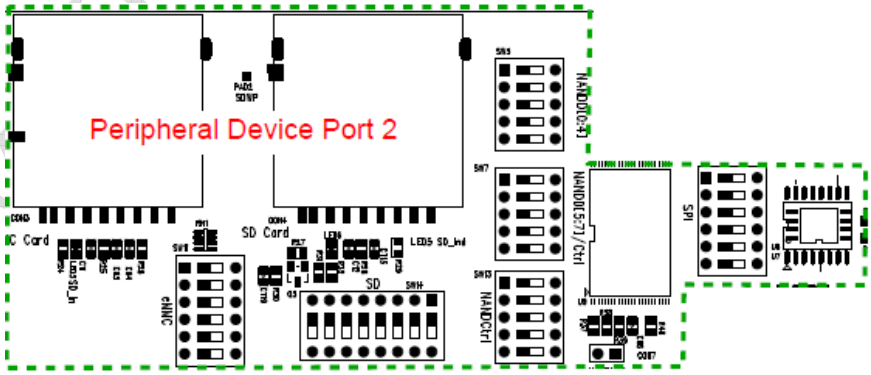
Each one of the device has to be turned on by the corresponding switch which all of the GPIO and DIP switched are listed as below:

eMMC	PC[0:5]	SW11	CON3
SD	PD[0:7]	SW14	CON4
NAND Flash	PC[0:14]	SW3, SW7, SW13	U9
SPI Flash	PB[6:11]	SW8	U6/U7

Note:

1. The PC[0:5] of eMMC conflicts with NAND flash.

2. Only one (U6 or U7) SPI flash can be used.



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3.4 Peripheral Device 1 –

This partitioned block includes IIS, Ethernet, USB device, USB host, and SIM card socket.

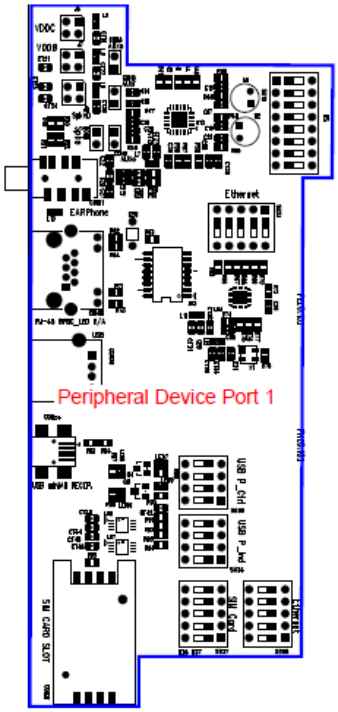
Add one CODEC chip (NUC8822L) to IIS port which is easier to verify.

For Ethernet port, the NUC972 support RMII interface which add one Ethernet phy to RJ45.

Either is USB device or host, there is power protection chip is placed on the USB power bus. The corresponding DIP switches have to be turned on for the power control. If the USB power control chip isn't control by GPIO, the system is reserved a switch for manual control. The OC pin will active low when the USB power is fault, the fault LED will be turned to red from green.

IIS	PG[0:1], PG[10:14], PE12	SW15	U10
USB device	USB0_DP/DM/ID, PE14, PH1	SW30.1	U16, CON24
USB host	USB1_DP/DM, PE15, PH1	SW30.4	U17, CON20
Ethernet	PF[0:9]	SW38, SW21	U14, CON18
SIM card	PG[10:14]	SW37	CON31

Note: SW34 is USB power chip enable by hardware force and fault LED setting.



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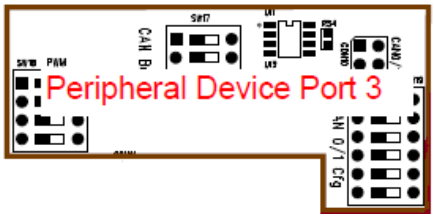
3.5 Peripheral Device 3 –

Is only reserved two CAN bus ports with pin headers on the board.

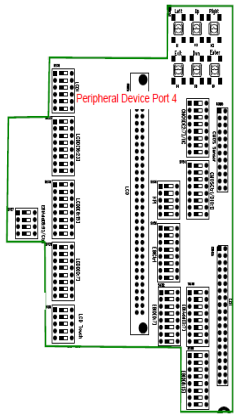
CAN bus 0	CON10[1:2]	PH[2:3]	SW17[1:2]
CAN bus 1	CON10[3:4]	PH[4:5]	SW17[3:4]



3.6 Peripheral Device 4 –

This block are is mainly for external bus which includes the 24-bit LCD panel, resister-type touch panel ADC, CMOS sensor , external bus interface (EBI) port and a 3 by 2 matrix keypads. PWM is only reserved with pin header. The LCD backlight could be controlled by the PWM if one of the PWM switch is switched on.

Key pads	PH[4:6], PH[9:10]	SW26	K[1:6]
PWM	PB[2:3], PH[2:3]	SW18	CON23.27
LCD	PG[2:9], PD[8:15], PA[0:15]	SW20, 23, 29, 25	CON23
Touch ADC	ADC[3:7]	SW36	CON23
CMOS sensor	PI[0:15], PB[0:1]	SW24, 22	CON16
EBI	PD[15:8], PH[4:15], PI[0:15],	SW37	CON31



3.7 Peripheral Device Port 5 –

CPU will recognize the state as the port setting in power on initial. The system designer has to know which one of the state want to use by oneself. Causing there is a scanning time; these pins are in input mode. If possible, the system designer should prevent to use these pins as input mode in this period. All of the configuration setting is listed as below.

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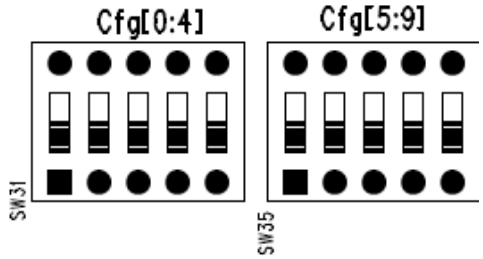
Configure Bit	Configured Function	SW
Cfg[1:0] =	00 : Boot from USB. 01 : Boor from eMMC. 10 : Boot from NANA Flash. 11 : Boot from SPI Flash.	SW31.2, SW31.1
Cfg2 =	0 : System clock is from 12 MHz crystal. 1 : System clock is from UPLL output.	SW31.3
Cfg3 =	0 : WDT is OFF after power-on. 1 : WDT is ON after power-on.	SW31.4
Cfg4 =	0 : Pin PJ[4:0] used as GPIO pin. 1 : Pin PJ[4:0] used as JTAG interface.	SW31.5
Cfg5 =	0 : UART 0 debug message output ON. 1 : UART 0 debug message output OFF	SW35.1
Cfg[7:6] =	00 : NAND Flash page size is 2KB. 01 : NAND Flash page size is 4KB. 10 : NAND Flash page size is 8KB. 11 : Ignore Power-On Setting.	SW35.3, SW35.2
Cfg[9:8] =	00 : NAND Flash ECC type is BCH T12. 01 : NAND Flash ECC type is BCH T15. 10 : NAND Flash ECC type is BCH T24. 11 : Ignore Power-On Setting.	SW35.5, SW35.4
		

Note: The configured pin should be pulled low with a 10KΩ.

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4 Pin Function assignment

Pin No.	NUC972	1st Function	2nd Function	3rd Function
1	PG.3	LCD BL En		
2	PG.2	LCD En		
3	PG.1	IIC0SDA		
4	PG.0	IIC0SCK		
5	PG.14	IIS LRCk	SMC0 CD	
6	PG.13	IIS BClk	SMC0 PWR	
7	PG.12	IIS Di	SMC0 DAT	
8	PG.11	IIS Do	SMC0 CLK	
9	PG.10	IIS MClk	SMC0 RST	
10	VDD33			
11	VSS			
12	VDD12			
13	MVSS			
14	MVDD			
15	MVSS			
16	MVDD			
17	MVSS			
18	MVDD			
19	MVSS			
20	VDD33			
21	VDD12			
22	PF.14		UR2CTS	
23	PF.13		UR2RTS	
24	PF.12		UR2Rx	
25	PF.11		UR2Tx	
26	PG.9	LCD DEN		
27	PG.8	LCD Vsync		
28	PG.7	LCD Hsync		
29	PG.6	LCD Clk		
30	PD.15	LCD D23		EBI nWait

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31	PD.14	LCD D22		EBI nOE
32	PD.13	LCD D21		EBI nWE
33	PD.12	LCD D20		EBI nCS4
34	PD.11	LCD D19		EBI nCS3
35	PD.10	LCD D18		EBI nCS2
36	PD.9	LCD D17		EBI nCS1
37	PD.8	LCD D16		EBI nCS0
38	PA.15	LCD D15		
39	PA.14	LCD D14		
40	PA.13	LCD D13		
41	PA.12	LCD D12		
42	PA.11	LCD D11		
43	PA.10	LCD D10		
44	VDD33			
45	PA.9	LCD D9		
46	PA.8	LCD D8		
47	PA.7	LCD D7		
48	PA.6	LCD D6		
49	PA.5	LCD D5		
50	PA.4	LCD D4		
51	PA.3	LCD D3		
52	PA.2	LCD D2		
53	PA.1	LCD D1		
54	PA.0	LCD D0		
55	ADC0			
56	ADC6			
57	ADC4			
58	AVSS			
59	AVDD			
60	ADC7			
61	ADC5			
62	ADC1			
63	ADC3			

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64	ADC2			
65	VREF			
66	RTC_VDD			
67	SYS_PWREn			
68	SYS_nWkUp			
69	X32_IN			
70	X32_OUT			
71	PH.4	Key Row0		EBI Add0
72	PH.5	Key Row1		EBI Add1
73	PH.6	Key Row2		EBI Add2
74	PH.7			EBI Add3
75	PH.8	Key Col0		EBI Add4
76	PH.9	Key Col1		EBI Add5
77	PH.10			EBI Add6
78	PH.11			EBI Add7
79	PH.12			EBI Add8
80	VDD33			
81	VSS			
82	VDD12			
83	PH.13			EBI Add9
84	PH.14	CAN1Rx		EBI nBE0
85	PH.15	CAN1Tx		EBI nBE1
86	PI.0	VCAP PwDn		EBI D0
87	PI.1			EBI D1
88	PI.2			EBI D2
89	PI.3	VCAP SCLKo		EBI D3
90	PI.4	VCAP SPCLK		EBI D4
91	PI.5	VCAP SHsync		EBI D5
92	PI.6	VCAP SVsync		EBI D6
93	PI.7	VCAP SField		EBI D7
94	PI.8	VCAP SD0		EBI D8
95	PI.9	VCAP SD1		EBI D9
96	PI.10	VCAP SD2		EBI D10

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97	PI.11	VCAP SD3		EBI D11
98	PI.12	VCAP SD4		EBI D12
99	PI.13	VCAP SD5		EBI D13
100	PI.14	VCAP SD6		EBI D14
101	PI.15	VCAP SD7		EBI D15
102	VDD12			
103	VSS			
104	VDD33			
105	PB.0	IIC1SCK		
106	PB.1	IIC1SDA		
107	PB.2		UR6Tx	PWM0
108	PB.3		UR6Rx	PWM1
109	PB.4		UR6RTS	
110	PB.5		UR6CTS	
111	PB.6	SPI0 CS0		
112	PB.7	SPI0 CLK		
113	PB.8	SPI0 DoD0		
114	PB.9	SPI0 DiD1		
115	PB.10	SPI0 D2		
116	PB.11	SPI0 D3		
117	PB.12		UR10Tx	
118	PB.13		UR10Rx	
119	PB.14		UR10RTS	
120	PB.15		UR10CTS	
121	PG.4			
122	PG.5			
123	PC.0	ND0	eMMC D0	
124	PC.1	ND1	eMMC D1	
125	PC.2	ND2	eMMC D2	
126	PC.3	ND3	eMMC D3	
127	PC.4	ND4	eMMC CMD	
128	PC.5	ND5	eMMC CLK	
129	PC.6	ND6		

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130	PC.7	ND7		
131	PC.8	NCS0		
132	PC.9	NALE		
133	PC.10	NCLE		
134	PC.11	NWE		
135	PC.12	NRE		
136	PC.13	NRDY0		
137	PC.14	NWP		
138	PJ.3			TDO
139	PJ.0			TCK
140	PJ.1			TMS
141	PJ.2			TDI
142	PJ.4			nTRST
143	nRESET			
144	VDD33			
145	VSS			
146	VDD12			
147	MVSS			
148	MVDD			
149	MVSS			
150	MVDD			
151	MVSS			
152	MVDD			
153	VSS			
154	VDD33			
155	PD.0	SD0 CMD		
156	PD.1	SD0 CLK		
157	PD.2	SD0 D0		
158	PD.3	SD0 D1		
159	PD.4	SD0 D2		
160	PD.5	SD0 D3		
161	PD.6	SD0 CD		
162	PD.7	SD0 PWR		

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163	VDD12			
164	PLL_VDD12			
165	PLL_VSS			
166	VDD12			
167	PH.3		CAN0Tx	PWM3
168	PH.2		CAN0Rx	PWM2
169	PE.13			
170	PE.12	I2S CS		
171	PE.11			
172	PE.10			
173	PE.9			
174	PE.8			
175	PE.7			
176	PE.6			
177	PE.5			UR1CTS
178	PE.4			UR1RTS
179	PE.3			UR1Rx
180	PE.2			UR1Tx
181	PE.1			UR0Rx
182	PE.0			UR0Tx
183	VDD33			
184	MainXi			
185	MainXo			
186	VSS			
187	PF.9	RMII0 RxErr		
188	PF.8	RMII0 CRSDV		
189	PF.7	RMII0 RxD1		
190	PF.6	RMII0 RxD0		
191	PF.5	RMII0 RefCLK		
192	PF.4	RMII0 TxEn		
193	PF.3	RMII0 TxD1		
194	PF.2	RMII0 TxD0		
195	PF.1	RMII0 MDio		

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196	PF.0	RMII0 MDC		
197	PH.1	USB0 OC		
198	PH.0	USB0 VbusDet		
199	PF.10	USB0 PWREn		
200	PE.15	USB1 PWREn		
201	PE.14	USB0 PWREn		
202	VSS			
203	VDD12			
204	USBPll1			
	VDD	1.2Vusb		
205	USB1 VSS			
206	USB1 DM	Host DM		
207	USB1 DP	Host DP		
208	USB1 VDD	3.3Vusb		
209	USB1 REXT	12.1K		
210	USBPll0			
	VDD	1.2Vusb		
211	USB0 VSS			
212	USB0 DM	OTG DM		
213	USB0 DP	OTG DP		
214	USB0 VDD			
215	USB0 REXT	12.1K		
216	USB0 ID	OTG ID		

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5 Document Revision History

Date	Revision	Remarks
09/10/2014	A1.0	Release version A1.0.

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6 Schematics

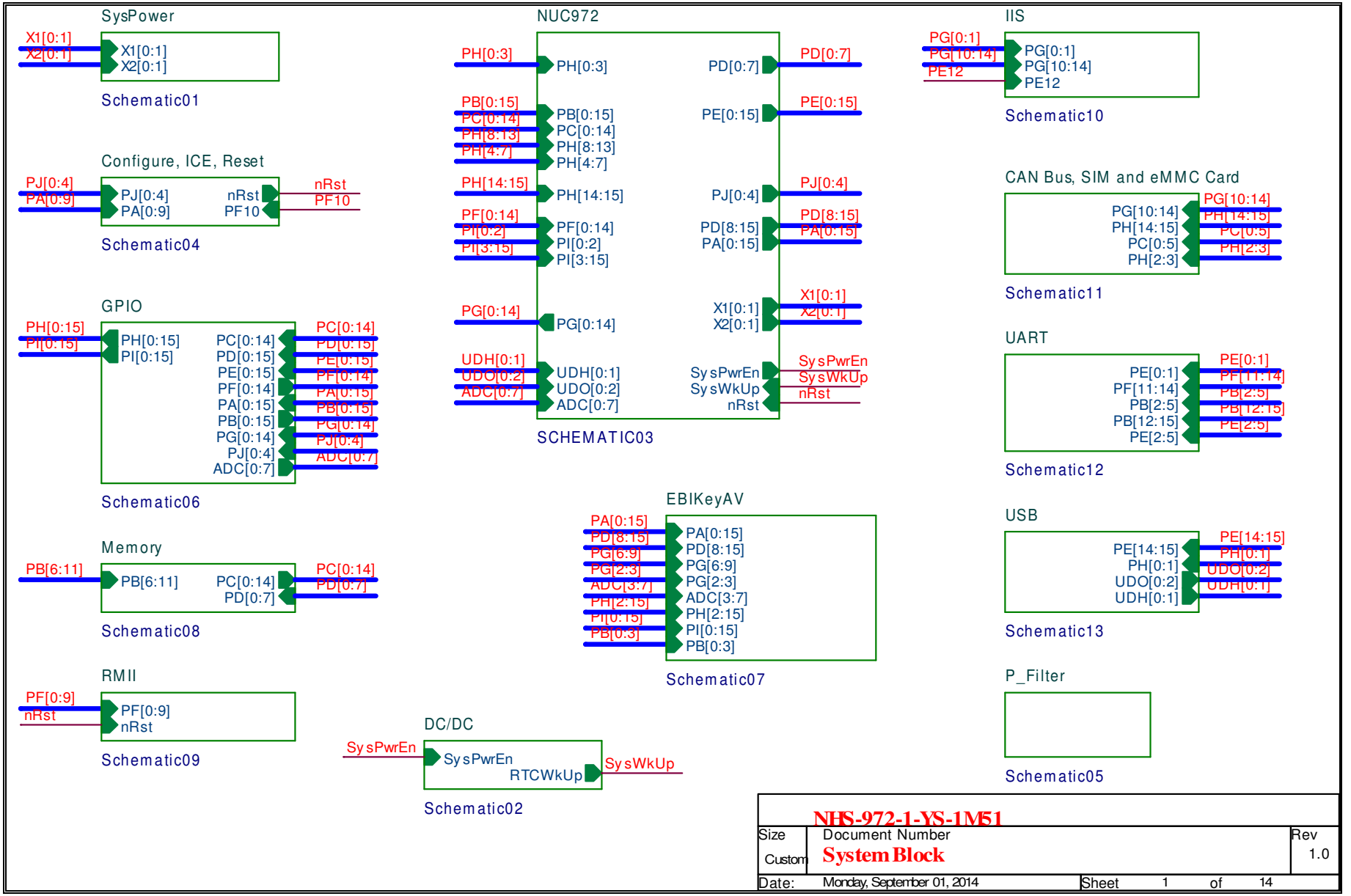

Figure 6-1Block Diagram

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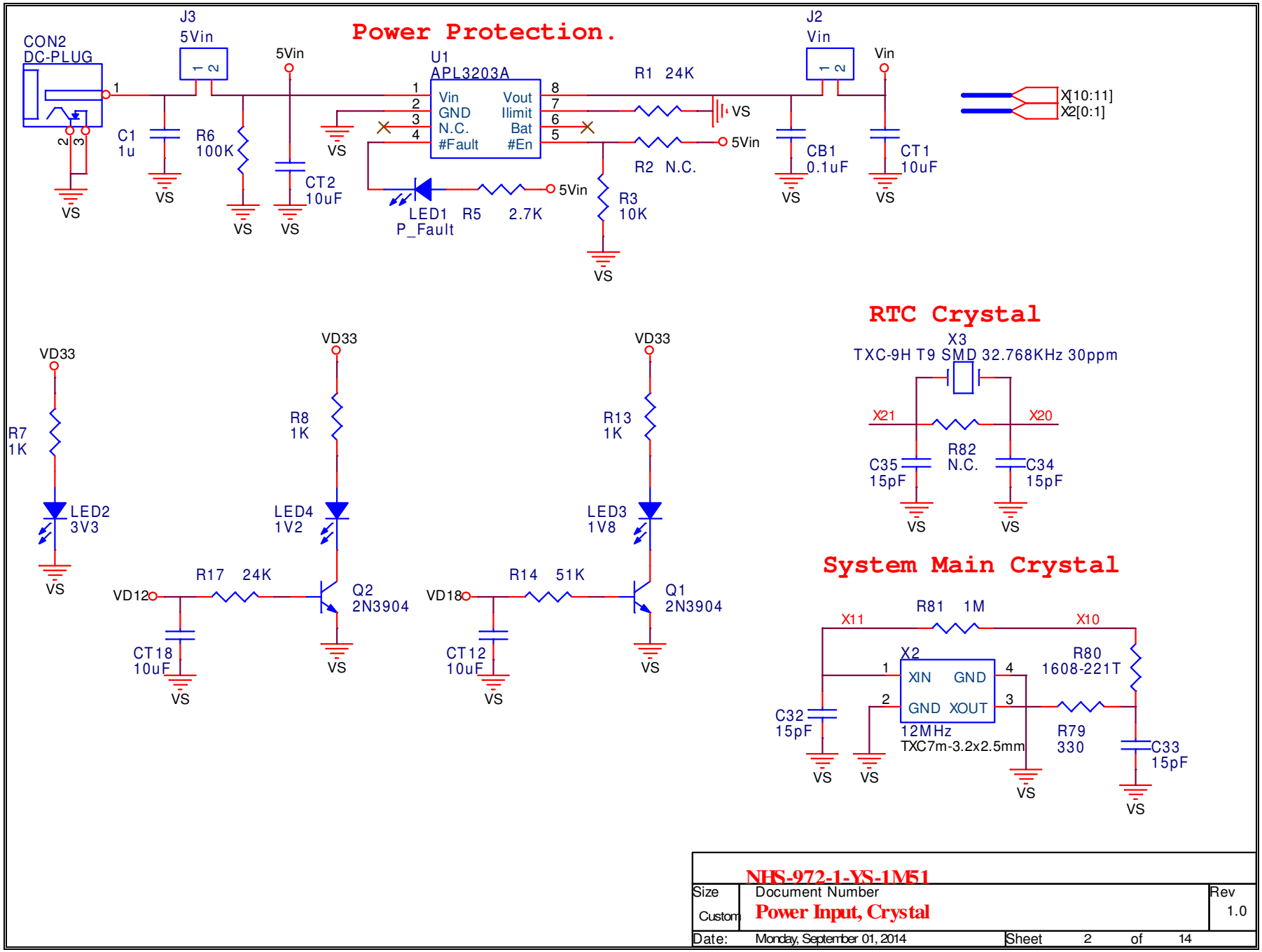

Figure 6-2 System Power

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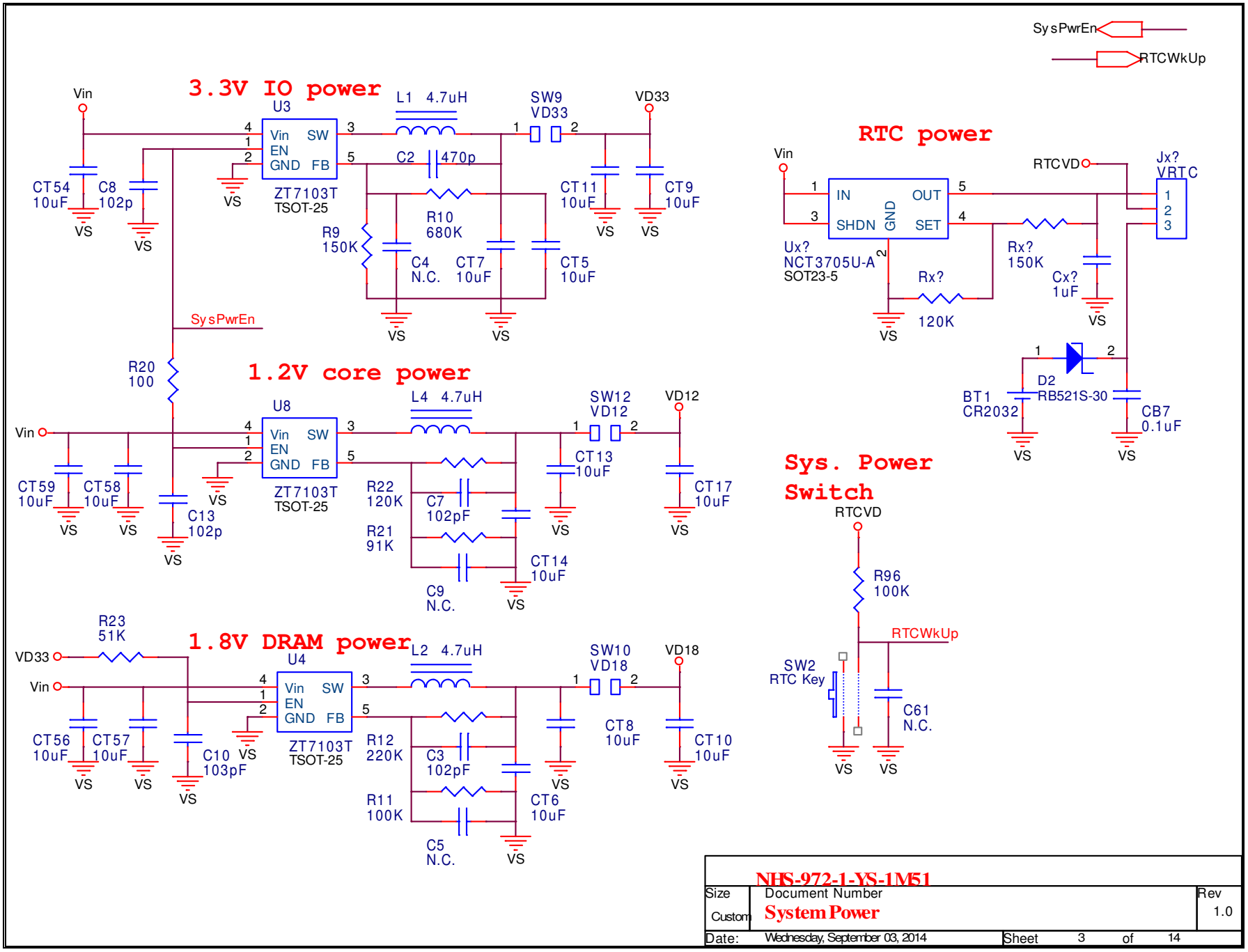

Figure 6-3 DC/DC

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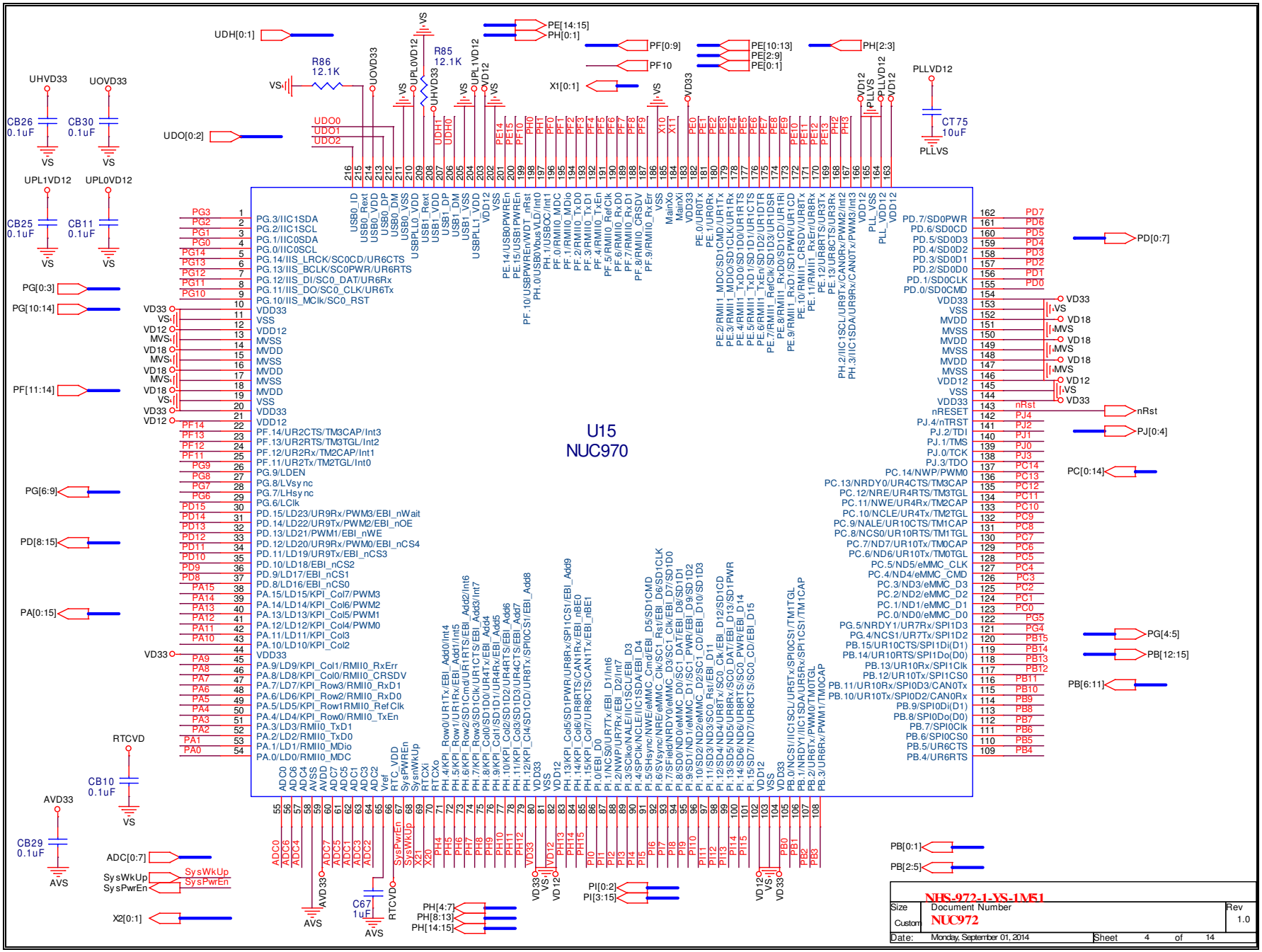

Figure 6-4 NUC972

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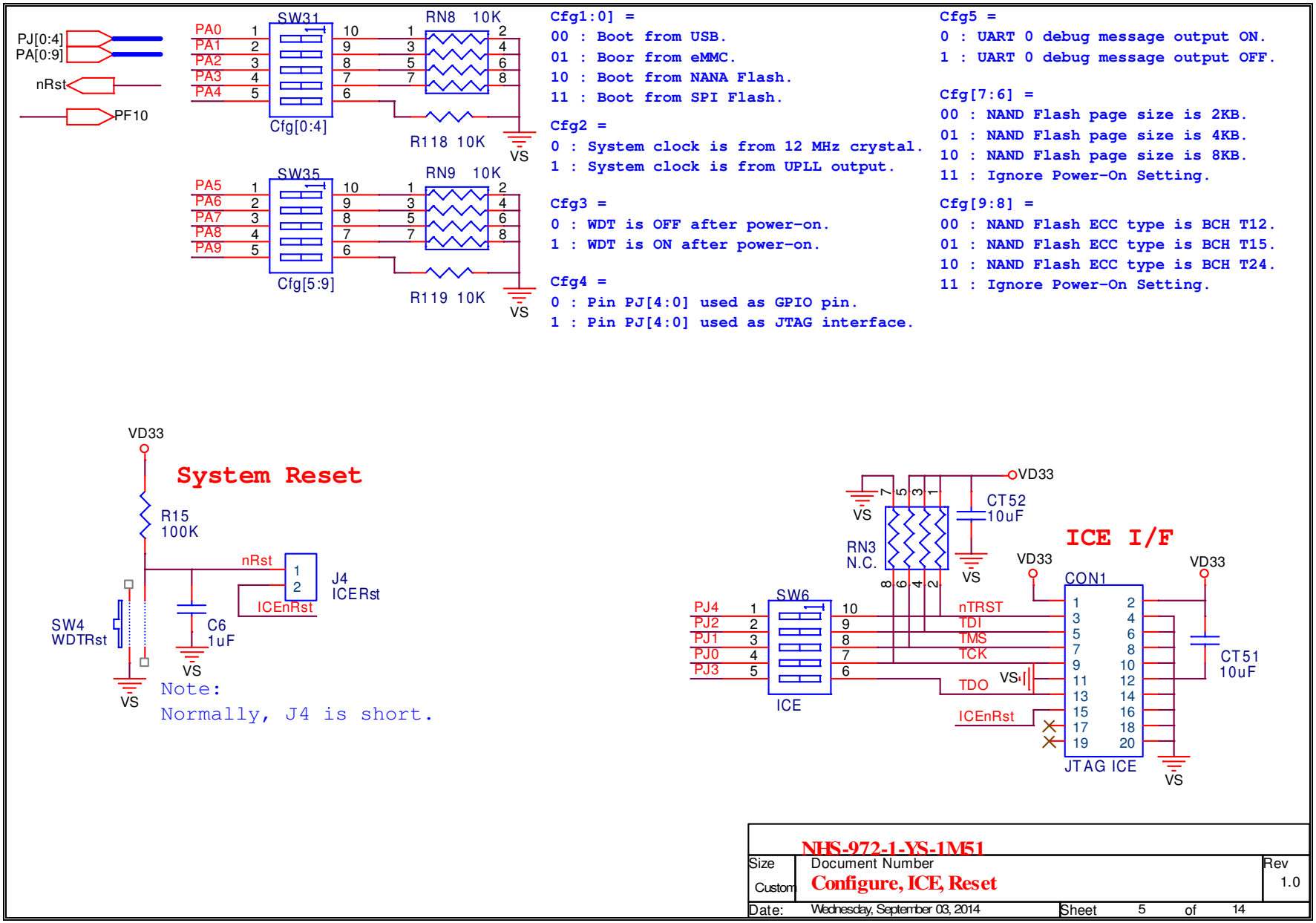

Figure 6-5 Configure, ICE Reset

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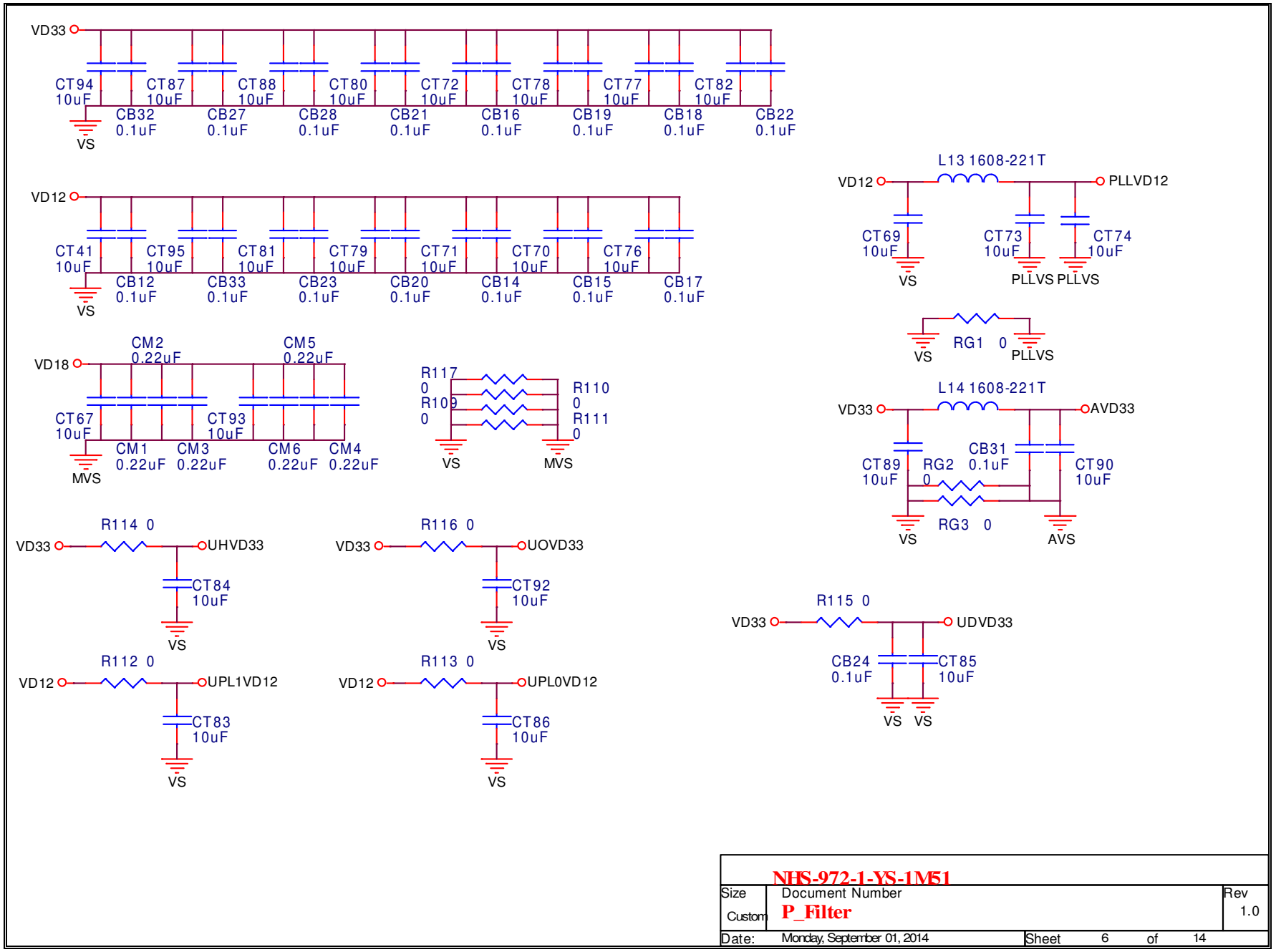

Figure 6-6 P_Filter

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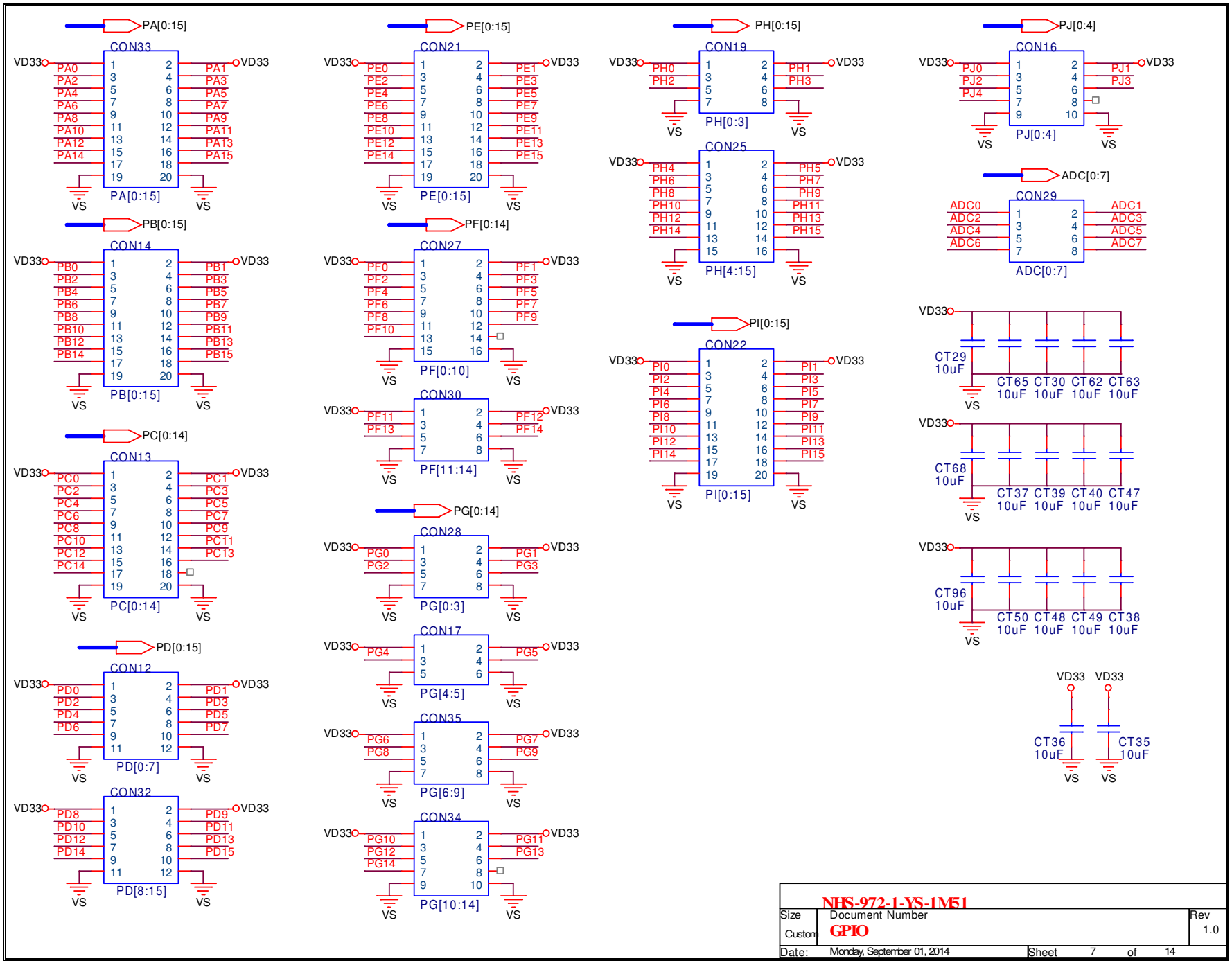

Figure 6-7 GPIO

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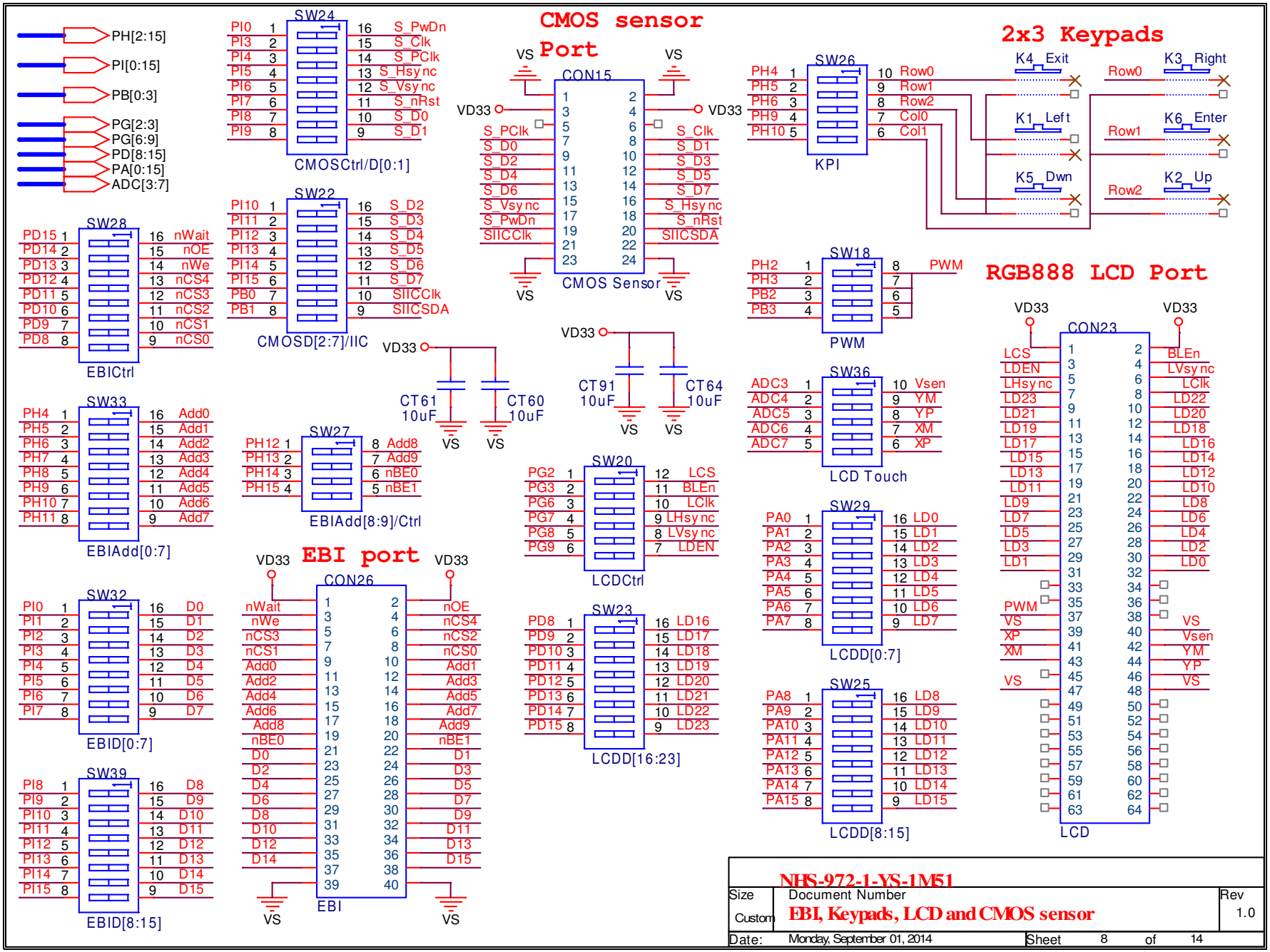

Figure 6-8 EBI, Keys, AV

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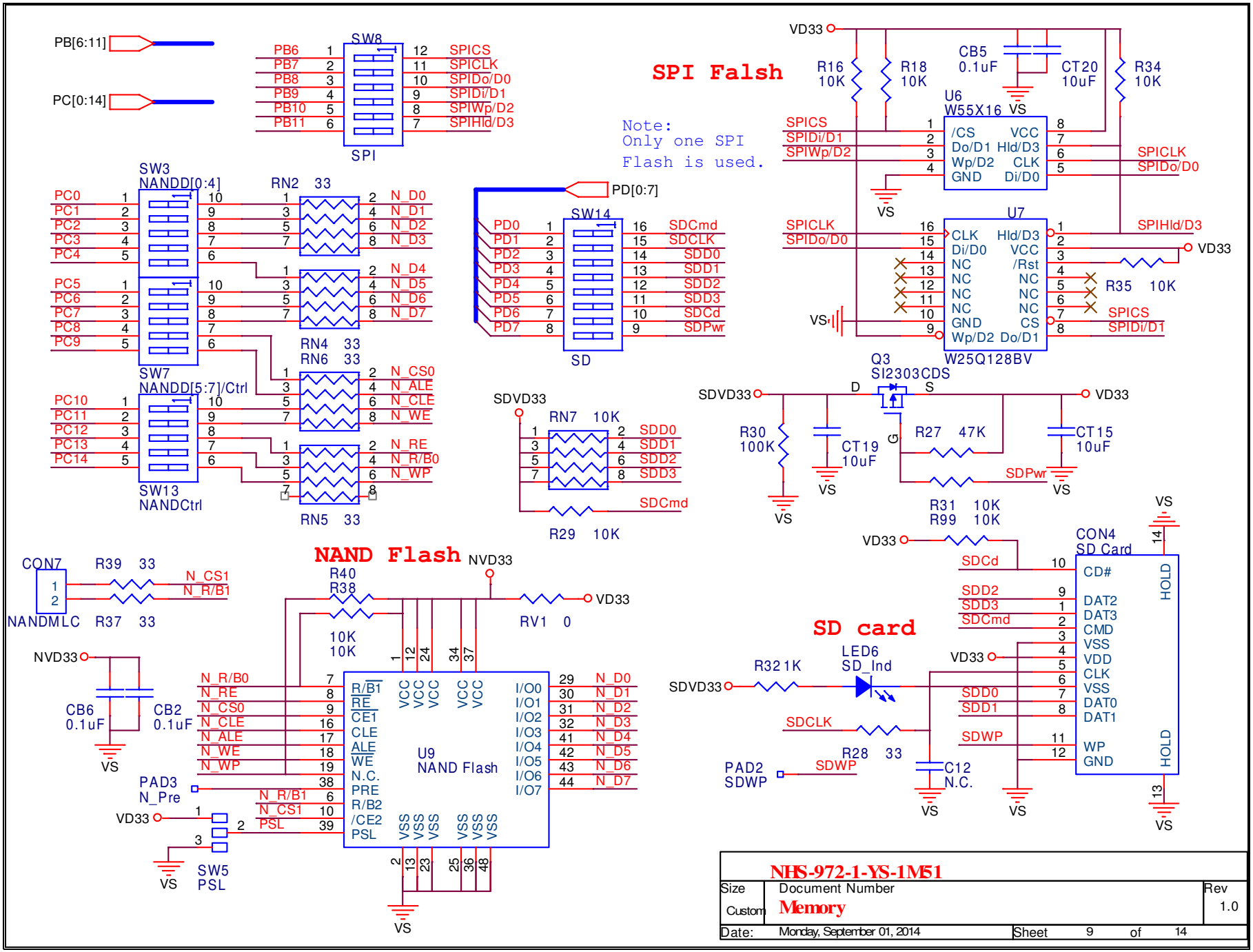

Figure 6-9 RMII

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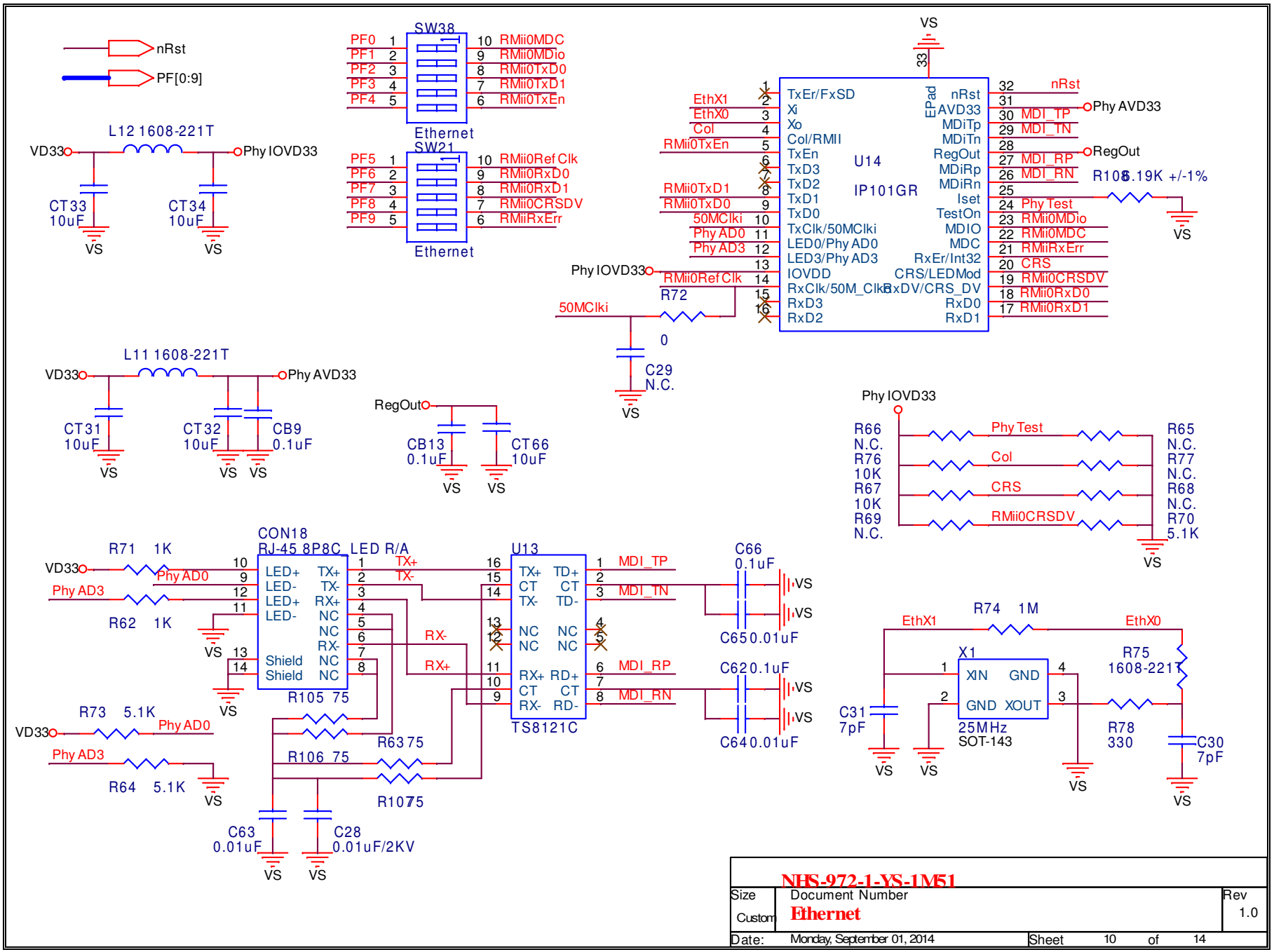

Figure 6-10 RMII

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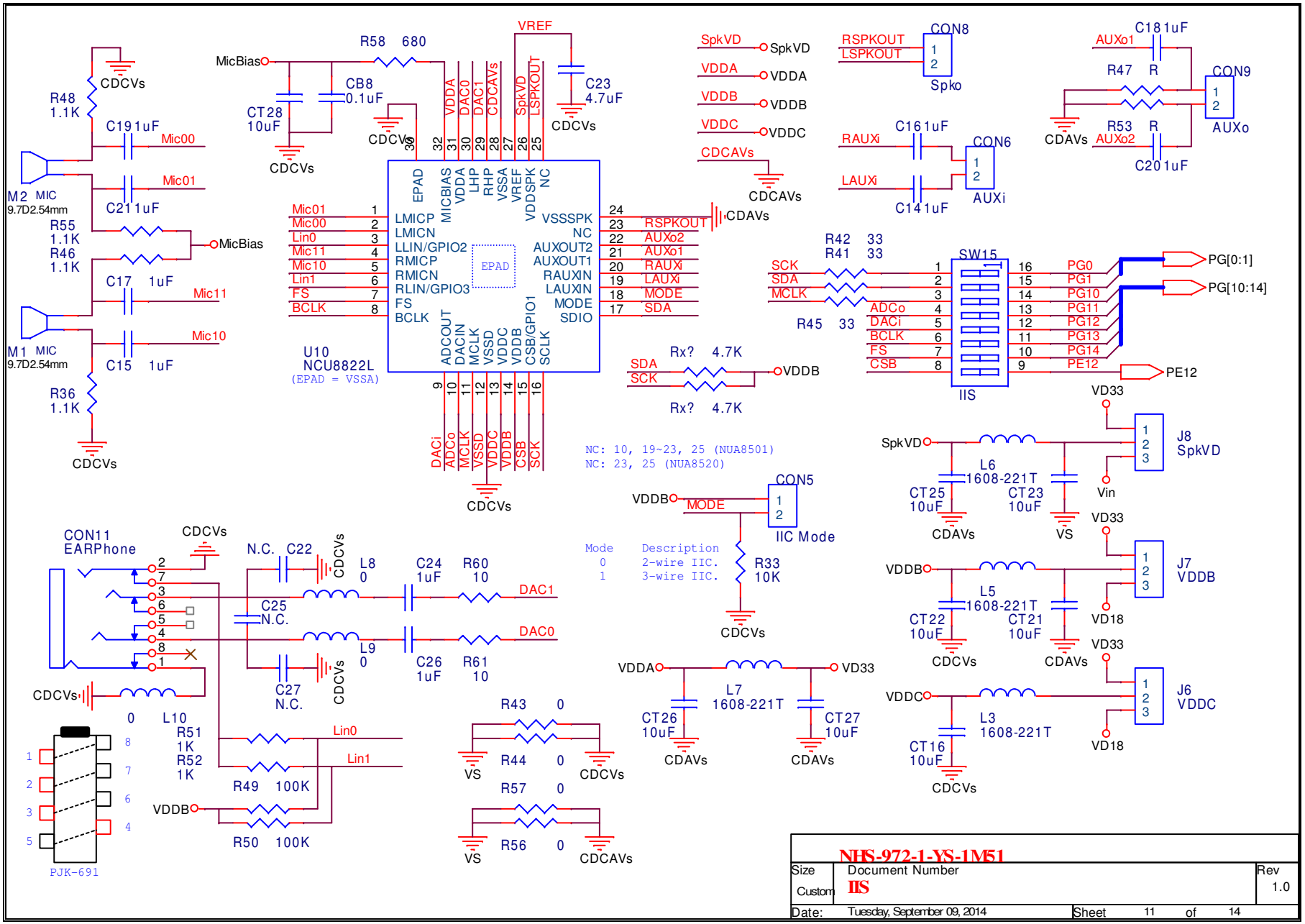

Figure 6-11 IIS

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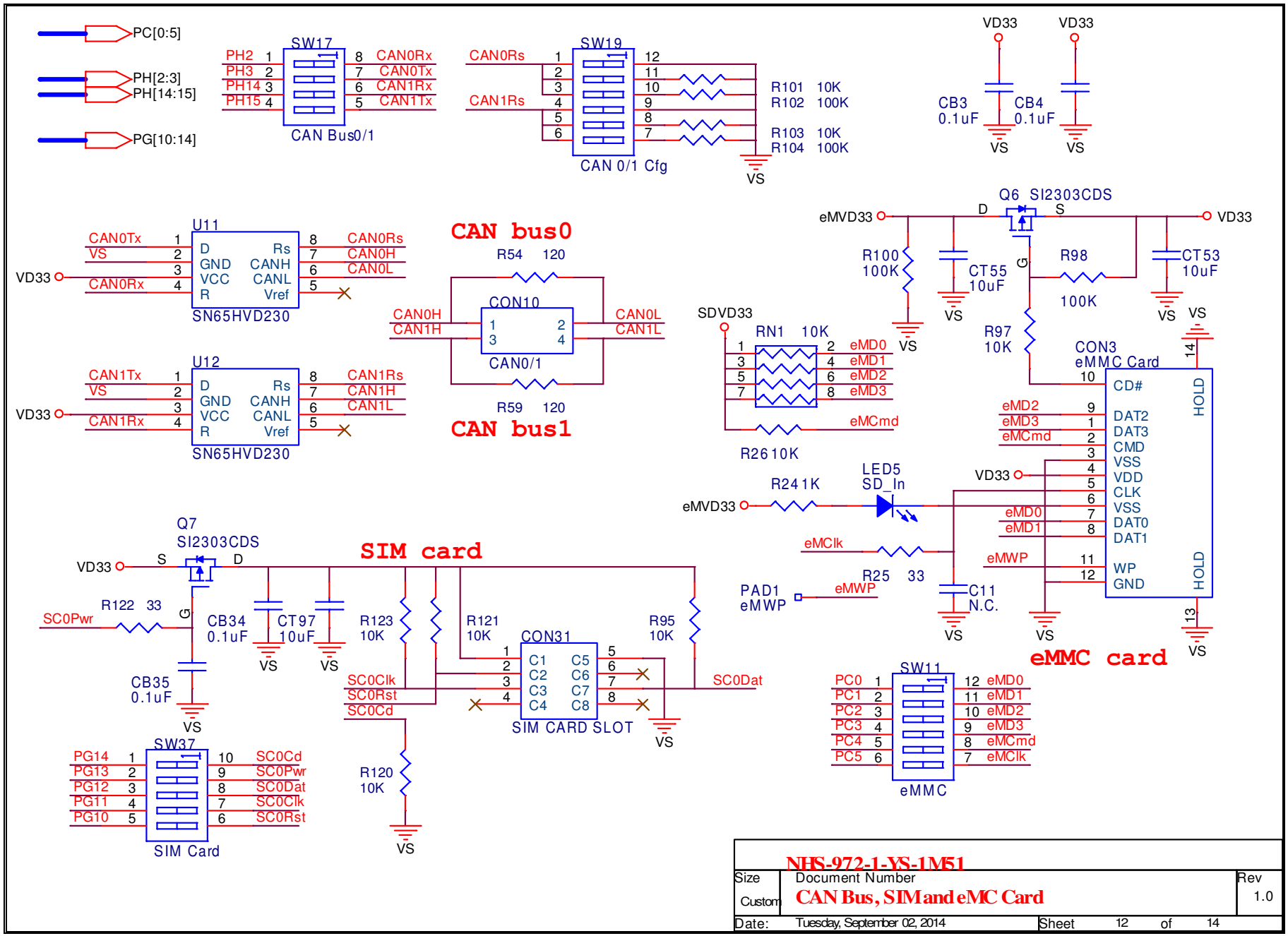

Figure 6-12 CAN Bus, SIM card and eMMC

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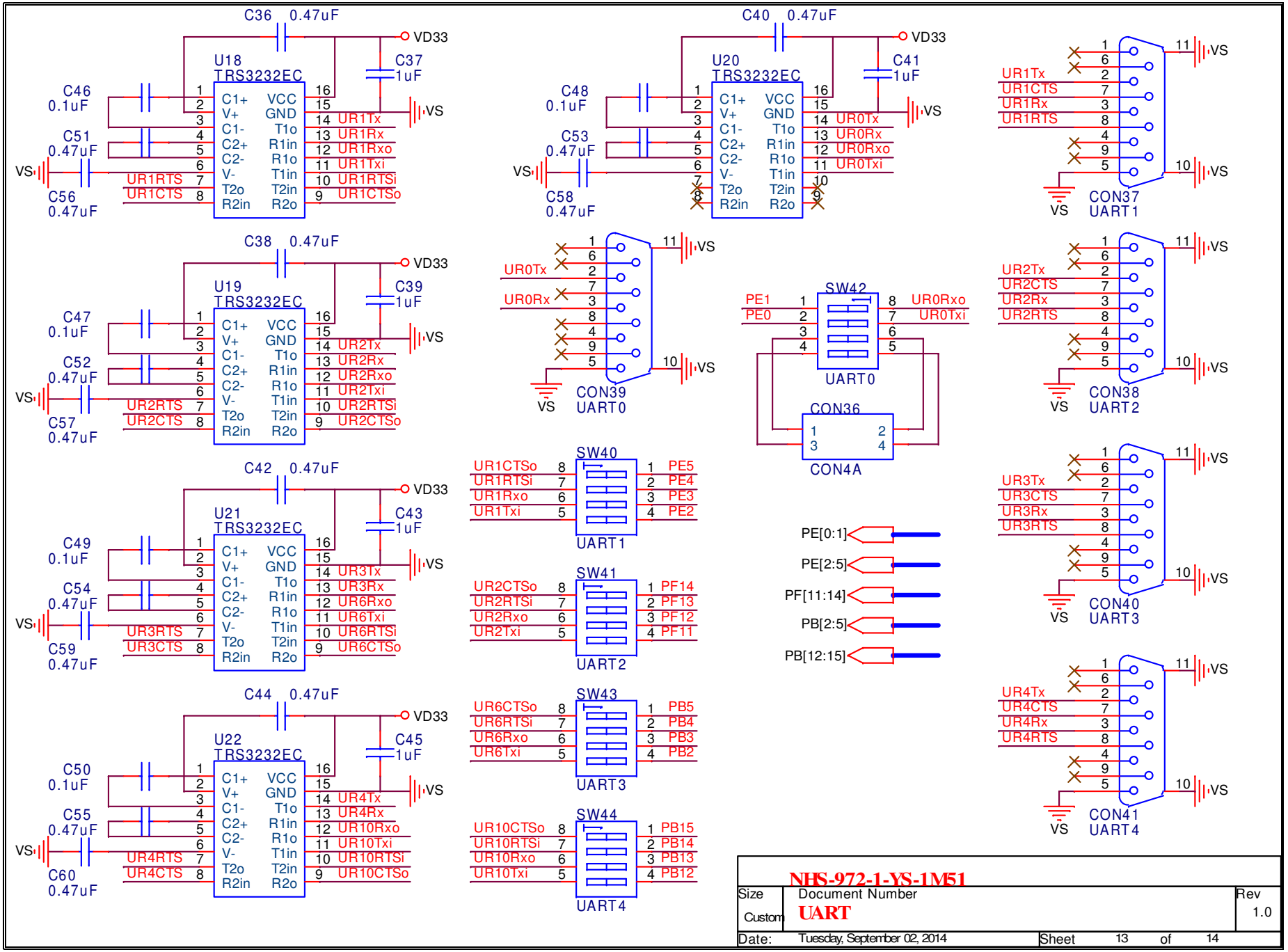

Figure 6-13 UART

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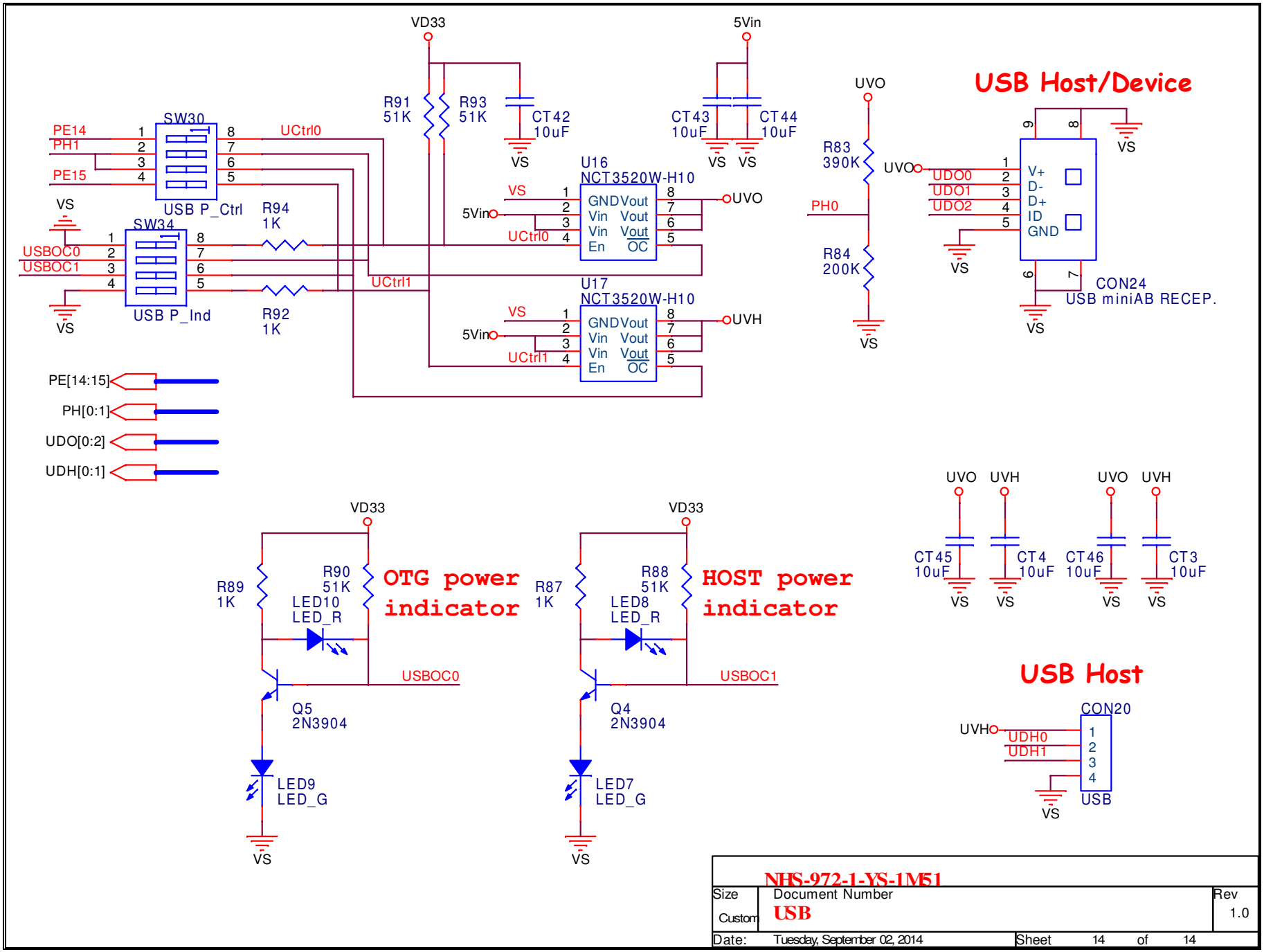

Figure 6-14 USB

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