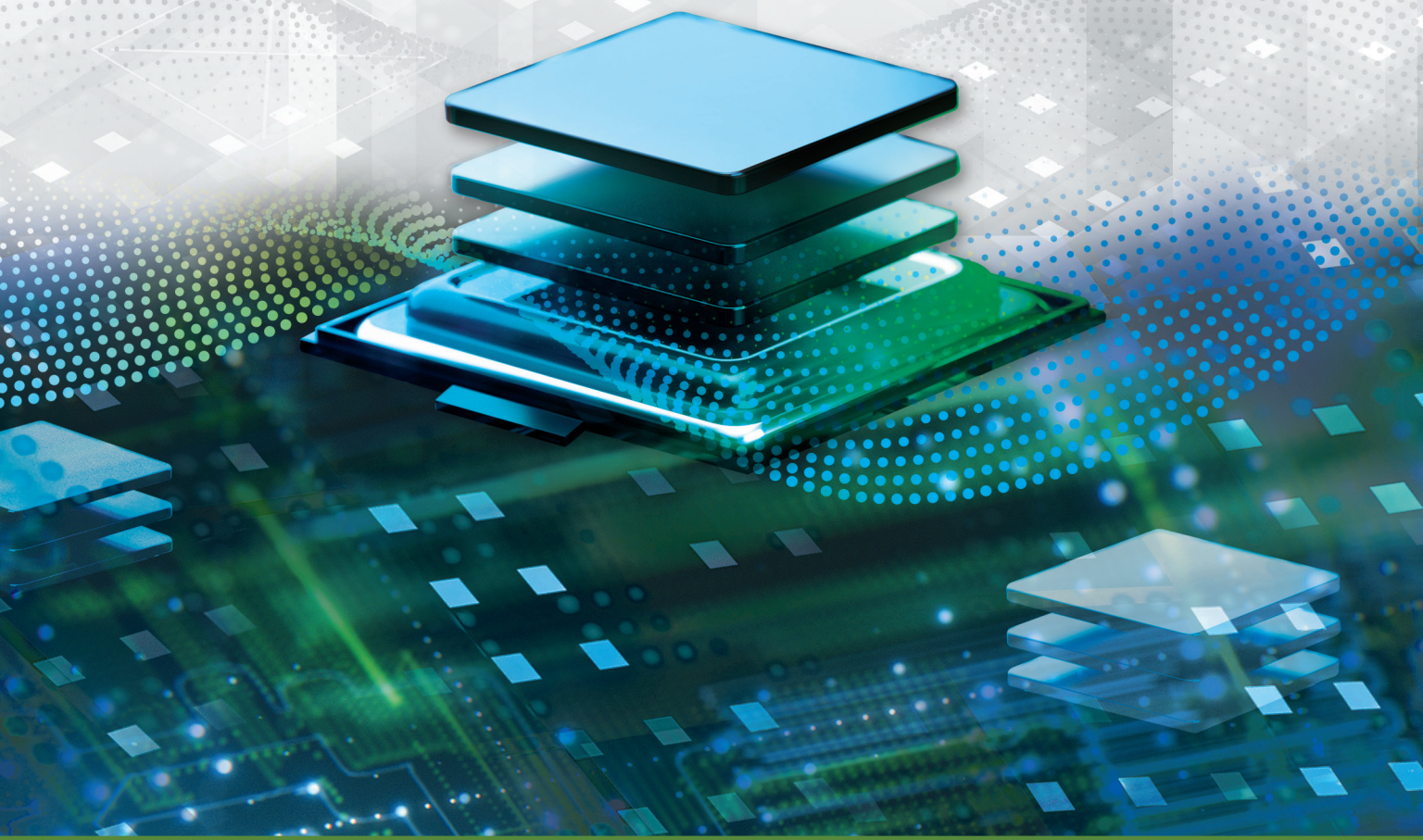
MKS HANDBOOK

Process Technologies in Advanced Packaging

by the Office of the CTO



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Office of the CTO (OCTO)

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Foreword

Semiconductor devices are essential and ubiquitous parts of our lives, enabling everything from artificial intelligence (AI) to autonomous vehicles to wireless networks. Driven by Moore's Law, which states that the number of transistors on a microchip doubles approximately every two years, the industry has pursued a relentless reduction in cost per function for the better part of a century. Historically, the industry used Dennard scaling and multi-core architectures to achieve these results. However, traditional transistor scaling has slowed, but the need to continue reducing cost per function at the same historical pace is paramount; otherwise, new innovations will become cost prohibitive.

The latest technological evolution introduced to overcome this limitation is called heterogeneous packaging, often referred to as Advanced Packaging. Traditional packaging involves packaging a single semiconductor chip, while Advanced Packaging integrates multiple specialized chips into a single package, allowing them to function as a single chip. This enables continued performance gains for electronic devices, despite the slowdown of traditional transistor scaling.

Advanced Packaging encompasses a wide variety of architectures and process technologies, enabling a modular approach to integrating more semiconductor devices with ever greater IO (Input/Output) density. It has become essential for various modern microelectronic applications, including AI and High-Performance Computing servers that require raw compute power with integrated high bandwidth memory and mobile devices that demand specific size, weight, and power requirements. These needs continue to drive its development. Advanced Packaging is a key innovation, often referred to as "More than Moore's Law," helping to keep the industry on the trajectory predicted by Moore's Law.

Integral to this packaging are interconnect process technologies. MKS has strategically expanded its portfolio of foundational solutions, acquiring Electro Scientific Industries, a leader in laser via drilling systems, in 2019, and Atotech, a critical provider of specialty chemistry solutions to uniquely enable next-generation interconnect formation, in 2022. The combination of these capabilities within MKS enables an accelerated time-to-market with a turn-key solution comprising MKS' Optimize the Interconnect® offering.

The purpose of this Handbook is to introduce the reader to the basics of Semiconductor Advanced Packaging and its process technologies, as well as the key products and applications that Optimize the Interconnect. As with our first two Handbooks, *MKS Instruments Handbook of Semiconductor Devices and Process Technology, 2nd Edition and MKS Instruments Handbook of Principles and Applications in Photonics Technologies*, we've learned from working alongside you for many decades and we hope you find this Handbook informative and useful. We welcome your feedback and input for future editions. Rapidly evolving technology will continue to shape and transform this industry in the years to come. MKS looks forward to addressing the opportunities and challenges this will present – together.

John T.C. Lee
President & Chief Executive Officer

About MKS Inc.

MKS Inc. enables technologies that transform our world. We deliver foundational technology solutions to leading edge semiconductor manufacturing, electronics and packaging, and specialty industrial applications. We apply our broad science and engineering capabilities to create instruments, subsystems, systems, process control solutions and specialty chemicals technology that improve process performance, optimize productivity and enable unique innovations for many of the world's leading technology and industrial companies. Our solutions are critical to addressing the challenges of miniaturization and complexity in advanced device manufacturing by enabling increased power, speed, feature enhancement, and optimized connectivity. Our solutions are also critical to addressing ever-increasing performance requirements across a wide array of specialty industrial applications. Additional information can be found at www.mks.com.

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Chapter 1

Semiconductor Packaging

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1.1 Introduction

A semiconductor package (component level/level 1) is the enclosure of one or more integrated circuit (IC) dies and serves as a bridge between the IC (chip level/level 0) and the next assembly level (board level/level 2), allowing for easy integration into electronic applications and systems (system level/level 3).

Figure 1 illustrates the main purposes of a package [1,2]:

- **Interconnect to the Next Assembly Level:** The package facilitates electrical interconnection between the die and the external circuitry at the next assembly level, enabling the flow of electrical signals and power.
- **Environmental Protection and Mechanical Support:** The package shields the semiconductor die from thermal, environmental stresses, and electrostatic discharge. It also provides structural support for the chip, ensuring it remains securely attached to the substrate or circuit board, improving its robustness, reliability, and lifespan.
- **Thermal Path Solutions:** Semiconductor devices generate heat during operation and the package must facilitate thermal transfer to dissipate the heat. Packages often incorporate heat sinks, thermal pads, or other thermal transport solutions that prevent overheating and allow the IC to function optimally, even in high-temperature environments.
- **Test and System Integration:** The package facilitates the integration of the chip into more complex electronic devices, allowing for easier handling and assembly at the next level of manufacturing as well as electrical testing.

Since the advent of semiconductor packaging technology in the 1950s, several thousand package types have evolved with two major trends standing out: the desire for ever higher input/output (I/O) channels and achieving the smallest possible device footprint. Early semiconductor devices were packaged using 'Transistor Outline' (TO) metal cans (Figure 1) or ceramic packages and simple wire bonding for electrical connections. As the industry evolved, there was a need for smaller, more reliable,

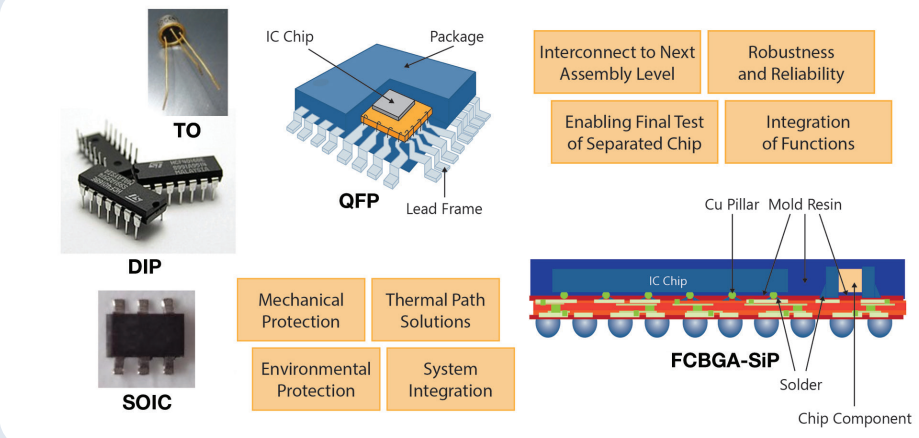

Figure 1. Basic construction and functions of a few standard (DIP, QFP, SOIC) and advanced (FCBGA) semiconductor packages. (Source: Steffen Kröhnert, ESPAT-Consulting, 2022 https://www.espat-consulting.com/)

and cost-effective packaging solutions. This led to the development of Dual In-line Packages (DIPs), which came to volume production in the 1970s. As shown in Figure 1, DIPs had a rectangular body with two parallel rows of pins that could be directly plugged into sockets on circuit boards. Later in the 1970s, Plastic Quad Flat Packages (PQFPs) with a plastic body replaced traditional ceramic packages. These had a smaller form factor, a lower cost and better manufacturability and could be surface mounted on printed circuit boards (PCBs). Also, PQFPs improved thermal and electrical performance. Further advances in surface mount technology (SMT) led to the development of small-outline integrated circuit (SOIC) packages with smaller footprints and improved thermal characteristics compared to DIPs.

Semiconductor dies became larger in the 1980s and 1990s, driven by the increasing functionality and I/O count needed for computing, networking, and storage application requirements. Chips with 1 million transistors were introduced [1], and packaging technology had to evolve to accommodate the significant increases in the number of I/O counts. Pin Grid Arrays (PGA) and Ball Grid Arrays (BGA) (Figure 6) became significant packaging modes. These featured an array of solder balls on the underside of the package that provided the electrical connections to the PCB. Such grid arrays improved electrical performance, reduced inductance, and enhanced thermal management, making them suitable for high-speed and high-density applications. In the 90s, the Chip Scale Package (CSP) was introduced to address even higher pin counts within a very compact size requirement. Wafer-Level Packaging (WLP) which provides the electrical connections and encapsulation of semiconductor chips before singulation, i.e. 'at the wafer level' gained traction in the 2000s. WLP introduced technologies such as Redistribution Layers (RDL) and Through Silicon Vias (TSVs) that enhanced interconnectivity and 3D integration. These marked the beginnings of what today is called 'Advanced Packaging'. As with most technologies, standard or 'traditional' packaging is not going anywhere but continues to be applied at scale for products where cost-effectiveness, reliability, and ease of manufacturing are the primary considerations. [2]

As the design costs of the most advanced semiconductor nodes increased exponentially and high yields for ever larger size chips at these advanced nodes became ever more challenging to maintain in the pursuit of maintaining Moore's Law, a 'new' approach gained traction as an attractive alternative which Gordon Moore already anticipated in 1965 [10]: "It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected." Where monolithic, traditional chips provide all functionalities on a single silicon die necessarily manufactured at the most advanced process technology node needed for its highest performing aspect, chiplets break down the capabilities of a chip into smaller, modular dies that have a reduced or singular function and are designed to communicate with each other [13]. This allows for heterogeneous integration [12]: different chiplets are to be manufactured using different process nodes, different semiconductor materials, and even different manufacturers, appropriate for their specific function, which may go well beyond 'just' digital and can include RF communications, sensors, actuators, etc. This 'functional diversification' that goes beyond the shrinking of physical feature sizes of logic and memory is referred to as 'More than Moore' [20]. This modular approach enables easier scaling and upgrading as not all components need to be redesigned for every generation. In conjunction with the better yield of smaller individual die sizes and older process nodes for some of the chiplets, a more cost-effective and faster time to market has opened [5, 6, 7, BCG2024 "Advanced Packaging is Radically Reshaping the Chip Ecosystem"]. A corresponding 'Heterogeneous Integration Roadmap' was developed by IEEE in 2019 and is regularly updated. [3]

Advanced Packaging has emerged as the critical, enabling technology capable of connecting these smaller chips and chiplets next to and on top of each other in a wide variety of architectures for 2.XD and 3.XD packaging. These new architectures provide very high bandwidth through higher interconnect density and shorter connections in cost-effective, compact packages that leverage ever more sophisticated interconnect, interposer, and substrate technologies.

1.1.1 Design and Manufacturing

Modern package design requires careful modeling and simulation to ensure that these performance characteristics are met, taking the interplay of all components including the die, substrates, and interposers into account (Chapter 1.2). Package manufacturing involves several critical steps employing a broad swath of material and process technologies:

- **Die Preparation:** The wafer is thinned to the required thickness, diced into individual dies, and then attached to the substrate or package.
- **Interconnect Formation:** This step involves creating electrical connections between the die and the substrate. Techniques include horizontal, e.g., redistribution layers (RDL), as well as vertical interconnects, e.g., Through Silicon Vias (TSVs).
- **Encapsulation:** The die and interconnects are encapsulated to protect them from environmental damage. This can be done using molding compounds or other encapsulation materials.
- **Substrate Attachment:** The encapsulated die is attached to a substrate, which provides mechanical support and additional electrical connections.
- **More Interconnects:** For certain packaging types, leadframes or solder bumps are formed to facilitate connections to the next level of assembly.
- **Testing and Inspection:** The assembled package undergoes electrical testing and inspection to ensure functionality and reliability.
- **Marking and Packing:** Finally, the packages are marked for identification and packed in trays, tape and reel, or other formats for shipment and integration into electronic devices.

1.1.2 Applications and Future Trends

Since their inception, smartphones and other mobile electronic devices have driven the integration of high-performance components into compact form factors using techniques like Fan-Out Wafer-Level Packaging (FOWLP) and System-in-Package (SiP). Advanced Packaging is essential for reliably and robustly connecting and integrating the manifold components, from Antenna-in-Package (AiP) systems that support higher frequencies for next-generation wireless communications (5G to 6G), to processors, memory, cameras, LiDAR, and other sensors.

Advanced Packaging has also become a key enabler for artificial intelligence (AI) and high-performance computing (HPC) as these applications require immense processing power harnessed across many interconnected chips, particularly to high bandwidth memory (HBM) (Figure 2), and efficient heat dissipation.

In the automotive sector, the shift towards autonomous and electric vehicles demands electronics that are not only powerful but also environmentally robust and reliable. Advanced Packaging ensures that these electronic components can withstand harsh conditions while maintaining high performance. Similarly, in the realm of biosensors and the Internet of Things (IoT), Advanced Packaging enables the integration of multiple functions into small, efficient packages, facilitating the development of compact and versatile devices.

Looking ahead, the future of Advanced Packaging is bright. According to a recent White House review [4], cited in [5] "…Advanced Packaging through heterogeneous integration will be critical as it… provides an alternative avenue for innovation in density and size of products." Moreover, "just as Moore's law led to the advancement of the global semiconductor industry over the past 55 years, heterogeneous integration is and will be the key technology direction going forward [6]."

Advanced Packaging has evolved into not just a complementary technology but a foundational one that supports the most advanced semiconductor technologies and is here to stay. Its role is critical in a world where electronic applications are ubiquitous and ever-expanding, ensuring that devices are more powerful, more efficient, and more reliable than ever before.

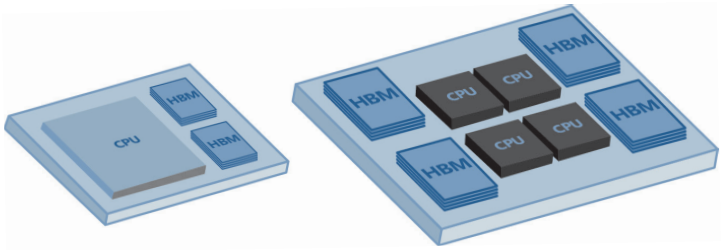

Figure 2. Multi-die system in a package with 3D stacked HBM.

1.1.3 Book Overview

The remainder of this handbook is structured as follows:

Chapter 1 provides a high-level overview of semiconductor package design and fabrication, as well as the associated roadmaps.

Chapter 2 covers packaging architectures and their nomenclature, interposer and interconnect technologies.

Chapter 3 discusses organic laminate IC substrates in terms of materials and process flows.

Chapter 4 goes into some detail exploring the process technologies necessary for IC substrate manufacturing, from the substrate core base materials and lamination, to via drilling, metallization and patterning, as well as metal deposition, circuitization, and final finishing.

Chapter 5 specifically addresses flip chip packaging and assembly in its various forms, their respective advantages and disadvantages, process flows and techniques, all the way to final marking, inspection, electrical test, and packaging.

Chapter 6 reviews wafer level packaging, both fan-in and fan-out in its various configurations, and its extension to panel level packaging.

Lastly, Chapter 7, presents the developments of integration in packaging from the monolithic System-on-Chip to System-on-Package, Package-on-Package, Heterogeneous Integration and Chiplets.

Throughout these Chapters, we point to specifically relevant MKS products in separately called out sections, except in cases where products are uniquely enabling process steps.

1.2 Semiconductor Package Design

While manufacturing technologies and designs may vary, all semiconductor packages must achieve certain minimal mechanical and environmental parameters:

- **Power Management, Efficiency, and Integrity:** Energy consumption in electronic devices is currently doubling every three years and device efficiencies are not keeping pace [5]. In advanced devices, power losses during transmission and conversion must be minimized. Designs for power delivery networks need to manage high current densities while minimizing voltage drops and ensuring adequate power to each component. Furthermore, maintaining stable and precise voltage levels is challenging, especially when different components may have varying voltage requirements.

- **Signal Integrity (SI):** Signal speed, noise sensitivity, and electromagnetic interference are becoming critical parameters due to the operating speeds of modern processors. Substrates that incorporate high speed interconnects are required to have a much lower dielectric constant than in the past. Noisy circuits can generate electromagnetic interference that can hamper the functionality of neighboring circuits. In some cases, interfering circuits may need to be separated from the other sensitive circuits by shielding the device or filtering the power and signal lines.

- **Heat Dissipation:** The heat generated during circuit operation can impact the circuit's functionality and reliability, if not properly dissipated. Proper package design must provide a path for thermal transfer that maintains the IC junction temperatures below the threshold value. A package's ability to dissipate a chip's operational heat directly correlates with device reliability.

Modern packages must be optimized to minimize device size/weight, power consumption and cost (SWaP-C). Therefore, the design phase for electronic devices now employs next-generation Electronic Design Automation (EDA) software (Figure 3, Figure 4) that can incorporate all needed components and physical parameters to predict system behavior and cost. EDA simulations incorporate a comprehensive multi-scale sign-off approach that simulates physical phenomena such as power optimization, signal integrity, electrostatic discharge (ESD) effects, electromagnetic interference/electromagnetic compatibility (EMI/EMC), heat transfer, fluid dynamics and structural mechanics across chips, packages, and systems.

EDA software cannot, however, address all the design needs for multiple point tools/software, many of these have separate user interfaces and models, or are supported on different platforms that make data sharing almost impossible. A unified platform is needed that offers tight integration of system level signal, power, and thermal analysis while delivering automated power, thermal, and noise aware optimization. A consolidated view of the entire system is especially important since the power and thermal analysis of an individual die in isolation is no longer enough in a multi-die environment.

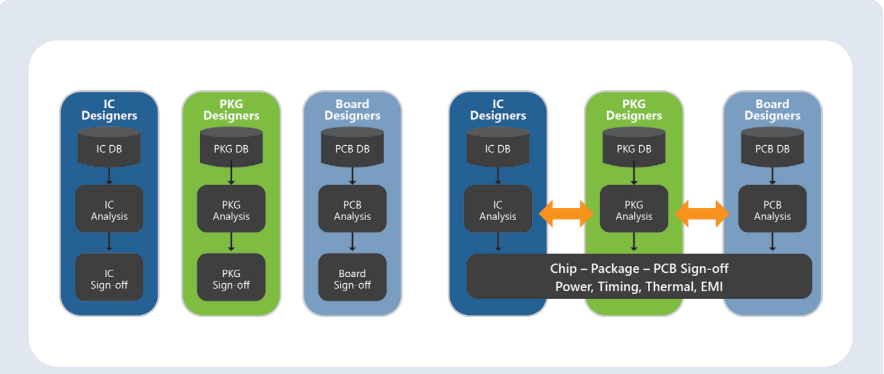

Figure 3. Traditional EDA approach (left) vs. modern chip-package-system flow (right).

1.2.1 Semiconductor Packaging Substrates

This discussion will focus on the classification of IC packages based on substrate type (Figure 4). The substrate serves as an intermediary that provides both mechanical support for the die and electrical connections to surrounding systems. This classification also includes two unique cases (i) where no substrate is used, and (ii) embedded die technology, which will be explored in this chapter. Three broad substrate classifications can be defined:

- **Organic Substrates:** These are made of organic materials such as FR-4, which is a glass-reinforced epoxy laminate, or other polymer materials. Organic substrates are generally cost-effective and offer flexibility in design. They provide good electrical performance for a wide range of applications and are commonly used in consumer electronics.
- **Leadframe:** A leadframe is a metal structure consisting of a central pad on which the die is placed surrounded by leads that connect the wiring from tiny electrical terminals on the semiconductor surface to the large-scale circuit connections on a circuit board (Figure 1). Leadframe substrates are typically low cost and offer excellent electrical and thermal performance. They have low design complexity and are easy to manufacture in bulk. They are suitable for various devices and applications from microcontrollers to power management ICs.
- **Ceramic Substrates:** These are often made from materials like alumina or aluminum nitride. They offer high thermal conductivity, exceptional electrical insulation, robustness, reliability and can endure extreme environmental conditions, including elevated temperatures. Ceramic substrates are typically used in aerospace, automotive, and military applications where design reliability is critical.

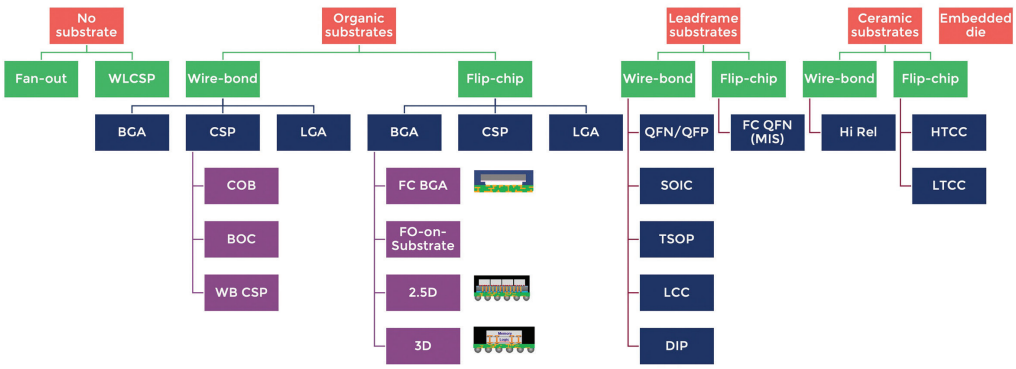

Figure 4. Types of packaging platforms based on substrate type [21].

Substrates are further classified by their distinct interconnect techniques, namely wire bond and flip chip technologies.

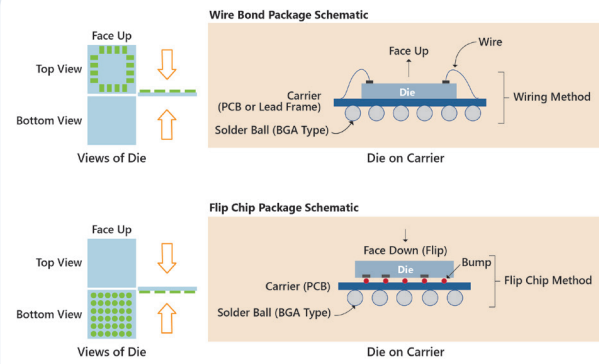

Figure 5. Wire Bond versus Flip Chip package schematic related to assembly and interconnect on substrate.

- **Wire Bonding (WB):** Wire bonding is the traditional IC packaging method which provides versatility to suit various applications, is cost-effective for low to medium productions and has established reliability for processes and equipment. It is an interconnection process that uses a thin wire, heat, pressure, and ultrasonic energy in a welding process to create an electrical interconnection between the die and its carrier and, ultimately, the outside world (Figure 5). Wire bonding is classified based on the bonding type (ball bonding, wedge bonding, ribbon bonding, heavy wire bonding), type of input energy used for joining (thermocompression bonding, ultrasonic bonding, thermosonic bonding), and wire material (aluminum, copper, silver, gold). The major challenge for wire bonding technology is its scaling limitation in meeting density and performance requirements.

- **Flip Chip (FC):** In the FC process, the die is placed directly on the substrate with the active surface at the bottom, without any further connecting wires i.e., the die is 'flipped' so that its top side faces down (Figure 5). In this process, solder "bumps" are first applied at electrical connection pads on the face of the chip. This allows for a higher pin count that can be achieved using wire bonding, reducing necessary die size, and optimizing signal integrity. Bump composition may be, for example, gold, a eutectic, lead, tin, or copper. The bumped die is flipped onto the substrate with its pads aligned with corresponding pads on the substrate, hence the name "flip chip." Bumps are bonded with the substrate pads by a variety of methods including thermosonic, and ultrasonic welding and thermocompression. Flip chip packages can be classified based on surface mount type that is employed, for example, Small Outline Integrated Circuit (SOIC), Small Outline Package (SOP), Quad Flat Pack (QFP), Plastic Leaded Chip Carrier, (PLCC), Ball Grid Array (BGA), Chip Scale Package (CSP) etc.

1.2.1.1 IC Packages with Substrates

- **Chip Scale Packages (CSP):** A Chip Scale Package is a surface mountable integrated circuit (IC) package that has an area not more than 1.2 times the original die area. IPC's (Institute for Interconnecting and Packaging Electronic Circuits) standard J-STD-012 for Implementation of Flip Chip and Chip Scale Technology states that a chip must be a single-die and have a ball pitch of not more than 1 mm before it can qualify as a chip scale package. Chip scale packages are classified as:
  - Customized leadframe based CSP (LFCSP)
  - Flexible substrate based CSP
  - Flip chip CSP (FCCSP)
  - Rigid substrate based CSP
  - Wafer level redistribution CSP (WL-CSP)

- **Ball Grid Array (BGA):** A BGA package is a type of surface-mount packaging that employs an array of metal spheres called solder balls for electrical interconnection. The underside of the package is used for the connections, where solder balls are attached to a laminated substrate in a grid pattern. This substrate has conductive traces on the inside that connect the die-to-substrate bonds to the substrate-to-ball array bonds, using wire bonding or flip chip technology. Land Grid Array (LGA) and Pin Grid Array (PGA) are variations on this type of package (Figure 6). LGA packages use flat contact pads, or "lands," on the bottom of the package. The corresponding contacts on the motherboard or socket interface with these lands establish electrical connections. PGA packages use pins protruding from the underside of the package, arranged in a grid pattern. These pins are inserted into corresponding sockets on the PCB.

- **Quad Flat Package (QFP):** This package type is a surface-mount technology that has a square or rectangular form, with multiple electrical contacts located on the bottom surface. Unlike traditional leaded packages, the QFP does not have any leads extending from its sides. It may include a central exposed pad that serves as a thermal relief and an electrical ground. QFPs offer a blend of advantages, including a compact footprint, good thermal performance, cost-effectiveness, and robustness however, they can present severe thermal management and soldering complexity challenges.

- **High-Reliability (Hi-Rel) Ceramic Substrates:** High-reliability ceramic substrates are typically made from alumina (aluminum oxide) or other ceramic materials and provide a rigid and thermally stable platform for mounting passive components and interconnects. They have excellent thermal conductivity and electrical insulation properties, making them ideal for use in high-power electronic modules, power amplifiers, microwave devices, and other applications that demand reliable operation in harsh environments.

- **Low-Temperature Co-Fired Ceramic (LTCC):** These substrates are manufactured using a low-temperature (<1000°C) firing process and offer advantages such as high integration density, excellent RF/microwave performance, and the ability to create 3D structures within the package. Radiofrequency (RF), microwave applications, and sensors are the common uses for this substrate type.

- **High-Temperature Co-Fired Ceramic (HTCC):** HTCC is similar to LTCC but is fired at much higher temperatures, often exceeding 1600°C. This high-temperature process allows for the use of specialized materials like alumina, aluminum nitride, or other ceramics that offer enhanced thermal and electrical properties. HTCC is preferred for applications where materials must withstand extreme temperatures, high power densities, and harsh operating conditions. This includes high-power semiconductors, automotive and aerospace electronics, and sensors for extreme environments.

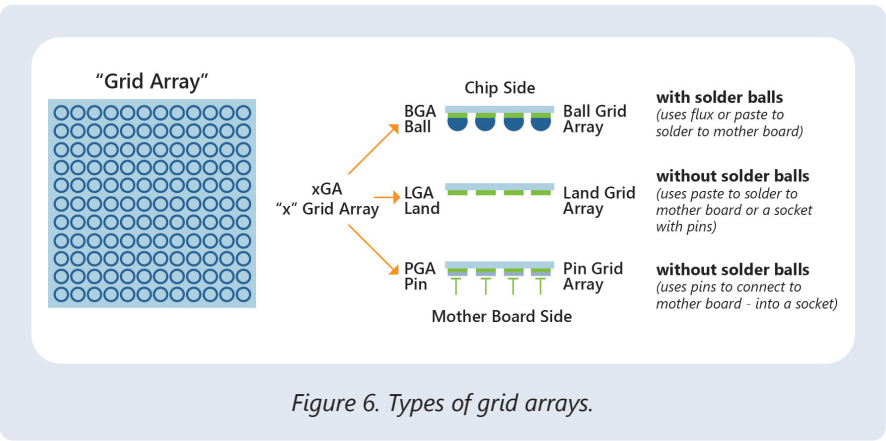

Figure 6. Types of grid arrays.

1.2.1.2 IC Packages without Substrates

Packages that do not employ a substrate use a production process that is referred to as Wafer Level Packaging (WLP). WLP packages the die while it is still on the wafer; that is, protective layers and electrical connections are added to the substrate before dicing. The sides of the die are not coated, resulting in a smaller size for the packaged chip which is obviously preferred for smaller device applications. WLP helps reduce manufacturing costs while allowing higher levels of integration. Figure 7 shows a comparison of WLP with conventional packaging process flow. WLP processes include:

- **Wafer Level Chip Scale Packaging (WLCSP):** WLCSP is the smallest package currently available. It is just a bare die with a redistribution layer (RDL) to rearrange the pins or contacts on the die so they are big enough and have sufficient spacing to be managed. The advantage of WLCSP is not only its cost-to-performance ratio, but also its small die size—making it one of the most popular packaging techniques in the industry. However, its small size becomes a limiting factor for the number of inputs and outputs (I/O).

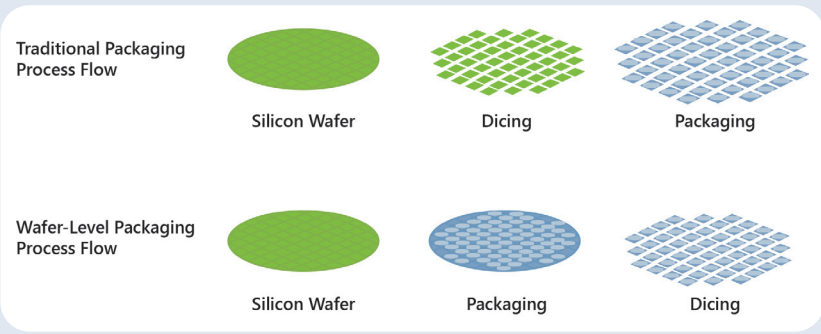

Figure 7. Packaging process flow: Traditional vs. WLP.

- **Fan-Out (FOWLP) and Fan-In Wafer Level Packaging (FIWLP):** FOWLP and FIWLP enable increased functionality, low power consumption, and more I/O with smaller technology nodes and smaller dies. They allow stable or limited shrinkability in the I/O pitch while using standard PCBs in the next assembly level. The key difference between FOWLP and FIWLP is the size of the interposer relating to the die (Figure 8). An interposer is basically an electrical connection, and its purpose is to extend or reroute a connection. An interposer on a die in FIWLP is usually the same size as the die itself, whereas in FOWLP the interposer is larger than the die.

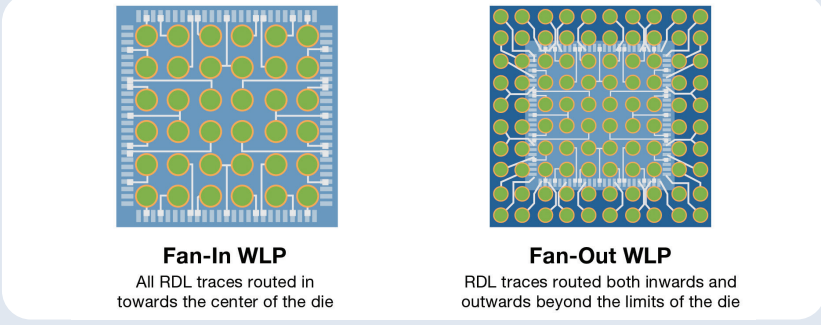

Figure 8. Fan-Out WLP and Fan-In WLP schematics.

1.2.1.3 Embedded Die Substrates

Embedded die substrates embed the die directly within a PCB or a leadframe substrate during its formation process. The die is connected to other components on the substrate using copper-plated vias and conductive traces on the substrate surface [7]. This allows for significant reductions in electronic device package size.

1.3 Evolution in Packaging Architecture

The need for increased speed and reliability in electronic devices has produced important, but limited, innovations in IC packaging over the past few decades. The advent of flip chip packaging technology in the mid-90s was particularly important since it introduced a new paradigm for making interconnections between the semiconductor die and substrates. Following the introduction of flip chip, innovative approaches that further increase I/O counts, speed, and reliability in chip packages have evolved. In particular, the development of silicon interposer and Through Silicon Via (TSV) technology has enabled 2.5D and 3D heterogeneous integration in advanced device packaging. These approaches have facilitated dramatic advances in device size, I/O, speed, etc., but at the price of significant increases in manufacturing complexity and cost (Figure 9).

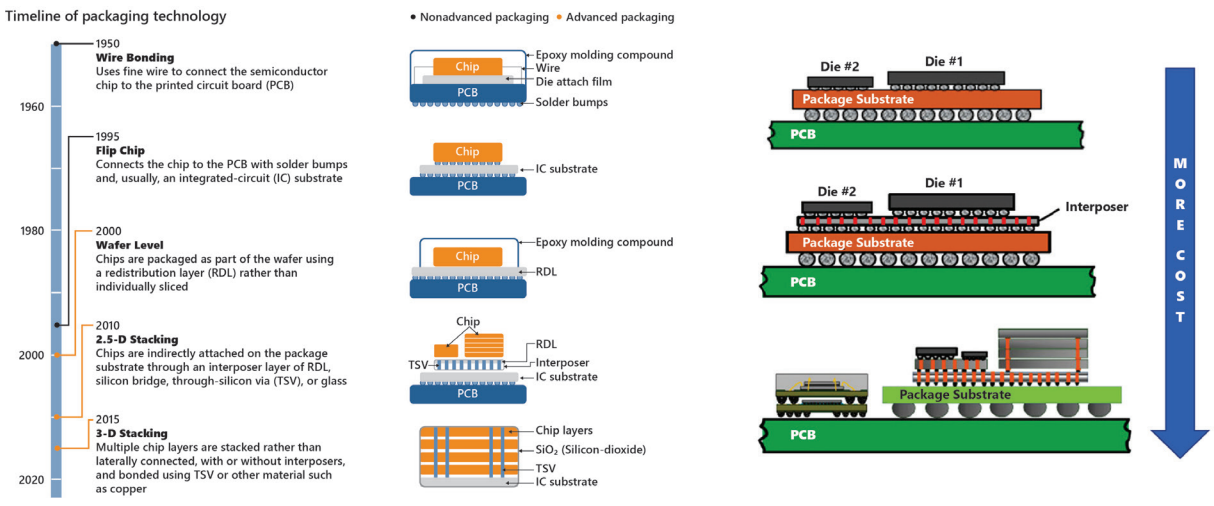

Figure 9. Increasing complexity and cost in packaging technology [22], [35].

Consequently, manufacturers continue to seek innovative interconnect bonding technologies that can reduce the cost of manufacture. For example, recent innovations in 3D integration use solder-free "bump-less direct bonding" interconnects between two die surfaces [8]. In a unique Thermal Compression Bonding (TCB) process, two die surfaces are joined so that the metal pad areas on each die are aligned. Once in contact, the TCB process is used to expand and join the die-to-die metal contacts to form an electrical connection while abutting dielectric surfaces on the two dies become bonded. This process has been labeled Hybrid Bonding. It is used extensively for device packages that employ chiplets to reduce the cost of manufacturing complex die. "Bump-less" interconnect technologies permit higher pitch scaling and reduce the cost of ownership compared to conventional bumping. Both Face-to-Face (F2F) and Face-to-Back (F2B) die orientations are supported, as described below. Figure 10 provides a schematic to assist in understanding the different terms used for advanced packaging schemes [9].

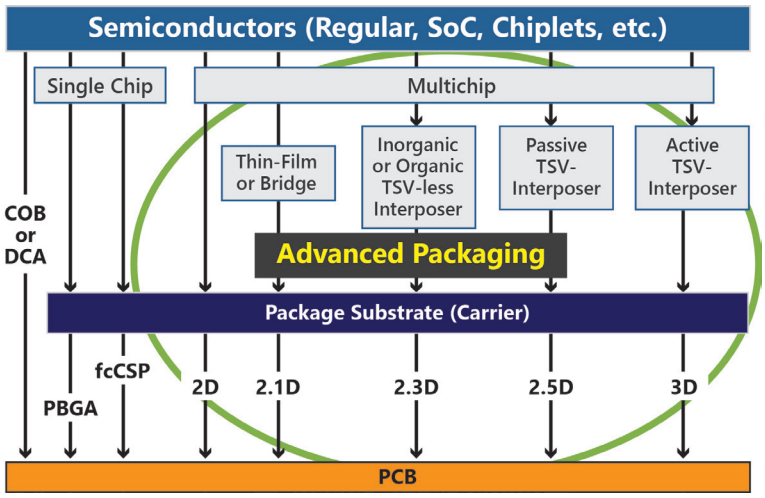

Figure 10. Advanced packaging definitions: 2D, 2.1D, 2.3D, 2.5D and 3D integration [9].

1.4 System-in-Package (SiP)

Packages that contain more than one chip and are designed to perform a specific task that can be a sub-task of a board, module or system, can be defined as a system-in-package (SiP). The development of SiPs is driven by application-specific requirements for the optimization of an intended function, e.g., mobile front-end / antenna modules, high performance computing chip sets, smart watch packages, etc. The availability of appropriate chiplets with needed functionality and integration capabilites are also factors that influence SiP design. There are many different SiPs available, each uniquely designed for a specific task.

The efficient connection of the various dies to each other and to the substrate is critical to the functioning of a SiP. While the most common interconnection processes remain wirebonding and Flip Chip (FC), continuing innovation has expanded the interconnection toolbox for SiP heterogeneous integration. Through Silicon Via (TSV), Through Mold Via (TMV), Through Glass Via ("TxV" in Figure 11) and Cu to Cu hybrid bonding have emerged as effective technologies for vertical interconnects. Innovations in horizontal or lateral interconnection, including redistribution layers embedded in dielectric interposers and embedded interconnect technologies such as the use of a silicon bridge die have facilitated the development of state-of-the-art SiPs.

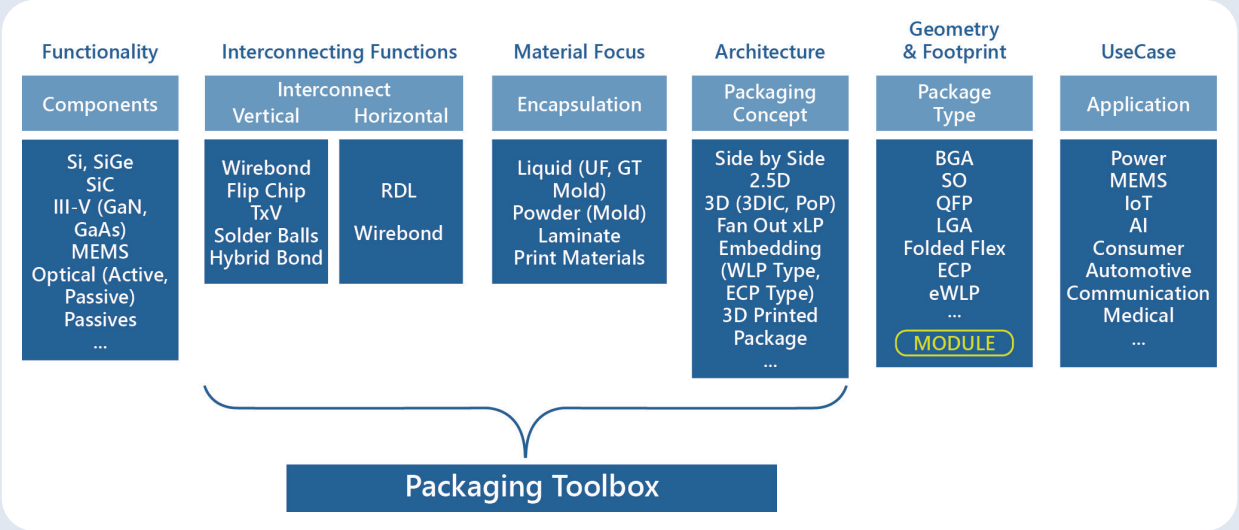

Figure 11. Concept of "Packaging Toolbox."

1.4.1 SIP Modules

SiP modules are designed to enable complete system performance in a single small form factor unit in which several packaged components may be present. The level of integration can vary, but for the most complex systems such as smart phone and smart watch applications it is considerable, with RF components, MEMS, AP, memory, power, battery, display control and passive components all integrated onto a small HDI or SLPCB substrate (Figure 12). Packing density in these modules is very high, with die-to-die spacing typically in the one hundred microns or less range. Additionally, all real estate on both sides of the substrate is fully utilized to reduce the factor. In some mobile applications, a vertical

"donut" spacer containing vertical interconnects may be used to stack and connect two substrates with mounted components. Packaging concepts for the subcomponents in mobile applications (e.g., the low noise power amplifiers (PA), RF filters, front-end modules (FEM), and antennae) have changed dramatically as bandwidth requirements have increased. 5G cellular communication protocols, especially, have produced significant changes in packaging technology, as can be seen from the RF Packaging Roadmap compiled by Yole Development (Figure 13). The requirement for bandwidth increases at shorter wavelengths and higher frequencies produced a greater need for the low-loss integration of RF components, typically through the use of better dielectrics and shorter interconnects with improved trace smoothness. It is logical, therefore, to integrate all RF front end module components into a single SiP type package directly coupled to the Rx/Tx antenna to maximize performance.

Figure 12. Apple Watch Gen 3, an example module type SiP.

Due to the increased atmospheric signal attenuation at 5G transmission frequencies, antenna design has simultaneously undergone drastic changes. From the traditional omnidirectional dipole antenna in use for 4G and older communication protocols, there has been a shift towards integrating patch-based phased array antennas which allow transmission beam focusing and steering to reduce overall energy required for mobile communications at distance. Modern packaging concepts have allowed a fully integrated approach of moving patch antenna into the same module as the FEM components.

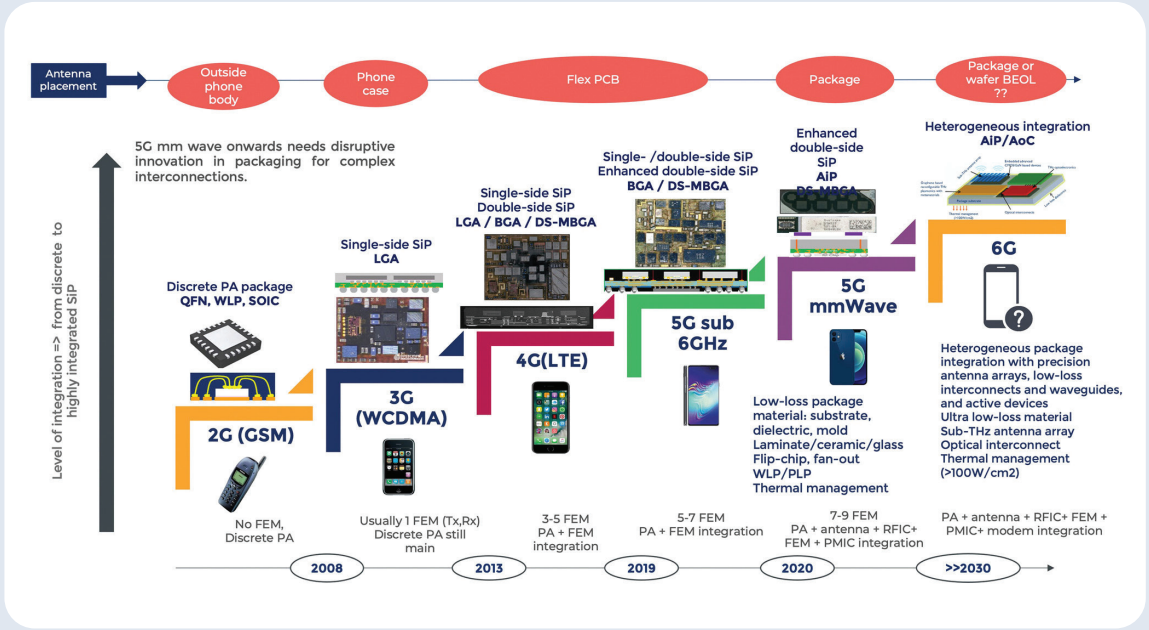

Figure 13. Mobile trends from 2G to 5G and beyond. (Source: System-in-Package report, Yole Group, 2023)

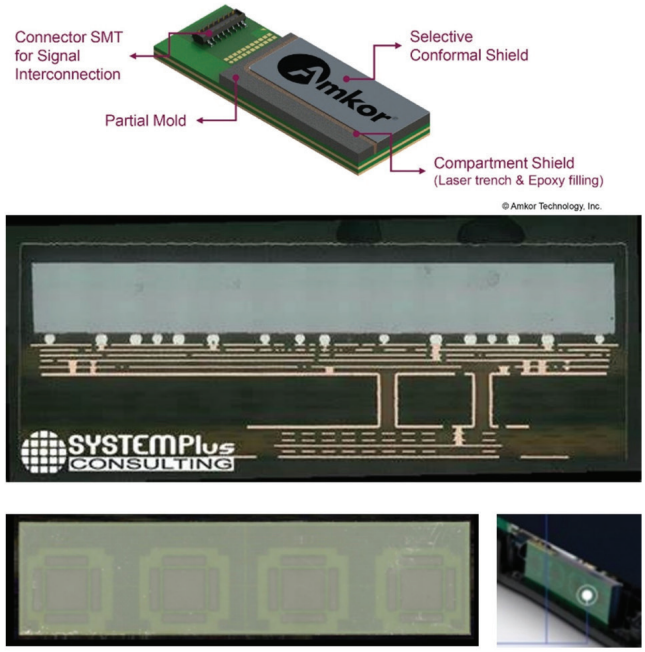

Figure 14. 5G antenna in package modules, showing overall structure (top) cross-section and antenna patch array (bottom).

A fine example here is the QTM052 mobile RF/FE Antenna-in-Package (AiP) module from Qualcomm, manufactured by Amkor, an outsourced assembly and test provider (OSAT). This first-generation mobile RF/AiP module, designed for 5G, consists of a SiP containing several chips for signal processing, conditioning, and antenna control, all integrated into a single molded package as well as a patch array antenna made on the opposite side of the same laminate substrate (Figure 14) [36]. The use of Ajinomoto build-up film as the supporting build-up dielectric allows excellent low-loss signal processing. A typical 5G compatible handset will contain up to five of these modules to enhance connectivity as the phased array patch antenna typically has a limited transmission cone. Additionally, the signal can easily be blocked by obstacles like walls, foliage, and even hands which makes the case for improved connectivity through several modules placed at the mobile handset case periphery [37].

Other OSATs such as ASE, SPIL and IDM/Assembly giants such as TSMC and Samsung also provide their take on AiP. The integration with laminate substrate had been a typical OSAT approach whereas the IDMs such as TSMC were, from their inception, leveraging their fan-out wafer level packaging technologies. The Integrated Fan-Out Antenna in Package (InFO_AiP) approach from TSMC claims to improve on the laminate approach by selecting different dielectrics and embedding the RF components into a mold compound which reduces package thickness, shortens interconnect path lengths, decreases overall thermal resistance and improves overall signal quality. The Fan-Out AiP approach has been followed by many OSATs to date.

1.5 PCB and IC Substrate Fabrication and Packaging

A printed circuit board (PCB) is the foundation of most electronic devices. The PCB is the framework where all components are assembled to form an electronic device. It provides the electrical and mechanical support to the circuitry. Essentially, the PCB uses copper traces/pads and conductive planes to route the signals/power to the different components associated with the product. Today's PCBs integrate advanced packages, surface-mounted components, resistors, capacitors, various sensors, and antennas/amplifiers based on its application, making the PCB the backbone of most devices.

PCBs can have a varying degree of electrical and mechanical properties. These properties are determined by the properties of the materials used in their fabrication. These include dielectric properties, Dk and Df, and CTE. Conductor thickness and length also play a critical role in signal integrity. Additional contributors are conductor roughness and the surface finish applied to the copper traces and the soldermask.

One of the key developments for the PCB has been the substrate materials the industry has accumulated in nearly a hundred years of history. The development of each stage of the substrate materials industry is driven by innovations in electronics, semiconductor manufacturing technology, electronic mounting technology, and electronic circuit manufacturing technology. Its development characteristics are mainly manifested in the resin, reinforcing materials, and insulating substrates. These have created the necessary conditions for the advent and development of the most typical substrate material for PCBs, the copper clad laminate.

There are different types of PCBs. The basic types are single layer (single sided) and double layer (double sided) which are ideal for simple electronic devices. Some PCBs are flexible, some are rigid. A flexible PCB enables the circuits to fold and bend into shape. Multi-layer PCBs are constructed with a core and built from alternating layers of conductive copper with layers of electrically insulating material. The number of layers in a PCB range from 1 to 40 layers with the multi-layer PCB being best suited for complex hardware.

While the industry continued to improve manufacturing processes for multilayer PCBs, high-density interconnect (HDI) PCBs arrived. Today, HDI PCBs are one of the fastest growing technologies in the PCB market. They contain blind and/or buried vias and often contain microvias of 60 - 70 micron or less in diameter. HDI has a higher interconnect circuitry density than traditional printed circuit boards. There are multiple types of HDI boards, through vias from surface to surface, with buried vias and through vias, two or more HDI layers with through vias and stacked vias, etc. By using HDI technology, designers now have the option to place more components on both sides of the raw PCB. Multiple via processes, including via-in-pad and blind via technology, allow for more PCB real estate to place components that are smaller, even closer together. Decreased component size and pitch allow for more I/O in smaller geometries. This means faster transmission of signals and a significant reduction in signal loss and crossing delays.

As the smartphone technology advanced from 3G to 4G LTE, the complexity of antenna configurations has made the RF front end take up more space in smartphones. In addition, the amount of data that needs to be processed has also grown enormously. So both of these needs have increased the number of components in a cell phone. Additionally, this has required an increase in battery capacity, which means that PCBs and other electronic components must be compressed. This has pushed HDI PCB toward thinner, smaller, and more complex processes achieving higher density and smaller form factor. A new printed circuit board, called Substrate-Like PCB (SL-PCB), was developed, reducing the volume of the mainboard by 30%, while all of the chips remained. The SL-PCB requires a more sophisticated manufacturing process, a modified Semi-Additive Process (mSAP), developed by PCB manufacturers and key supply chain partners such as Atotech. The more sophisticated manufacturing process allows for much finer line/space (L/S) dimensions to support the fine pitch BGA. Several years ago, 0.6 mm - 0.8 mm pitch

was applied in handheld devices. This generation of smartphones equips 0.4 - 0.3 mm pitch technology extensively due to the number of component I/Os and product miniaturization, which requires trace/spacing of 30/30 µm. The current HDI technology cannot meet this requirement any longer.

Originally, the IC substrate technology was developed from the HDI technology [38]. There is a certain correlation between both, but the technical threshold of an IC substrate board is much higher than an HDI or an ordinary multilayer PCB. Connecting the die and the printed circuit board, the IC substrate board is used as the middle interconnect. The IC substrate supports the routing of the die circuitry, with the PCB, and safeguards, supports, and reinforces the die, thereby giving it a thermal dissipation path. An IC substrate board can be seen as a high-end PCB, which has the characteristics of high density, high precision, high I/O, high performance, miniaturization, and thinness. It has higher requirements in a variety of technical parameters, especially the line width/line space parameter. Compared with ordinary PCB, there are many technical difficulties in IC substrate manufacturing.

A typical IC substrate is thin and easy to deform, especially when the thickness is less than 0.2 mm. To overcome this difficulty, breakthroughs have been made in plating thickness reduction, lamination parameters, and layer positioning systems to effectively control substrate warpage. In a word, an IC substrate PCB has more requirements than standard PCB and HDI PCB. The barriers of the IC substrate industry are high, not limited to the technical threshold. High technical requirements and numerous patent restrictions have created a high threshold of the IC substrate industry, and the barriers within the industry also include capital and manufacturers.

The verification system for an IC substrate manufacturer is stricter than for a PCB manufacturer, in relation to both the quality of the die and the PCB connection. Industry generally adopts the "qualified supplier system". This requires suppliers to have a sound operation network, efficient information management system, rich industry experience, good brand reputation, and the ability to pass strict certification procedures. IC Packaging substrate is the largest cost of IC packaging, accounting for more than 30%. The cost of IC packaging includes packaging substrate, packaging materials, equipment depreciation, and testing. Shown in Figure 15, the substrate landscape from the PCB to semiconductor is changing. The call for high IO/mm^2 density, increased computer processing, and larger silicon die, drives the advanced packaging industry. So, the substrate landscape is being pushed for shrinkage of lines and space, and to keep costs at a minimum. However, this shift is not simple and clearly requires considerable shift in technology, manufacturing methodologies, and capital investments. At the same time the substrate manufacturers must maintain process yield and reliability which becomes challenging.

Advancements of the substrate technologies cannot be kept in line with semiconductor technologies' advancements, as the resources and capital spend on substrate development is a fraction of those of the semiconductor industry. This gap is decreasing but at a very slow rate. Ultimately, it comes down to the total cost of the device. Cost also has to meet the expectations of the customer, so this gap will remain and the use of glass core technology in the IC substrate will help shrink this gap in the near future.

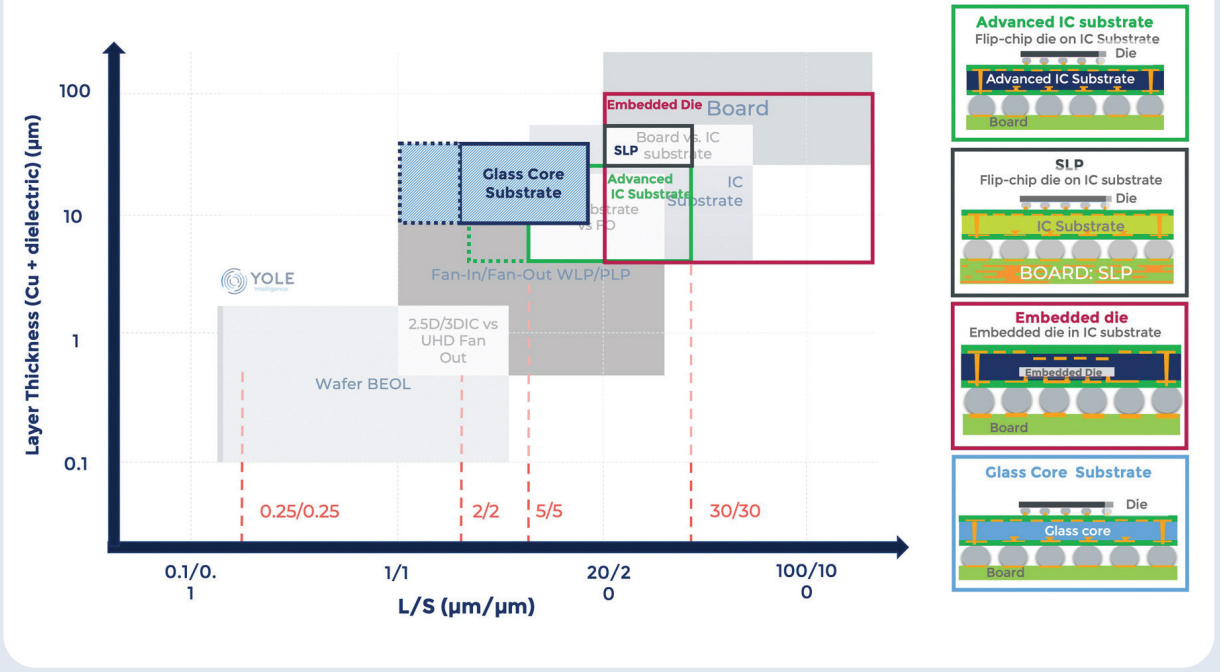

Figure 15. Substrate landscape showing the relationship of lines/space and layer thickness. (Source: Status of the Advanced IC Substrate report, Yole Group, 2024)

1.6 Technology Roadmaps

The first U.S. National Technology Roadmaps for Semiconductor (NTRS™) were developed in the late 1980s by SEMATECH, a consortium between government and the U.S.-based semiconductor industry, formed in Austin, TX in 1987. The first NTRS report was produced in 1994 followed by a revision in 1997. By 1998, the U.S., European, and Asian semiconductor industries had become much closer and an industry-wide team of experts from Europe, Japan, Korea, Taiwan, and the US began to collaborate on producing an International Technology Roadmap for Semiconductors (ITRS™). Beginning in 2001, the ITRS underwent nine revisions, the last published in 2015. It served as the main reference for development efforts in various areas of semiconductor device technology for university, consortia, and industry researchers. Recently, it has become clear that the industry is moving beyond conventional CMOS device technology. Consequently the semiconductor industry has reorganized its approach to these technology roadmaps. The Semiconductor Research Corporation has published the "2030 Decadal Plan for Semiconductors" [10] in 2020 with the goal to "outline(s) research priorities in information processing, sensing, communication, storage, and security." SRC extended this work in 2023 with the release of the "Microelectronics and Advanced Packaging Technologies Roadmap" (SRC-MAPT) [5].

The Institute of Electrical Electronics Engineers (IEEE) recently released an extension of the NTRS/ITRS that takes a more systems-oriented approach to a roadmap for future electronic devices. This "International Roadmap for Devices and Systems" (IRDS™) has the stated mission: "To identify the roadmap of the electronic industry from devices to systems and from systems to devices". This broad approach spans topics from devices to systems and from systems to devices, "in which the AI-centric IoT-social-infrastructures with high-speed network communication will be built on the semiconductor device and process technologies" [11]. It is intended to encourage innovation using non-traditional paradigms for system development and to encompass a broad scope of development directions for future electronic devices and systems (Figure 16).

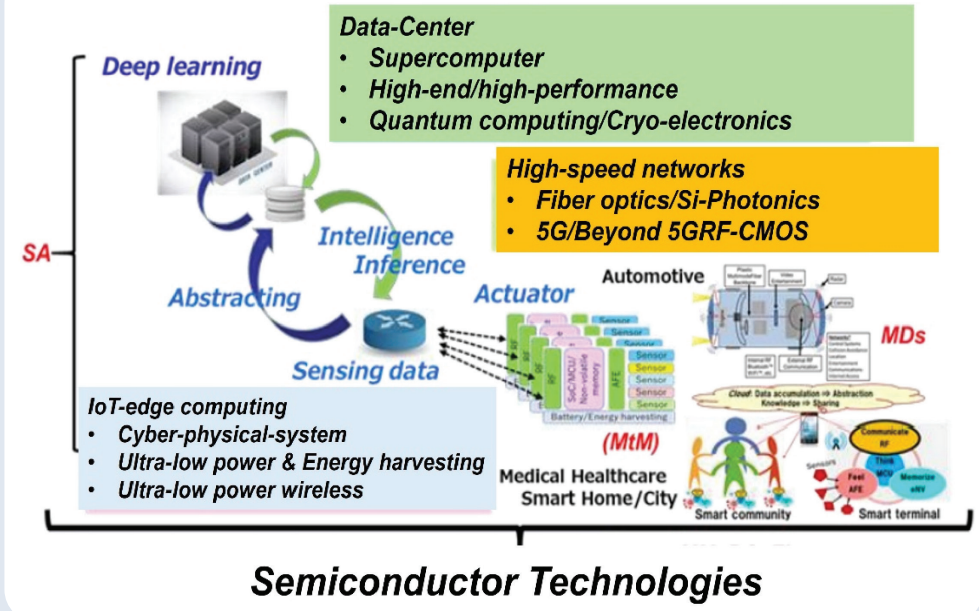

Figure 16. The scope of the IRDS roadmap.

This shift and evolution of the roadmap from the ITRS to the IRDS has translated to an expanded focus on systems. The IDRS has the following goals [11]:

- To identify key trends related to devices, systems, and all related technologies by generating a roadmap with a 15-year horizon.
- To determine generic devices' and systems' needs, challenges, potential solutions, and opportunities for innovation.
- To encourage related activities worldwide through collaborative events, such as related IEEE conferences and roadmap workshops.

The foreseeable technological innovations needed in future computing and sensing applications have been outlined in the SRC-MAPT and IRDS reports. Semiconductor packaging will evolve to include a range of technologies such as 2.5D/3D heterogeneous integration, chiplets, FOWLP, and SiP. Each of these offers an array of options for assembling and integrating complex dies in an advanced package, providing die customers with many possible ways to differentiate their new IC designs. The SRC-MAPT report especially emphasizes the need for intimate coordination throughout the design cycle for application-specific chiplet and packaging combinations (Figure 17). System architects must be involved in all phases of the design process to "analyze the system and packages, partition the design into various chiplets, and assess necessary tradeoffs in computing data movement and fabrication costs" [5]. This means that the relevant aspects of the packaging design must be considered during each step of the design cycle. This is a very different approach to the current one in which ASIC and package design phases are separate activities. Within this approach, there are many possible configurations, making design choices for a particular application very challenging even for the most sophisticated design teams. HI system designs will have to pay special attention to challenges in timing analysis for the chiplet-to-chiplet interface, thermal/mechanical stress analyses, and power delivery and integrity [5]. Intel, AMD, Arm, and all three leading-edge foundries are currently involved in the joint development of a new open standard for chiplet interconnects which is named Universal Chiplet Interconnect Express, or UCIe. The UCIe will enable very fine pitch I/O and L/S circuitry for chiplet interconnects. This new standard will facilitate the achievement of the fundamental performance requirements of higher bandwidth and efficiency in future electronic devices.

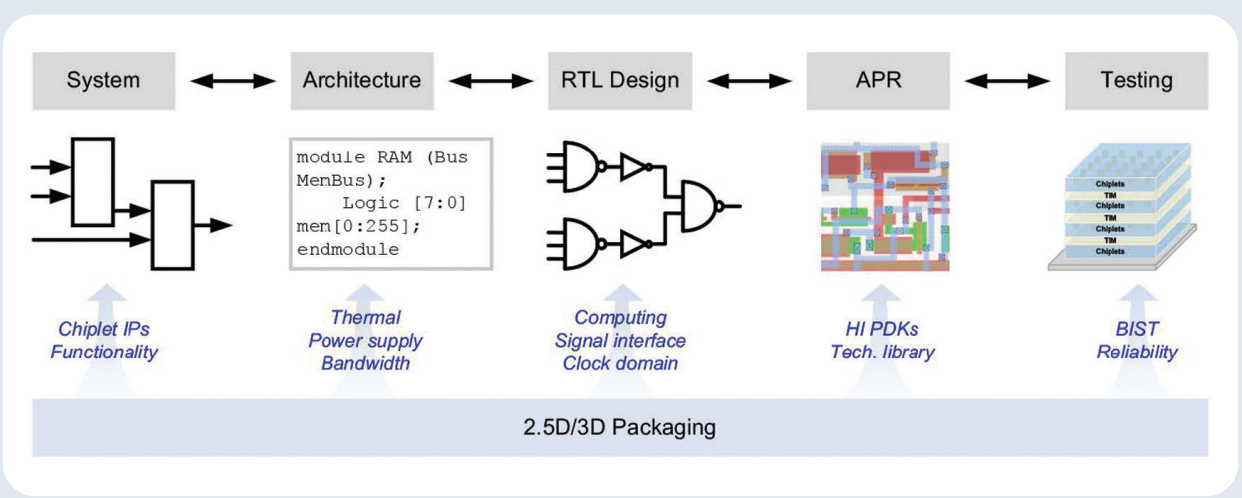

Figure 17. SRC-MAPT concept for the workflow of a chiplet-package co-design [5].

Advanced packaging concerns are thus playing a bigger role across the semiconductor industry. Networking equipment, servers, smartphones and even watches are among the applications that are adopting advanced packaging approaches. While not all chips require advanced packages and most chips are assembled and housed in mature and commodity packages, even for these products, IC vendors still seek new packages with smaller form factors and better electrical performance.

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Chapter 2

Packaging Architecture, Interposers, and Interconnect Technologies

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2.1 Introduction

An "interposer" is something put in between two structures that fulfills a function. Interposers in advanced IC packages fulfill two primary functions. They accommodate mismatches in the thermal expansion characteristics between different component levels and they provide a physical interface that translates the pitch of the chip I/O to the pitch of the substrate on which the chip or chip aggregate is integrated. Figure 1 shows an advanced IC package that uses a silicon interposer to accommodate differences in Coefficient of Thermal Expansion (CTE) and I/O count. The figure on the right shows the "Reliability Pyramid" that can be followed in cases in which there is a strong CTE mismatch between the chip (very low CTE) and PCB (high CTE). Interposer technology has been developed for flip chip (FC) and for multi-chip modules designed for High Performance Computing (HPC) applications. Most often, interposer technology is used with expensive high-density PCBs (component pitch down to 300 µm possible); standard PCBs allow for component pitches of typically 600-800 µm and larger. The first section of this chapter will review the technologies associated with leadframes, silicon interposers, organic interposers, glass interposers, and the use of embedded bridges. Note that embedded bridges are not a true interposer technology but serve as a pitch translation bridge that circumvents less capable substrate technologies. It can be used to complement both interposer and substrate technologies.

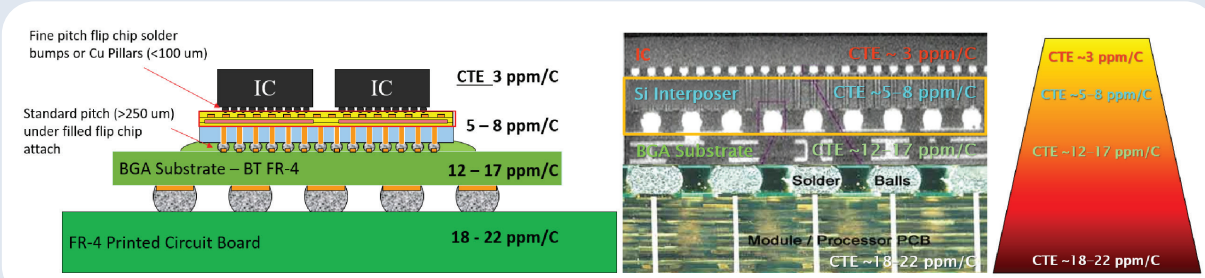

Figure 1. Interposers accommodate transitions in CTE and I/O pitch. (Source: Phil Marcoux, Managing Director, PPM Associates)

In the second section of this chapter, we will review the different interconnect technologies that are used to form the electrical connections between the components, interposers, and substrates. We will first review wirebond technology (Figure 2), followed by discussions of more advanced methods such as redistribution layers (RDLs), microvia, microbumps, copper pillar, through silicon via and recent innovations in thermal compression bonding and hybrid copper-to-copper bonding. The latter two technologies are slated for use in the next generations of advanced chip stacking designs. Wafer-to-wafer and chip-to-wafer bonding schemes will be reviewed in the final sections of this chapter.

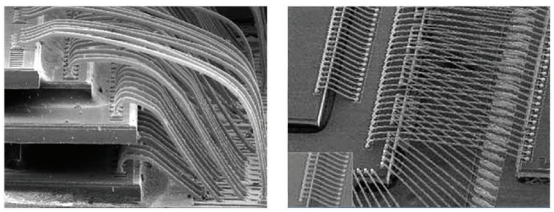

Figure 2. Examples of advanced wirebond technology [67].

2.2 Packaging Architecture

2.2.1 2D Architecture

In 2D architectures, all active and passive devices are mounted side-by-side and interconnected on a single plane on the surface of either an organic or an inorganic substrate. Devices may be embedded into the core or buildup layers of the substrate. FO (Fan-Out Level) and Fan-In WLP for Package-on-Package (PoP) are also categorized as 2D. For all 2D architectures, all electrical connections need to pass through the substrate.

2.2.2 Enhanced Architectures

Architectures intermediate between 2D and full 3D (2D Enhanced Architecture, Figure 3), have historically been labelled using 2.XD nomenclature, where X = 1, 3, or 5 (Figure 4). 2.1D architecture is defined as fabricated, employing fine metal L/S on build-up package substrates; 2.3D is fabricated as a coreless organic/inorganic architecture on a build-up substrate with the addition of a Controlled Collapse Chip Connection (C4) layer; 2.5D structures add a passive TSV interposer which is attached to the package substrate; reference [1], pp 249, 257, and 299, respectively). IEEE's Heterogeneous Integration Roadmap [2] has recently proposed an alternative nomenclature for enhanced 2D architectures as "2DX" where "X" = O or S denotes either an organic or a silicon or glass interposer (Chapter 2.3). In this discussion, we will use 2.XD nomenclature. 2D enhanced architectures introduced the use of an interposer layer between the substrate and the die to either spread out the connectors or to re-route the connections between multiple chips in, for example, 2D FCBGA architecture. Typically, these organic build-up layers are directly manufactured on the First Level Interconnect (FLI) side. Figure 4 shows an example of a 2.1D enhanced packaging architecture.

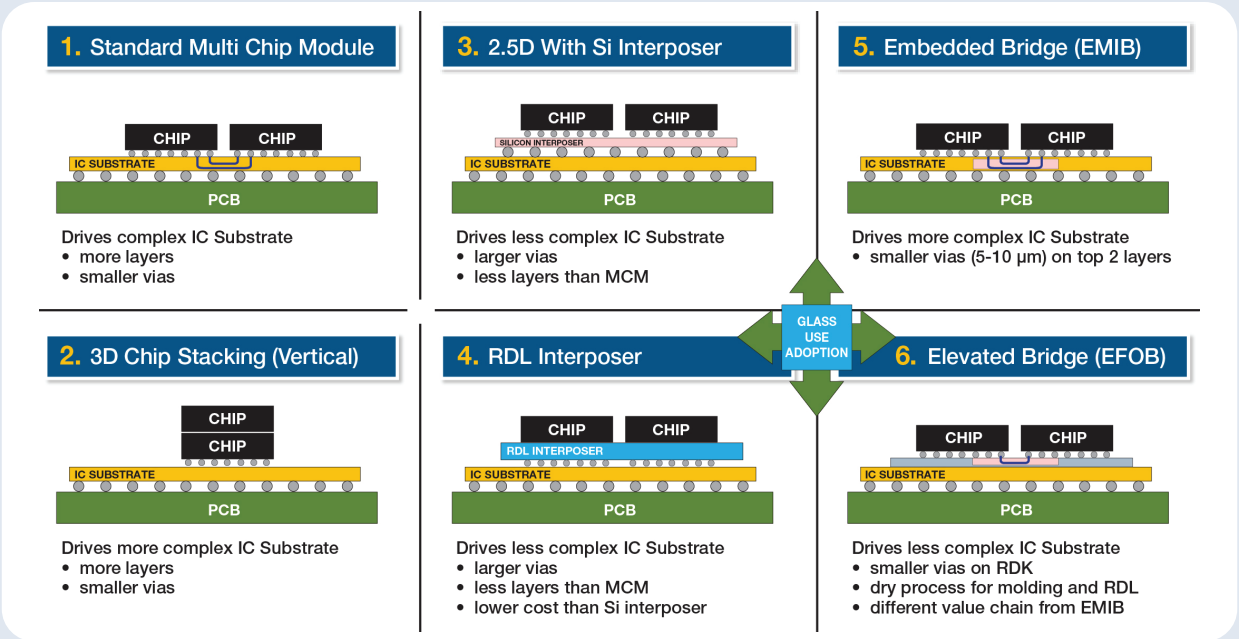

Figure 3. Overview of various package types.

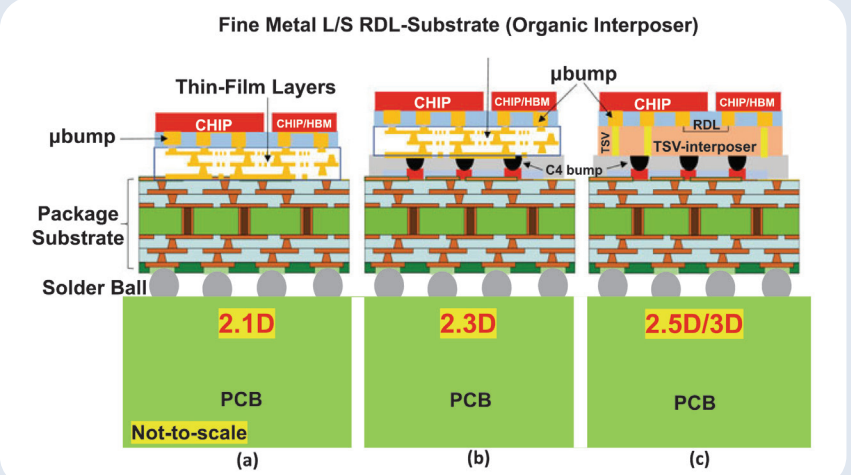

Figure 4. Classification of 2.XD enhanced 2D architectures [1].

2.5D architectures exhibit features typical of both 2D and 3D integration. 2.5D employs silicon, glass, or organic interposers for interconnect scale matching between the semiconductor devices and the organic substrate. Through Silicon Vias are used to achieve ultra-fine pitch wiring and logic and stacked memory devices are mounted in the same plane on the interposer [3] [4] [5].

2.2.3 2D/3D Architectures - Classification and Nomenclature

A 2D architecture is defined as an architecture where two or more active silicon devices are placed side-by-side on a package and are interconnected on the package. If the interconnect is "enhanced", e.g., has higher interconnect density than mainstream organic packages, it is further designated as 2.XD, X=1, 3, 5. The distinguishing features of the different 2.XD architectures are described in Section 2.2.2. A 3D architecture is defined as an architecture where two or more active silicon devices are stacked and interconnected without the agency of the package.

The advent of 2.XD and 3D technology has led to a wide variety of implementations of these paradigms with multiple configurations using fan-outs, fan-ins, System-In-Package, etc. currently in the technology space. To avoid confusion as this technology continues to develop, IEEE has developed a comprehensive classification framework for these architectures based on a common set of metrics that clearly differentiate the different types of 2D and 3D constructions [6]:

- Number of wires per millimeter exiting the die edge (the key metric for comparing 2D architectures)
- Speed of data transmission (Gbps)
- Process differentials (Chip-first vs. Chip-last)
- Areal interconnect density (Bumps/mm^2/Bump pitch (µm))
- Power delivery resistance (Less resistive/Highly resistive)

Table 1 provides a broad overview of different architectures for various applications described in the literature.

Architecture Type	Typical Application	Dielectric			Conductor		Tightness Patch	Typical Interconnect		Advantages
		Material	Loss Tangent (tan δ)	Thickness	Material	Thickness		Material	Process	
2D	Automotive, LCD drivers, sensors, ASIC's, controllers	std. organic DE	0.005-0.01	15-20 µm	copper	15-20 µm	25 µm	wire bonding	wire bonding	Low cost of ownership, Flexible process, easy to test/rework wire-bonds
2D and 2D enhanced	CPU, GPU, FPGA, network servers, gaming, console servers	enhanced organic (photo, laser)	0.002-0.005	3-10 µm	copper	3-12 µm	20 µm	microbumps, C4s, TSVs, passive interposer	TCB, mass reflow	Packaging enables high performance; multifunction HI (e.g., ASIC + HBM)
3D (die-to-die, die-to-wafer)	AI, HPC, AR/VR, 5G	inorganic (SiO_2)	≤ 0.001	0.5 µm	copper	1-2 µm	5 µm	microbumps, TSVs, Cu-CU bonding	F2F, F2B direct Cu-Cu bonding	Pitch scalability
3D (wafer-to-wafer)	AI, HPC, AR/VR, 5G	---	---	---	copper	1-2 µm	0.9 µm	solder bumps, Cu-Cu bonding	F2F, F2B direct Cu-Cu bonding	High 3D interconnect density with ultra-low bonding latency

Table 1. Examples of typical applications as a function of the different packaging architecture and process/material attributes [7] [5].

2.3 Interposer Types

As defined in the introduction, ''interposers'' are the ''in-between'' structures that connect two interconnect levels and spread connections to a wider pitch and/or reroute connections. Before we explore more advanced 2.5D silicon, organic, and glass interposers, as well as embedded dies, we provide a detailed baseline with the classic 2D leadframe process flow. Organic laminate IC substrates are discussed in detail in Chapter 3 and glass core laminates in Chapter 4.3, while the historic treatment of ceramic laminate substrates is beyond the scope of this handbook.

2.3.1 2D Leadframes

Overview

While not always identified as such, leadframes constitute the most common form of interposer used in semiconductor packaging. Most semiconductor chips are still packaged in standard package types such as Small Outline Integrated Circuits (SOICs), Quad Flat Packages (QFPs) or Quad Flat Pack No Leads (QFNs) (Chapter 1). All of these are built on alloy metal (e.g., Cu, FeNi, etc.) leadframe structures in which the chip is attached in the center of the frame (Figure 5). The die can be placed on the die pad of the leadframe either above or below the leads of the leadframe (see right-hand schematic in Figure 5). Wirebond lead attachments are also possible with both "stacked die" and flip chip assemblies in leadframe packages (Figure 6). The chip and leadframe are encased in a mold so that only the lead ends (outer leads) protrude from the package.

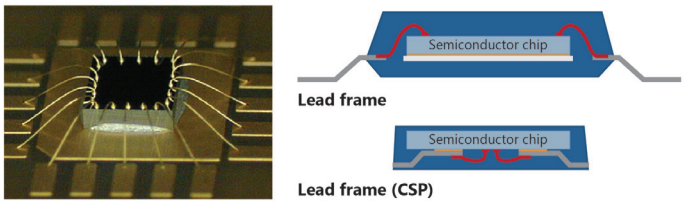

Figure 5. Traditional chip in leadframe package.

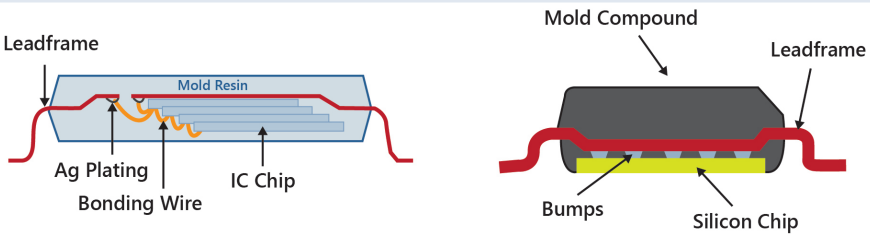

Figure 6. Wirebonding with stacked die (left) and flip chip (right).

A minimum of two different surface finishes are needed on leadframes: one finish makes the leads compatible with the wire bonding process that attaches the wires that connect the leads to the chip bond pads.

The second finish is applied to the outer leads that accept solder as the means of attachment and connection between the lead and the PCB. Wire bondable surface finishes are typically composed of copper, silver, nickel-palladium-gold, or nickel-gold stacks while solderable surfaces are usually based on tin.

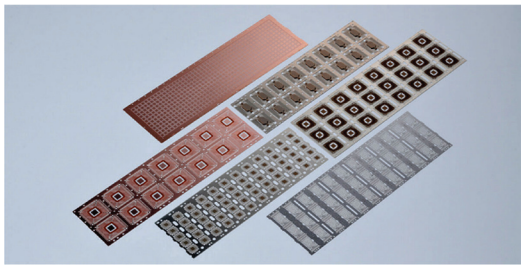

Figure 7. Different kinds of leadframe strips in various metals.

Leadframes are supplied in strips, as shown in Figure 7. Most are fabricated from copper-based alloys (e.g., C194 brass, C70250 copper-nickel alloy, or MF202 bronze). Figure 8 shows a representative process flow for the coating processes used with copper leadframes. The leadframe is first cleaned, then plated with a fresh copper strike that promotes silver adhesion and silver is plated on those parts that need to take up the wire bonds. Following this procedure, the leadframe is coated with an additional adhesion promoter ensuring that the metal surface will adhere to the mold material that is to encapsulate the package. The leadframe receives a coating ("anti-epoxy") that minimizes problems with epoxy bleed onto the leadframe in the subsequent die attach process. The die is then attached to the center pad using epoxy glue and the epoxy is cured.

Following die attach and cure, the electrical connection between lead and chip is established using wire bonding. The package is then molded (typically in a transfer-mold process), cured, and excess mold epoxy removed. Dedam and dejunk steps remove the shortcut between the leads (so-called dam bar, Figure 7), which acts as a mold barrier, and residual mold junk between package body and the cut dam bar.

At this stage, only the terminals of the leadframes and the back of the center pad are free of mold material. These parts are tin plated, protected, and cleaned prior to package singulation. Singulation cuts through the leads and opens an uncoated flank of the lead that is again plated with tin and protected. The package is then ready for mounting onto a PCB. All processes are performed using automated, high-speed tools, with most processes completed within a few seconds (except for epoxy removal).

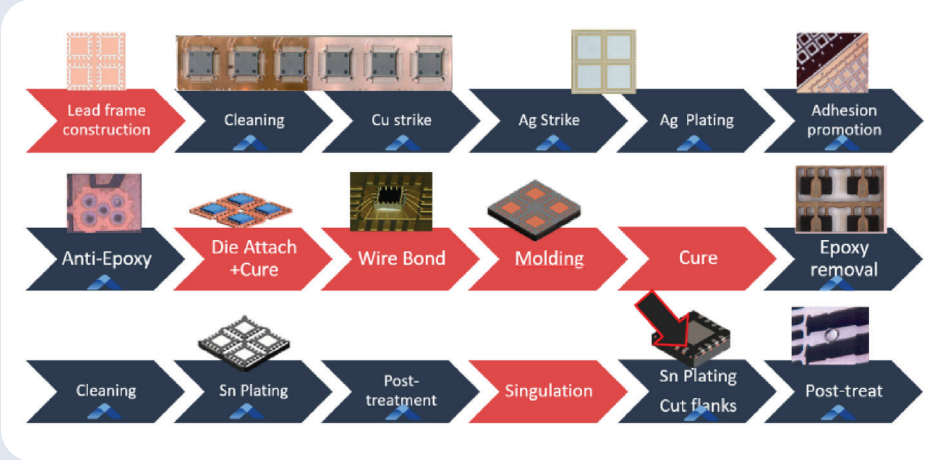

Figure 8. Process flow of Ag spot plated Cu leadframes. All blue sequences require surface treatments.

Etched leadframes are also available. For lower volumes or special design requirements, stamped leadframes may not be a good solution (cost, long lead times and design rule restrictions with stamping tools). The shape of the leads is also different for stamped and etched leadframe. Sidewalls are flatter with stamped leadframes, while the surface for wirebonding is flatter with etched leadframes; stamped leads have a more rounded surface and some burr on the bottom.

Stamping

Leadframe patterns (Figure 7) can be created in blank metal bands by etching or, in most cases, by stamping. Stamping is a high-speed mechanical process that is done reel-to-reel and cut into strips later. It is a very complicated, costly multi-step punch process, with up to 10 punches with different punch tools needed to produce one leadframe. Leadframe production is normally outsourced to specialized producers. No chemicals are associated with the stamping process other than the oil used to lubricate the stamping tools.

Leadframe Manufacturing

Cleaning

A typical cleaning process for leadframes includes three steps. A soak cleaner, an electro-cleaning step, and a mild etchant. These cleaning processes:

- Remove oil and dirt from the stamping process.
- Remove insoluble smut from the base material composed of Si and Fe compounds that are formed during the alkaline cleaning step.
- Remove oxide layers.

Additionally, an electropolishing step can be applied, especially if the stamping process created burrs. Figure 9 shows the impact of an electropolishing step for removal of burrs on the edges of the leadframe structures.

MKS' Atotech Cleaning Products:

- **Puronon RTR**: alkaline cleaner that can be used as soak cleaner and electro cleaner.
- **Electroglow**: an anodic electropolishing process for copper alloys with smut removal capacity.

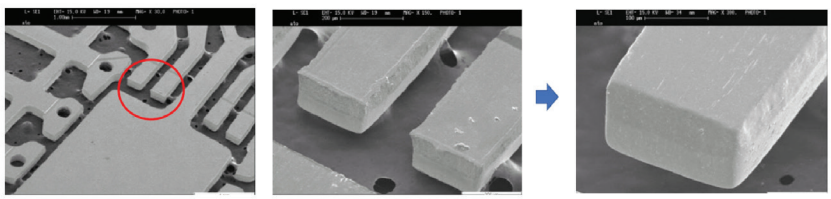

Figure 9. Electropolishing effect (right) on leadframe structures with burrs (left and middle).

Copper Plating

A thin (1-2 µm) layer of pure copper ("Cu strike") that ensures good adhesion of the subsequent, thicker metal film to the base material is applied. This layer also acts as a diffusion barrier for zinc when the leadframe is fabricated from brass. As well, the Cu strike layer may be used to planarize irregularities in the leadframe material. This layer is normally applied in a high-speed process (up to 5 µm/min).

MKS' Atotech Copper Plating Products:

- **Cupracid HSR Plus** – acidic, non-cyanide high speed copper plating process

Silver Plating

Silver plating is used to deposit a wire bondable surface on the leadframe. Silver film may be plated over the entire leadframe or on only the landing pads for the wire bonds (selective silver plating). The latter process is preferred simply due to cost savings. The deposition process uses cyanide-based electrolytic solutions that do not contain hardener metals. It is an extremely fast process (up to 1 µm/s) that produces a 2-4 µm thick, soft silver surface (70-90 HV). During silver plating, traces of silver may be deposited on unwanted areas. This silver must be stripped using a specific silver stripper prior to subsequent processing of the leadframe. A protective layer containing an organic thiol is applied to the freshly plated silver surface to keep it from tarnishing. Figure 10 shows an image of a leadframe that has undergone selective silver plating.

MKS' Atotech Silver Plating Products:

- **Silvertech HS** – High speed pure silver-plating process with low amount of free cyanide
- **Silvertech LED** – Highly reflective silver deposit for LED leadframes
- **Argatex 8000** – Electrolytic silver stripping process for copper base materials
- **Argalin T** – Chromate-free aqueous emulsion that deposits a monolayer of thiols to prevent tarnishing

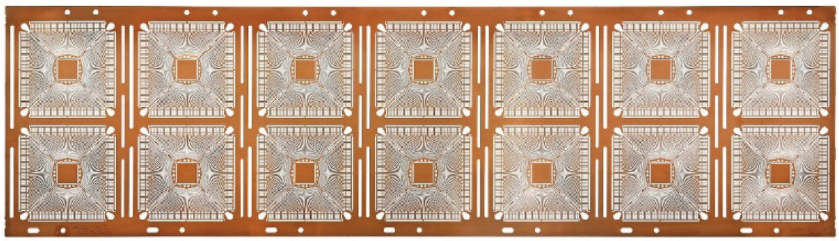

Figure 10. Selective silver-plated leadframe.

Adhesion Promotors

Heat and humidity can produce delamination and corrosion of the metal in the leadframe when the bond between the mold material and the metal is not strong. Consequently, strong adhesion between the mold material and the metal of the leadframe is critically important to device function. Adhesion can be improved by modification of the surface structure of the leadframe (roughening) and/or by creating a chemical bond between the two materials. There are industry rating systems for how long parts can

be exposed to ambient conditions before being soldered, and for the use of adhesion promotors aids in meeting high temperature and moisture sensitivity level (MSL) specifications. Meeting these specifications is particularly important for devices that are used in the automotive industry. The most common adhesion promoter process is roughening of the copper surfaces that are not covered by silver. In this process approximately 1 µm is etched from the copper surface and a rough organometallic surface layer is created that bonds very well with common mold materials.

Exposed silver surfaces also need adhesion promotors to optimize wire bonding. In this case, roughening is cost-prohibitive and non-etching chemical adhesion promotors are preferred.

MKS' Atotech Adhesion Promotion Products:

- **Moldprep HMC** – a copper roughening process for all common leadframe and mold materials. Easy to apply either in dip or on spray tool.
- **AgPrep** – a unique non-etching adhesion promotor that produces chemical bonds between silver and mold materials.
- **ppfPrep** – a unique non-etching adhesion promotor for leadframes that use stacked Ni-Pd-Au for wire bonding.

Die Attach Overview

Die attach, also known as Die Bonding or Die Mount, is the process of attaching the silicon die to the die attach pad of a supporting structure such as a leadframe. The performance of the die attach procedure can profoundly influence the functionality and reliability of an electronic device. A variety of processes are employed for die attach, including:

- Epoxy Die Attach
- Soft Solder Die Attach
- Flip Chip Die Attach
- Eutectic Die Attach
- UV Die Attach
- Thermocompression Die Attach

The most commonly used die attach process is Epoxy Die Attach and we discuss one important issue with this process below. More in-depth discussions of die attach processes are available on the internet [8] [9]. The next process step is wirebond which is an interconnect technology and, as such, will be described in Section 2.4 of this chapter.

Anti-Epoxy Bleed Out

A droplet of epoxy glue is used to attach the die to the center pad of the leadframe. Chemical components of the epoxy can slowly leach out of this droplet and spread over the leadframe surface as shown in Figure 11. This often happens with roughened copper surfaces, and it creates problems for the subsequent processes such as tin plating.

MKS' Atotech Anti-Epoxy Bleed Out Products:

- **AntiEBO T14** – a neutral treatment used before chip attach to prevent epoxy bleed out. Fully compatible with bonding processes.

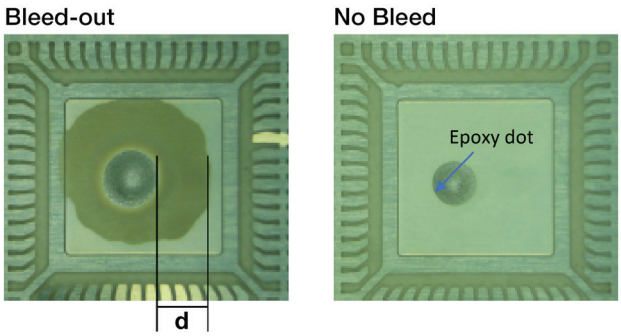

Figure 11. Bleed-out from an epoxy-based glue dot on a leadframe that has been cured for 30 min at 175°C (left); similar epoxy dot showing no bleed-out after treatment of the leadframe surface with an anti-epoxy-bleed out chemical (Anti-EBO) (right).

Molding

Following die attach, an over-molding process is used to protect the wired IC from mechanical and environmental damage. An epoxy-based mold compound is employed as it is cost-effective and offers the desired mechanical strength. Specialty mold compounds with fillers such as aluminum and silver are sometimes used to improve heat dissipation. The encapsulants are applied using injection or transfer molding in cavities (the molds) that contain the IC package. These are filled with liquid (heated) epoxy under pressure, allowed to cool to harden the epoxy, then opened to release the encapsulated IC package (Figure 12). The mold mass covers the entire chip except for the outer leads that are needed to attach the package to the printed circuit board.

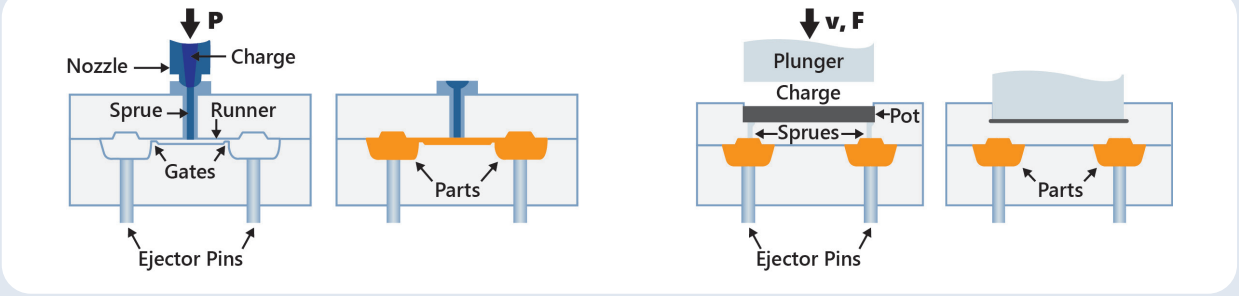

Figure 12. Simplified injection and transfer molding process.
Molten epoxy mass is injected or pressed into cavities which contain the IC package.

Mold Removal – Deflashing

During the molding process, material can be deposited on unwanted areas. These traces of mold (flashes) must be removed using a combination of chemical and mechanical steps known as a deflashing process. The first step subjects the whole molded package to a chemical swelling process. Swelling and

softening affects the thin flash residues much more than the thick mold capsule. A subsequent etch step physically and chemically degrades the flash material at the boundary between the base material and the mold, without significant damage to the mold. The degraded flash material is removed using a high-pressure water jet (200-400 bar) that attacks the weakened flash but not the thick mold capsule around the chip. Figure 13 shows flash at the edges of a pattern and the same area after the deflashing process. The freshly etched copper surface is protected from further oxidation in a subsequent post treatment step.

MKS' Atotech Deflashing Products:

- **Deflash GR1** – a chemical immersion treatment for swelling and softening mold flashes.
- **Descabase Cu (DM)** – a mild acidic etchant that attacks copper base materials.
- **SuperDip Cu 1000** – an organic treatment to suppress re-oxidation of copper surfaces.

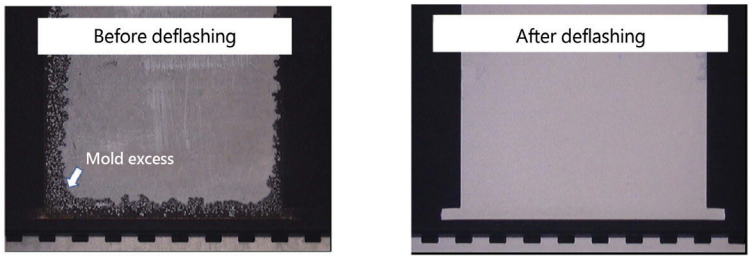

Figure 13. Mold excess (flash) at the edges of a pattern (left); the same area after the deflashing process (right).

Tin Plating

Most packages use a layer of tin (with some dopants) deposited on the outer leads to create a solderable surface. Tin-lead deposits are substituted for tin in some critical safety related products (e.g., aviation). These solder-compatibility layers must produce perfectly solderable surfaces with low potential for solder whisker formation.

In tin deposition processes, MSA-based high speed electrolytic processes are used to produce semi-bright or matte tin layers of 5-7 µm thickness. Low whisker propensity is achieved using high deposition rates of >10 µm/min that produce layers of very pure tin with a large grain structure (Figure 14). Immediately following tin plating, the tin layer must be protected with an anti-tarnish treatment since leadframes are often transported to the outsourced assembly and test providers (OSATs) before they are soldered onto a PCB. Specific anti-tarnishes have been developed that make the tin surface hydrophobic to suppress moisture adsorption. This helps to avoid oxidation and corrosion.

Singulation for Leadless Leadframes

Singulation for leadless leadframes is performed by dicing, punching, or etching. These processes all leave some exposed base material (copper alloy) at the flanks of the outer leads. Figure 15 shows examples of the singulation of a QFN by punching and dicing. Punching creates a smear of soft tin over the copper flanks while dicing leaves clean exposed flank surfaces.

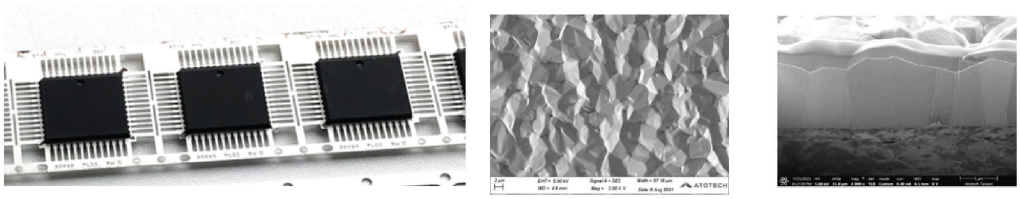

Figure 14. Tin deposition on the outer leads (left); tin layer surface structure (middle); and tin layer grain structure (right).

Tin Plating on Open Flanks

The open flanks that are present after singulation (Figure 16) can lead to soldering issues since the copper oxidizes and solder material may not properly adhere to it (de-wetting) [68]. Therefore, an electroless tin plating process in which copper is chemically replaced by tin needs to be performed to coat these flanks. This process requires pre-processing that etches and cleans the flank surfaces. The electroless plating process deposits roughly a 1.0-2.0 µm tin, including an intermetallic layer of Cu/Sn.

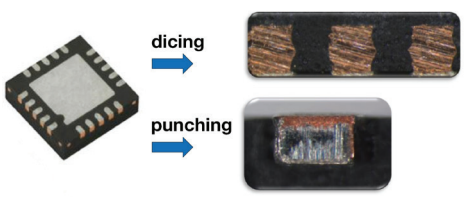

Figure 15. Singulated QFN after punching or dicing showing exposed base copper [54].

MKS' Atotech Tin Plating Products:

- **StannaQ Etch** – Alkaline etching pretreatment step prior to the immersion process.
- **StannaQ Protect** – An acidic clean for copper and copper alloys.
- **StannaQ 2** – A two-step immersion tin deposition process. A conditioning step deposits a dense, void-free first layer of tin which is reinforced by a second immersion tin deposition process. It employs a special anti-whisker additive.
- **StannaQ Post-Dip** – Protects fresh tin surfaces from tarnishing and preserves solderability.

Soldering processes for the assembly of the device on a PCB mainly use lead-free solders that are screen-printed onto the PCB. The IC package is accurately placed on the PCB using pick-and-place machines and the package leads are completely covered by the solder during a reflow process. Figure 17 shows an example of perfect solder joints with a QFN.

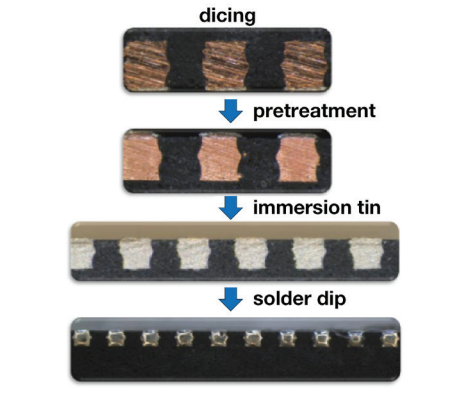

Figure 16. Open flanks after dicing, pretreatment, immersion, and protection and finally after solder dip.

2.3.2 2.1D Organic Interposers

2.1D is an IC integration scheme that enables fine metal L/S (down to 2/2 um) by adding thin-film layers (eHDF – embedded high density film) on a typical build-up package substrate (e.g., FC-BGA). 2.1D architectures typically include either a core [10] [11] or a stiffener layer (e.g., JCET's Ultra Fine Pitch Organic Substrate - uFOS) [12] to keep the substrate sufficienctly flat during the manufacturing process for yield, as well as handling and reliability.

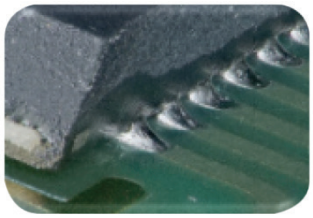

Figure 17. Perfect solder coverage of leads for a QFN package.

Unlike 2.3D and 2.5D, there is no additional interposer layer connected via C4 (or C2) bumps between the package substrate and the chip that enable further pitch reductions to the chip layer.

2.3.3 2.3D Organic Interposers

Recently, there has been a focus on development of alternatives to TSVs due to the high cost of silicon interposers. While solutions such as embedded bridges offer a high die-to-die connectivity, the complexity of bridge embedding and the limitations imposed by standard package substrate process technologies negatively impact overall package yield. Similarly, package substrate technology does not lend itself to flip chip assembly of HPC aggregates due to the limits of line/space sizes inherent in the semi-additive process (SAP - Chapter 3). Organic RDL technologies offer several cost and performance advantages in HPC applications. SHINKO Japan employs an organic RDL stack in the "i-THOP®", integrated Thin film High density Organic Package HPC application, Figure 18 [13]. I-THOP employs a thin film RDL stack on a coreless substrate that is bonded to an organic package substrate through solder interposers. The thin film RDL and coreless substrate form the organic interposer and are pre-assembled on the package substrate in a chip-last, known good die (KGD) assembly process. The elimination of TSVs in this approach offers similar connectivity to embedded bridge and some silicon interposer technologies at a lower cost. Additionally, organic RDLs provide superior performance in high frequency applications than silicon interposers. Drawbacks to RDL technology include reduced mechanical stability for larger multi-chip modules and CTE mismatch between organics and Si chip sets. To enhance mechanical stability and reduce overall package warping, metal stiffener rings are employed in larger multi-chip modules.

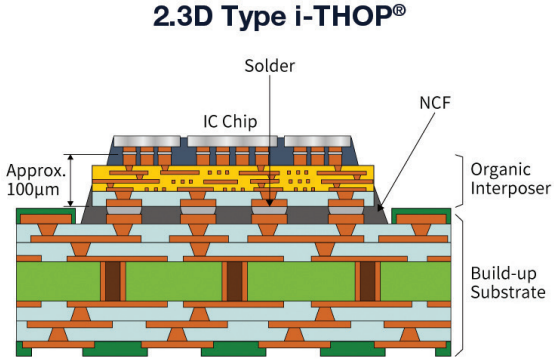

Figure 18. Schematic cross-section of i-THOP® substrate organic interposer after flip chip assembly [13].

TSMC also employs a lower cost organic alternative for HPC applications, using a Fan-Out RDL to assemble Multi-Chip Modules (MCM). Their InFO (Integrated Fan-Out) RDL/organic substrate (InFO_R/oS, Figure 19) assembly route offers 5 RDL layers with 2/2 µm lines/spaces to match the connectivity that that EMIB, for example, can provide.

Further application of TSMC's RDL technology can be found in their CoWoS®-R design (Chip-on-Wafer-on-Substrate, Figure 20). It differs from InFO_R in that it has several silicon dies – in this case HBM - that are 3D stacked rather than assembled side by side. Both InFO_R and CoWoS-R are made using a chip-last assembly

process in which the RDLs are made first on a carrier then the chips are assembled and underfill is applied. The assembled chips are then over-molded, after which excessive mold is ground away to reveal the chip backside.

Another integration scheme developed by TSMC uses a molded interposer containing embedded Si bridges (Local Silicon Interconnect, LSI) made using a 0.4 µm L/S silicon damascene process. In this process, the RDL is fabricated on a carrier, tall copper pillars are plated for vertical connections, then silicon bridges are assembled on the RDL. The pillars and silicon bridges are sealed in an over-mold, and the mold compound is ground back to reveal the Cu pillars and Si bridges. Finally, several RDL layers are built for the flip chip assembly. This approach has the advantage of using silicon bridges without the need for embedding them into the package substrate, while the mold compound offers additional mechanical stability for the assembled package.

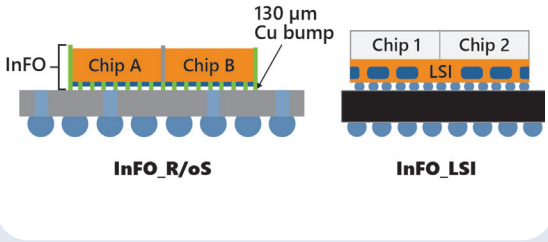

Figure 19. TSMC's InFO_R/oS and InFO_LSI [44].

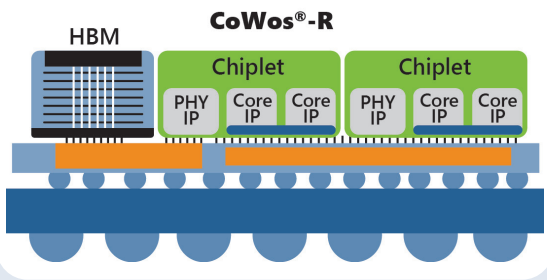

Figure 20. TSMC's CoWoS®-R [44] [48].

There are several OSATs and integrated device manufacturers (IDMs) that have their own approach to using organic interposers in advanced packaging applications. For additional information, see Samsung's R-Cube, ASE's FOCoS-B and, in particular, SPIL's FO-EB (Fan-Out Elevated Bridge) which optionally adds TSVs for local power delivery. The use of silicon bridges to enhance the organic RDL interposer appears popular, especially for HPC applications, and will remain with us for the foreseeable future.

2.3.4 2.5D Organic Interposer - Special Form - Embedded Die (Si Bridges, EMIB)

HPC has been and remains a major driver in advanced packaging technology. Development of the next generation of hardware for applications such as artificial intelligence, data centers, 5G infrastructure, cloud computing, and autonomous vehicles will rely on an ability to generate, process, and store exponentially increasing amounts of data at ever increasing rates. The key metrics for the packaged technologies in this sector relate to cost, power usage, performance, and reliability. Much of the burden for meeting these metrics in heterogeneous integration designs has fallen on advanced packaging methodologies; significant efforts are underway to employ these methodologies in growing bandwidth capacity and increasing energy efficiency in system modules.

Currently, dies are bonded to a laminate package substrate using flip chip methods. The substrates typically have an FR4 organic/woven glass fiber core for stiffness and a layered build-up of dielectric resin/glass filler films such as Ajinomoto's build-up film (ABF) series. The on-package die-to-die as well as the off-package interconnections to the main PCB are part of the core and build-up. As such, they are limited by the manufacturing technologies developed for such substrates. For example, currently the most advanced package substrates in high volume production are made with a 9/12 µm Line/Space (L/S) in the final layers of the build-up. The design rule for this approach limits the number of lateral on-package die-to-die I/O connections (breakout density) to just about 50 per mm per layer of build-up.

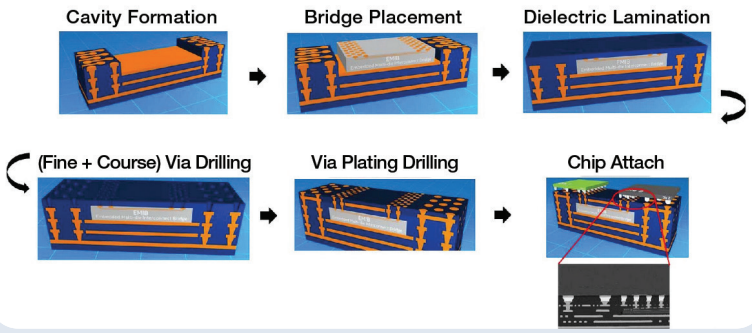

Figure 21. EMIB process flow [51].

Adding more build-up layers that fulfill the finest L/S design rules can imperil overall package substrate yield in a technology that is already highly cost sensitive. Nevertheless, die-to-die communication speed is critical to overall system performance, and it is imperative that an interconnect technology is developed that enables a roadmap to much higher I/O densities with standard package substrate technology. Intel was the first to come up with a solution to this problem – the Embedded Multidie Interconnect Bridge (EMIB). This approach embeds a thinned-down silicon die with several layers of silicon back-end damascene interconnects into the top layers of the package substrate. The embedded die is covered with a standard ABF layer and Soldermask, and vias, lines and solder bumps on the package substrate side are used to connect the EMIB to the flip chip solder bump array (Figure 21, Figure 22).

Die-to-die I/O can be established more efficiently using Intel's EMIB, since well-proven damascene technology can be used to achieve much smaller L/S dimensions at high yield. At a L/S specification of 1 µm, the total I/O per mm per layer exceeds 500 and this reaches 1000 per mm per layer in a typical 2-signal layer EMIB design (Figure 23). Further decrease in linewidth is easily achieved with silicon backend processes, allowing continued scaling to meet future needs.

Bandwidth is highly dependent on I/O length. For this reason, it is important to minimize the link length on the EMIB by keeping the on-chip die-to-die pads close to the chip edges. This design criterion constitutes the main limiting factor for continuing the EMIB roadmap since the connection between chip and substrate is achieved with vias that are laser drilled in the top ABF layer and Soldermask [14]. These vias are produced using standard semi additive process (SAP) technology and are therefore limited in minimum pitch capability. Currently Intel is using a mixed pitch bump array on the substrate and chip sides: 90 µm pitch for the C4 array that connects to standard package substrate technology; 55 µm and less for the bumps connecting to the substrate pads that connect to the EMIB. Intel's roadmap calls for further reducing via and pad sizes to connect to EMIB as existing limitations on I/O density are mostly a result of large pad sizes.

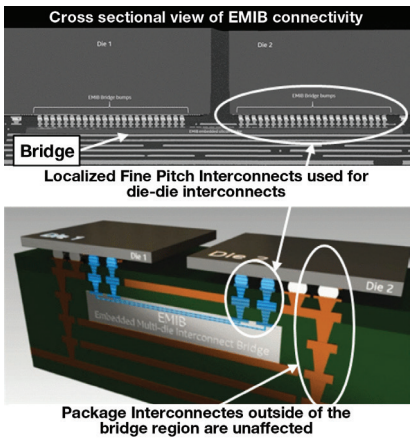

Figure 22. EMIB embedded in package substrate showing multi-pitch bumps on the first layer interconnect and chip side [52].

These limit the area density of vertical connections to the EMIB and take up valuable real estate on the silicon dies. Via and pad size reduction is expected to be a challenge as significant improvements are needed to standard laser drilling methods and to the accuracy of EMIB embedding and flip chip processes. Additionally, having a mixed pitch bump array can produce issues in terms of differences in the total plated solder availability between small and large pitch microbumps. This can give rise to a non-coplanar bump array during the FC bonding process.

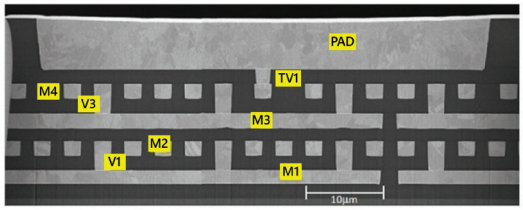

Figure 23. FIB/SEM cross-section of Intel's EMIB Si bridge, showing two signal layers (M2 and M4) surrounded by GND (M1, M2/V1, M3, M4/V3) [51].

TSMC and OSATs like SPIL/ASE embed the silicon bridge into a mold compound interposer. In addition to allowing through-mold vias, these methods can be built up with standard Fan-Out RDL technology. The approach is cost-effective, with clever re-use of several IP blocks that reduce lithography constraints. In addition, it is possible to embed passive components into the mold compound.

TSMC's Integrated Fan-Out Local Silicon Interconnect (InFO_LSI, Figure 19) is one example. SPIL's bridge technology is like TSMC and is in production with AMD as the Elevated Fan-Out Bridge (EFB). Their approach to the mold compound interposer is marketed as Fan-Out Embedded Bridge (FOEB) and, according to SPIL, offers several advantages in cost and complexity over the Intel EMIB approach (Figure 24). Figure 25 shows a typical process flow for a molded interposer with embedded silicon bridges.

IBM has employed silicon bridges in its Direct Bonded Heterogeneous Integration (DBHi) technology. In DBHi, a silicon bridge die is embedded in the package substrate and bonded to the dies before placing the assembly on the package substrate. Another essential difference is the use of microbumps to connect

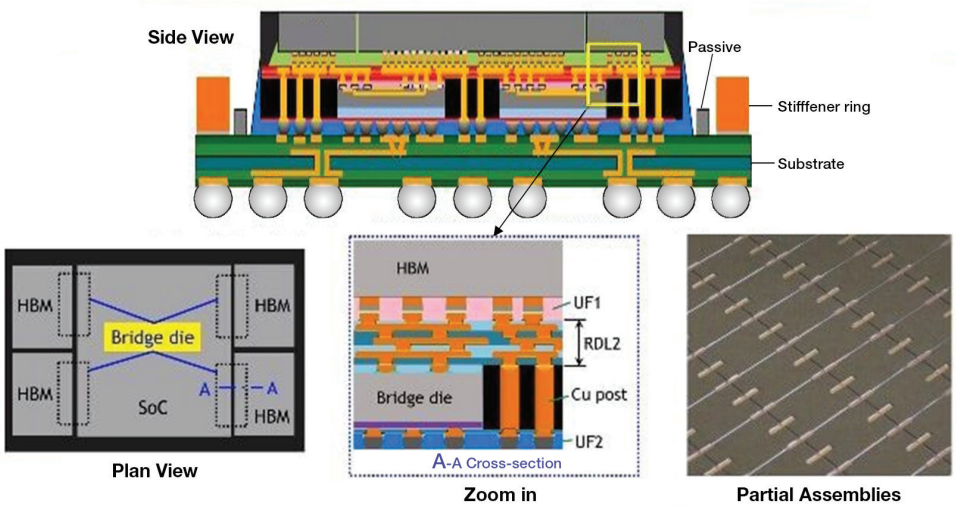

Figure 24. SPIL's Fan-Out Embedded Bridge (FOEB) [49], [50].

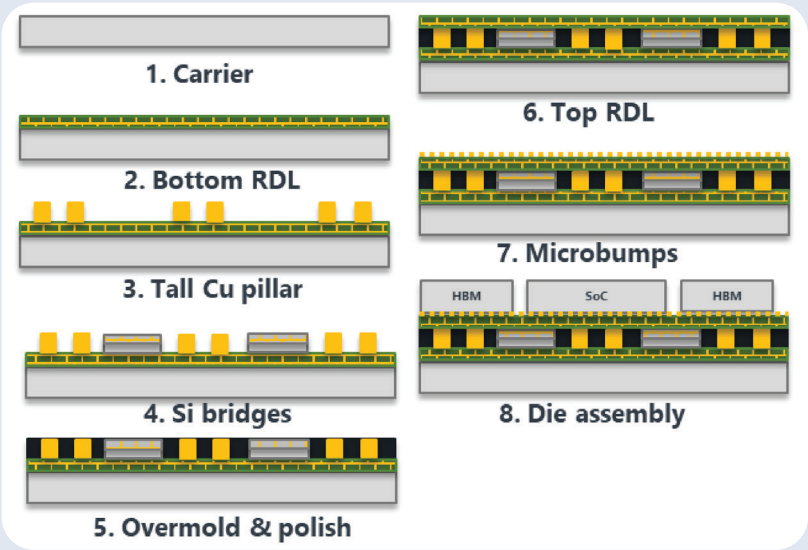

Figure 25. Typical process flow for molded interposer with embedded silicon bridges.

the chips to the bridge. This allows single pitch microbumps to be processed at each level and avoids the need for mixed small and large pitch bumps on the package substrate.

The use of silicon bridges has allowed augmented, standard package substrate technology to meet current HPC I/O data rate demands at a lower cost than silicon interposers and a higher capability than organic RDL approaches. Silicon bridges will be used for the foreseeable future as they fill the gap between package substrate capability and HPC needs. It remains to be seen whether new solid core substrate technologies will supplant silicon bridges.

2.3.5 2.5D Silicon Interposers - TSV (Passive and Active Solutions)

High-performance computing (HPC) applications require the integration of multiple chips/chiplets on a silicon interposer as shown in Figure 26. This approach offers several advantages for HPC heterogeneous integration. Very fine line and space designs for die-to-die interconnects can be fabricated using standard back-end damascene technology. TSVs in a thinned (~100 µm) interposer are used for vertical connections to the package substrate, with multiple chips that are flip chip bonded to the interposer using microbump technology.

A silicon interposer has several advantages for HPC, including improved device reliability (see the reliability pyramid shown in Figure 1). Silicon has a high Young's modulus which helps reduce package warping and prevent solder joint failures, especially at the interposer/chiplet interface. This is especially important for HPC as the chip aggregates generate a lot of heat. Additionally, using silicon as an interposer has the inherent advantage that the CTE of the interposer is equal to that of the silicon-based chips that are bonded to it, preventing warping of the bonded chip stack even under high thermal loads. Finally, silicon has a high thermal conductivity. By itself this assists in spreading the heat that is generated in hot spots across the real estate occupied by multiple chiplets.

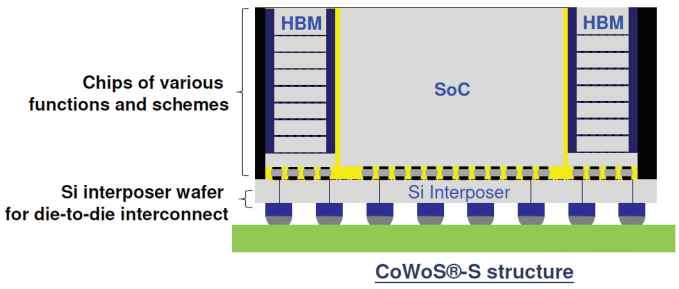

Figure 26. A silicon interposer-based integration scheme. A System-on-Chip (SoC) is co-packaged with HBM stacks in this example from TSMC's CoWoS®-S technology [43].

Silicon interposers can be either a passive or an active component in a device package. Passive silicon interposers provide interconnections between chips and translate the smaller chip I/O pitch to the wider substrate I/O pitch; the interposer has only passive components such as interconnects and, in some cases, deep trench capacitors embedded in the silicon. Active interposers (Figure 27) use the additional silicon real estate that the interposer provides to add active circuit elements such as memory I/O controllers and voltage regulators for power management. The use of silicon interposer real estate for circuitry requires a trade-off with vertical connectivity as the TSV density is reduced. Active interposers are, therefore, used mainly in designs that have no need for high-density vertical interconnects to the package substrate.

Silicon interposers also present certain drawbacks in terms of cost and the scalability. As chiplet aggregates become more complex and take up additional in-plane real estate, the size of the silicon interposers must increase. The fabrication of larger interposers can require multiple reticles per level and this adds significantly to the overall package cost since lithography costs tend to dominate in the fabrication process. Additionally, and depending on the technology used, stitching of the reticle exposure fields can have a negative effect on overall yield, with consequent increases in cost. Furthermore, increasing the size of silicon interposers reduces the number of interposers that can be fabricated on one wafer, impacting the cost of the subsequent package.

Intel employs a variant on 2.5D interposers in their Foveros technology. For instance, the Ponte Vecchio architecture is made by assembling 47 separate chiplets ("tiles") with a combination of embedded multi-die interconnect bridge (EMIB) and silicon interposer technology (Figure 28). Intel's roadmap seems to favor eliminating the TSV-containing interposer for a direct hybrid copper-to-copper bonding solution (Foveros Direct technology) that eliminates underfill requirements, solder bumps, and reduces vertical I/O pitch. Due to the increasing cost of larger silicon interposers, there have been

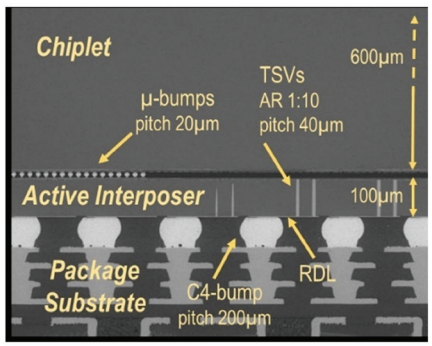

Figure 27. An example of an active silicon interposer showing chiplet, microbumps, TSVs, and C4 bumps to the package substrate [53].

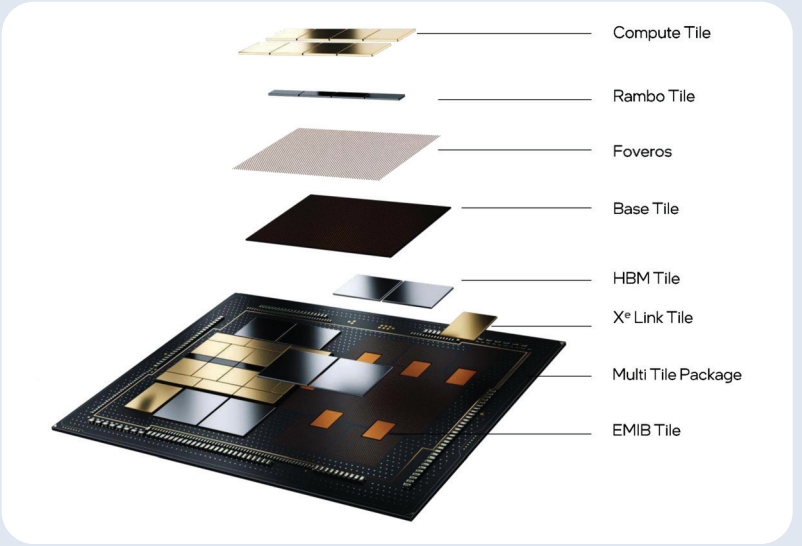

Figure 28. Intel Ponte Vecchio structure, showing a 47 chiplet aggregate with core and cache tile assembles on a silicon interposer base tile. [46].

several other technology developments that achieve similar connectivity capabilities at a lower cost. Embedded silicon bridges, RDL interposers, or combinations thereof have all been successfully adapted for HPC applications. These will be discussed in separate chapters of this handbook.

2.3.6 2.5D Glass Interposers - TGV

Recently, glass has been explored as a structural interposer material for high-density vertical and horizontal I/O. Glass can provide advantages in terms of cost and reduced electrical losses compared to silicon interposers [15] [16]. Glass also offers several advantages over organic interposers/substrates. The vertical I/O density that can be achieved is much higher, the coefficient of thermal expansion can be tailored to be much closer to that of silicon, and the high Young's modulus of glass allows a much more stable package configuration, especially in multi-chip modules. Additionally, the extreme smoothness and planarity of glass facilitates high resolution lithography.

As early as 2016, 2 µm lines/spaces were demonstrated on glass (Figure 29, [17]) in a study that also showed that there is no expectation of limits to further scaling imposed by the use of glass. Rather, the expected limits arise from the use of dry film photoresists and metal deposition techniques that are common for panel scale fabrication. Table 2 provides a comparison of interposer types.

It is important to distinguish between a glass interposer and a glass-core organic laminate substrate. While a glass interposer

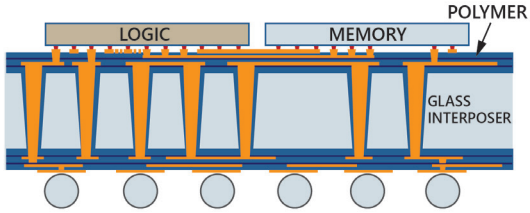

Figure 29. Glass interposer schematic showing polymer RDL buildup Through-Glass Vias (TGVs) [17].

Interposer Type	Silicon	Organic	Glass
RDL Line and Space (µm)	<1 (Xilinx)	2 (Shinko) 6 (Kyocera)	2 (Georgia Tech PRC)
Wiring Density	Very High	Medium	Medium-High
RDL Metal	CU, Al	Cu	Cu
Bump Pitch (µm)	40 µm	40-50 µm	20-40 µm
Cost	High	Medium	Low
Process	Wafer	PCB/Package	PCB/Package

Table 2. Interposer capabilities: a comparison between silicon, organic and glass options [17].

serves as an alternative to a silicon interposer, glass-core organic laminate substrates are targeted for use as advanced Flip Chip Ball Grid Array (FCBGA) package substrates.

The latter are traditionally fabricated with an organic core. Similar to a silicon interposer, a glass interposer still requires a standard package substrate for integration into a complete package. Glass-core package substrates will be discussed in detail in a later chapter. Glass interposers are typically between 100 to 200 µm thick, with 100 µm (similar to a silicon interposer) being most common. This allows standard metallization schemes such as TSV copper fill to be used for the TGV processing as well as WLP processes such as standard RDL.

The adoption of glass interposers has been slow, primarily due to the strong entrenchment of silicon interposer designs and to the lack of a clear cost advantage for waferscale fabrication. As well, silicon interposers can be made "active" through the fabrication of additional circuitry on the interposer, freeing up silicon real estate on the FC bonded chip sets. The use of glass interposers allows some embedding techniques, however this complicates manufacturing. The development of processes for manufacturing glass interposers in panel format would improve their cost/performance, however several key technologies have not yet been transferred into HVM (high volume manufacturing) but are continuoulsy progressing in development.

More promising application spaces for glass interposer technology can be found in the field of photonics integration, currently gaining momentum for medium-haul interconnects (Figure 30) [18]. The optical properties of glass are well-suited for optics integration and standard interposer fabrication techniques can be employed [19] [20]. Additionally, the glass CTE can be varied with sufficient range to match that of the sensitive optical components [21] [22].

Finally, there are several ongoing productizations that rely on the excellent dielectric properties of glass for RF applications. The high smoothness of glass is well-suited to high frequency and passive component manufacture [23], as well as to trace and antenna component fabrication. RF components such as low noise amplifiers can be readily integrated into a glass interposer based front end module (FEM) [24]. Despite these advances, the total market volume remains small, albeit growing.

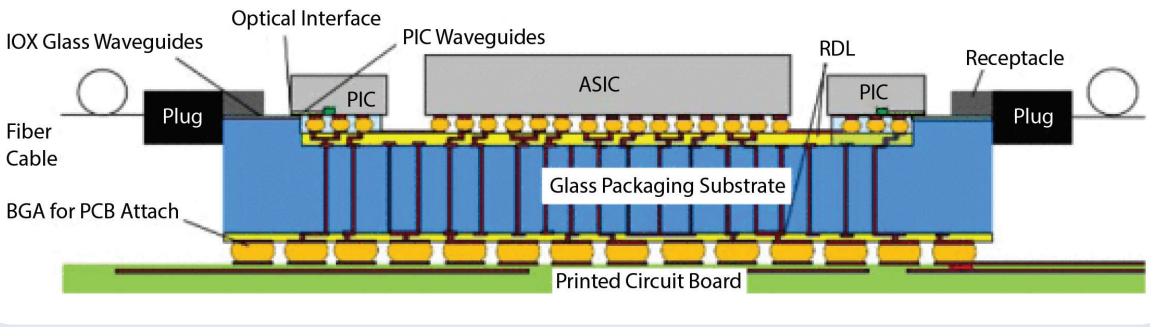

Figure 30. Photonics integrated circuits integrated with glass interposer and package substrate [20].

2.3.7 3D Interposer Architecture

A 3D architecture has two or more active silicon devices stacked and interconnected above the level of the package. 3D architecture is illustrated by the DRAM-tower on the logic die shown in Figure 31. 3D architectures stack all active and passive devices above the plane of the substrate. This die stacking architecture has evolved rapidly over the past few years. 3D architectures employ through silicon vias (TSVs – Section 2.4.6 of this chapter) drilled directly through the die to connect the stacked DRAM memory die. The use of "microbumps" at the end of the TSVs has enabled impressive levels of vertical stacking e.g., twelve memory die plus a base logic controller die in HBM2 technology. As product architects are exploring the opportunities available with these packaging technologies, there is growing interest in combining "front-end" 3D stacked system on integrated circuit (SoIC) configurations with enhanced 2D "back-end" RDL patterning and assembly.

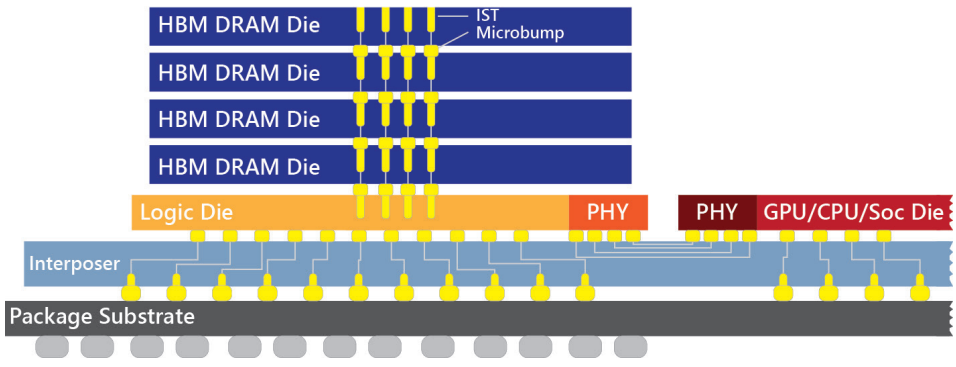

Figure 31. 3D packaging example: a graphics card with stacked HBM DRAM (Image: PC World).

2.4 Interconnect Technologies

Interconnects are a key component of any electronics system. They provide data and power connections between the various components of the system as well as connections to the outside world. There are many interconnect technologies employed in Advanced Packaging. Most often, a combination of different interconnect technologies are used to provide all the connectivity required for a system in package to function. Feature size differences span approximately five orders of magnitude between the silicon transistor level and the printed circuit board; these must be bridged by interconnect technologies to create a functional system. The choice of technology to interconnect the various components in an advanced package is primarily driven by the application which determines the required interconnect density. Cost and performance are secondary drivers, as there are several areas where interconnect technologies overlap in density capability. Table 3 provides a comparison of some 2D, 2.5D, and 3D advanced packaging schemes. The I/O density is highlighted in Table 3 as it is the main selection criterion for interconnect technology in a packaging application. For instance, a high-bandwidth memory (HBM) stack has different requirements for interconnect density to a silicon interposer than a silicon interposer has to an IC substrate. There are several options for connections to the active silicon. It is obvious that when a silicon-based substrate such as a silicon interposer or another die is used, the capabilities are much higher than with organic based technologies such as laminate IC substrate or organic interposer.

Interconnect technologies can be categorized in two ways: horizontal interconnects and vertical interconnects. (Note: In Table 3, the I/O density for horizontal interconnects has the units of #/mm/layer whereas the vertical I/O density has the units of #/mm^2.) Horizontal interconnects normally connect individual package components to others with similar feature sizes. The traces on a redistribution layer, an IC substrate, a PCB or even the damascene traces in the buildup of integrated circuits are all examples of horizontal interconnects. They provide both in-plane pitch translation for integration with other interconnect technologies and in-plane connection paths for different components or sections within components. Vertical interconnects can be further subdivided into two categories: interconnects that connect two types of components such as chip to interposer, or interposer to IC substrate; and interconnects that provide connections within the layers of a single package component such as blind microvias in a package substrate or in stacked redistribution layers.

Organic FCXGA	Glass Core Substrate	Intel EMIB	Organic Interposer	Silicon Interposer	Package Stacking	Die Stacking
IO/mm/lyr = 40-50	IO/mm/lyr = 100	IO/mm/lyr = 100	IO/mm/lyr = >100	IO/mm/lyr = 500+	PoP Pitch 0.27 mm	IO/mm = N/A
IO/mm^2 = 80-120	IO/mm^2 = 331	IO/mm^2 = 331	IO/mm^2 = 625	IO/mm^2 = 1600	N/A	IO/mm^2 = Variable based pitch
Bump Pitch = 110-90 µm	Bump Pitch = 55 µm	Bump Pitch = 110 µm EMIB Bump Pitch = 55 µm	Bump Pitch = 40 µm	Bump Pitch = 25 µm	N/A	Bump Pitch = 10-30 µm
9/12 µm L/S	2/2 µm L/S	2/2 µm L/S	2/2-1/1 µm L/S	0.4 µm L/S	N/A	N/A

Table 3. Overview of 2D, 2.5D, and 3D advanced packaging schemes.

Figure 32, Figure 33, and Figure 34 offer an overview of the different types of vertical and horizontal interconnects to be found in advanced packaging technologies. While these figures do not show all available technologies, they are representative of most advanced packaging methods currently in use. As previously noted, a typical package employs a number of horizontal and vertical interconnect technologies to form an integrated system.

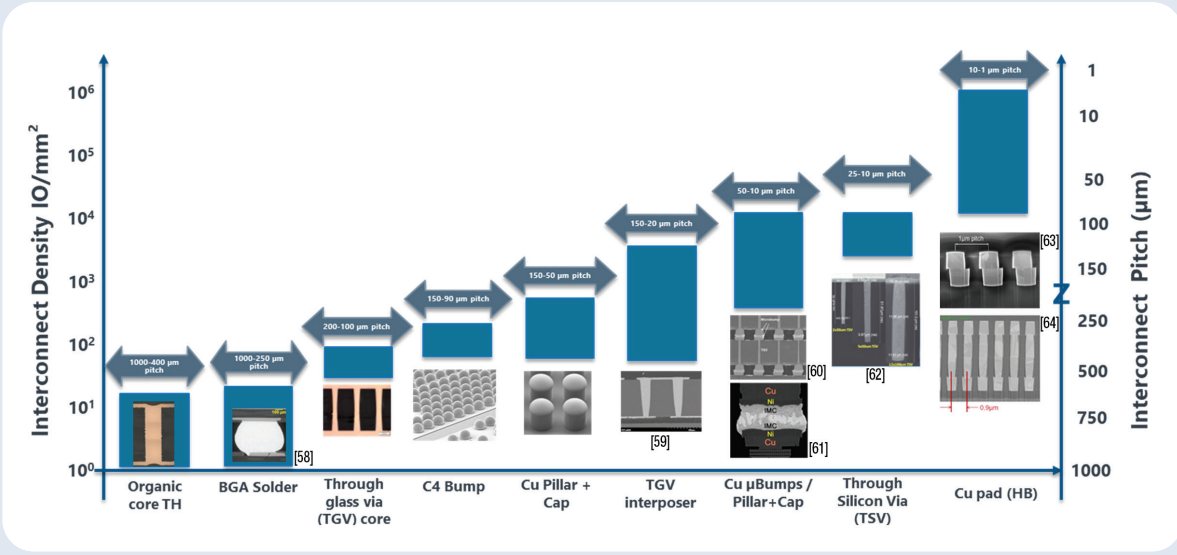

Figure 32. Vertical interconnect types to bridge connections between different substrates/feature sizes arranged by pitch and IO density per square millimeter [58], [59], [60], [61], [62], [63], [64].

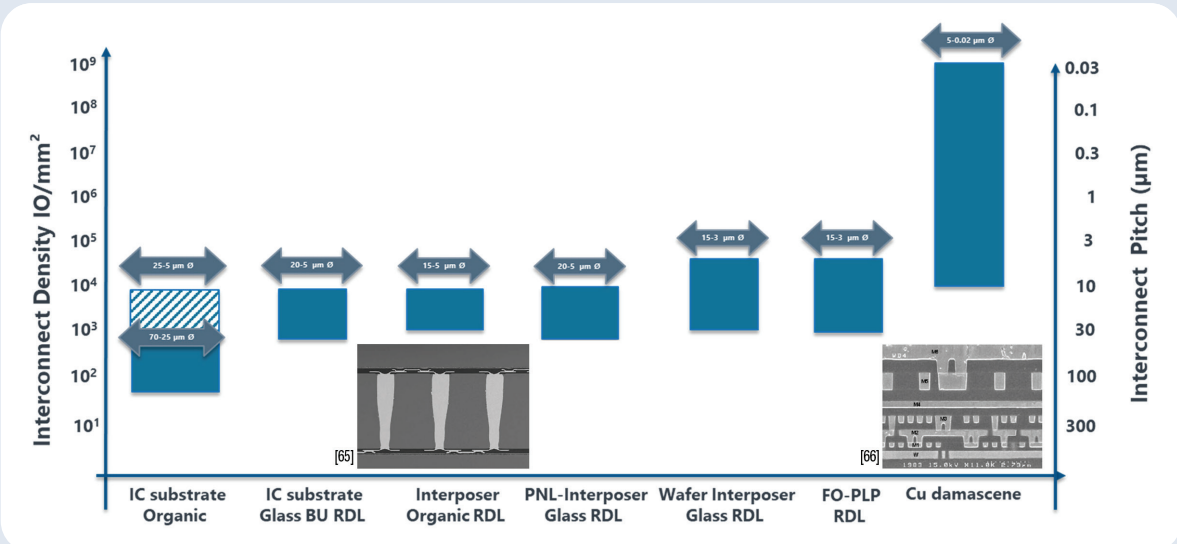

Figure 33. Vertical interconnect types within substrates arranged by pitch and IO density per square millimeter. The shaded bar areas indicate state of the art developments [65], [66].

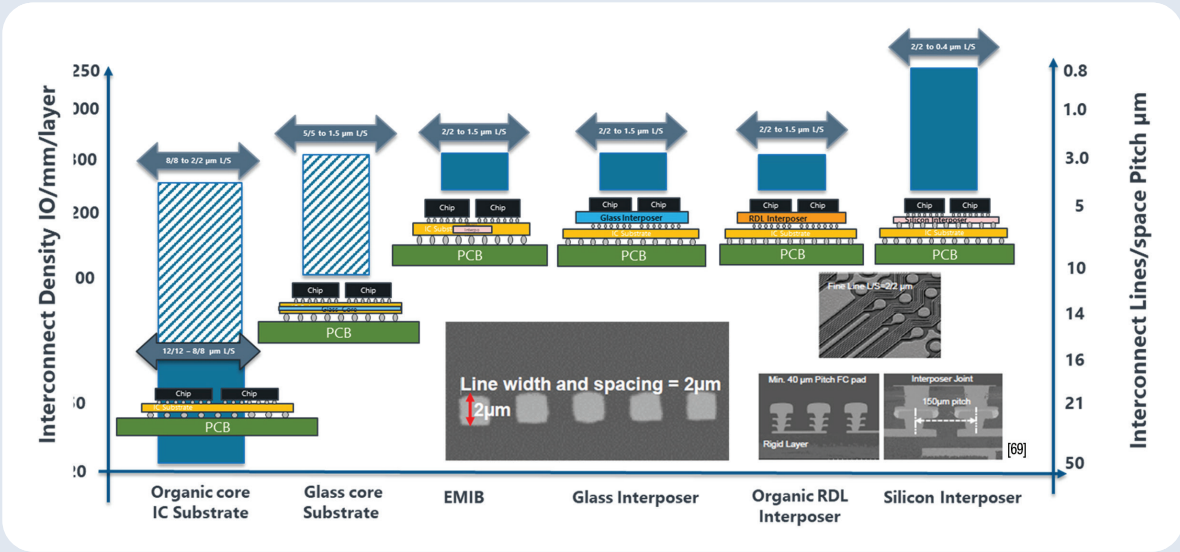

Figure 34. Horizontal interconnect types arranged by pitch and IO density per layer per millimeter. The shaded bar graph areas indicate state of the art developments [69].

The key metrics for development of new interconnect technologies is the number of interconnects (I/Os) per millimeter, per layer for horizontal interconnects, and number of interconnects per square millimeter for vertical interconnects. New technologies are continuously in development. For instance, copper-to-copper hybrid bonding can offer vertical interconnect densities previously only achievable in monolithically integrated dies. This enables heterogeneously integrated dies to be stacked with die-to-die interconnect performance rivalling that of standard backend damascene technology.

2.4.1 Wirebond

Wire bonding (Figure 2, Figure 35) is used to create electrical connections between multiple chips (integrated circuits/ICs) and between chips and 2D interposers (e.g., metal leadframe, organic laminate substrate). Less commonly, wire bonding can be used to connect an IC to other electronics or to connect one printed circuit board (PCB) to another. The process employs fine (e.g., 25 µm) bonding wires, most commonly made of gold, but can be made of other materials such as aluminum or copper. The two most common wire bonding processes are gold ball bonding and aluminum wedge bonding. Ball bonding uses a combination of heat, pressure, and ultrasonic energy to create a bond at each end of the gold wire (Figure 36). In the ball bonding process, the bond pad surface is heated, typically as high as 150°C. A gold wire is fed through a capillary and a high voltage discharge is used to create a gold ball at the end of the wire. The ball is positioned over a bonding pad on the IC, then pressed against the pad. Heat and ultrasonic energy bonds the ball and the pad. Once

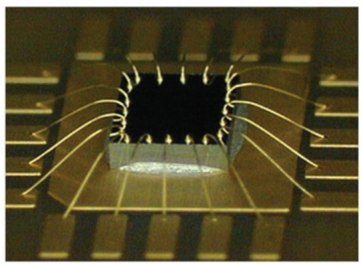

Figure 35. Traditional chip in leadframe package showing wirebonds.

this bond is formed, the capillary with the gold wire is positioned over the bond pad on the substrate or leadframe. The wire is sealed to this bond pad using heat, pressure, and ultrasonic energy, creating the electrical connection between the IC and the interposer or leadframe. The wire is then severed, and the tool moves on to create the next wirebond. Wedge bonding is typically used with aluminum wire bonds. With wedge bonding, the bond pad surface does not need to be heated. Wedge bonding process flow is like that of ball bonding, with the exception that the wire bond to the IC pad is formed solely by pressure and ultrasonic energy. Wire bonding is generally considered the most cost-effective and flexible interconnect technology and is used to assemble most semiconductor packages.

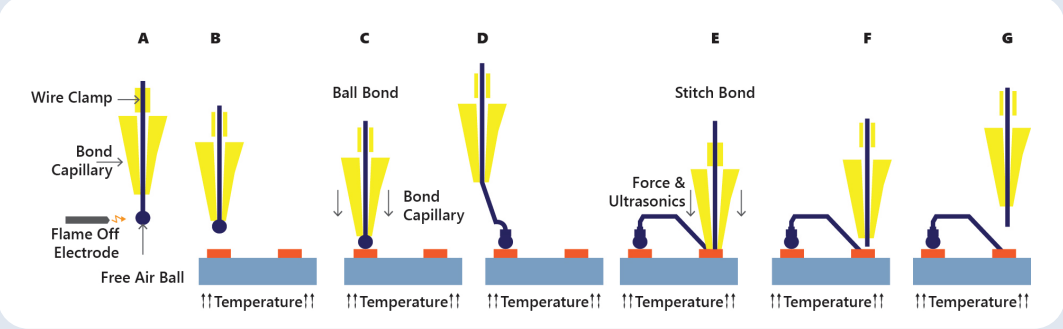

Figure 36. Ball bonding process sequence [70].

MKS' Atotech Wirebond Products:

Xenolyte® Electroless Plating Solutions

The Xenolyte® Ni, Xenolyte® Pd, and Xenolyte® Au series of electroless plating solutions produce hard, corrosion-free, and stress-minimized metal stacks that protect underlying structures. These provide a robust, stable, and low resistance solder joint connection to IC substrates. All Xenolyte® processes are compatible with batch processing. Note that, prior to deposition of nickel, specific surface activation that depends on the respective substrate is required. Suitable processes for copper, aluminum, aluminum alloys, and silicon materials are available.

- **Xenolyte® Ni C, Xenolyte® Ni MC, and Xenolyte® Ni RE:** Solutions for electroless deposition processes that produce nickel layers with medium (7% - 10%) phosphorous content.
- **Xenolyte® Ni LF:** Solutions for electroless deposition processes that produce lead-free, medium phosphorous content nickel deposits.
- **Xenolyte® Ni HP:** Solutions for electroless deposition processes that produce nickel deposits with high phosphorous contents from 9% to 12%.
- **Xenolyte® Ni TR:** Solutions for electroless deposition processes that produce nickel depositions suitable for high temperature applications, e.g., in the field of automotive industry. The resulting Ni/X/P alloy provides significantly improved reliability under such conditions and very low deposition stress.
- **Xenolyte® Pd LL, Xenolyte® Pd RS, and Xenolyte® Pd HS:** Solutions for electroless deposition processes that produce pure palladium deposits that are suitable for bonding. These solutions enable highly stable processes that are proven in mass production for automotive power chips.

- **Xenolyte® Au C, Xenolyte® Au CF 2 and Xenolyte® Au TG (Plus):** Solutions for electroless deposition processes that produce extremely stable gold layers on nickel or palladium. Xenolyte® Au C solutions are designed for use in cyanide-based processes while Xenolyte® Au CF 2 solutions are designed for cyanide-free processing. Xenolyte® Au TG solutions are designed for use in processes to produce thick gold layers. Xenolyte® Au TG solutions are available for use in processes with cyanide-based and cyanide-free dosing.

2.4.2 Flip Chip, Solder Balls and C4 Bumps

Flip chip, also known as controlled collapse chip connection or its abbreviation, C4, [25] is a method for interconnecting semiconductor devices to external circuitry using stacked solder bumps. The solder bumps are created by first electrodepositing copper on the device bond pads then depositing larger solder bumps composed of tin- or tin/silver-based solder material [1] onto the copper. The process flow for solder bump formation is shown in Figure 37. The technique was developed by General Electric's Light Military Electronics Department, Utica, New York [26]. Solder bumps (diameter ca. 100 µm) are deposited on the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is reflowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and fine wires are welded onto the chip pads and leadframe contacts to interconnect the chip pads to external circuitry [27].

The solder material may be prepared by different processes, including printed solder and controlled collapse chip connection (C4). The largest bumps are usually formed by stencil printing of solder balls on top of copper (lower cost, batch process, not as accurate as pre-formed bumps/solder balls). The stencil is commonly prepared by laser drilling of stainless steel. In the case of printed solder material, the diameters of the structures and pitches, i.e., the distances between the bumps, are in the range of several 100 µm. The corresponding heights of the copper pads are in the range of 50 to 100 µm, while

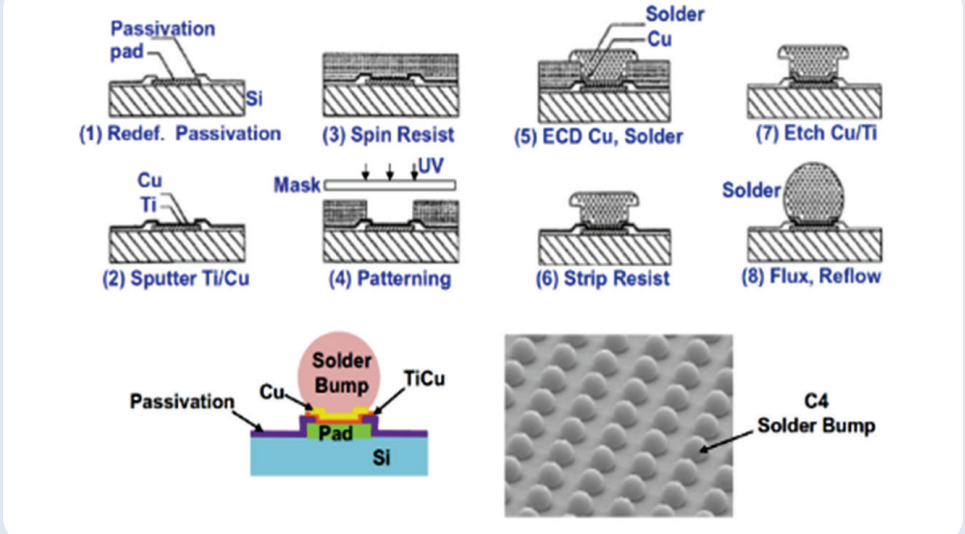

Figure 37. C4 bump formation process with electrodeposition of copper and tin or tin/silver [1].

those of the printed solder material are in the range of several 100 µm. In turn, C4 bumps are prepared by electrodeposition of tin- or tin-silver-based solder materials into patterend resists. The complete process flow, including sputtering of titanium or titanium/tungsten as well as copper as under bump metallization (UBM), resist formation and patterning, electrodeposition of copper followed by either tin or tin/silver, resist strip, etch of the UBM and, eventually, solder ball formation upon reflow is shown in Figure 37.

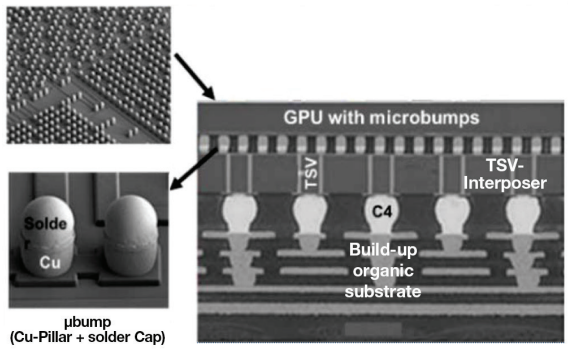

Figure 38. AMD's Radeon Graphics Processor Unit with interconnection of a TSV interposer to an organic substrate by C4 bumps and GPU to the interposer by microbumps [55].

The copper pillar is usually 5 to 10 µm high, while the solder material is deposited into a 40 µm resist layer and requires deposition over the resist by about 15 µm to obtain a mushroom shape, which is changed into a solder ball of approximately 100 µm height upon reflow. After preparation of the solder bumps, the device is eventually flipped, aligned to the substrate, and all joints are prepared simultaneously upon performing a reflow process step. AMD's Radeon Graphics Processor Unit (GPU) constitutes an example for interconnection of a TSV interposer to an organic substrate by C4 bumps and is shown in Figure 38.

2.4.3 Redistribution Layers, RDLs

RDLs are a critical part of 2D WLP (Fan-In and Fan-Out) and PLP (Fan-Out), 2.XD and 3D interconnect integration. They reroute connections to allow lateral communication between devices that are attached to the interposer [28]. Two approaches for fabricating RDLs are the deposition of copper metal onto a patterned polymer-based dielectric and Damascene-type copper deposition using silicon dioxide as a dielectric. Many descriptions of the Damascene process are available in the literature, reference [29] is typical. Figure 39 shows the preparation of an RDL using a polymeric dielectric. The process may be repeated to obtain stacks of RDLs. Copper electrodeposition processes provide good uniformity, excellent mechanical and electrical properties of the resulting trace, and via filling in the case of multilayer RDLs.

Figure 40 shows the process flow for RDL fabrication with a silicon dioxide dielectric using Damascene-type copper electrodeposition. As with polymer dielectrics, this process may be repeated for the preparation of multilayer structures. Alternatively, two layers may be prepared in a single copper electrodeposition step by employing a dual Damascene process. Requirements for the copper electrodeposition process include good filling of recessed features with minimal deposition on the top surface as well as excellent mechanical and electrical properties of the resulting trace. Figure 41 shows a multilayer RDL with filled vias based on the InFO technology of TSMC.

Generally, polymer-based dielectric materials are employed for larger traces, on the order of 1 to 10 µm, while silicon dioxide-based dielectric is used with smaller traces, typically below 2 µm. This rule is not hard and fast, with known instances of traces of less than 2 µm used with both polymeric and silicon dioxide dielectric materials.

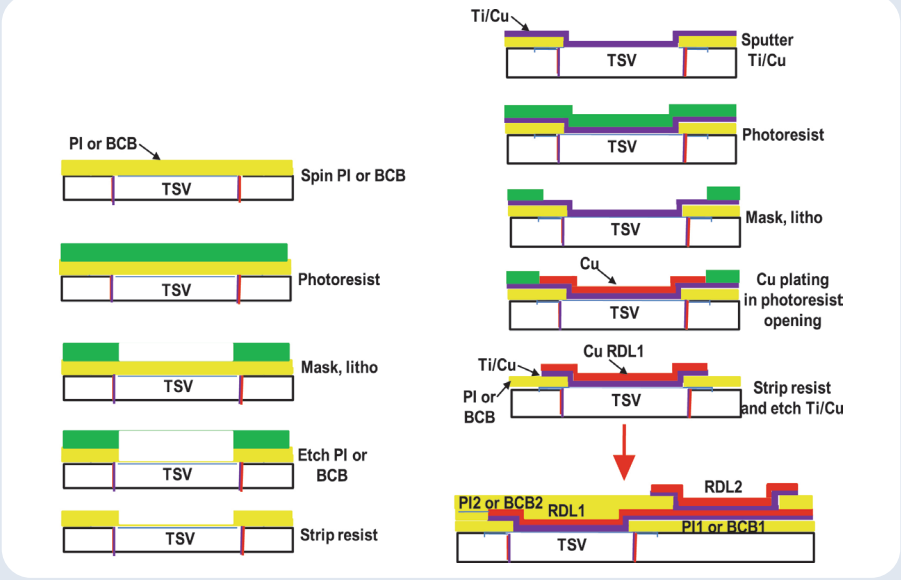

Figure 39. Schematic representation of RDL fabrication with polymers as dielectric [28].

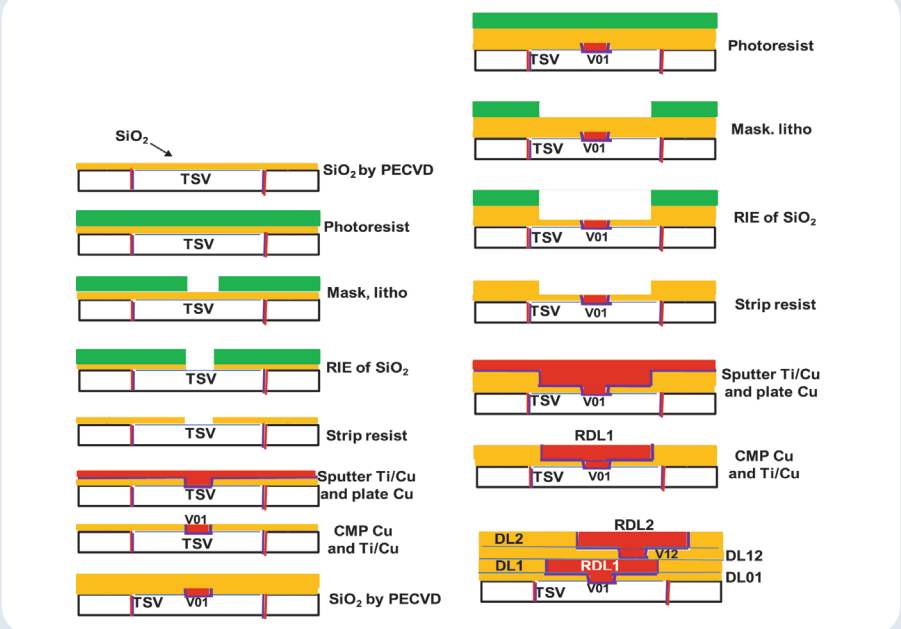

Figure 40. Schematic representation of RDL fabrication with silicon oxide as dielectric [28].

MKS' Atotech RDL Products:

- **Spherolyte Cu UF 3:** Solutions for electrolytic deposition of copper. For use in the fabrication of RDLs with microvias on patterned substrates with polymer dielectric. The process is especially suitable for Fan-Out Wafer Level Packaging (FOWLP) due to the excellent mechanical properties of the resulting material [30] [31]. The copper produced in this process is highly reliable, even for sub-5 µm conductor traces, due to the high ductility characteristic of extremely pure metal. In addition, the process allows for filling of recessed vias, low internal stress, and low resistivity. RDL structures without via filling may also be achieved with Spherolyte Cu UF 2 and the mechanical properties of the resulting copper are optimized for Fan-In Wafer Level Packaging and certain automotive applications.

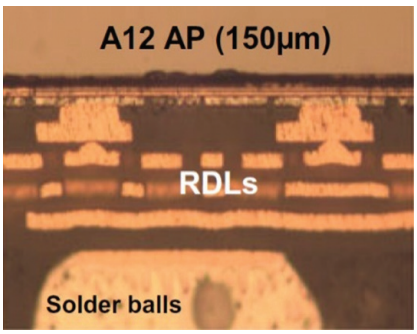

Figure 41. RDL of Apple iPhone based on TSMCs InFO technology [1].

- **Everplate 2TF:** Solutions for electrolytic deposition of copper traces for RDLs that use silicon dioxide dielectric materials and Damascene-type processes. The process is optimized for challenging via filling applications. The mechanical properties of the copper are especially suitable for this type of dielectric material.

2.4.4 Microbumps

The use of microbumps enables smaller pitches and increased I/O densities, as compared with C4 bumps. The process flow for microbumps, depicted in Figure 42 [1], is similar to that for C4 bumps. C4 and microbump interconnect methods differ primarily in the relative heights of the electrodeposited copper and tin or tin/silver bumps. Relative to the height of the copper/solder stack, the copper pillars in microbumps are usually thicker in comparison to the pads of the C4 bumps, while the thickness of the solder deposit is smaller. The decreased volume allows for smaller diameters and pitches, in the range of 10 to 100 µm. Even smaller bumps with diameters below 10 µm have recently been reported. Due to the decreased solder volume, self-alignment based on surface tension is not possible and, therefore, microbumps are also denoted as chip connection (C2) bumps. The increasing ratio of copper material at the expense of tin or tin/silver also allows for improved thermal and electrical conductivity. Some applications require an additional layer in between copper and solder material to improve the reliability by inhibiting interdiffusion of copper and tin or tin/silver. These interlayers consist of electrodeposited nickel or nickel alloys and are usually thin, on the order of 1 to 5 µm. Challenges for the different electrodeposition processes include improving uniformity, especially coplanarity (reduced height variations of the deposits across the substrate surface), and optimizing bump or pillar shape to obtain reliable bonds. Ideally, the pillar shape may be modified in the copper electrodeposition process. A micrograph showing copper pillars for interconnection of a GPU to an interposer by microbumps is included in Figure 42.

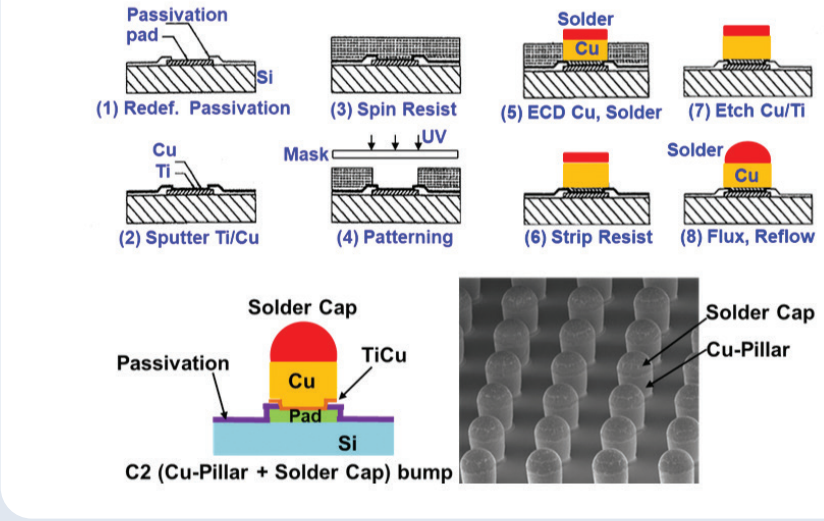

Figure 42. Microbump formation process with electrodeposition of copper and tin or tin/silver [1].

MKS' Atotech C4 and Microbump Products:

- **Spherolyte Cu UF 2/3/5:** Copper pads and pillars of high uniformity for C4 and microbump applications may be produced with Spherolyte Cu UF 2. The process allows a large operating window with regard to the concentration of the organic additives and current density. Furthermore, the process exhibits good stability, stable performance over the lifetime of the electrolyte, and is proven in mass production e.g., in automotive applications. Deposits prepared with Spherolyte Cu UF 2 require the deposition of a nickel barrier between the copper and tin or tin/silver-based solder materials to avoid the formation of voids under thermal load. In contrast, pad, bump, and pillar structures prepared with Spherolyte Cu UF 3 do not require a barrier owing to the high purity of the deposit. The Spherolyte Cu UF 3 process also exhibits excellent layer uniformity and allows for the application of high current densities with only minor attack on the polymer resist. The Spherolyte Cu UF 5 process combines the benefits of Spherolyte Cu UF 3 (i.e., highest purity deposit and excellent uniformity even at high current densities) with improved bump or pillar profile. The process allows for adjustment of the profile by modification of the process parameters and additive concentrations. Upcoming hybrid bump designs contain pillars of different diameters. This may require purposeful adjustment of the relative copper deposit heights, depending on the respective diameter, to obtain the best overall uniformity of the copper and tin or tin/silver stacks after reflow. The Spherolyte Cu UF 5 process was shown to be especially suitable for this type of application [32].

- **Spherolyte Ni, Spherolyte NiFe, and Spherolyte NiW:** Nickel layers between copper and tin or tin/silver solder materials may be obtained using the Spherolyte Ni process. The resulting deposits are highly uniform and have excellent copper diffusion barrier properties. The process allows for a wide operating window, good stability, and easy handling of all liquid products. The stress of the deposits may be adjusted using organic additives, depending on the requirements of the application. Further improvements in barrier properties may be obtained by additional additives that produce nickel/iron alloys (Spherolyte NiFe). Alternatively, the Spherolyte NiW process produces nickel/tungsten alloys that also provide improved barrier properties over pure nickel.

- **Spherolyte Sn and Spherolyte SnAg:** Spherolyte Sn 2/3 processes produce pure tin solder deposits. Spherolyte Sn 2 is a three additive process with excellent process control, while Spherolyte Sn 3 is essentially identical but based on a single additive, allowing for simplified process control. The resulting deposits exhibit identical properties. Both processes provide good layer uniformity, operate at room temperature, and allow for application of high current densities. The tin deposits exhibit good solderability and no voids after reflow. Tin/silver alloy-based solder deposits are industry standard and may be obtained by the Spherolyte SnAg process. The process operates at room temperature, provides excellent uniformity, allows for deposition at high current densities and produces uniform deposits with adjustable alloy composition, and no voids after reflow. Ultra low alpha tin sources are available for all of the above-mentioned processes.

2.4.5 Tall Pillar (Pre-formed Through Package Vertical Contacts/Vias (TPV))

Increasing device integration can be achieved with 2.5D and 3D stacking of package components. Commonly, 2.5D and 3D integration rely on expensive TSV technologies. Tall pillars are a low cost alternative to TSVs and may be used for vertical interconnection within a package. An example of the use of tall pillars is found in TSMCs Integrated Fan-Out (InFO) wafer level packaging. This design features high density RDL and tall pillars for vertical connection of logic and DRAM (Figure 43). The structural dimensions of the pillars may reach heights of up to 350 µm and diameters range from 40 to 250 µm. The copper pillars are prepared by electrodeposition on patterned resists with UBM. The process flow is similar to that used with copper pillars for the microbumps as described in Section 4. Challenges for the deposition process include excellent uniformity at the high current densities (i.e., deposition rates) required for acceptable throughput. Excellent coplanarity is required for such pillars, especially considering their large overall heights. This also poses challenges for the deposition process.

MKS' Atotech Tall Pillar Products:

- **Spherolyte Cu UF 5:** Tall copper pillars can be produced using the Spherolyte Cu UF 5 process. This process allows deposition at very high current densities for optimized throughput as well as excellent deposit purity and uniformity. Due to the high aspect ratio of the patterned structures, application of suitable current ramps is required.

- **Spherolyte Cu MSA:** MSA-based copper process for tall pillar plating at high current densities. Deposits feature high uniformity, high purity and excellent performance on varying aspect ratios. Application of current ramps is required for high aspect ratio targets.

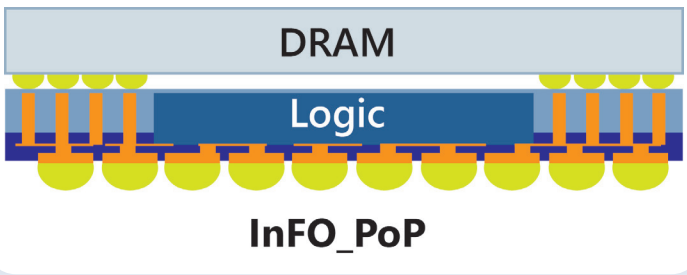

Figure 43. Schematic representation of TSMCs InFO package on package.

2.4.6 Through Silicon Vias (TSV)

Through Silicon Vias are used for vertical interconnections in 3D ICs (via first, middle, last process, vide infra) and in Si/Glass 2.5D Interposers. In addition, memory stacks can be produced using vertical interconnections based on TSVs.

TSVs are recessed features with high aspect ratios, i.e., the ratio of height to diameter is 10:1 or greater. Typically, the height of TSVs varies from 50 to 100 µm with diameters of 3 to 10 µm. The TSV fabrication process is depicted in Figure 44. It involves the formation of an insulation layer of silicon nitride or silicon oxide by thermal oxidation or chemical vapor deposition (CVD), application and lithography of a photoresist, an insulation layer etch, TSV etch into the silicon substrate by a Bosch-type deep reactive ion etch, CVD of a silicon oxide liner, as well as application of a titanium or tantalum barrier, and a copper seed layer by physical vapor deposition (PVD). Afterwards, the vias are filled with copper using an electrodeposition process specifically tailored to provide a good fill for these high aspect ratio features. The TSV electrodeposition process does not rely on patterned resists but uses strong organic additives to direct the deposition into the vias with negligible deposition on the top surface. Excessive copper on the top surface is removed afterwards by chemical-mechanical polishing (CMP). Sufficient throughput (minimized process times) and electrolyte stability constitute the main challenges for the electrodeposition process.

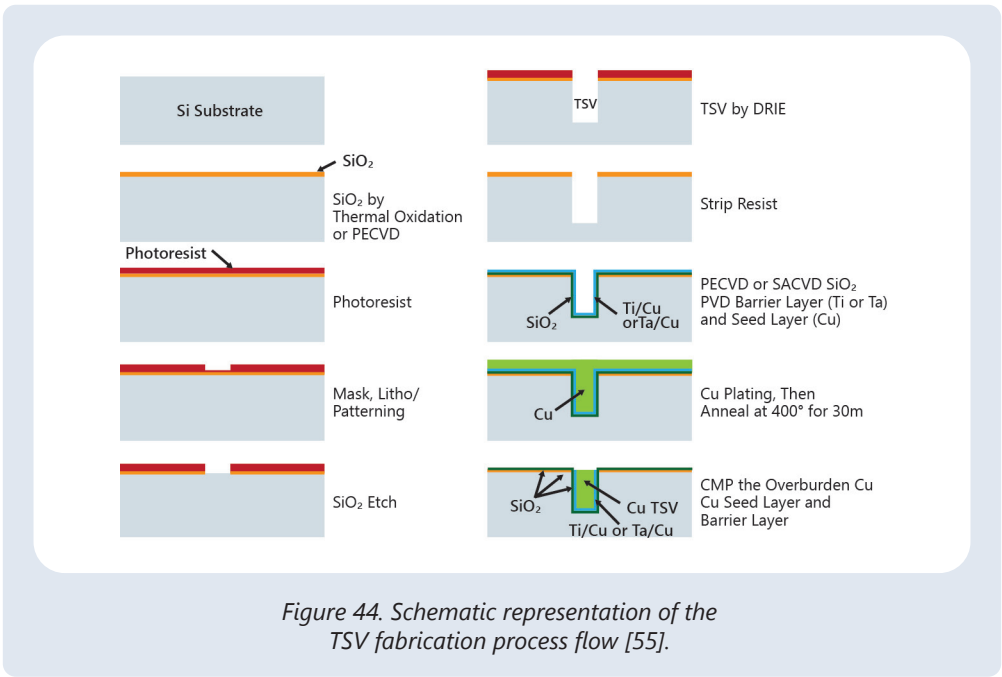

Figure 44. Schematic representation of the TSV fabrication process flow [55].

After the overburden removal by CMP is complete, the wafers are flipped and bonded to a temporary carrier. They then undergo a "TSV reveal" backside silicon wafer grind/polish to remove excess silicon. Depending on the application, the final wafer thickness ranges between 50 µm for memory and 100 µm for silicon interposer. There are several ways to integrate the TSV process into the process flow, depending on the final application of the silicon die in which the TSVs reside (Figure 45):

1. Via-first relies on forming the TSV prior to other substrate process steps. This method is normally used with passive silicon interposers since the process of building active, front-end (FEOL) transistor devices would exceed the thermal budget of already-present TSVs. With passive interposer devices, the only subsequent steps are the build up of pads and routing patterns in one or more layers which can be achieved using standard Damascene technology. Additionally, any copper deposition steps could contaminate an FEOL device build, producing low yields of active devices.

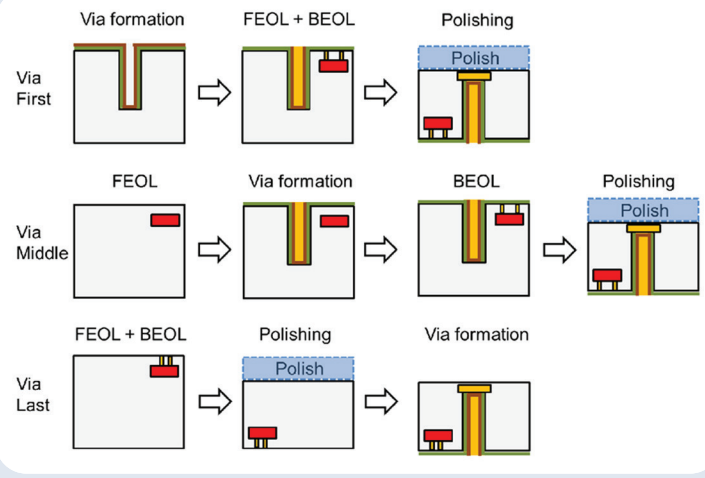

Figure 45. Via first, middle and last methods [71].

2. The second way to integrate TSVs into the process flow is a "via-middle" process that works with active interposer designs. In this method, TSVs are created after the fabrication of FEOL devices. This allows TSV-to-circuitry alignment from one side of the wafer while not exceeding the thermal budget of the TSV interconnections. It also provides some flexibility in etch depth uniformity across the wafer; over-etch can ensure a minimum TSV depth that meets design criteria while the subsequent backside TSV reveal can be used to thin to spec.

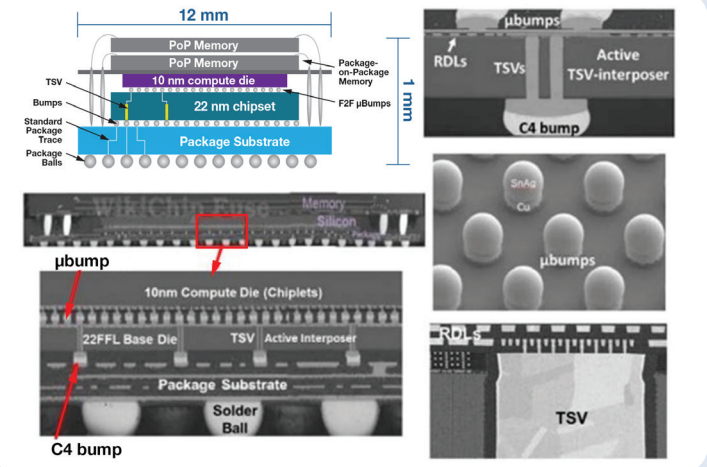

Figure 46. Intel's Lakefield processor based on 3D integration, employing active TSV interposers. (Source: Intel)

3. The third TSV integration scheme is via last. This method also allows full processing of FEOL device layers prior to formation of the TSVs. However, it is more complicated than via-middle integration as the TSV etch and fill have to be done from the wafer backside. This presents challenges with backside to frontside alignment, as well as issues with stopping the Bosch dry etch at the right depth, i.e., at the interface with the FEOL device layer across the wafer.

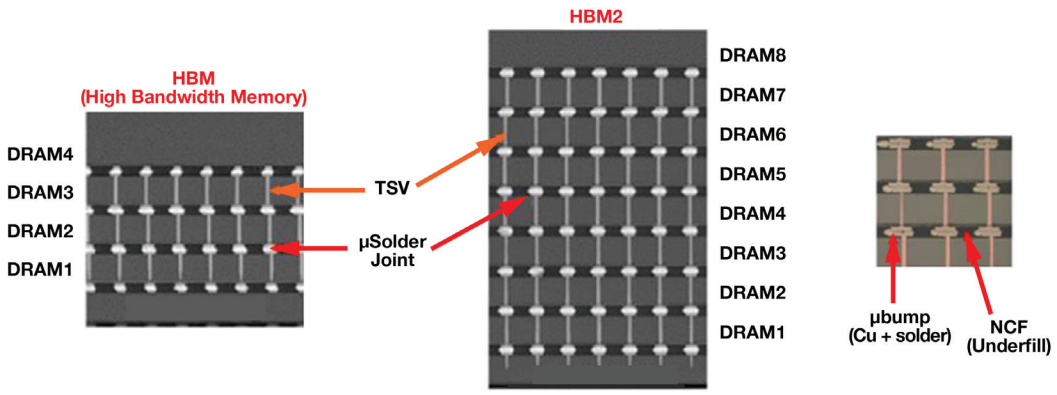

Figure 47. High bandwidth memory (HBM) and HBM2 stacks as produced by Samsung and SK Hynix [72].

All of the TSV technologies that have been implemented for interposer or memory 3D stacking are mature, albeit costly, and can benefit from improvements in process times. Intel's Lakefield processor, based on their FOVEROS technology, constitutes an example of Advanced Packaging with a TSV interposer (Figure 46). An example of stacked memory dies is depicted in Figure 47.

MKS' Atotech TSV Products:

- **Spherolyte Cu TSV:** This series allows for filling of high aspect ratio TSV structures with copper. The Spherolyte Cu TSV 6 process is currently under development and is expected to provide competitive deposition times and excellent process stability.

2.4.7 Direct Bonding

Further increases in interconnect density with corresponding scaling of the pitch of flip chip applications requires direct copper-to-copper bond formation. The best pitch for flip chip applications based on microbumps is predicted to be limited to no less than 10 µm since solder material may be squeezed out during the bonding creating electrical shorts [33]. The formation of direct copper-to-copper interconnects overcomes these issues, reducing limit on pitch to below 5 µm [1] [34]. In addition, these connections provide lower electrical resistivity in comparison to other joints. The formation of direct copper-to-copper interconnects is achieved by thermal compression and hybrid bonding.

2.4.8 Thermal Compression Bonding

The formation of direct copper-to-copper contacts was initially performed using thermal compression bonding [1], [35]. This technology operates at elevated temperatures, usually above 350°C, and high pressures. It produces diffusion of copper atoms and grain growth at the bond interface. The process requires long process times, in the range of one to two hours, and this is a problem for throughput and device reliability. As well, the process temperature may produce degradation of sensitive devices, e.g., DRAM [36], [37]. Finally, issues may arise from extensive oxide formation on the copper surface at elevated temperatures, which may affect the reliability of the bond [38].

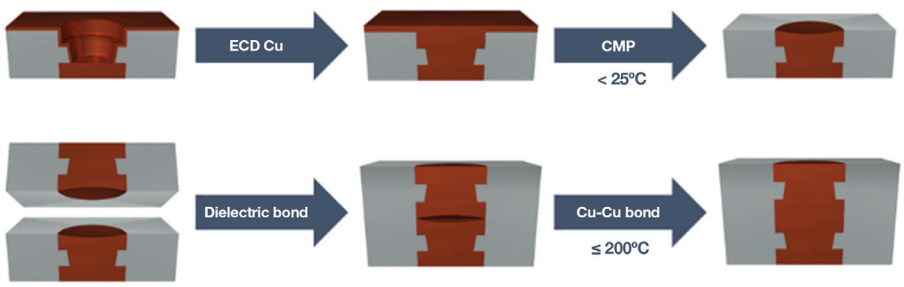

Figure 48. Schematic representation of the hybrid bonding process, including with copper electrodeposition, CMP, dielectric and copper-to-copper bond formations [73].

2.4.9 Hybrid Bonding

The above noted problems with thermal compression bonding forced the development of an alternative low temperature process for the formation of direct copper-to-copper interconnects. Hybrid bonding, also known as direct bond interconnect, combines a dielectric bond with a metal bond and is intended to overcome the limitations of thermal compression bonding [1] [35] [37] [39] [40]. The process employs Damascene-type copper electrodeposition, chemical-mechanical polishing (CMP), and dielectric bonding at room temperature, followed by the formation of the copper-to-copper interconnects at moderately increased temperatures (Figure 48). Initial dielectric-to-dielectric bond formation occurs spontaneously at room temperature and adheres the wafers or dies that are to be connected to the substrate. Dielectric bonds are further strengthened during the copper-to-copper bond annealing step. The temperature of the latter step should be less than 300°C to be compatible with sensitive devices. The CMP process provides excellent uniformity, with roughness values of less than 0.5 nm and recesses into the copper in the range of a few nm [1]. This recess is required due to the larger CTE of copper as compared with the dielectric material. The copper-to-copper bond is established at elevated temperatures that produce expansion of the metal and build-up of internal pressure. The application of external pressure is optional for this process.

Significant efforts were required to develop hybrid bonding, especially with regards to surface preparation and CMP processing [37] [39] [40]. Silicon dioxide, silicon nitride, or silicon carbon nitride are typically employed as dielectric materials. The copper electrodeposition process is required to fill Damascene-type recessed features with a copper microstructure that is suitable for proper copper-to-copper bond formation [32] [41] [42]. Examples of packages based on direct copper-to-copper interconnects formed with hybrid bonding processes include image sensor packages produced by Sony and Intel's Foveros Direct technology (Figure 49).

MKS' Atotech Hybrid Bonding Products:

- **Everplate Cu 2TF:** This product allows for Damascene-type copper deposition and for filling of recessed features with copper having a microstructure suitable for direct copper-to-copper bond formation by hybrid bonding. The resulting copper may be bonded at low temperatures. The corresponding microstructure of copper can be fine-tuned to not alter over 4 weeks.
- **Spherolyte Cu DB:** Use of this product further minimizes the hybrid bonding temperature to 200°C or even below. The microstructure of copper prepared by this process is stable for several days.

Both Everplate Cu 2TH and Spherolyte Cu DB, were especially designed for compatibility with hybrid bonding processes. They facilitate all required process steps between copper electrodeposition and copper-to-copper bond formation while employing low bonding temperatures [41] [42]. They provide excellent filling and mircrostructural uniformity in the deposited copper. Some implementations of copper-to-copper direct bonding require nano-twinned microstructures, which may be obtained by copper electrodeposition with the Spherolyte NT Cu process.

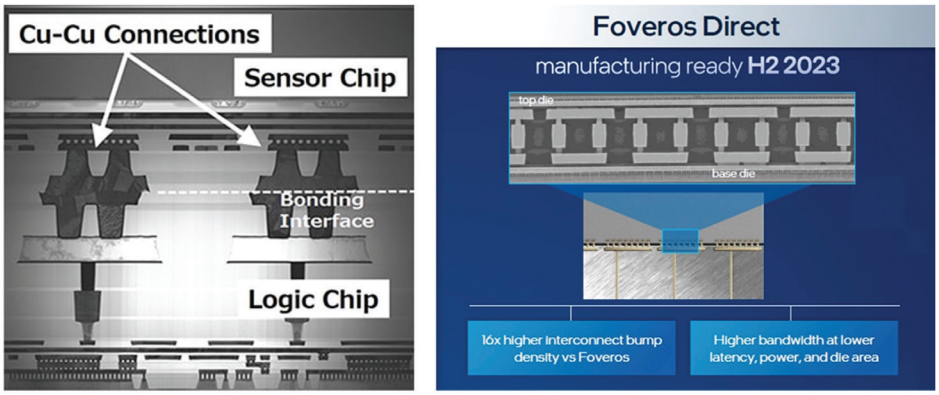

Figure 49. Image sensor package of Sony (left), (Source: Sony) and Foveros Direct of Intel (right), (Source: Intel).

2.4.10 Wafer-to-Wafer (W2W) vs. Die-to-Wafer (D2W) Interconnect Formation

Interconnect formation between the different components can be performed by bonding two wafers to each other (denoted as wafer-to-wafer, W2W, bonding) or by bonding singulated dies to a wafer (denoted as die-to-wafer, D2W, bonding). The W2W approach provides high throughput and good alignment accuracy, however, limitations arise from chip sizes and yield issues. W2W is challenged by alignment accuracy, wafer warpage and yield problems. As well, not all chiplets are of the same size nor do all wafers have the same yield which prevents stacking without the potential for losing good dies. D2W bonding offers increased flexibility and potentially improved yields since singulation allows selection of only good dies. Challenges with D2W arise from edge effects, contamination—especially particles originating from singulation—problems with pick and place accuracy, and the need for additional pad area to compensate pick and place tolerance. D2W is significantly more advanced than W2W and industrial implementation has started.

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Chapter 3

Organic Laminate Structure

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In Section 3.1 common formats and materials are introduced, highlighting the importance of surface roughness and material properties which are essential for the reliability and performance of the final electronic device. This section covers resin systems and woven glass fabrics which form the prepregs. Together with copper foils, these prepregs are the foundational elements of the Copper Clad Laminates (CCL) used for both multilayer PCB manufacturing and for the core of an IC substrate. Section 3.2 shifts the focus of discussion to Semi-Additive Processes (SAP) and Ajinomoto Build-up Films (ABF). The use of SAP and ABF represent a departure from traditional PCB manufacturing methods and is critical for the production of fine-pitch circuits and the higher component density common to IC packages. Section 3.3 discusses the role of the solder masks that protect copper traces and ensure precise soldering. The variety of solder masks and the processes for their application are discussed, with emphasis on the importance of correct development and curing in order to avoid defects and ensure functionality. In Section 3.4 High Density Interconnect (HDI) technology and further details on SAP processes are given, including descriptions for modified SAP (mSAP) and advanced modified SAP (amSAP) processes. This section includes a discussion of embedded structures and components and how these advanced techniques enable the creation of more compact high-performance electronic devices.

The following sections show the innovation and technological evolution, from the basic materials that make up a PCB to the cutting-edge processes that define the future in IC substrate manufacturing (Chapter 4).

3.1 Introduction to Common Formats and Materials

The processes and the materials used for Printed Circuit Board (PCB) manufacture are equally important to the reliability of the finished PCB. Copper foils, typically formed by electroplating, are deposited and patterned to create the electrical circuitry on the board. Surface roughness of these foils is a critical variable since it impacts the adhesion of the resin, and therefore PCB reliability. Different degrees of roughness are desirable, depending on the final application. The PCB resin impacts electrical reliability since it provides insulation between the copper layers in the final PCB. The most widely used resin system is based on epoxies, but other materials such as polyimide and some exotic polymer blends are employed in applications such as flexible or “high speed” PCBs. Resin systems are typically reinforced with a woven

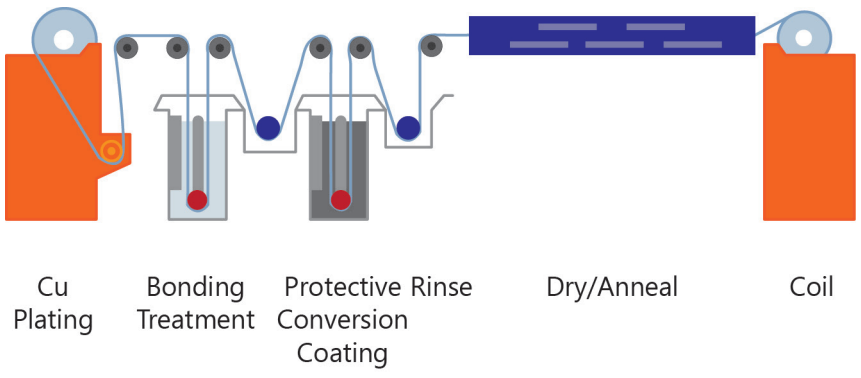


Figure 1. Schematic of copper foil production [7].

glass fabric to provide specific mechanical properties or, in the case of packaging applications, particulate reinforcement where it offers several advantages. Glass reinforced materials are called "Prepregs" and the use of heat and pressure to combine Cu foils and prepregs generates a "Copper Clad Laminate" (CCL), which is commonly used for "core" production in multilayer PCB manufacturing.

3.1.1 Copper Foils

Copper tracks and layers are required to carry electrical signals in a PCB assembly. Typically, these tracks are formed using a combination of masking, plating, and etching operations that are applied to a pre-existing copper layer that is either part of a copper clad laminate (CCL) material (see Section 3.4) or a copper foil.

Copper foils of varying thickness are produced by electroplating a continuous copper layer onto a rotating titanium drum that is partially immersed in a copper rich electrolyte. A copper layer is deposited on the drum until a target foil thickness value is obtained, (typically 2-72µm), then the foil is peeled off the rotating drum as a continuous sheet (Figure 1). The side of the foil that was in contact with the drum, usually referred to as the "drum side", is typically of "low roughness" while the deposited or "matte side" can be treated to create greater roughness that aids in adhesion with the resin system during CCL or PCB production (Figure 2). The degree of roughness of the "treated side" is typically dependent upon the final PCB application. While a "standard" treatment is suitable for many applications, there are cases where a higher or lower roughness level is preferred. There are a wide variety of foils available, ranging from those with low roughness, ideal for high frequency applications in which surface roughness is detrimental to signal integrity, to foils with increased roughness for applications where roughness that promotes adhesion with the resin system is more important.

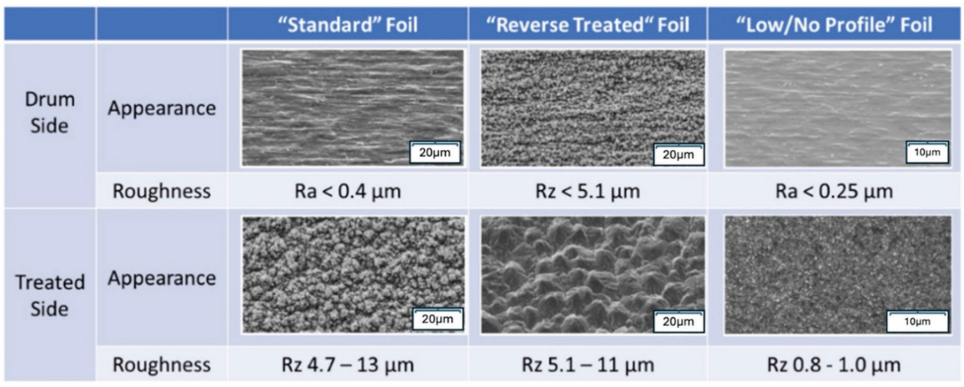


Figure 2. Examples of drum and treated side of copper foils [8].

3.1.2 Resin and Woven Glass Fabric

Polymer Resins

Electrical isolation between the two copper layers on CCL, and within the final PCB assembly is maintained using an electrically insulating material. Early PCBs were based on paper insulators; however, the industry has migrated to the use of polymer insulating materials since these are readily integrated into manufacturing processes and offer a wider range of physical and electrical properties. Epoxy resin is the most common polymeric material used for rigid PCB production while polyimide is typically employed for flexible PCBs. Other resin systems such as bismaleimide triazine (BT), polytetrafluoroethylene (PTFE), poly (p-phenylene oxide) (PPO), and poly (p-phenylene ether) (PPE) are used in applications where the unique properties of these polymers are beneficial.

Woven Glass Fabric

Other than flexible PCBs, where a simple polyimide layer is the norm, resin insulators are commonly reinforced. Reinforcement provides a number of benefits, such as:

- Thickness control
- Increased strength and toughness
- Reduced thermal expansion
- Improved electrical properties in the insulator layer

The most widely used reinforcing medium for PCB insulating layers is woven glass fabric. These media are available in several sizes and styles (Figure 3), each with different fiber diameters and weave densities. Glass cloth specifications and designations (e.g., 106, 1080, 2116, see Figure 3) are detailed in IPC4412 [1]. Selection of the glass cloth style is typically based on the target separation between copper layers and on the electrical property requirements.

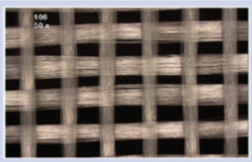
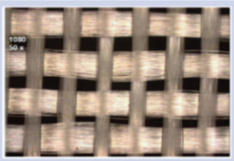
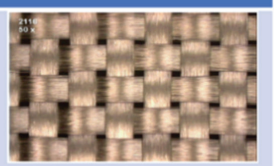
	106	1080	2116
Appearance			
Warp & Fill Count (ends/inch)	56 x 56	60 x 47	60 x 58
Thickness	0.038 mm	0.064 mm	0.097 mm

Figure 3. Examples of woven glass fabric styles [9].

Special glass fabric weaves are employed when laser drilling of microvias is required. The laser ablation rate for glass is significantly lower than that of the surrounding resin system. In traditional glass cloth weaves, the locations where the warp and weft yarns cross can lead to issues with hole quality during the laser drilling process. Specific glass fabric styles have been developed to combat this. They make use of "spread yarns", Figure 4, that have a more uniform distribution of glass fibers which produces more uniform ablation during laser drilling.

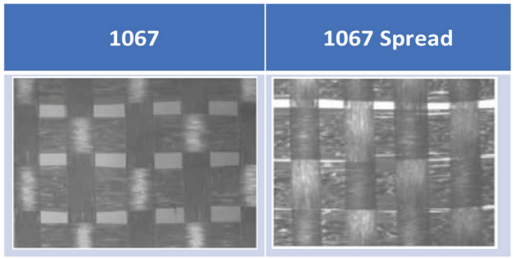


Figure 4. Standard and spread glass style [10].

3.1.3 Prepreg and Copper Clad Laminate (CCL)

Prepreg

"Prepreg" is the term commonly used for the combination of a resin system with glass fabric. The term derives from the fact that the glass fabric is pre-impregnated with a resin (Figure 5). Prepreg nomenclature follows that used for woven glass fabrics and is usually based on the glass fabric style that it contains, i.e. 106, 1080, etc. (Figure 3).

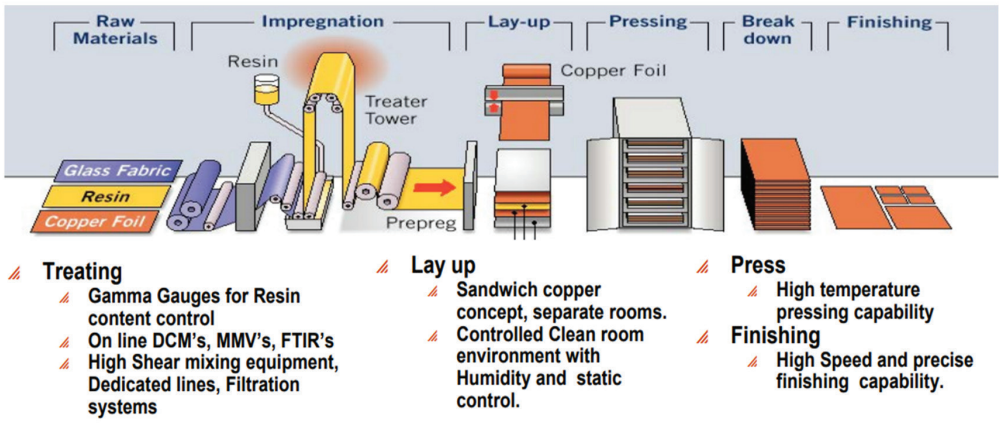


Figure 5. Schematic of prepreg and laminate production [9].

Copper Clad Laminate

Copper Clad Laminate, often referred to as "CCL" or "Laminate", is widely used for "core" production during the manufacture of multilayer PCB (Section 3.4). CCL consists of two copper foils that are bonded to either side of a single, or multiple layers of prepreg. It is supplied in a wide variety of types and thicknesses and is bonded with copper foils and prepreg to produce a multilayer assembly (Figure 6).

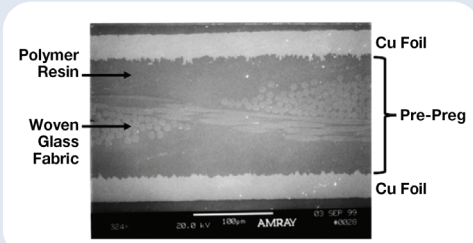


Figure 6. Cross section of copper clad laminate [9].

Processing of Prepregs and Laminates

The simplest multilayer PCBs consist of a combination of cores made from laminates interspaced with prepreg layers and then capped with copper foils (Figure 7). Prepreg layers are used to bond all the component parts together and ensure that there are no voids or cavities within the final assembly. Typically, prepreg layers, unlike laminates, are not fully cured in their "as supplied" condition, with the final cure occurring when the PCB is heated to a temperature that allows the resin to flow, fill cavities, and chemically cross link to a fully "cured" condition. Figure 8 shows a typical example of the conditions during a press cycle. This bonding or lamination process usually occurs in large presses that can apply heat and pressure to produce the desired resin flow in the PCB stack while maintaining a vacuum to ensure that no chemical oxidation occurs.

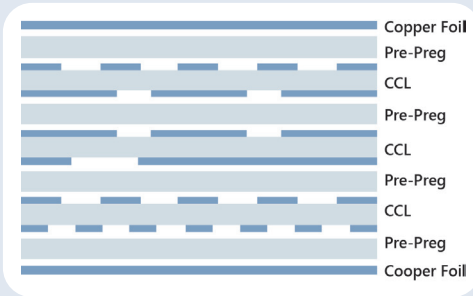


Figure 7. Schematic of multilayer PCB after lay-up.

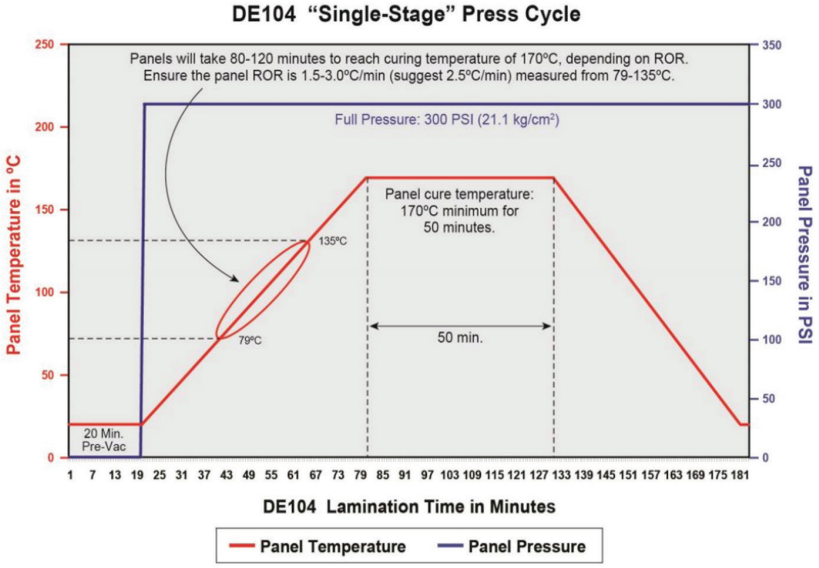


Figure 8. Lamination press profile [11].

3.2 Semi-Additive Process and Build-Up Films

A semi-additive process (SAP) for PCB production (Figure 9) deposits copper onto only selected areas of the surface of a substrate. SAP-produced PCBs employ build-up films and a vacuum lamination process rather than prepregs for substrate. Where prepregs use a glass weave structure to maintain stability and minimize thermal elongation, build-up films contain glass spheres and are much thinner. SAP process is used in the manufacture of IC substrates that have a higher density of components and traces than traditional PCBs. It can be used to create circuits with trace widths as small as 4 µm and spacing as small as 6 µm, creating fine-pitch circuits and high-density interconnects with a greater degree of precision than is possible using traditional PCB manufacturing processes.

In SAP, the electroplated copper is deposited only in the areas where it is needed, rather than over the entire surface of the board. This is done by applying a resist to the surface of the board treated with electroless copper, then copper is selectively removed using a photolithography process to expose areas where additional copper is needed as shown in Figure 9 (steps 5-10). These areas are then plated with copper using an electroplating process. The resist is then removed, leaving behind the desired pattern of copper traces. This process allows for the creation of complex circuitry on a small PCB, enabling the development of compact and high-performance electronic devices.

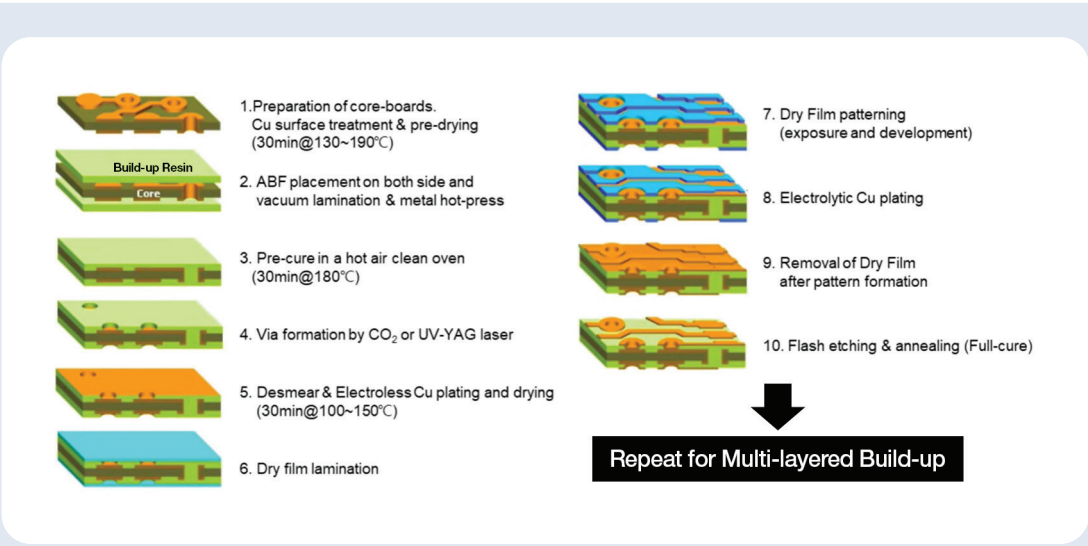


Figure 9. SAP process flow schematic.
(Source Ajinomoto Nishimura ETC conference)

Build-up films are much thinner than conventional prepregs and require vacuum lamination to produce conformal films on the structured core board. Figure 10 shows a schematic process flow for a vacuum laminator. In Step A, the substrate (green) is covered with the build-up film or Dryfilm resist and added to the heated vacuum laminator. In Step B, the vacuum laminator is evacuated to conformally glue the build-up film or dry film resist to the substrate without any air inclusions.

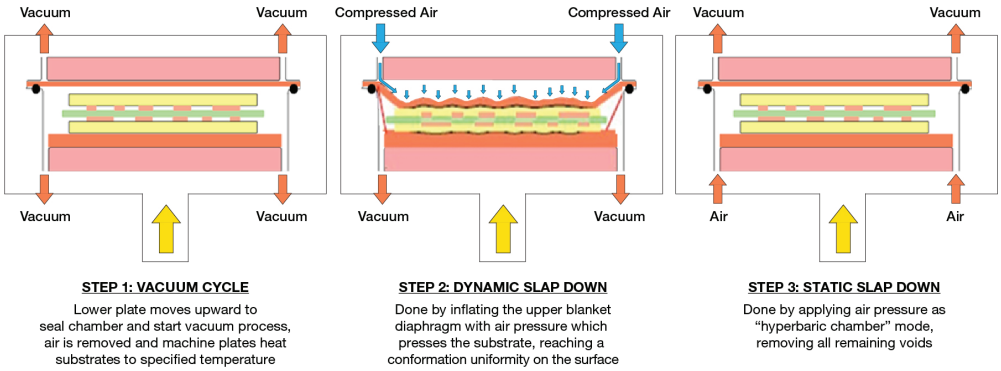


Figure 10. Vacuum lamination process.
(Source: Dynachem)

Finally, in Step C, compressed air is introduced to pressurize the vacuum laminator to 7 bar, compressing the film onto the substrate surface and maximizing the adhesion between the substrate and the film. Figure 11 shows an automated vacuum laminator.

Figure 11. Automated vacuum laminator.
(Dynachem D548_AVPL Line_EN22_Rev00p)

ABF Material	With or Without Supporter Film	Full Cure (Peel Strength)	Pre Semi-Cure (Before Laser Drilling)	Post Semi-Cure (Final Cure Stack)
GX-92 GX-92 R	Without With	90 min @ 190°C 90 min @ 190°C	30 min @ 180°C 1st step: 30 min @ 100°C 2nd step: 30 min @ 180°C	60 min @ 190°C 60 min @ 190°C
GX-T31	Without	1st step: 30 min @ 100°C 2nd step: 30 min @ 180°C 3rd step: 60 min @ 190°C	1st step: 30 min @ 100°C 2nd step: 30 min @ 180°C	60 min @ 190°C
GX-T31 R	With	90 min @ 190°C	1st step: 30 min @ 100°C 2nd step: 30 min @ 175°C	60 min @ 190°C
GZ-41	Not defined	1st step: 30 min @ 100°C 2nd step: 30 min @ 180°C 3rd step: 60 min @ 200°C	1st step: 30 min @ 100°C 2nd step: 30 min @ 180°C	60 min @ 200°C
GL102	With	90 min @ 200°C	1st step: 30 min @ 130°C 2nd step: 30 min @ 180°C	60 min @ 200°C
GL103	With	90 min @ 200°C	1st step: 30 min @ 130°C 2nd step: 30 min @ 165°C	60 min @ 200°C

Table 1. Curing conditions for different ABF materials.

During vacuum lamination, the build-up film is heated up to 100-130°C to promote adhesion of the build material to the substate. Curing of the build-up film material (full polymerization) requires two curing steps. The first curing step is performed before laser drilling of vias. This preliminary cure partially polymerizes the build-up film material, allowing the chemical cleaning process (desmear) to remove build-up smear from the capture pad and roughen the surface. Two possibilities are available for the first curing step: either with or without supporter film on top. Ajinomoto specifies the curing with supporter film on top as R (release). Following metallization of the build-up film, the final cure step is performed to fully polymerize the build-up film and further improve adhesion to the interface between the film and metal layers.

Table 1 shows curing conditions for different ABF materials, with and without supporter film (Figure 12) as part of the curing process. The final cure can be applied directly after lamination if copper foils are to be used to test peel strength.

Build-up films, unlike HDI dielectrics (Figure 9 and accompanying text), are applied as a liquid on a supporter film carrier foil. Once dry, the composite is protected by a cover film and rolled to the final product (Figure 12). The resin system is mainly based on epoxy with different blends containing, for instance, cyanate ester or phenolic ester (Figure 13).

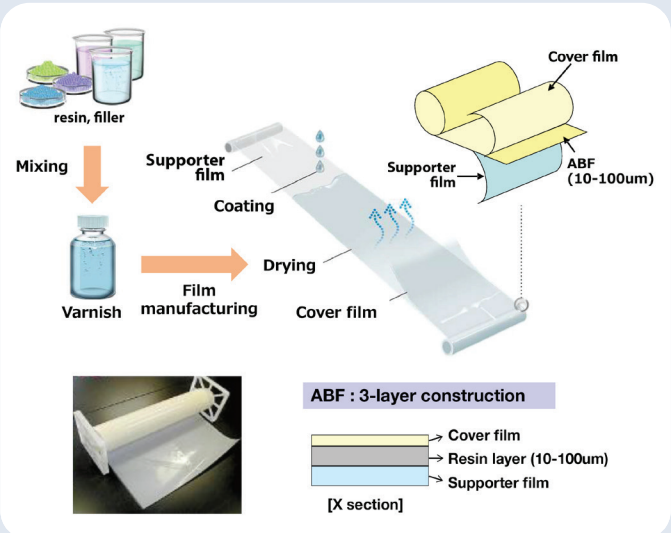
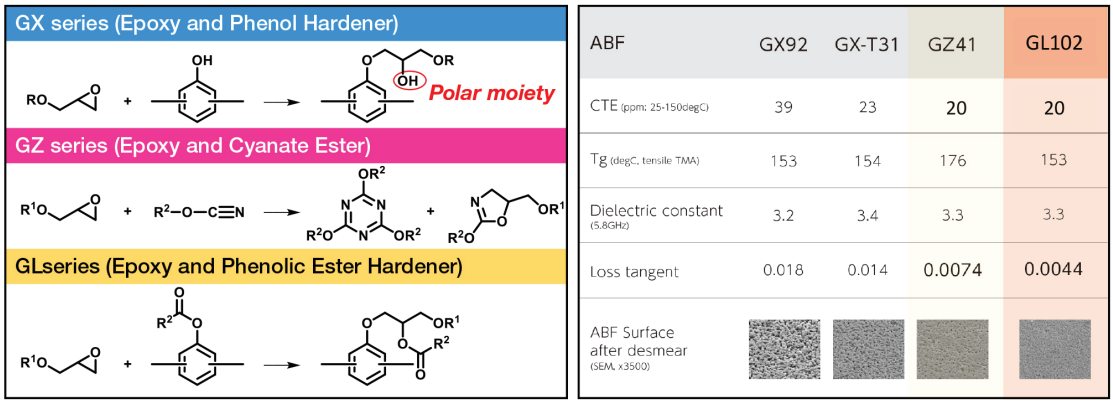


Figure 12. 3-layer construction for ABF. (Source Ajinomoto Nishimura ETC conference)



ABF	GX92	GX-T31	GZ41	GL102
CTE (ppm: 25-150degC)	39	23	20	20
Tg (degC, tensile TMA)	153	154	176	153
Dielectric constant (5.8GHz)	3.2	3.4	3.3	3.3
Loss tangent	0.018	0.014	0.0074	0.0044
ABF Surface after desmear (SEM, x3500)				

Figure 13. Different resin systems.

The thermal elongation and dielectric properties of the resin system are controlled by the amount of glass or SiO_2 spheres added to the resin. Filling grades of up to 75% are available to meet different CTE and electrical specifications (Figure 14) and can significantly improve signal loss in PCBs with fine lines and spaces. Ajinomoto offers different resin systems that meet varying requirements for lower thermal expansion (CTE) and improved signal loss properties (Figure 14).

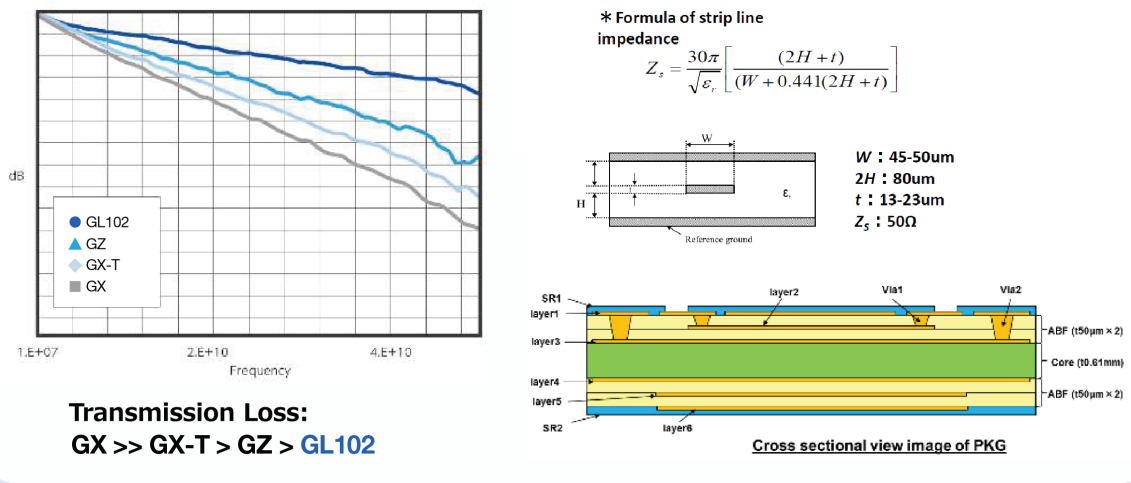


Figure 14. Representative variations in electrical property for different resin systems. (Source: SEMI KOREA APC Workshop 2022, Ajinomoto Co., Inc.)

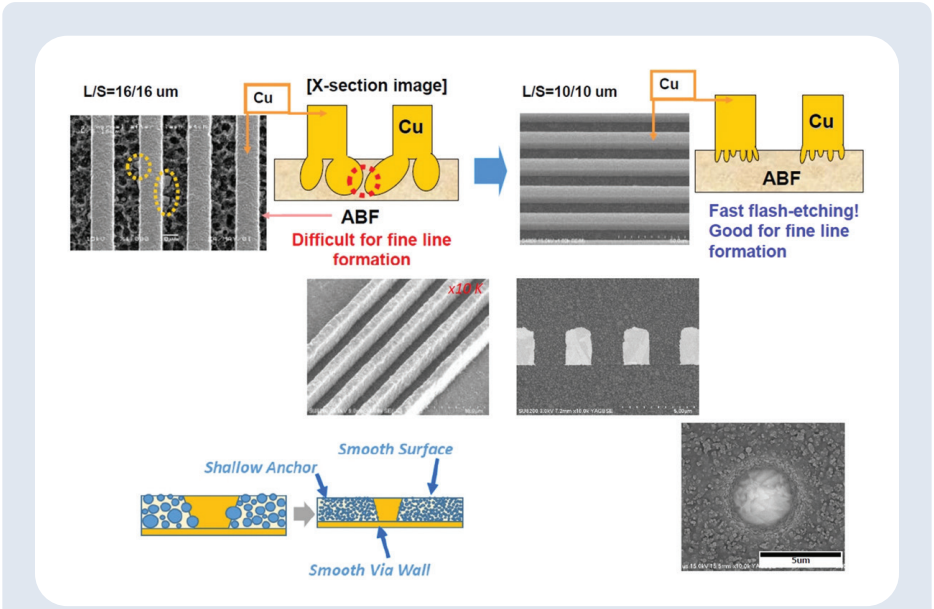


Figure 15. Key aspects of fine line and via formation.
(Source: SEMI KOREA APC Workshop 2022, Ajinomoto Co., Inc.)

Surface roughness of the ABF after desmear is driven by the exposed glass spheres and can be significantly reduced by using filler material having smaller diameters (Figure 15). This allows the manufacturing of finer conductor lines and smaller laser vias. Figure 15 shows 2 µm line/space conductors and a 5 µm laser drilled via along with different factors that impact fine line formation.

3.3 Solder Masks

Solder masks, also known as solder resists, are lacquer coatings that are applied to the printed circuit board to protect the copper traces. Solder masks also ensure that the solder is wetted only on the open contact areas to keep solder bridges from forming between neighboring pads. They help to protect the substrate against mechanical damage as well.

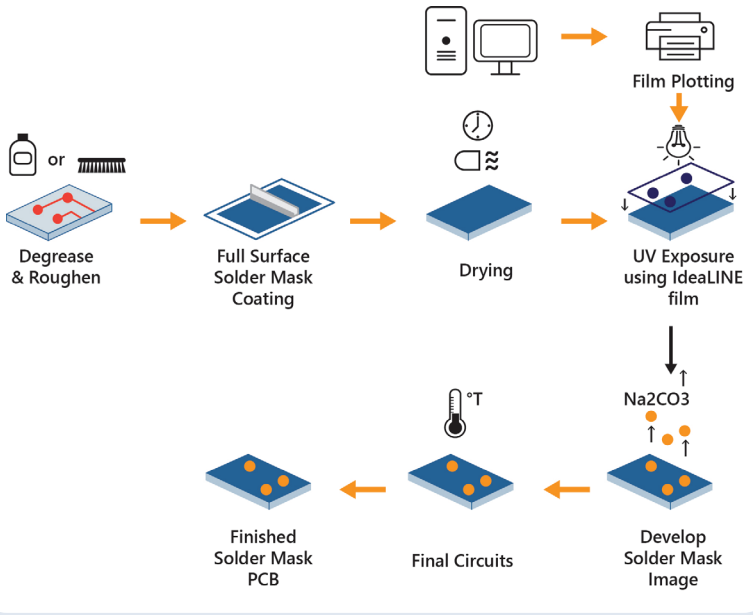


Figure 16. Solder mask process [16].

Different types of solder masks are available for different target applications. The most common and lowest cost option is an epoxy-based material that is silkscreened onto the PCB. Liquid photo imageable solder masks (LPSM) or dry film photo imageable solder masks (DFSM), especially for packaging applications, are also available. The solder mask typically consists of a binder or resin, filler material, dyes or pigments, additives to adjust the wetting or foaming properties of the lacquer, and solvents [2]. Thermal curing, which induces limited chemical crosslinking in the resin, is used to harden organic solder masks. After the application of the LPSM by screen printing or curtain coating the solder mask is dried at elevated temperature to evaporate the solvent. The solder mask is then selectively exposed to UV light and produces cross linking in the organic resin in the coating. The areas on the PCB that are intended to be free of solder mask coating during the metallization process are covered during the UV treatment and do not undergo crosslinking. They are dissolved by chemical reaction after the UV process. This development process uses a slight alkaline developer solution that is sprayed onto the PCB to remove the soluble solder mask areas. The solder mask process is shown schematically in Figure 16. Process failures and contamination that occur during the solder mask application can have a strong negative impact on subsequent process steps. For example:

- Insufficient crosslinking in the resin caused by, for example, low UV energy can lead to an increased risk of evaporation or leaching of organic components in the final finish plating process or in the assembly.
- Poor development using contaminated developer or poor rinsing leading to contamination residues on PCB and copper pads can produce plating defects such as skip plating or uneven deposition in the final finish process.

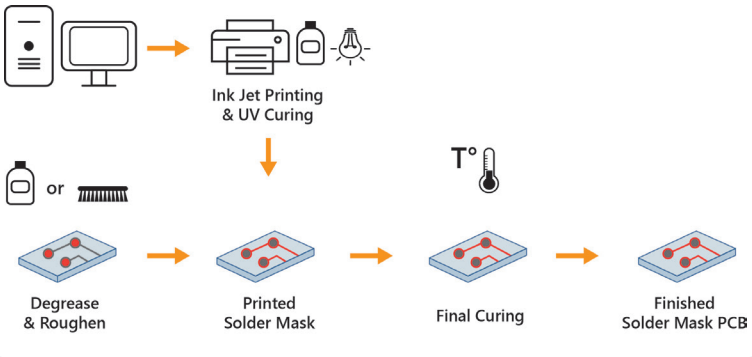


Figure 17. Digital inkjet printing of solder masks [17].

Inkjet printing of solder masks has been developed as a means of overcoming some of the drawbacks of the standard solder mask processing. As with Laser Direct Imaging (LDI) of dry film, inkjet printing of solder masks is a digital process. The inkjet printing process for solder masks is shown in Figure 17.

Figure 18. Inkjet printers for solder masks [14], [15].

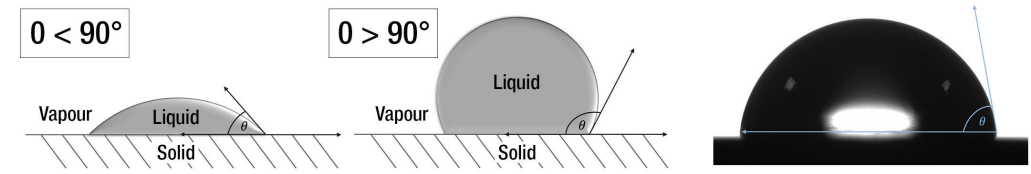


Figure 19. Drop shape parameters showing contact angle.

Depending on the required solder mask thickness, the solder mask, and the inkjet printer, different printing strategies will be employed. Generally, the solder mask is printed using a layer-by-layer process in which each layer undergoes UV lamp exposure before the next layer is applied. A final thermal curing step is applied after printing, sometimes followed by an additional UV exposure. Since inkjet solder mask printing requires no photomasks that can be damaged or contaminated and no development step, it has a significantly reduced environmental footprint. Various equipment manufacturers offer inkjet printers for solder mask. Two examples are shown in Figure 18.

Inkjet printing requires a specialized solder mask ink such as the DiPaMAT® series from Agfa or the IJSR-4000 JM Series from Taiyo that have a much lower viscosity than traditional solder mask materials. Such low viscosity fluids require a high contact angle, preferably 60-80°, preventing uncontrolled bleeding of the ink. Contact angle is defined as shown in Figure 19. The preferred value of the contact angle results from a compromise between high print resolution and printing speed. At lower contact angles greater overlap of the individual ink drops is ensured, but at the cost of reduced resolution, while at higher contact angles increased resolution is achieved at the cost of reduced printing speed. Using Drop Shape Analysis (DSA) tools such as the Krüss DSA-series (Figure 20), the contact angle of the ink jet solder mask ink can be measured directly on treated copper surfaces.

Figure 20. KRÜSS Drop Shape Analyzer (DSA25) [16].

Failures in the curing step can significantly impact the final finish properties of the solder mask and the reliability of the solder joint. Investigations on different solder masks could show that solder mask formulations can differ in the risk to release critical components [2]. In addition to a proper curing process, the solder mask should also be selected carefully, considering the subsequent final finish and assembly steps.

3.4 Process Flows

3.4.1 High Density Interconnect Technology

High Density Interconnect (HDI) boards (Figure 21) were developed in the late 1990s as a sequential build-up technology for advanced multilayer board designs. HDI enables increased interconnection density through miniaturization of holes, pads, and conductors, ensuring the complex connectivity needed for the next system level of IC substrates as chip attachments. Additionally, it allows smaller PCB designs for mobile devices and leaves more space for batteries.

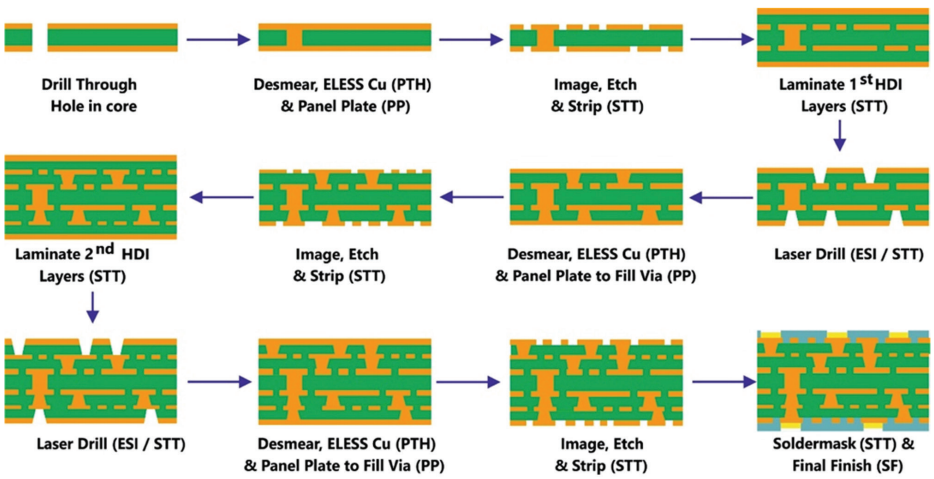


Figure 21. Sequential build-up of advanced HDI boards.

3.4.2 Semi-Additive Processes (SAP)

Further increases in the number of inputs and outputs of integrated circuits require additional miniaturization and other design improvements to HDI build-ups. These include:

- Smaller conductor lines and spaces (L/S)
- Smaller vertical interconnect accesses (VIAs)
- Improved electrical performance of faster signal speeds
- Improved thermal properties of the substrates by integrated heat-sinks
- Decreasing radio frequency interference/electromagnetic interference/electrostatic discharge (RFI/EMI/ESD)

Copper layer thickness, along with dielectric material properties of the substrate, are a particular focus of the “Semi-Additive Processes” (Figure 22).

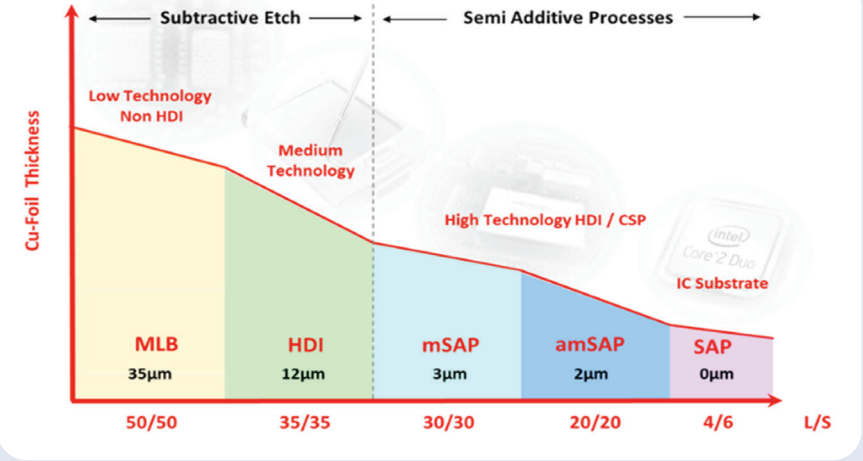


Figure 22. Impact of Cu-foil thickness on conductor line and space capability.

In addition to the specific dielectric material properties of the substrate, the copper layer thickness is a particular focus of the "Semi-Additive Processes" (SAP). Depending on the L&S requirements, different SAP techniques are applied (Figure 23):

- Modified SAP (mSAP) and advanced modified SAP (amSAP) using FR4/FR5 glass-fiber reinforced epoxy resin dielectrics combined with 2-3 µm copper foils:
  - In some applications copper foils of 9 or 12 µm are chemically etched to approximately 3 µm ("thinning"). This saves costs related to the purchase of the very thin copper foils.
- SAP substrates have a modified dielectric surface layer consisting of glass filler particles in an epoxy matrix without any Cu foil on top:
  - After via formation the dielectric surfaces need to be chemically micro-roughened ("desmeared") using a Sweller/Permanganate process and metallized using electroless copper deposition.

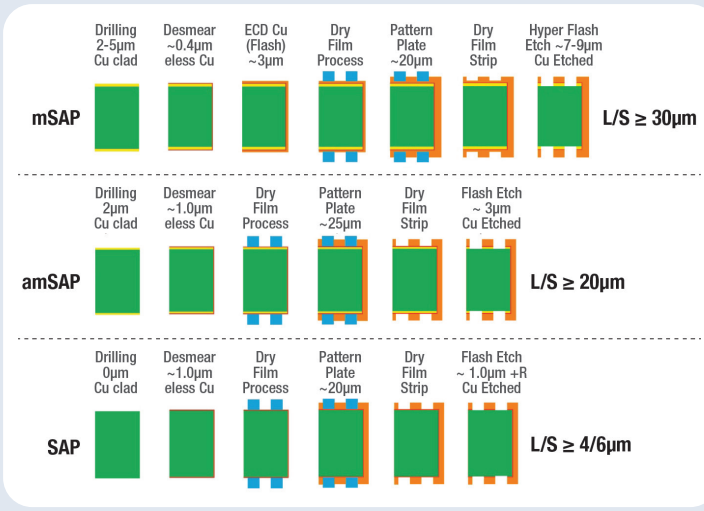


Figure 23. Process sequences for mSAP, amSAP, and SAP.

Prior structures are created by electrochemically deposited (ECD) Cu pattern plating.

3.4.3 Embedded Structures

In traditional integrated circuit substrate (ICS) manufacturing, the metal interconnects are created by depositing metal layers on top of the substrate material, adding additional layers and thickness to the overall device. More recent structural concepts embed the conductor lines in trenches within the dielectric substrate material, resulting in a more compact and streamlined device.

Embedded Trenches

Embedded trenches offer several advantages over traditional ICS manufacturing techniques, including:

1. **Reduced size and weight:** By embedding the metal traces directly into the substrate material, the devices can be made thinner and lighter than traditional ICSs.
2. **Improved electrical performance:** Embedded trenches reducing parasitic capacitance and inductance in the metal interconnects, which can improve the overall electrical performance of the device.
3. **Enhanced reliability:** By eliminating the need for multiple metal layers, the devices are more reliable and less prone to failure.
4. **Lower manufacturing costs:** Embedded trenches simplify the manufacturing process by reducing the number of process steps, lowering manufacturing costs.

Embedded Trace Substrates - ETS

Embedded Trace Substrates (ETS) have a coreless structure with fine conductor lines and spaces (Figure 24). These are formed by ECD Cu pattern plating onto traces on the top layer separated by dry film. On a FR4 core, ECD Cu is pattern-plated, followed by the lamination of dielectric films (Resin Coated Copper Foils – RCC or RCF) on both sides of the substrate. This is structured by laser ablation and ECD Cu plating (SAP sequence, see above). A peelable copper foil allows the detachment of each build-up layer side. After differential flash etch of the one-sided copper foil, the double-sided build-up substrate can be further processed. Figure 25 shows the ETS process sequence. The exact process flow can vary depending on the specific materials and manufacturing processes used, but the steps outlined in the figure are typical of the ETS process.

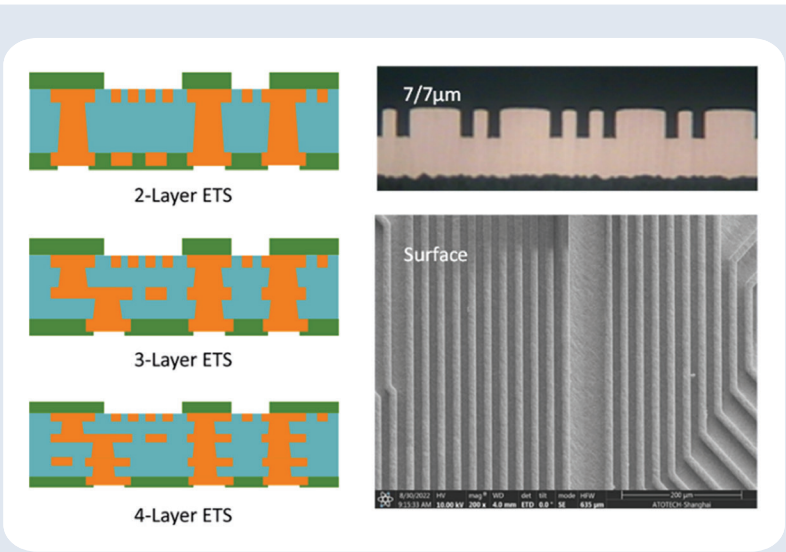


Figure 24. ETS designs.

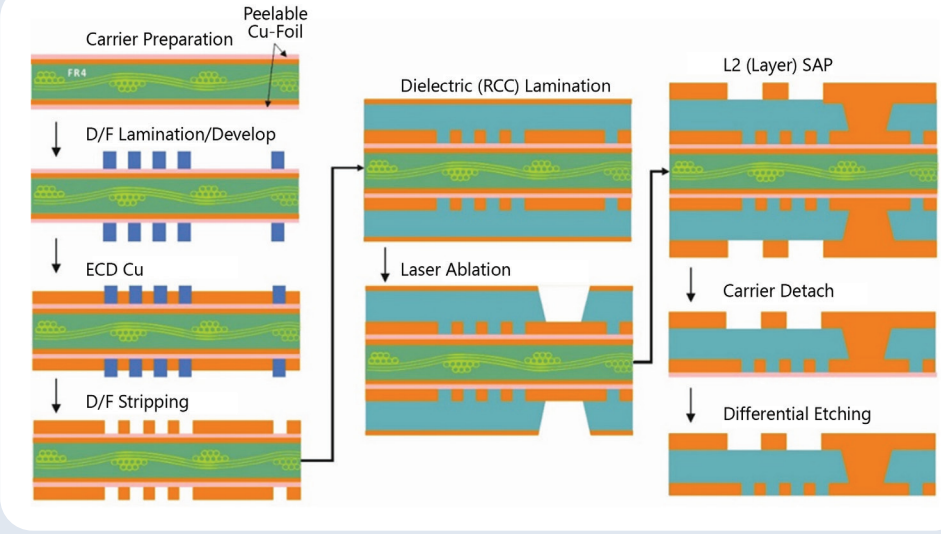


Figure 25. ETS process sequence.

Laser Embedded Conductor Substrate (LECS)

In contrast to ETC, LECS traces are ECD Cu plated onto the laser-structured dielectric surface of an ICS (Figure 26). As with SAP, the entire dielectric surface is micro-roughened and plated using electroless copper prior to trench filling by ECD Cu. LECS layer topography can remain quite smooth relative to the roughness required for SAP substrates (Figure 27). The smooth LECS dielectric surface facilitates final

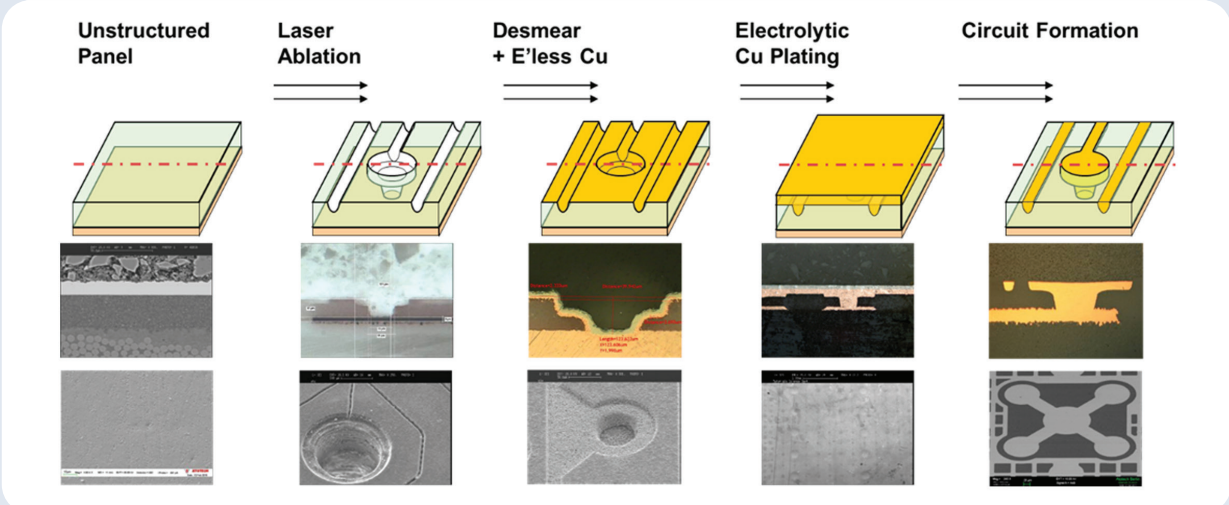


Figure 26. Process sequence for LECS.

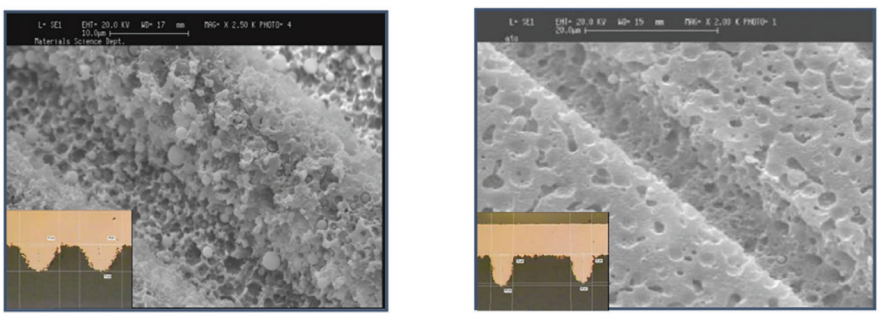


Figure 27. SAP vs. LECS micro-roughening requirements.

circuit formation steps such as Flash Etch and Palladium-strip. LECA and SAP can be used in combination in some applications (Figure 28).

The main advantages of LECS over ETS and SAP include:

- Reliable final circuit formation due to low dielectric roughness.
- The lack of handling of dry films for fine line applications results in higher product yields, reducing production costs.
- Conductor shape, flatness, and roughness is optimal for high frequency applications in impedance-controlled designs.
- Embedded structures give higher peel strength and lower the potential for damage.

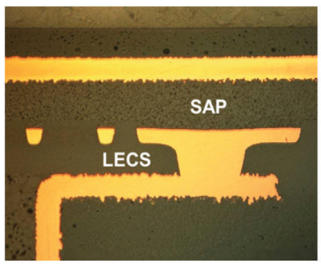


Figure 28. Combined build-ups of LECS and SAP layers.

Via in Pad Plated Over – VIPPO / Plated Over Filled Via - POFV

BGAs (ball grid arrays) in a PCB design can be redesigned as via-in-pad plated over (VIPPO) or Plated Over Filled Via (POFV) structures that offer designers a means to further increase the integration density and hence the performance of ICSs. VIPPO and POFV designs improve signal integrity, especially in high frequency applications, and increase device packaging density on the substrate surface. Compared to "Dog-Bone" via designs, VIPPO structures shorten signal path lengths and reduce high frequency RC signal losses and interference (Figure 29). Key feature of the VIPPO/POFV process are filled vias, either plugged by epoxy resin and wrap-plating or copper filled by inclusion-free ECD Cu plating (Figure 30, Chapter 4.5). Additionally, ECD Cu-filled vias can act as heat sinks, allowing the improved dissipation of heat from the substrate. Advanced ICS build-ups can contain different combinations of filled via types (Figure 31).

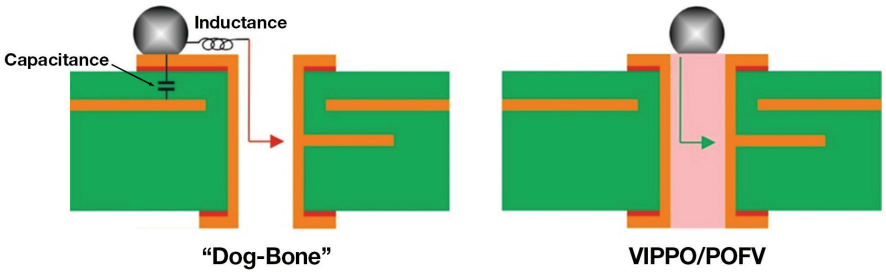


Figure 29. Electrical interference: "Dog-Bone" vs VIPPO/POFV via design.

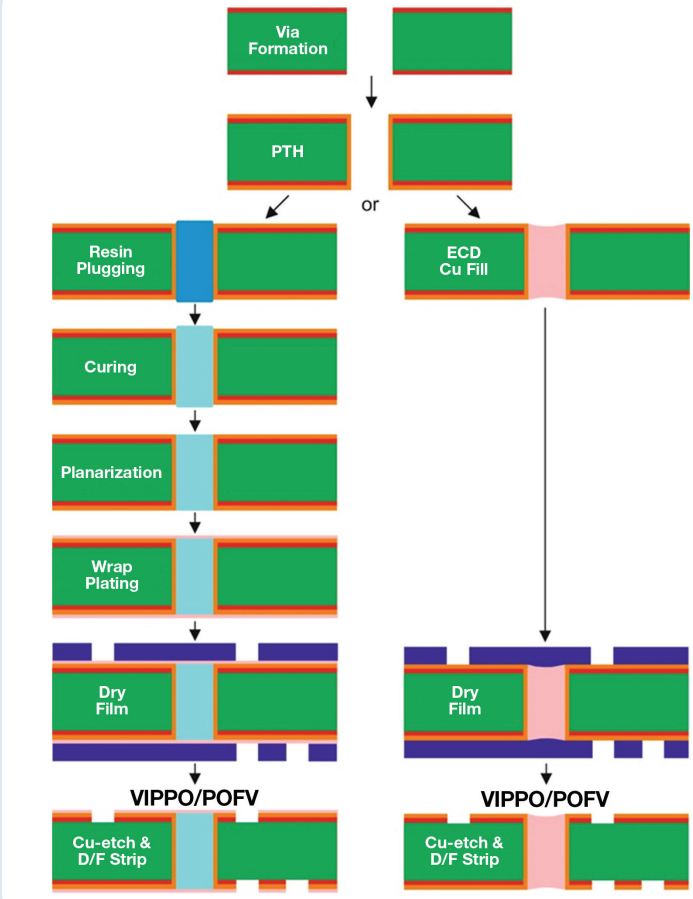


Figure 30. Process sequence for VIPPO/POFV.

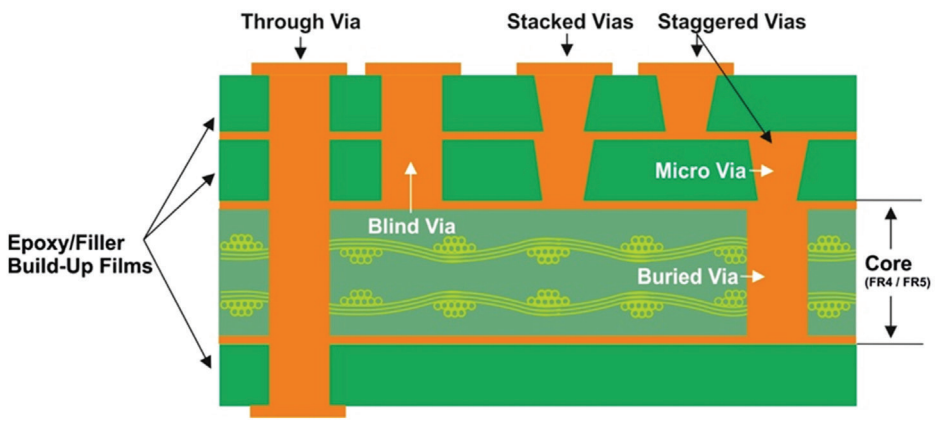


Figure 31. Possible ECD Cu-filled via designs for VIPPO/POFV.

Embedded Components

Further miniaturization of the PCB/package size and even better signal integrity can be achieved by embedding electrical components within the build-up of the substrate of, for example, a dielectric polymer resin composition (plastic encapsulation), a glass fiber epoxy composite (FR4 type materials), or a ceramic composite material. In such designs SMT devices like resistors, capacitors or even semiconductor dies are embedded in the inner layers of the PCB package (Figure 32, Figure 33).

A single die, multiple dies, MEMS, or passives can be embedded side-by-side within the core of an organic laminate substrate. The components are connected using copper-plated vias. As well, the embedded package resides on the board, freeing up space in a system.

Embedded die technology provides distinct advantages. Stacking all dies vertically within a substrate can reduce area requirements by 65% as compared with pure 2D placement. This helps to reduce transmission distance and increase transmission speed and bandwidth. Low power loss and consumption are further advantages, as well as optimized heat dissipation by heat sinks created by ECD Cu-filled through holes (Figure 34) [3] [4].

Finally, embedded components allow shorter trace lengths between electrical components without the addition of via holes. This provides the following advantages:

- Reduced number of metal interfaces (improved reliability)
- Improved signal integrity (high frequency)
- Reduced environmental corrosion of electrical embedded components (automotive)
- Improved heat dissipation via the substrate (Cu-filled vias)
- Reduced manufacturing costs of the assembled ICS package
- Protection of conceptual IP of the overall package design

It is noteworthy that, once components are embedded, reworking of the entire package is no longer possible. This makes yield losses a significant cost risk for designs that employ embedded components.

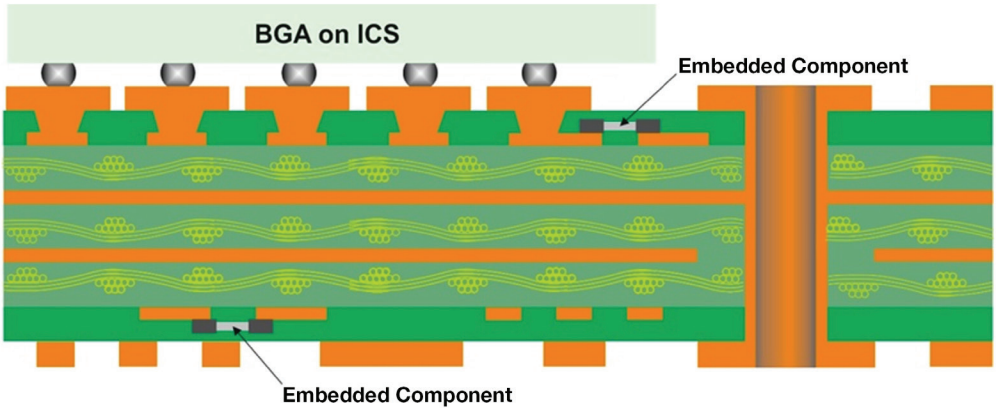


Figure 32. Embedded "passive" components like resistors or capacitors in ICS build-up.

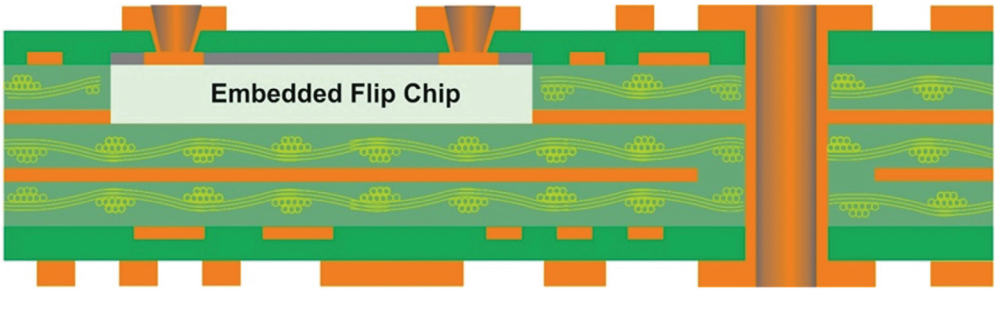


Figure 33. Embedded flip chip in ICS build-up.

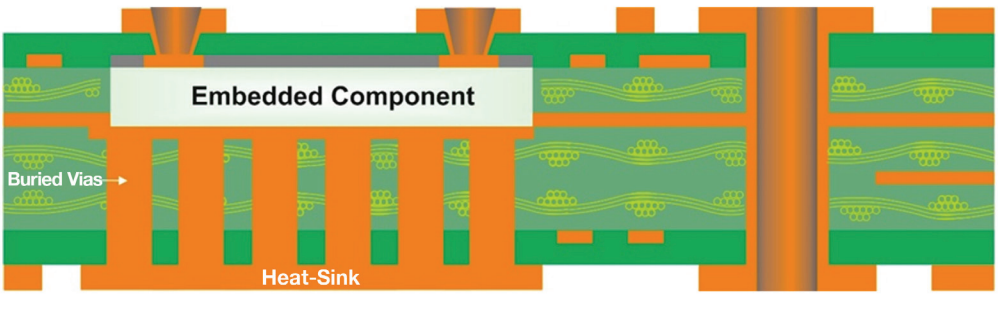


Figure 34. Embedded component with heat-sinks by buried vias.

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Chapter 4

IC Substrate Manufacturing Process Technologies/Equipment

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4.1 Introduction

Fabricating the structure (substrate) that supports and integrates semiconductor and ancillary components in a successful electronic device requires processes that exhibit high levels of accuracy, repeatability, reliability, and, of course, productivity. This, in turn, requires the right combination of tools, materials, and chemistries in the fabrication process. This chapter reviews the typical process steps, materials, and equipment used in IC substrate manufacturing. The discussion will provide specific examples of the systems and chemistries used in high performance substrate manufacturing. In addition, the text will explore some potential emerging technologies.

Our discussion starts with substrate core manufacturing. The core is a critical part of the substrate that provides structural rigidity, planarity, and electrical interconnectivity in the final electronic device. This will be followed by a description of how different layers are fabricated on the core using lamination techniques and by a discussion of laser via drilling processes for interlayer connections. The different options for the multi-step and multi-chemistry processes for patterning and metallization that produce certain circuit features in the substrate are then reviewed. The review includes discussions of various sub-processes such as desmear and electroless plating and provides a brief overview of some primary equipment options that are used in the execution of these processes. Next, we will describe the concepts, processes, and fundamental process parameters of electrochemical metallization. Advanced plating techniques such as reverse-pulse plating and Cu pillar growth are described.

Circuitization is the process of creating the final circuitry that routes electrical signals and power, and sometimes heat throughout the final multi-layer substrate. Section 4.8 describes the process steps that create the very fine circuitization features, along with different options for equipment and chemistry. This is followed by a discussion of the production of the final finish (both metallic and organic) that protects the integrity of exposed Cu features and optimizes the finished substrate surface for subsequent soldering onto the substrate. Various concepts and parameters needed for reliable solderability conclude this chapter.

4.2 Substrate Core

4.2.1 Overview

The substrate core (Figure 1) provides structural integrity in the final package and serves functional roles such as thermal management. The base material of a core is usually a glass-woven prepreg (FR4, BT) of variable thickness. Through-hole vias (THVs) in the core layer are created using either a mechanical or a laser drilling process, with the choice dependant on the board design and via density. Unlike subsequent build-up layers on the substrate, which are constructed using additive, semi-additive or modified semi-additive processes, layer structures in the core are normally produced using subtractive processes such as panel plating/DES (develop, etch, strip) to create patterns in a Cu layer.

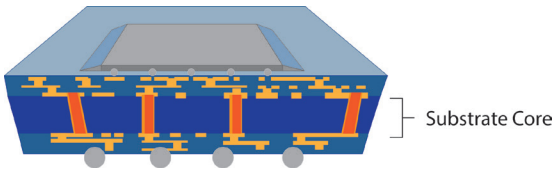


Figure 1. Organic substrate core.

4.2.2 Base Materials

The base of the substrate core consists of a woven glass fabric impregnated with either an FR4 epoxy or a BT (Bismaleimide-Triazine) dielectric polymer resin. BT offers advantages in terms of greater thermal stability and moisture resistance which ensures less warpage and an increased dimensional stability. Core thicknesses normally ranges between 50 µm (ultra-thin core) and 500 µm, with 100-200 µm being the most commonly used for low line/space (L/S) dimensions in subsequently added thin layers of ABF. The core is supplied by the manufacturer with electrolytically deposited Cu foil pre-laminated on both sides (Copper Clad Laminate – CCL, Figure 2; Chapter 3.1.3). The overall thickness of the CCL depends on the intended application, package size, and function. The thickness of the Cu foil can range between 1.5 µm to 18 µm, depending on the L/S parameter and the electrical specifications of the finished product. Figure 2 provides an illustration of the CCL structure.

Figure 2. Copper Clad Laminate (CCL) structure.

4.2.3 Substrate Fabrication Processes

The CCL first has holes drilled through it. The holes are then Cu-plated to create THVs. Substrates with low via densities (e.g., <50K vias) normally have mechanically drilled vias with larger diameters (e.g., >200 µm). Substrates with higher via densities and lower via diameters employ laser systems to drill the vias. Laser through holes (LTH) are drilled in a two-step "X-via" process in which the via is first opened on the top side, then the panel is flipped and the remainder of the via is drilled from the bottom side. CO_2-laser systems (such as the MKS Geode) are usually used for LTH core drilling. These systems have throughput/efficiency benefits for a range of via sizes and are better for drilling through glass cloth (CO_2-laser energy couples better with woven glass, enabling more effective material ablation). When a core requires LTHs, the Cu surface must be treated to facilitate laser energy absorption (black oxide or alternative oxides such as MKS' Bondfilm®). Alternatively, the area to be drilled can be Cu-relieved prior to drilling using photolithography and DES processes or UV laser-based Cu ablation.

Once the vias have been created, the panel undergoes desmear, electroless Cu plating, and electrolytic Cu plating in a "panel-plating process" that produces an even conducting layer on the top and bottom of the laminate and on the sidewalls of the THVs. The remaining space within the THVs is filled with conductor using a curable pasted in a squeegee/template process (mechanically drilled THVs) or using an additional electrolytic Cu-fill process step (LTHs). Following the squeegee/template process, the panel undergoes a grinding process in which any residual cured paste is removed to create a planar panel surface. The choice of whether to fill LTHs with electrolytic Cu is subject to aspect ratio considerations.

The circuit pattern on the plated core is created using photolithography followed by a DES process or by Laser Direct Imaging (LDI). The panel is first cleaned, producing a micro-roughened surface that ensures proper adhesion of a photosensitive dry film (DF). The panel surfaces are then coated with a layer of DF and undergo patterned exposure to UV light, either in a photolithographic process or using a UV LDI system. The panel is treated with an aqueous developer process that removes DF in areas that have not been exposed, creating a negative pattern on the panel surface. The Cu in the DF-free areas is removed using an HCl acid process and the panel undergoes a stripping step that removes the remaining DF, revealing the final circuit pattern on the panel surfaces (Figure 3).

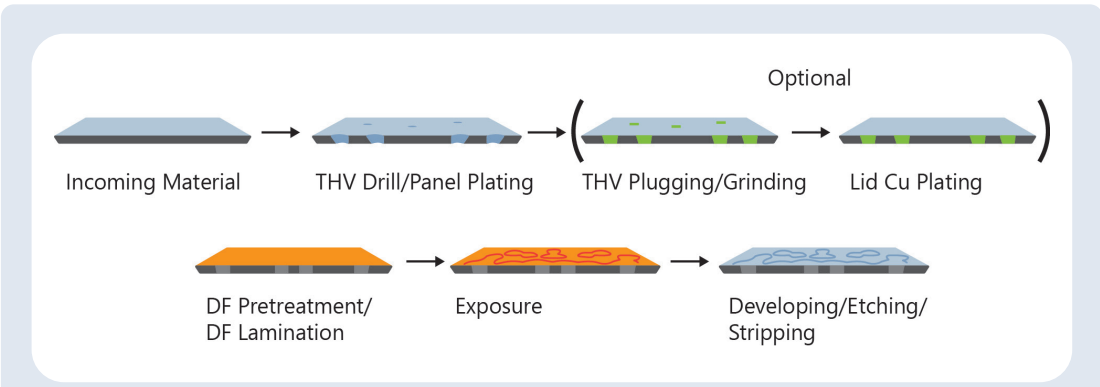


Figure 3. IC substrate fabrication process.

4.2.4 Glass Core Substrate (GCS)

Glass core substrates are a promising alternative to organic (glass fiber/resin) core substrates. They offer higher structural integrity, resistance to vibration and temperature, environmental ruggedness, and low electrical loss. These properties contribute to faster speeds, smaller signal-to-signal spacing and ease of use, making them ideal for next-generation electronic device designs. Figure 4 compares the properties of glass vs. organic core substrates. Glass substrates are lower cost (even for larger packages), allow direct attachment of the package to the PCB, and offer better electrical performance with lower RC delays. These properties make glass core substrates (GCS) better suited than organic cores for extremely dense wiring. Glass is also stiffer, has a lower coefficient of thermal expansion and is much smoother, which allows more advanced lithography techniques to be used in creating hole and circuit patterns in the panel.

Glass core substrates permit high aspect ratio Through Glass Vias (TGVs, i.e., 6:1 → 10:1 → 20:1), higher via density, and much finer pitch as compared to organic core substrates. This allows for a much higher I/O density and, if the TGVs are copper filled, provides better thermal heat management than is possible with organic core substrates. Glass is also much more rigid than organic core substrates, which minimizes warpage issues. This means that co-planarity is improved on the surface of glass core substrates, enabling much finer Redistribution Layer (RDL) structures for chip-to-substrate interconnects. Glass core substrates are well suited for next-generation device designs requiring faster speeds, smaller signal-to-signal spacing, and greater simplicity in the fabrication of large body packages (>100 mm x 100 mm).

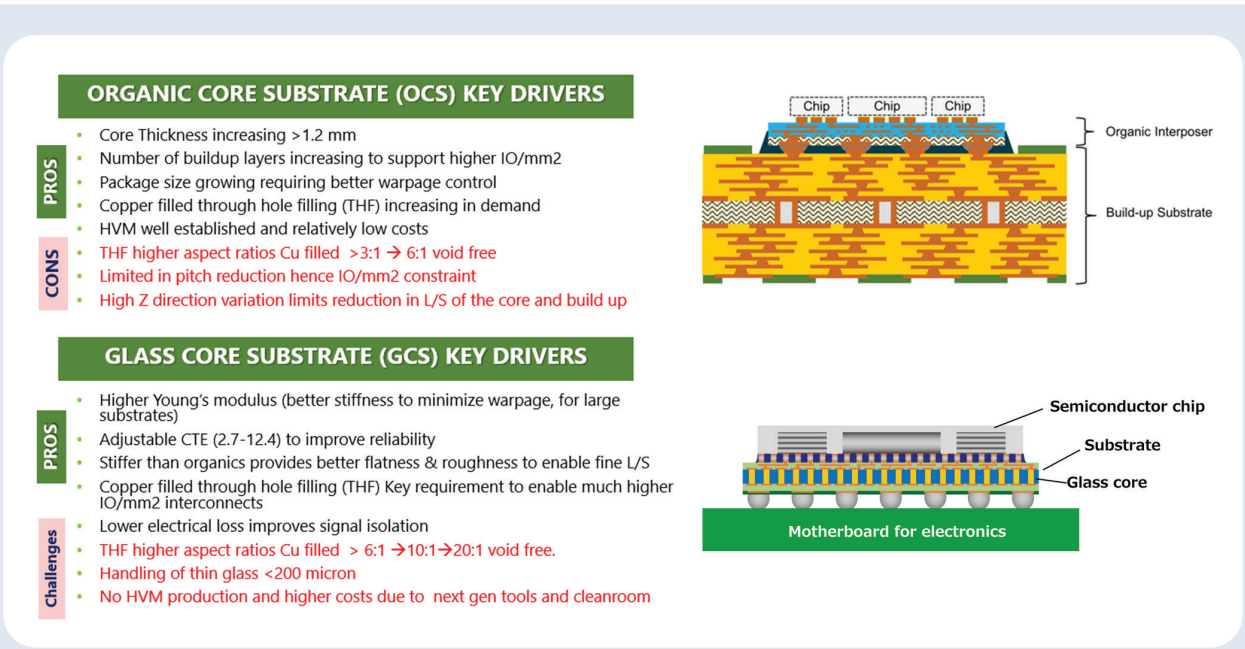


Figure 4. Organic vs. glass substrate core [39], [40].

4.3 Lamination

Lamination uses a combination of heat, pressure, and vacuum in a sequential build-up (SBU) process to add new layers of dielectric (and Cu foil) for subsequent mSAP or subtractive patterning processes (Figure 5). The resulting laminated panel is ready for the further processing of a new Cu-patterned layer on front and back. ABF (Ajinimoto Build-Up Film) is commonly used for the layers laminated onto the core. However, BT, FR4 and any combination of those with ABF may be employed (albeit with differing Cu plating schemes). Optimal adhesion between the new layers (with dielectric) and the completed (patterned) layers is promoted by modifying the surfaces before pressing/laminating. This treatment

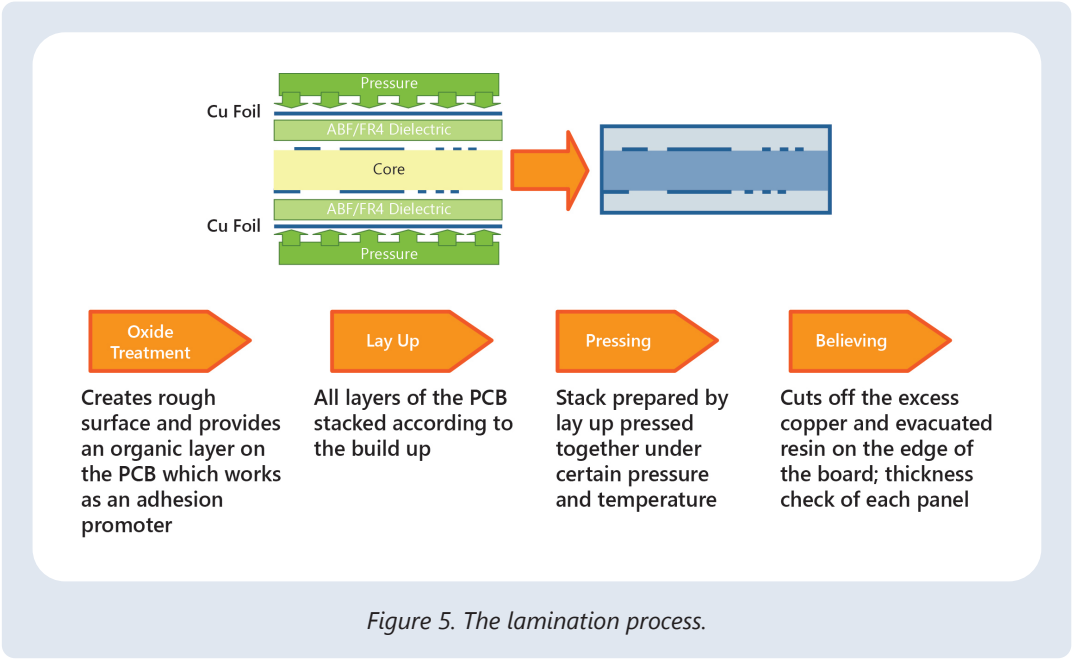


Figure 5. The lamination process.

uses a series of wet processes containing an adhesion promoter and several pre-and post-treatments that micro-roughen the exposed Cu surfaces on the front and back of the panel. This provides better topographical anchorage to the melting resin/epoxy during and after the lamination cycle. Inter-material adhesion is crucial for reliability during later process cycles (further lamination, surface mount technology, reflow cycles, etc), as well as for the optimal operation of the final product.

Following adhesion promotion of the core surfaces, layers of new materials are added in what is known as lay-up (Figure 6). Normally, a Semi-Additive Process (SAP) for lay-up includes only the ABF dielectric, protected with a thin layer of PET. For other modified-SAP (mSAP) and subtractive patterning processes, a Cu foil is added at lay-up. The stacked materials for lamination are then placed between large steel plates that support an even distribution of heat and pressure across the entire panel. The lamination follows a particular "recipe" of heat (relative to the base material's glass transition temperature, Tg), pressure, and vacuum (to remove any entrapped air and support even material distribution) over time. After a pre-determined cooling period, the laminated panels are removed from the press. Since some resin/epoxy is squeezed out of the panel during pressing, the rough, uneven panel edges must be bevelled or cut to achieve the dimensions and quality needed for further processing.

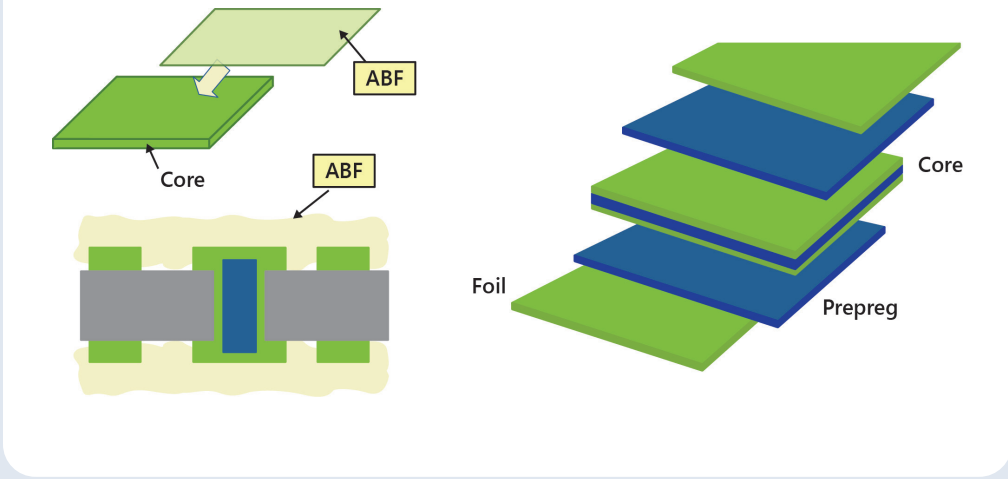


Figure 6. Adding layers during lay-up.

4.4 Via Drilling

4.4.1 Introduction

There are two basic types of vias: through vias and blind vias. Through vias pass through all copper layers in the build-up and are drilled from either a single side or both sides of the panel, depending on the material stack and drilling system. Blind vias are drilled through one, or occasionally two ("skip via"), layers in a PCB stack-up. Buried, stacked (vertically aligned), and staggered (vertically offset) vias are special implementations of blind vias. Thermal vias provide additional Cu density for heat dissipation and can be either through or blind vias. Microvias are generally designed to have a maximum aspect ratio of 1:1 for hole depth/diameter having a total depth of no more than 250 µm [1], but more challenging designs often exceed this aspect ratio.

Mechanical drills can reliably form vias larger than 100 µm. Lasers are needed for smaller vias in the 10-100 µm range [2] [3] [4]. For even smaller vias (<10 µm) a variety of drilling technologies are in active development, from more advanced UV laser systems to shorter wavelength DUV and Excimer lasers [5] [6] [7]. Our discussion will focus on the proven technologies of CO_2 and UV laser drilling.

Laser drilling offers the following advantages:

- It is a non-contact process
- Greater diameter tunability and shape flexibility
- Better drilling accuracy
- Superior depth control

CO_2 laser-based systems with up to kilowatt laser powers offer the best combination of throughput, quality, and general capability for advanced packaging applications [8] [9]. High volume manufacturing using these lasers can create blind microvias in both copper-clad and unclad materials with a finished (plated) diameter of <50 µm. Systems such as the MKS Geode can reliably produce vias with as-drilled diameters of <30 µm in copper-clad materials and ~30 µm in unclad ABF laminates. CO_2 laser processes become wavelength-limited below 30 µm and UV laser-based systems with wavelengths of 343 nm or 355 nm are used for drilling through vias or for blind microvia with diameters <30 µm. Laser systems operating at green (~515-532 nm) and near-IR (~1030-1064 nm) wavelengths may also be employed for certain specialty via drilling applications but are not common.

Section 4.4.2 and 4.4.3 reviews the critical issues for producing state-of-the-art throughput and quality in microvias for Advanced Packaging. The discussion will include via drilling for copper-clad materials and Ajinomoto build-up film (ABF), along with some other materials of interest.

4.4.2 Via Drilling for Glass-reinforced Copper-clad Laminate (CCL)

CCL via drilling is performed in two phases: (1) formation of the copper opening to define the diameter and roundness of the via; (2) removal of the dielectric (e.g., FR4, ABF) to shape the sidewalls and clean the inner copper layer sufficiently in preparation for subsequent desmear and plating steps. Figure 7 shows the critical CCL BMV dimensions, and Table 1 provides representative performance targets for each characteristic. An 'ideal' via would have perfectly straight sidewalls with no glass fiber protrusion, and no remaining resin on the capture pad prior to desmear. Out-of-spec critical dimensions can result in microvoids and other defects that lower yield and reliability.

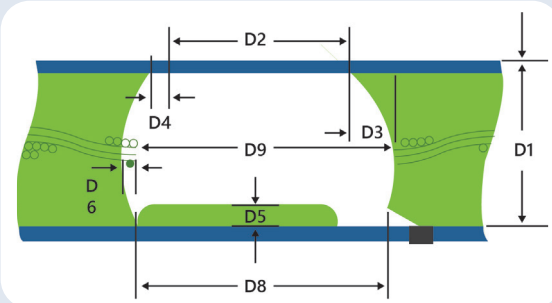


Figure 7. Critical parameters for via drilling of glass-reinforced CCL.

Microvia laser drilling processes must be robust while enabling high throughput at low cost. Achieving these characteristics is complicated by the fact that microvia drilling must efficiently ablate all the different material layers in a CCL since the effectiveness of laser drilling depends on the efficiency of the absorption of the laser energy by the material being drilled. Figure 8 shows the relative absorption of laser energy at different laser wavelengths by the copper, resin, and glass materials present in a CCL. While all three materials absorb strongly in the deep UV region (DUV, <280 nm), absorption efficiency is strongly dependent on the material at other laser wavelengths (i.e. UV lasers (343-355 nm), green lasers (515-532 nm), NIR lasers (1.03-1.64 µm), and CO_2 lasers (9.3-10.6 µm)). The prohibitive cost of DUV lasers and the marked disparities in laser energy absorption exhibited by copper, glass and resins at UV and green laser wavelengths make these choices less acceptable for achieving the preferred characteristics in microvia drilling applications. CO_2 lasers operating in the mid-infrared region (9.3-10.6 µm) provide an acceptable compromise that can achieve robustness, cost-effectiveness, and high throughput in microvia drilling applications. While laser energy absorption into copper is poor with CO_2 lasers, both glass and resins exhibit strong absorption at wavelengths around 10 µm, much better than with laser energies in the UV to NIR range. In a microvia drilling process, the laser energy absorption of copper can be significantly magnified through the addition of an oxide surface treatment such as MKS' BondFilm® LDD. These oxide layers are strongly absorbent at CO_2 laser wavelengths, enabling energy transfer from the laser to the underlying copper film. Highly effective CO_2 laser-based microvia drilling processes for glass-reinforced CCLs have been developed, however, the ablation dynamics of the different layers in a CCL are very different, making microvia drilling in glass-reinforced CCLs a remarkably complex process.

Characteristic	Label	Typical Performance Specification
Maximum Depth	D1	Includes top copper and dielectric thickness
Top Copper Diameter	D2	Target ± 10%, Mean ± 4σ
Undercut / Bulge / Barrelling	D3	D2 < 100 µm: Max 15% of D2 D2 > 100 µm: Max 15 µm
Undercut / Overhang	D4	D2 < 100 µm: Max 10% of D2 D2 > 100 µm: Max 10 µm
Remaining Resin after Drilling	D5	≤1 µm
Glass Fiber Protrusion (GFP)	D6	D2 < 100 µm: Max 10% of D2 D2 > 100 µm: Max 10 µm
Capture Pad Diameter	D8	0.8*D2 < D8 < 1.1*D2
Minimum Diameter (Middle)	D9	D9 ≥ D8; Max <3 µm

Table 1. Representative microvia parameter specifications for Advanced Packaging.

Copper Opening

Figure 9 shows a simulation of a process for copper opening through a 12 µm copper film (with black oxide, not shown) on resin using a CO_2 laser. The surface of the copper films first melts due to thermal energy transfer from the oxide layer. This produces a zone of liquid copper that has a much higher absorptivity than the reflective solid at 9.3 µm. The layer of liquid copper provides an energy coupler that melts the remainder of the underlying copper film. The heat from the melting copper is transferred to the copper/resin interface, producing a build-up of vapor pressure at the interface. As the liquid copper pool reaches the interface, the vapor is explosively released, ejecting the molten copper from the microvia [10]. The same copper melt formation and ejection mechanism occurs with thin advanced packaging copper foils. While the use of an oxide surface layer is not needed for copper films ≤3 µm thick, absorption-enhancing surface pretreatments continue to provide benefits in terms of via diameter, roundness, and recast/splash control.

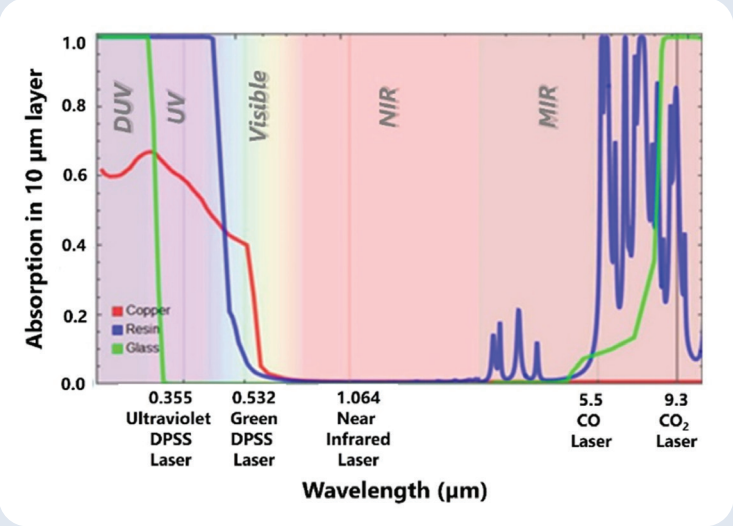


Figure 8. Example absorption spectra for the constituent materials comprising Advanced Packaging PCBs.

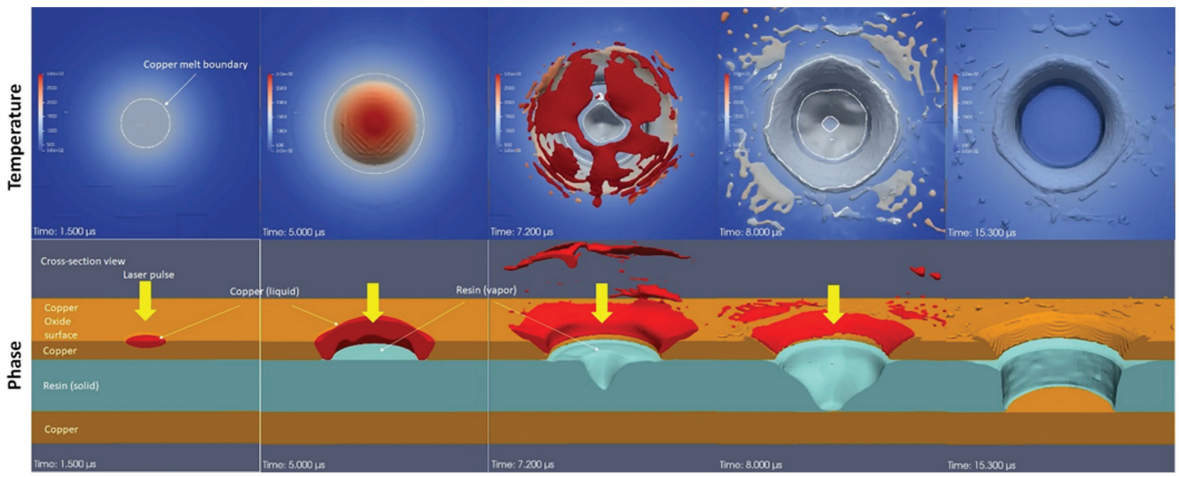


Figure 9. Multiphase simulations showing the dynamics of a CO_2 punch process on a standard CCL material, with time increasing from left to right. The top row shows the temperature and the bottom row shows the phase diagram. In the phase diagram, the solid copper surface is orange, with red showing the liquid/melted copper; the solid resin is dark teal, with the liquid/melted resin shown as lighter teal. (Source: ESB R&D group)

Dielectric Fiber Cloth Drilling

The challenges of drilling and clean-up of the dielectric glass fiber weave in CO_2 microvia drilling processes are very different from those encountered with copper opening. It is especially difficult to simultaneously minimize overhang and achieve an optimally high taper ratio, while keeping glass fiber protrusions in check. The image on the left side of Figure 10 shows the intrinsically inhomogeneous fiber distribution in a typical glass fiber cloth (type 1037). The nature of the cloth means that it is impractical to precisely place via drilling locations in areas of constant fiber density. This means that a single laser drilling process cannot be entirely deterministic in its results and microvia drilling recipe parameters must be a compromise that accommodate all possible glass fiber densities. The two images on the right-hand side of Figure 10 were drilled using the same process parameters in areas of different fiber density. These show the competitive balance between taper and overhang – the same process can produce a via with excellent taper but large overhang in a fiber-sparse region (top) and great overhang but poor taper in a fiber-dense region (bottom). This difference is due to the fact that resin and glass fibers have different absorption coefficients, ablation thresholds, and ablation rates. Other varieties of glass fabric (e.g., 1010, 1017, 1027) may have smaller diameter fibers and/or better spreading but some amount of variation will inevitably exist, and as via sizes continue to trend towards smaller target diameters, this delicate balancing act between taper and overhang remains an issue.

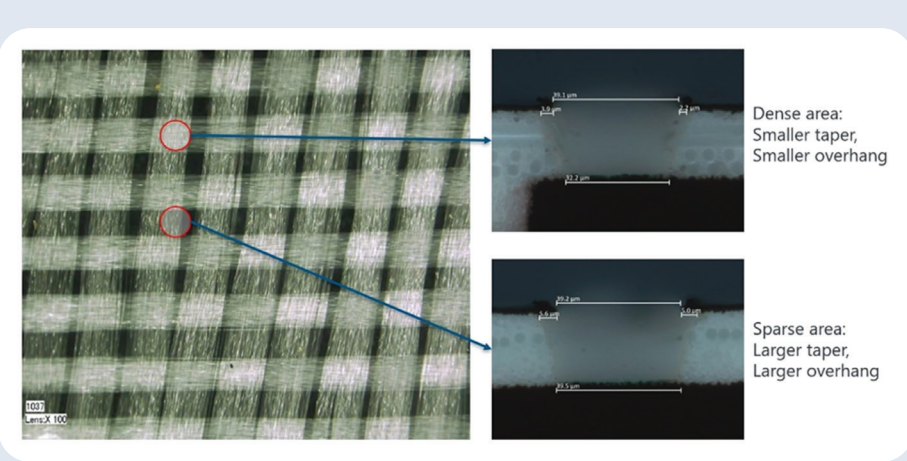


Figure 10. Image of typical 1037 glass fiber weave (left) [8]; the varying effect of identical drilling processes in sparse and dense glass fiber regions showing difference in taper and overhang (right). (Source: ESB process development)

UV ns Drilling of Glass-Reinforced CCLs

UV nanosecond (ns) laser systems are the industry standard for BMV drilling of Flexible PCB (FPCB) stackups. These systems have pulse durations in the tens of nanoseconds, average powers at the work surface of <30 W, and repetition rates ranging from 40-300 kHz. The shorter wavelength of the laser radiation allows much smaller spot sizes than is possible with CO_2 laser systems. UV ns laser systems are very effective for copper opening in CCL microvia drilling but are significantly less effective in drilling through the glass fiber bundles in FR4 where they are slow and expensive compared to CO_2 systems.

UV ns lasers have the advantage of being able to drill through copper by direct ablation rather than by the secondary melting process that occurs with CO_2 lasers (Figure 8 and Figure 9). In a UV ns drilling process, a train of low energy pulses is delivered to the work surface to produce a series of concentric circles as shown in Figure 11. Direct ablation allows much greater control and precision of the diameter, roundness, and splash/recast in the copper opening process. FR4 ablation with UV nanosecond lasers, on the other hand, is sub-optimal. As shown in Figure 8, the laser energy absorption of glass at 343-355 nm is quite poor, while that of resin is quite high. Furthermore, resin has a much lower ablation threshold and heat conduction than glass. This means that resin is easily removed, while the glass fibers act as a heat sink to produce barrelling and glass fiber protrusion. The poor ablation characteristics of glass also force dielectric clean-up steps that can lead to damage of the inner copper layer. For these reasons, UV ns laser drilling systems are usually reserved for CCL 'hybrid drilling' processes in which the UV ns laser performs the copper opening (i.e., because the copper is too thick for CO_2 direct laser drilling), while a CO_2 system drills through the FR4 layer in a subsequent step.

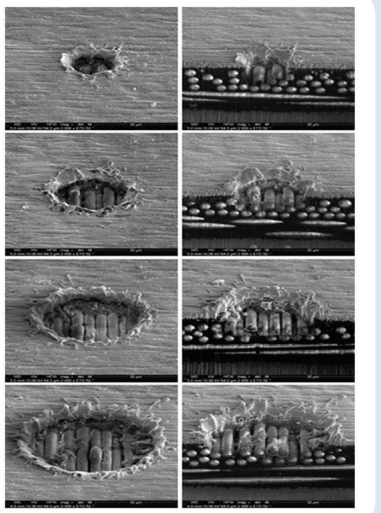


Figure 11. Copper opening process with a UV nanosecond laser and a small spot size, demonstrating a multi-pulse sequence from inward to outward that has good selectivity between the copper and dielectric layers. UV ns lasers have improved copper opening quality and control relative to CO_2, at the cost of decreased productivity. (Source: ESB process development)

Ultrafast Laser Drilling of Glass-reinforced CCLs

Recently, "ultrafast" femtosecond and picosecond UV and green laser systems (~300 fs – 10 ps) have been tested in this applications space [11] [12]. Ultrafast systems differ in comparison to UV ns laser systems in the following ways:

- The short pulse durations allow peak powers several orders of magnitude higher than are possible when using nanosecond pulsed lasers. This results in greater laser energy coupling into glass that would otherwise be transparent at the laser wavelength.
- The short pulse durations enable the design of laser processes that transfer much less thermal energy into the material during processing, reducing the heat affected zone (HAZ) and effects such as barrelling.

The shorter pulse durations are as effective in copper opening as ns UV laser processes, with potential reductions in splash, barrelling, and glass fiber protrusion. It is more difficult to achieve adequate taper, and the differentiation between ablation thresholds for dielectric and copper is reduced, making it problematic to reliably avoid damaging the inner copper layer [11]. Further validation of the performance, reliability, and yield in ultrafast laser drilling is required before these processes can be employed in production. Like UV ns lasers, their $/W cost is higher than CO_2 lasers.

4.4.3 Laser Drilling of Ajinomoto Build-up Film (ABF)

ABF panels (Figure 12) are laminated with a protective PET film on top of the dielectric ABF layer. Historically, the PET film was removed prior to any laser drilling, but as via diameters became smaller it became advantageous to leave the PET film on the ABF panels to enable smaller via diameters. PET has very high absorption at the ~9.3 µm wavelength of CO_2 lasers. Once the opening is drilled in PET at the beginning of the laser pulse, it acts like a mask or aperture for the rest of the pulse, similar to opening the top copper layer in a CCL but with a much smaller difference in performance relative to the dielectric. Non-CO_2 laser systems may still require the removal of the PET film prior to drilling for two reasons: some sources, such as UV nanosecond lasers, have very poor absorption in standard PET and are unable to drill it effectively; and drilling through the PET takes many additional pulses, significantly reducing throughput. With the smaller beam diameters enabled by shorter wavelength lasers, such as UV, via diameters smaller than those possible with CO_2-drilling of ABF with or without PET are feasible. Therefore, there is usually no good reason to leave the PET on when drilling ABF with non-CO_2 lasers (except for panel handling convenience). The target specifications for ABF vias are listed in Table 2.

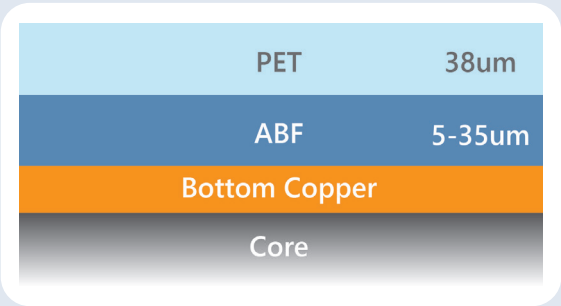


Figure 12. Schematic of a single layer of ABF laminated to a core, with protective PET layer still in place. ABF thickness range is representative of those used in Advanced Packaging applications.

Characteristic	Label	Typical Performance Specification
Material Thickness / Via Depth	D1	ABF only, PET not included
Top Diameter	D2	Target ± 10%, Mean ± 4σ
Remaining Resin after Drilling	D5	<1 µm
Capture Pad Diameter	D8	0.8*D2 < D8 < 1*D2

Table 2. General performance targets/ranges for each critical dimension of a typical ABF via (Figure 7 for label definitions).

CO_2 ABF drilling viability quickly becomes limited for target diameters ≤30µm. With current CO_2 drilling capabilities, these dimensions require many low energy pulses and the corresponding throughput reduction. Decreasing the CO_2 spot size beyond its current ~30 µm minimum in state-of-the-art tools is possible, but unattractive due to the system design complications necessitated by the shallow depth of focus. The industry state-of-the-art for drilling ABF vias with diameters from ~5-30 µm requires the use of high repetition rate UV laser systems. These systems enable capability in this diameter range at compelling throughputs, but typically cannot compete with CO_2 system throughput and $/via performance at larger diameters. Representative images of vias from ~7-15 µm diameter are shown in Figure 13.

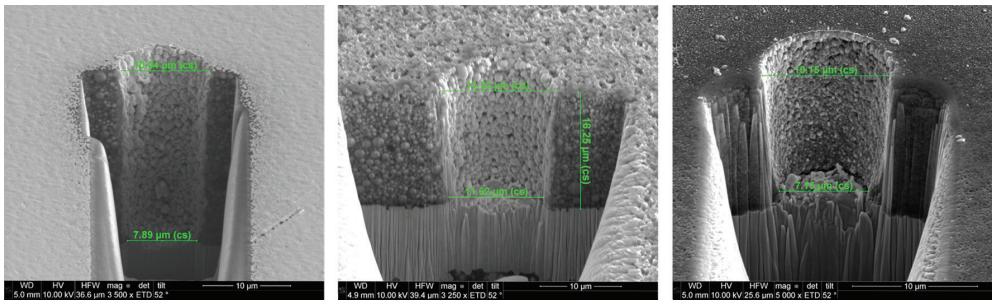


Figure 13. FIB-SEM images of UV-drilled vias <20 µm diameter.

4.4.4 Additional Materials of Interest: RCC and GCP

Recently, two materials that mix the characteristics of glass-reinforced CCLs and ABF have seen growing use in Advanced Packaging – resin coated copper (RCC) and glass cloth with primer (GCP).

There are two different types of RCC – (1) a legacy material that uses an uncured B-stage resin for the dielectric; and (2) a more recent version that uses ABF as the dielectric. The copper used in RCC is similar to that used with standard glass-reinforced CCL. RCC material can be processed similarly to glass-reinforced CCL, with two main differences: (1) the achievable sidewall quality with RCC is more uniform for all laser systems used in via formation since the lack of glass cloth presents a more homogeneous medium for drilling; and (2) non-CO_2 laser systems can effectively clean up dielectric using an out-of-focus beam. This allows for improved efficiency and easier avoidance of bottom copper damage. These differences greatly simplify process development and optimization for each of the laser options and make non-CO_2 options very attractive for drilled vias with diameters ≤30 µm, where CO_2 systems begin to struggle due to beam size and overhang.

GCP is ABF with glass cloth reinforcement and a sacrificial PET layer that remains in place for CO_2 laser drilling and may or may not be removed when drilling with non-CO_2 lasers. The inclusion of glass fiber makes process development more difficult with GCP than with standard ABF. It also results in larger statistical deviations in via quality, especially with respect to taper. As well, it introduces glass fiber protrusions to the via shape. With CO_2 laser processing, higher peak powers are required to cleave the glass fibers. This can lead to degradation of the via entrance, creating a less defined boundary between the top surface and the sidewall ('fluting'). It can also limit the minimum achievable via diameter to a larger size than with a similar traditional ABF layer.

4.4.5 MKS Products for Laser Drilling

MKS offers a broad selection of laser drilling systems configured for each demand. The Geode platform (Figure 14) features unique AOD-based (Acousto-Optic Device) processing that allows the user to finely tune energy and beam spatial displacement. While most Geode configurations are equipped with a standard pulsed CO_2 laser, the recently introduced Geode A (designed for ABF material applications), is the first laser via-drilling system of its kind to employ a QCW (Quasi-continuous Wave) CO_2 laser. This ensures that productivity is maximized without detriment to product quality. Furthermore, the AOD features allow the Geode A to run with significantly lower power consumption, making it a greener choice for advanced laser drilling. The Geode X, currently in development, will offer all the same features and benefits of the Geode platform in a UV laser-based system that can enable much smaller vias (~10 µm) for current and emerging advanced FCBGA applications.

Figure 14. MKS' Geode platform.

MKS' BondFilm® LDD pretreatment was developed to maximize the CO_2 laser energy absorption by the copper layer. The combination of strong intergranular etching and the presence of metal organic conversion coating maximizes the laser energy absorption.

To remove the copper splash after Laser Direct Drilling the BondFilm® LDD SR process can be used. Figure 15 illustrates the superior performance of the BondFilm® LDD SR process to remove the copper splash, reduce the surface roughness, and remove the metal organic conversion coating to protect subsequent processes.

The BondFilm® LDD process usually removes 1.5 µm or more copper. For mSAP applications with thin copper layer thickness of only 2-3 µm which do not permit this high etch depth, a specialized process with an etch depth of only 0.5-0.6 µm, BondFilm® LDD MSAP has been developed. Figure 16 shows the superior performance of BondFilm® LDD MSAP. Without treatment, at the same laser energy of 4mJ, no via was drilled; with BondFilm® LDD MSAP the desired 63 µm via was successfully drilled. To create the same via diameter without treatment, four times the amount of laser energy is needed which translates to four times the time needed to produce the desired via diameter. Therefore, productivity can be significantly increased through the use of BondFilm® LDD processes.

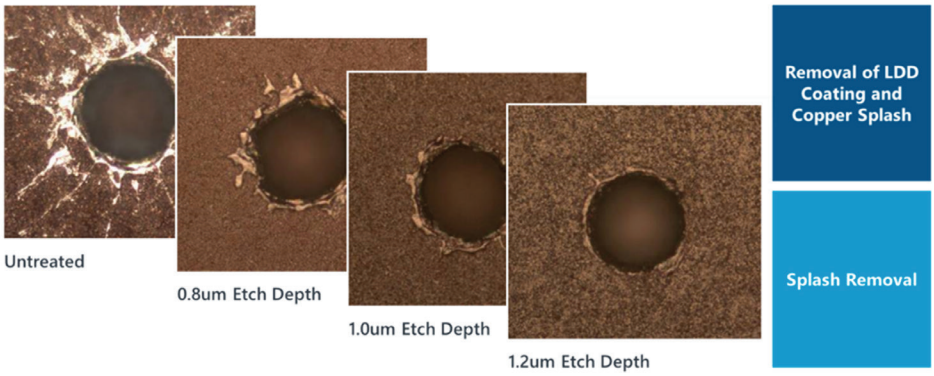


Figure 15. Removal of copper splash by BondFilm® LDD SR.

Product Performance				
No.	LDD Pretreatment (3 μm foil)	Large Parameter	Response	
		Laser Energy	Via Size (μm)	Roundness
1	CCL without pretreatment	4 mJ	0	0
2	BondFilm LDD MSAP	4 mJ	63.1	95.7%
3	CCL without pretreatment	13 mJ	65.2	91.6%

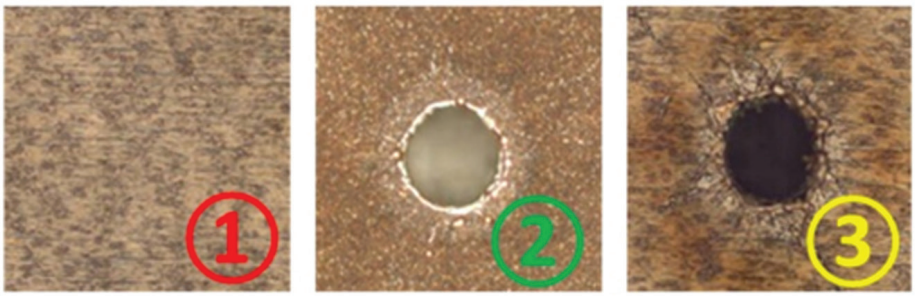


Figure 16. Performance of BondFilm® LDD MSAP.

4.5 Metallization: Desmear and Electroless Copper

Once vias have been formed it is necessary to coat the nonconductive materials on the substrate surface (i.e. dielectric and glass reinforcement) with a thin (<1µm) layer of copper that will enable the subsequent electrolytic copper plating process. Package and substrate processes typically deposit this thin layer using an electroless copper process. While "electroless copper" is often referred to as a single process, it is more realistic to consider it as consisting of three distinct stages: desmear; cleaning/activation; and electroless deposition (Figure 17).

Stage	Step	Function
Desmear	Sweller	Preparation of the resin for etch attack
	Permanganate Etch	Removal of smear and resin
	Reducer	Removal of breakdown products and surface cleaning
	Glass Filler Removal	Removal of any loose glass filler particles
Pretreatment & Activation	Cleaner	Cleaning of surface from organic residues
	Etch cleaner	Removal of copper oxides and micro roughening of the copper surfaces
	Pre dip	The pre dip protects the activator from drag in
	Activator	Adsorption of palladium ions on the conditioned surfaces
	Reducer	Reduction of palladium ions to metallic palladium
Plating	Electroless Copper	Palladium initiated auto-catalytic electroless copper deposition

Figure 17. Process sequence and functions within an electroless copper process.

4.5.1 Desmear

Desmear, as the name suggests, removes any post via drilling "smear" on the panel (Figure 18). "Smear" is unwanted resin residue that has been transferred onto inner layers and target pad copper as a result of the heat generated during mechanical or laser drilling. Desmear is a critical stage in the overall process as resin residues on the copper produce both electrical and mechanical defects that significantly impact the performance of the final packaged assembly. In the case of Advanced Package substrates, the majority of vias are laser-formed blind micro vias. The desmear target with these substrates is a clean target pad with no resin residues, minimum undercut, and no loose glass reinforcement within the BMV.

A second, equally important function of desmear is to chemically etch the resin surface to produce a moderate degree of roughness that improves the

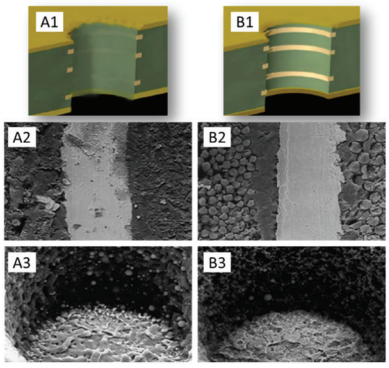


Figure 18. Schematics and images before (A) and after (B) desmear for mechanically (A2/B2) and laser (A3/B3) drilled vias.

adhesion of the subsequent electroless copper layer. Note however, that as the requirements for finer features and high frequency applications have increased, high levels of roughness have become undesirable. A significant and current challenge for desmear processes is the production of acceptable levels of adhesion while creating minimal roughness on the dielectric resin.

4.5.2 MKS Products for Desmear

$$\underset{\text{Resin}}{\text{-(CH)-}} + \underset{\text{Permanganate}}{5Mn(VII)O_4^-} + \underset{\text{Hydroxyl}}{7OH^-} \longrightarrow \underset{\text{Carbonate}}{CO_3^{2-}} + \underset{\text{Manganate}}{5Mn(VI)O_4^{2-}} + \underset{\text{Water}}{4H_2O} \qquad (1)$$

$$\underset{\text{Resin}}{\text{-2(CH)-}} + \underset{\text{Manganate}}{5Mn(VI)O_4^{2-}} + \underset{\text{Water}}{2H_2O} \longrightarrow \underset{\text{Carbonate}}{2CO_3^{2-}} + \underset{\text{Manganese Dioxide (sludge)}}{5Mn(IV)O_2} + \underset{\text{Hydroxyl}}{6OH^-} \qquad (2)$$

$$\underset{\text{Resin}}{\text{-3(CH)-}} + \underset{\text{Permanganate}}{5Mn(VII)O_4^-} + \underset{\text{Hydroxyl}}{OH^-} \longrightarrow \underset{\text{Carbonate}}{3CO_3^{2-}} + \underset{\text{Manganese Dioxide (sludge)}}{5Mn(IV)O_2} + \underset{\text{Water}}{2H_2O} \qquad (3)$$

Desmear consists of the individual steps shown above. For advanced packaging applications, MKS offers the Securiganth® MV series of products with unique agents for each step of the desmear process.

MKS' Securiganth® MV Sweller contains a high boiling organic solvent that penetrates the dielectric resin, weakening the cross-link bonds and opening the structure for chemical attack by Securiganth® MV P-Etch, a permanganate etch solution which oxidizes and removes any resin residues on the target pads and roughens the BMV side walls in a two-step chemical oxidation reaction:

Two etch reactions occur in the desmear process. The primary reaction between permanganate, $Mn(VII)O_4^-$, hydroxyl ions, and the organic resin produces a soluble carbonate, water, and soluble reduced manganate, $Mn(VI)O_4^{2-}$, as shown in reaction (1). If the $Mn(VI)O_4^{2-}$ product of Reaction (1) further reacts with the resin by reaction (2), it will produce insoluble manganese dioxide "sludge", which is detrimental to the success of the etch process. The overall reaction is shown in (3). Clearly an effective desmear process is one in which reaction (1) is much preferred over reaction (2). This can be accomplished through the continual addition of fresh permanganate and hydroxyl; however, this can be costly in terms of chemical use and process waste disposal.

MKS has developed a very efficient electrochemical alternative that avoids high chemical consumption and yields a highly stabile etch chemistry. MKS' Oxamat® Regeneration Tool (Figure 19) is a proprietary desmear etch regeneration tool which oxidizes the Mn(VI) manganate by-product back to the active Mn(VII) permanganate compound. While this does not diminish the manganese dioxide Mn(IV) sludge by-product, the use of an Oxamat® can effectively reduce the chemical consumption of fresh desmear etch chemicals by up to 95%.

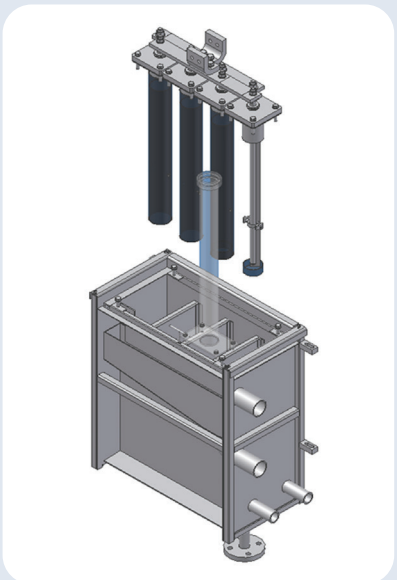


Figure 19. MKS Oxamat® Regeneration Tool for reduction in desmear etch chemical consumption.

The insoluble manganese dioxide sludge is difficult to remove, and it can build-up on the package substrate as well as within the process equipment. The desmear process therefore requires a third step to remove MnO_2. MKS' Securiganth® MV Reduction Solution converts manganese dioxide into a soluble manganese (II) compound that can be easily rinsed from the substrate.

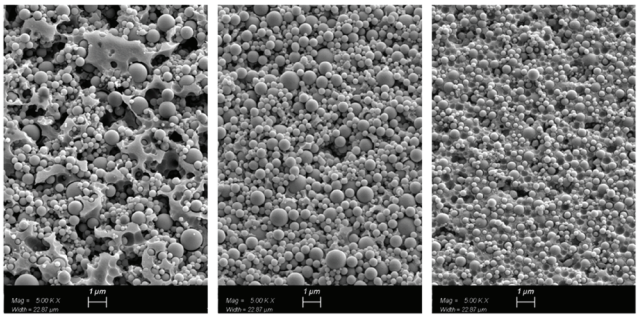


Figure 20. Residual glass reinforcement on the surface of different build up dielectrics.

After the Sweller, Permanganate Etch, and Reducer steps have removed the resin residue, and in conjunction with the rinsing steps, removed any loose materials, there may still be significant levels of reinforcement materials exposed on the surface that can also reduce the adhesion of the copper layer (Figure 20). Fluoride-based products are available that mildly etch or "frost" the surface of any exposed glass reinforcement, improving adhesion of the electroless copper. Their use, however, has not been widespread, due to the relatively high reactivity of fluoride chemistries and elevated risks for operator safety. MKS has developed Securiganth® MV Cleaner GFR, a fluoride-free solution, for the final step in a desmear process. It actively removes loose glass fillers from the surface of the dielectric system and maximizes the adhesion of the final electroless copper deposit, without any significant changes in surface roughness (Figure 21). Once the desmear process has been completed, any inner layer or microvia copper surfaces will be free of resin residues. The dielectric resin will have been mildly roughened, cleared of any loose particles, and any available glass reinforcement will have been conditioned (Figure 22).

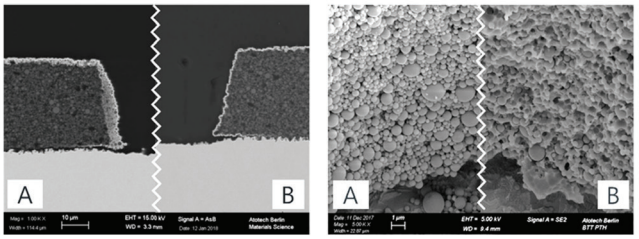


Figure 21. ABF GX-T31 dielectric after desmear without (A) and with (B) glass filler removal step.

4.5.3 Surface Activation and Patterning

Following desmear, surface residues and oxidation byproducts are removed from the dielectric and copper using chemical cleaning.

The electroless copper deposition requires the presence of a catalyst on the dielectric resin and glass reinforcement surfaces (the surface is "activated"). Traditionally, the PCB industry has employed palladium-based activation such as a Palladium-Tin (Pd/Sn) colloid or an ionic Pd solution. The ionic Pd system is considered superior to the Pd/Sn colloid as it is less prone to agglomeration, producing a more even distribution of the Pd catalyst (Figure 23) which facilitates a more uniform final electroless copper deposit. Ionic processes use a soluble Pd^{2+} salt which can be reduced to Pd^0 by reducing agents such as dimethylamine borane (DMAB) to yield the metallic Pd activation layer. Within the Advanced Packaging and IC substrate sector, the use of the ionic based systems is dominant.

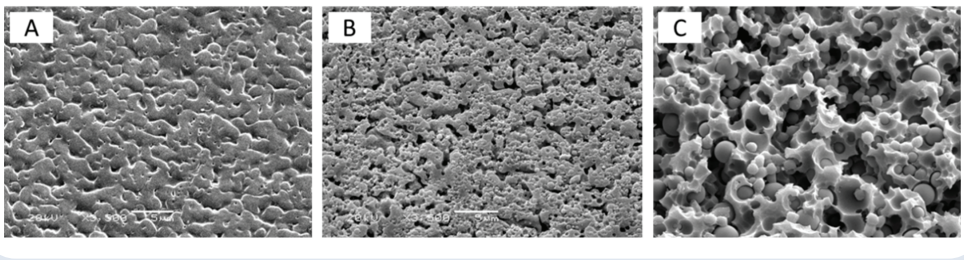


Figure 22. Build up films typical of advanced package production before (A) and after (B/C) desmear.

The final step in creating the patterned circuits (Chapter 4.8.5) is the etching of the electroless copper layer between the plated tracks. However, during such etching, the underlying Pd layer is not guaranteed to be removed and the potential of leaving residues is unacceptable. To mitigate this risk, an additional Pd etch is typically employed to remove any residues (Chapter 4.8.6). While this has been shown to be effective, there is also a corresponding reduction in the final track dimensions, which is undesirable. This, along with other factors, has led to the development of non-Pd based activation systems.

Historically, the use of copper-based activation has been attractive, however several technical issues have limited its market acceptance. Specifically, low stability of the metal in the working solution or a Cu colloid with low adhesion to the dielectric system have proven problematic. MKS has developed the first viable Cu based activation process that successfully solves these issues (Chapter 4.5.4).

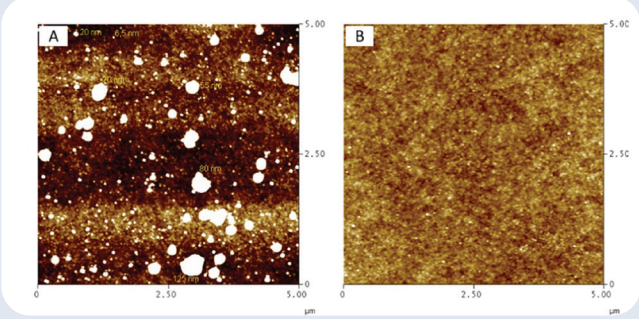
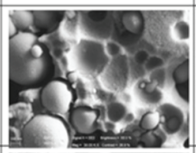
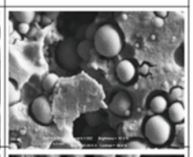
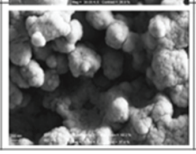
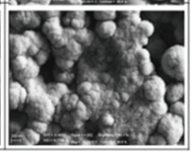


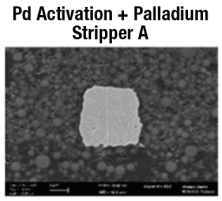
Figure 23. Activation layers produced from (A) Pd/Sn colloid and (B) ionic Pd based processes.

4.5.4 MKS Products for Surface Activation

MKS offers Neoganth® MV Activator, the leading ionic based Pd activation system used in IC substrate production.

MKS also offers Cupraganth® MV Activator, the first commercially available Cu based activation process for electroless copper deposition. Based on a nanoscale Cu colloid, in combination with a unique additive package, this Pd-free activation step overcomes the reported issues of low bath life and poor adhesion of the final electroless copper deposit. Furthermore, an additional Pd etch is no longer required with this Cu-based activation system, allowing all etching to be achieved in a single step and avoiding any final track dimension reduction associated with the Pd etch (Figure 24).

Dielectric		GX92	GXT31
Roughness Before Deposition (Sa)	um	0.262	0.164
Eless Cu Thickness (by weight gain)	um	0.273	0.294
Appearance SEM (30kx)	Before plating		
	After plating		



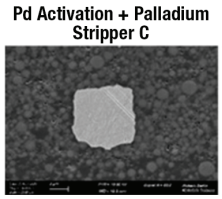


Figure 24. Typical deposits and improved line width control with Cupraganth® MV Activator.

4.5.5 Electroless Copper Deposition

Once the dielectric has been suitably prepared (desmear) and activated (Pd or Cu) the next stage is the deposition of the electroless copper layer itself. As the name implies, electroless copper deposition does not rely on the use of external electrical current to drive deposition with the metal produced using reductive chemical reactions. Electroless copper solutions are a complex mix of chemistries and typically contain the following constituents:

- Copper salt – Source of the copper to be deposited
- Complexing agents – Stabilizes the Cu in solution
- Reducing agent – Drives Cu deposition
- Additives – Stabilizes Cu, impacts deposition, coverage, and physical characteristics of the deposited Cu

From a chemical standpoint, there are two desirable reactions in operation where the solute Cu is reduced, typically by formaldehyde and hydroxides, which then drives Cu metal deposition onto

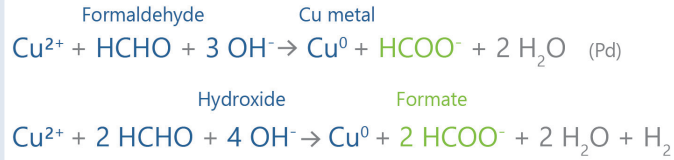


Figure 25. Desirable reactions — reduction of Cu by formaldehyde drives Cu deposition.

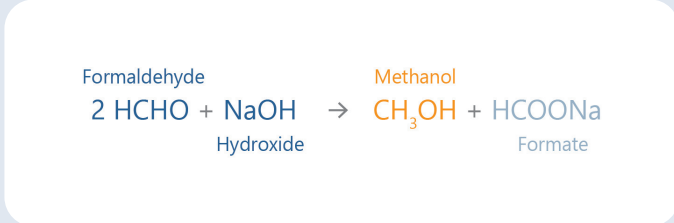


Figure 26. Cannizzaro reaction consumes formaldehyde and sodium hydroxide.

the active surface (Figure 25). However, these reactions do create by-products such as formate which, if left uncontrolled, will build up in the process solution.

The Cannizzaro reaction (a reaction between formaldehyde and hydroxide, Figure 26) is an undesirable side reaction that consumes the chemical components that drive the deposition. If left unchecked, this reaction increases the concentration of by-products and, more importantly, reduces the efficiency of both primary reduction reactions, inhibiting the deposition.

In addition to the Cannizzaro reaction, any formate produced will further react with the available hydroxide to form carbonates, which leads to the precipitation of $CuCO_3$ from solution, reducing the availability of dissolved Cu^{2+}-Ions for deposition (Figure 27).

$$CO_2 + 2\ NaOH \rightarrow Na_2CO_3 + H_2O$$

$$HCOONa + NaOH \rightarrow Na_2CO_3 + H_2$$

Formate Hydroxide Carbonate

Figure 27. Side reactions that consume chemical components, create by-products and lead to loss of Cu from solution.

Currently, advanced packaging technologies are moving to electroless copper deposition processes that produce very thin copper layers (typically less than 200 nm). This enables finer features to be formed and allows high throwing power into the laser formed microvias that ensures uniform and complete coverage.

4.5.6 MKS Products for Electroless Copper Deposition

MKS' Printoganth MV series of electroless copper baths have been specifically developed for such advanced packaging applications. MKS has conducted extensive research on the reliability of the Cu/Cu interfaces between electroless copper deposits and electrolytic copper in advanced packaging substrates (see below). The results of these studies have been used to create chemical formulations for the Printogranth MV series baths that produce industry-leading reliability and quality in these interfaces. Printoganth MV TP3 baths, for example, exhibit excellent throwing power in BMVs along with self-limiting deposition thickness, ensuring excellent product reliability at <5 µm line and space requirements (Figure 28).

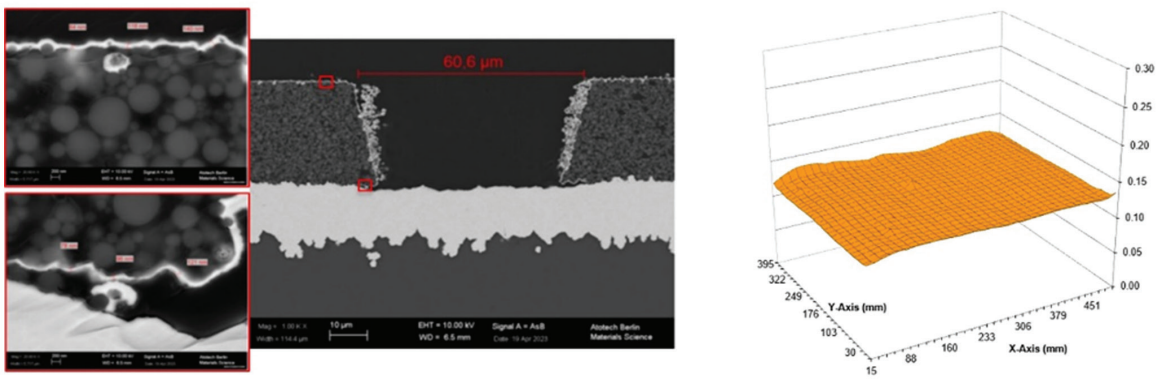


Figure 28. ABF GX-T31 processed with Printoganth MV TP3.

4.5.7 Electroless Copper and Joint Reliability

Advanced packages make significant use of laser formed blind micro-vias (BMV) to create layer-to-layer interconnects, and as these vias continue to decrease in size, their mechanical integrity and reliability become critical factors.

At the base of each BMV is a layered connection consisting of two primary interfaces (Figure 29), the interface between the underlying target pad and the electroless Cu; and the one between the electroless Cu and the overlying electroplated Cu. Each of these interfaces is a potential failure point during service.

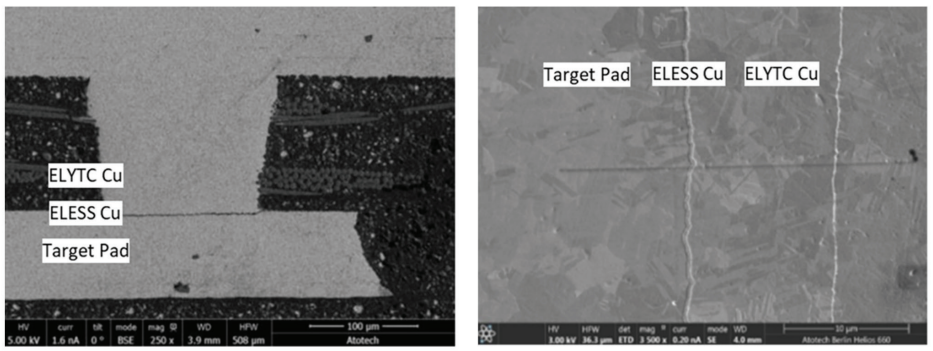


Figure 29. SEM images of BMV (left) and plated structure at the base of the BMV (right).

From a metallurgical point of view, any breaks or disruptions in the overall crystal structure across these two interfaces is a mechanical weakness, and such crystallographic disruptions are typically sites for preferential joint failure during thermomechanical testing [13] [14]. BMVs can form with a visible interface within the plated layers (Figure 30a) or without any interface evident at all (Figure 30b). The latter is clearly the more desirable. To control or even "engineer out" the visible interface, understanding how each of the two structures can be formed is necessary.

Immediately after deposition, both electroless and electroplated Cu are amorphous, i.e., they have no fixed, well-defined crystal structure. However, over time, typically less than two hours for an electroless layer and less than 36 hours for an electroplated layer, the plated Cu will recrystallize and develop its final structure. Preferably, this recrystallization occurs because of grain boundary diffusion and grain growth, and if these proceed unhindered, a structure such as that shown in Figure 30b will result. However, the presence of oxides or other contaminants on surfaces prior to plating, or a significant build-up of the additives found in all commercial plating baths, inhibits the diffusion mechanism. When this is the case, the plated layers will crystallize independently [15] [16]. In such cases, there is usually little or no alignment across the plating interfaces, and a final structure more like that in Figure 30a will occur. Hence, cleaning and preparing all surfaces prior to fresh copper deposition and optimizing and controlling all plating processes is of paramount importance to ensuring minimum additive co-deposition.

Modern plating baths are complex, multi-component solutions optimized to achieve the properties required in the final plated layer. Bath additives can significantly impact the crystallographic nature of plated deposits and contribute to achieving the preferred interface-free structure [17]. Figure 31 shows the impact of an additive applied to an electroless Cu bath and the crystal structure that subsequently developed.

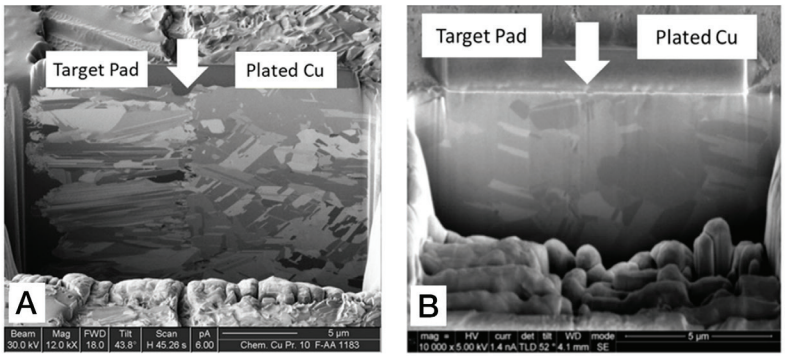


Figure 30. Plated micro via (A) with and (B) without visible interfaces.

Figure 31A shows the plated structure where the additive is not applied; there is a clearly visible interface at the electroless copper deposit. Conversely, when the additive is utilized in the electroless copper solution, (Figure 31B), there is clearly a significant level of grain diffusion and growth, as can be seen by the extension of red grains into the plated layers. Thus, a thorough understanding of the additives used in both electroless, and electrolytic plating baths is required to decrease the occurrence of weakened BMVs and increase plated joint reliability overall.

Extensive thermomechanical testing is the industry standard for evaluating final product performance. It can be a repetitive, time-consuming, and expensive procedure. To reduce the cycle time and costs associated with such testing, MKS has developed a technique that analyzes the plated microstructure and indicates the potential joint reliability. Known as "Normalized Tentative Crack Length" or "NCL" analysis, the method assesses the plated interface quality with respect to the degree of grain growth across an interface. Then, it calculates and assigns a numerical value to that interface. Testing has shown that NCL has a good correlation to plated interface reliability, and the higher the NCL value, the more reliable the overall plated joint characteristics [18], (Figure 32). Upon successful completion of the electroless copper process, the BMVs are coated with a firmly adhered, uniform, thin copper layer that, ideally, has a crystal structure indistinguishable from that of the underlying target pad. This freshly deposited copper is then cleaned and prepared for subsequent electroplating operations.

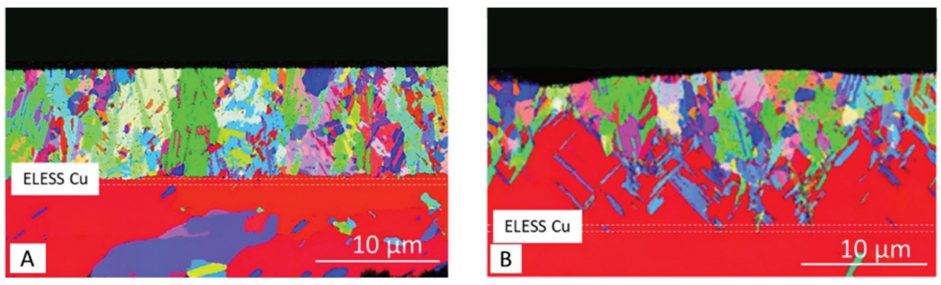


Figure 31. Electroless copper bath without plating additive (A), and with plating additive showing the resultant recrystallization (B).

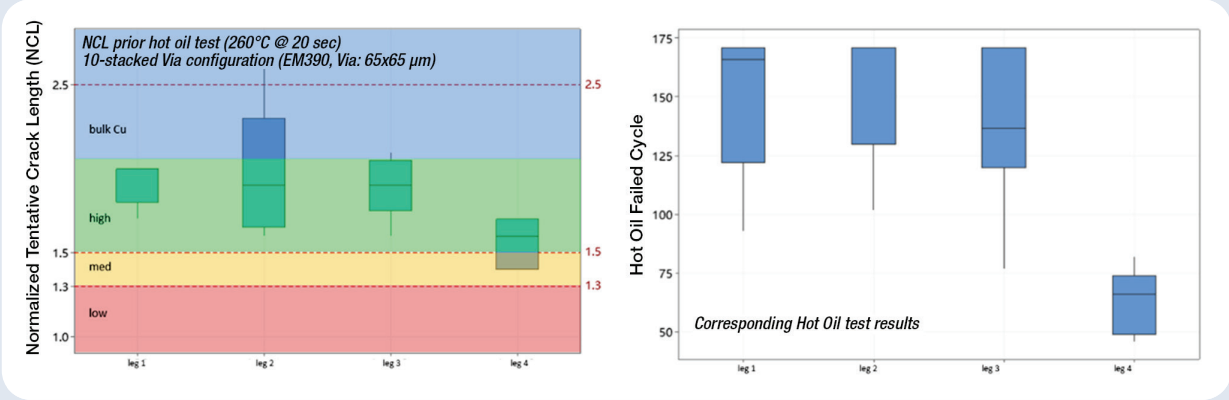


Figure 32. Correlation of "Normalized Tentative Crack Length" (left) to "Hot Oil Failed Cycle" (right).

4.5.8 MKS Production Equipment

MKS offers a suite of equipment and wet chemical process technology for surface treatment, metallization, electrolytic plating, final finishes, as well as for pad metallization, copper pillar, RDL and TSV. The equipment portfolio (Figure 33), consisting of horizontal and vertical processes, is designed for applications in growth areas, such as next-generation smartphones, electrical and autonomous vehicles, Internet of Things, 5G, virtual reality, and artificial intelligence.

Horizontal Equipment for Desmear and PTH

Horizontal equipment is primarily used in high volume manufacturing where the circuit board is automatically loaded and moved horizontally through the entire system using a rotating roller system. Horizontal operation facilitates continuous processing of the PCB through multiple post-laser-drilling process modules as shown for MKS' Uniplate® PLBCu system in Figure 34.

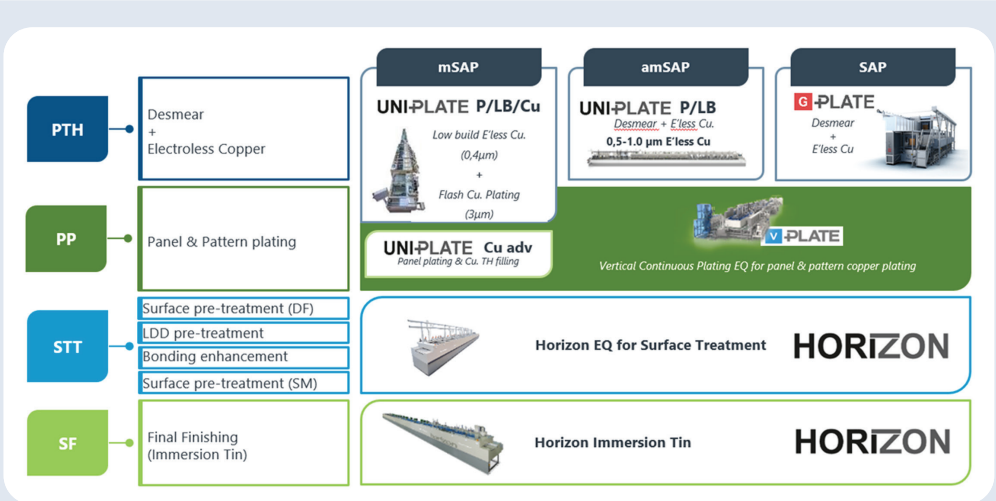


Figure 33. MKS equipment portfolio by production technology.

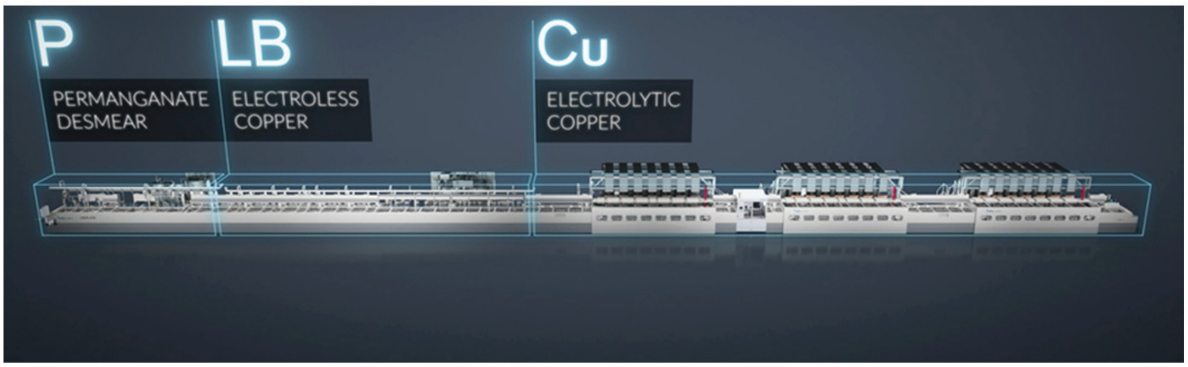


Figure 34. MKS' Uniplate® PLBCu, a Permanganate Desmear-Electroless Copper and Electrolytic Copper line.

Each process module has its own fluid delivery system which is tailored to the process chemistry and its behavior. Within each module, the liquid is filtered via a special flood-bar type and delivered onto both sides of the PCB surface. MKS has developed many different immersed flood-bar types (Figure 35) for individual process steps.

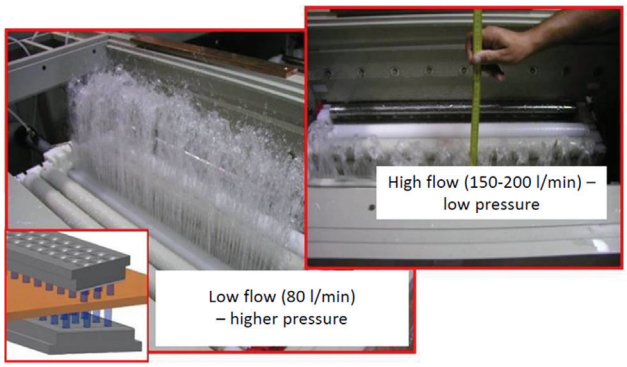


Figure 35. Demonstration of open flood bar water flow.

Vertical Equipment for Desmear and PTH

In vertical equipment the panels are transported and processed in a vertical orientation. This offers the advantage of avoiding contact with the product area of the panels. A robot system is usually used to load the panels with contact occurring only at the outer edges of the panel, the so called Keep Out Zone (KOZ). The panel transportation system can be either a basket line or a rack or gantry type.

In a basket line, the panels are placed in a basket by a robot or by hand. The baskets are designed so that the panels stacked vertically in the basket supported by a V- or U-shaped supporting structure on at least two sides (Figure 36). The baskets are designed with an open structure that allows solution flow to all surfaces on the panels. Up to 24 panels per basket can be transported simultaneously. Baskets are transported along the line by a gantry or hoist type of transporter, which lifts them from one tank to the next.

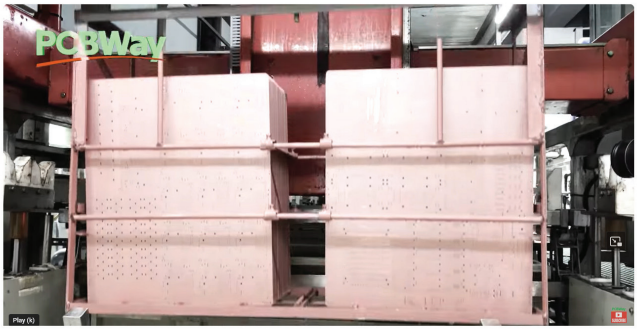


Figure 36. Baskets with panels arranged one behind each other [37].

MKS offers G-Plate® vertical equipment designed for processing high-end products such as fine line width/space design with high yield. For these products, the required etch back of the electroless Cu layer must be reduced to a minimum. This is achieved through the use of ultra-thin Cu seed layers with very even thickness uniformity and a homogeneous pre-treatment in Desmear. G-Plate (Figure 37, left) is designed for ultra-low particulate operation in every stage of processing. The loading and unloading areas of the tool are located in the user's cleanroom. Under clean, HEPA filtered air panels are transported along the line and, while docked in the module, HEPA filtered air continuously flows over the panel, eliminating particles during transfer to a module.

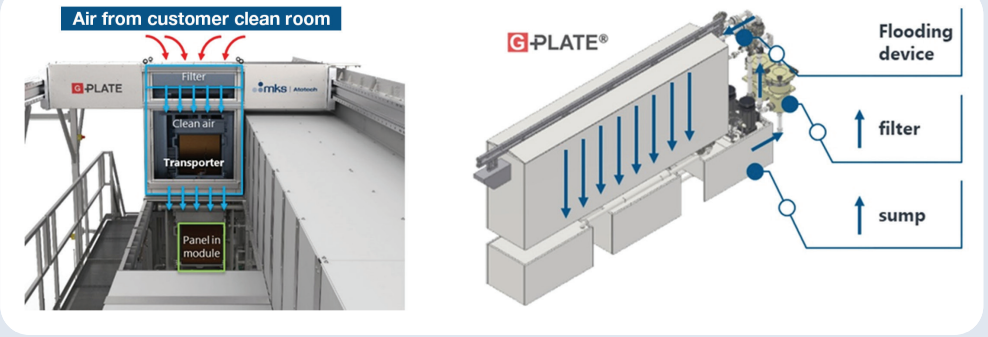


Figure 37. Mobile clean room transportation in G-Plate® (left); Solution flow and filtration in G-Plate® (right).

G-Plate® treats each panel separately to ensure optimal solution exchange and minimizes differences from panel to panel. The panels are located behind each other in the basket tools. For equal solution supply in G-Plate®, the panel is fixed in the middle of the empty tank. A flooding device on each side of the panel creates an equal flow to each panel surface. This system, called ECF, Equalized Curtain Flow, is shown on the right in Figure 37.

The combination of single panel approach with the very uniform ECF treatment enables the formation of very thin electroless Cu layers (as low as 150nm) with outstanding thickness uniformity.

4.6 Patterning

4.6.1 Overview

Different patterning technologies are available for IC substrate fabrication. By far, the most commonly used techniques employ dry film photoresists used as either an etch or plating resist in a patterning process. Plasma techniques such as RIE (Reactive Ion Etching) have been evaluated for desmear and for deep-etch patterning of lines and spaces. Sputter deposition has also been tested as a replacement for the more common electroless-Cu plating process. While plasma-based processes may offer advantages in certain applications, their limitations with respect to productivity/cost of ownership and material-compatibility make them generally unsuitable as a replacement for dry film patterning technologies in IC substrate fabrication. Our discussion of substrate patterning will therefore focus exclusively on patterning technologies that use dry film photoresist. Packaging applications typically use high-resolution dry film with thicknesses of 5 to 15 µm in patterning processes.

4.6.2 Dry Film Photoresist and Projection Photolithography

Dry film is a polymeric emulsion containing binders, monomers, plasticizers, adhesion promotors, dyes, and photoinitiators. The monomers and binders are normally acrylates with the binders chosen so that they can be washed away with mild alkaline solution; some special applications require solvent-developable binders. Dry films also contain a variety of adhesion promotors to enhance adhesion between the dry film and a clean copper surface. As with build-up films, dry films are produced by spreading the precursor emulsion onto a carrier PET foil and, after drying the emulsion, adding a cover foil (see Section 3.2). Dry films are normally laminated onto both sides of the PCB using a hot roll, with vacuum laminators also used for some special applications. Dry films are photosensitive and must be processed and stored in clean rooms under safe (usually yellow) light conditions. New dry films that provide higher resolution, better adhesion, and overall higher productivity are regularly introduced, especially for the packaging market.

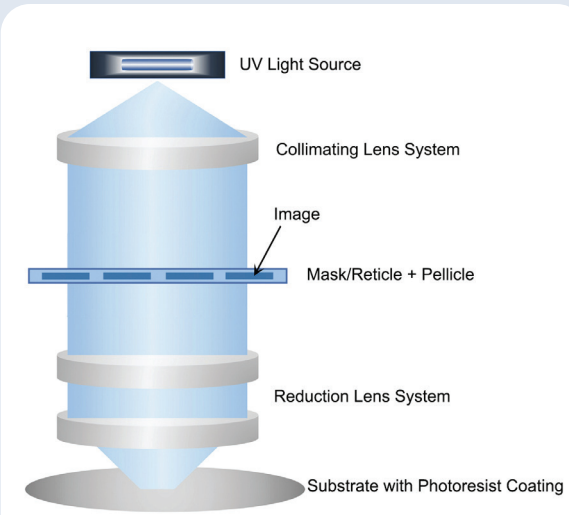


Figure 38. Projection photolithography. (Source: MKS Handbook: Semiconductor Devices and Process Technology)

Following lamination, the dry film is imaged using projection lithography with exposure to UV light (Figure 38). The principles of projection photolithography are covered in detail in MKS' Semiconductor Handbook [19]. Dry film imaging uses Laser Direct Imaging (LDI), contact exposure, or, for finest circuitry, steppers. Photoinitiators inside the dry film react with UV light, producing free radicals that cause cross-linking and consequent hardening in the exposed areas of the polymer.

Dry film structures such as that shown in Figure 39 are used as SAP plating resists in packaging substrate manufacturing. Between these fine dry film structures, electrolytically plated ultra-fine line copper-circuitry can be built up. Following the formation of copper circuitry, the patterned dry film is removed using stripping agents such as ResistStrip® IC2 by MKS.

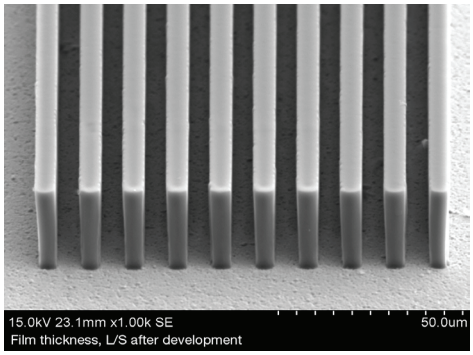


Figure 39. Ultra-fine dry film lines after developing. (Source: RY Series for PKG Board, Resonac Europe)

4.6.3 Mask/Stepper Based Patterning

Advanced Packaging uses I-line steppers with 1:1 or 1:2 projections to achieve resolution down to 1.5 µm L/S. Higher throughput may be achieved through use of more light with a broader spectrum (e.g., G+H+I line) at the expense of lower resolution. Unlike a mask aligner, which globally aligns to a substrate, a stepper can compensate for a larger set for distortions, as the field for each reticle can be aligned in up to six degrees of freedom (x, y, z, theta, tip/tilt) through the stage to generate a best fit. Further, the image size may be scaled through z-stepping the lithography optics. So, the substrate is typically first inspected, either in a separate tool or as part of a more complex stepper system, and the exposures accordingly adjusted. However, the reticle-by-reticle compensation does come at the expense of throughput. Another challenge for stepper systems is increased substrate sizes (up to 100 mm x 100 mm) that are larger than any commercially available reticle system (recent systems offer up to 60 mm x 60 mm exposure area). The exposure area then has to be stitched over the substrate. This is undesirable since even small overlay and stitching errors in the RDL lines can cause problems.

4.6.4 Maskless Patterning

Maskless patterning approaches generally cannot compete with mask-based patterning processes in terms of raw throughput at high resolution. However, maskless technologies excel in the low volume/high mix segment since they avoid the cost and complexity of mask production, storage, inspection, and maintenance. Within the context of Advanced Packaging, there are benefits for package types such as FOWLP/FOPLP. For these applications, mask aligners can only align to the substrate globally, and steppers locally, however, maskless systems can change the pattern itself to accommodate nonlinear distortions across the substrate. This ensures that fine wiring patterns connect properly to their endpoints, independent of e.g., any relative die shifts and rotations. This may require a separate tool to map out the reconstituted wafer or panel, or it can be part of a single, more complex tool that both maps and patterns the substrates.

The main maskless exposure or maskless aligner approach is based on projecting an image created using a high-power UV LED or diode laser illuminated digital light processing (DLP) micromirror array MEMS device onto the substrate. Modern micromirror arrays provide millions of micromirrors in a single package which can be updated in the ~10 kHz range, yielding data rates that can exceed >60 gigapixel per second. Multiple heads may run in parallel to further increase throughput. Another MEMS-based approach uses a Grating Light Valve (GLV), a 1D array of silicon nitride micro-ribbons as a programmable diffraction grating. This method has an actuator speed that is more than an order of magnitude higher

(~100's of kHz) and its inherently analog pure piston phase control avoids some of the aliasing effects of the DLP method. The total number of actuators (8192) is considerably lower and the system performance is far more sensitive to individual micro-ribbon failures than the micromirror array to individual mirror failure.

Another maskless approach is Laser Direct Imaging (LDI). Here a frequency tripled solid state UV laser, typically at 355 nm, is split into dozens of beamlets which are routed into an acousto-optic deflector array where each beamlet is individually modulated. The beamlet array is then routed through a rotating Polygon scanner and scanned across the full width of the substrate at high speeds. The substrate is indexed after each scan and the process is repeated. Unlike the other optical imaging systems, here the individual pixels are generated through the focus of a Gaussian beam, yielding a larger depth of focus. However, with typical acousto-optic deflector speeds of ~100 MHz, it is readily apparent that, even with dozens of beamlets, this approach struggles to achieve the same data rates as the micromirror array approach. Hence, it is typically used in lower resolution applications.

4.7 Electrochemical Deposition of Metals

The electrochemical deposition of metals, also known as electroplating, is defined as the deposition of a metallic layer onto a substrate through an electrochemical reaction. During electroplating, an electric current flows through an electrolyte solution containing metal ions. These ions are chemically reduced to the metal at the cathode (substrate) surface, forming a uniform and adherent metal layer. Factors such as current density, inorganic and organic bath components, temperature, and deposition time play crucial roles in determining the quality and properties of the plated metal. Electrochemical deposition permits precise control of plated thickness and composition, and defines properties of the plated metal such as ductility, tensile strength, and crystal structure, all of which impact the reliability of the manufactured products.

Electroplating is a critical process in the electronics industry, where its use enhances the functionality and performance of electronic components and improves their reliability. Key fields of application of electroplating in the electronics industry include:

1. **Printed Circuit Boards (PCBs):** Electroplating is extensively used in the manufacturing of PCBs. Typical metals that are electrolytically deposited on PCBs are copper and tin, with smaller amounts of electroplated nickel and gold employed for surface finishes.

2. **IC Substrates (ICS):** Electroplating is used to produce Ball-Grid Arrays (BGA), Chip Scale Packages (CSP) and Flip Chips (FC). It is used to deposit metal layers, mainly copper, that create circuit traces and filled vias within these devices, enabling the integration of multiple components on an ICS.

3. **Interposers:** Plated-through, copper-filled organic or glass substrates for establishing an electrical connection between the chips on the top of the interposer and the ICS, e.g., via microbumps:

    a. As a mounting surface for semiconductor dies in heterogeneously integrated components

    b. As a connection between semiconductor chips

    c. To connect the entire stack to a package substrate

    d. As ICS cores for thermal management and the reliable build-up of ICS core layers.

4. **Connectors and Contacts:** Electroplating is used to enhance the conductivity, durability, and corrosion resistance of connectors and contacts used in electronic devices. Thin layers of metals such as copper, gold, silver, or nickel are often electroplated onto the surfaces of these components to ensure reliable electrical connections and prevent oxidation or wear.

Within the context of PCBs and ICS', several features are commonly electroplated to enhance their functionality and performance. Some typical features that require electroplating processes are:

1. **Filled Through-Holes and Vias:** Through Vias (TV) and Blind Micro Vias (BMV) are mechanical, or laser drilled openings in a PCB or ICS that allow for the electrical connection between different layers. Filling of TVs and BMVs deposits copper within these openings to establish reliable electrical pathways. The copper also provides a pathway for heat dissipation owing to the excellent thermal conductivity of copper.

2. **Plated Through-Hole (PTH) Barrels:** PTH barrels are the copper-plated walls of through-holes or vias. During electroplating, copper is deposited on the inner surfaces of these holes, ensuring a continuous conductive pathway from one layer to another. PTH barrels contribute to the electrical integrity and stability of the PCB or ICS.

3. **Copper Traces and Conductive Paths:** Electroplating is used to create conductive copper traces on the surface of the PCB or ICS. These traces provide electrical connections between different components, pads, and vias. Copper electroplating offers good conductivity at reasonable costs, making it a common choice for these features. Future superstructures will also be realized as embedded designs in the form of ETS and LECS.

4. **Bumps and Pillars:** In advanced packaging technologies such as Flip Chip (FC) and Ball Grid Array (BGA), electroplating is used to create bumps or pillars on the substrate. These pillars provide the electrical and mechanical connections between the ICS and the chip. Common materials used for pillar plating include tin and copper.

The overview in Figure 40 reflects the wide variety of ECD Cu products, depending on the field of application.

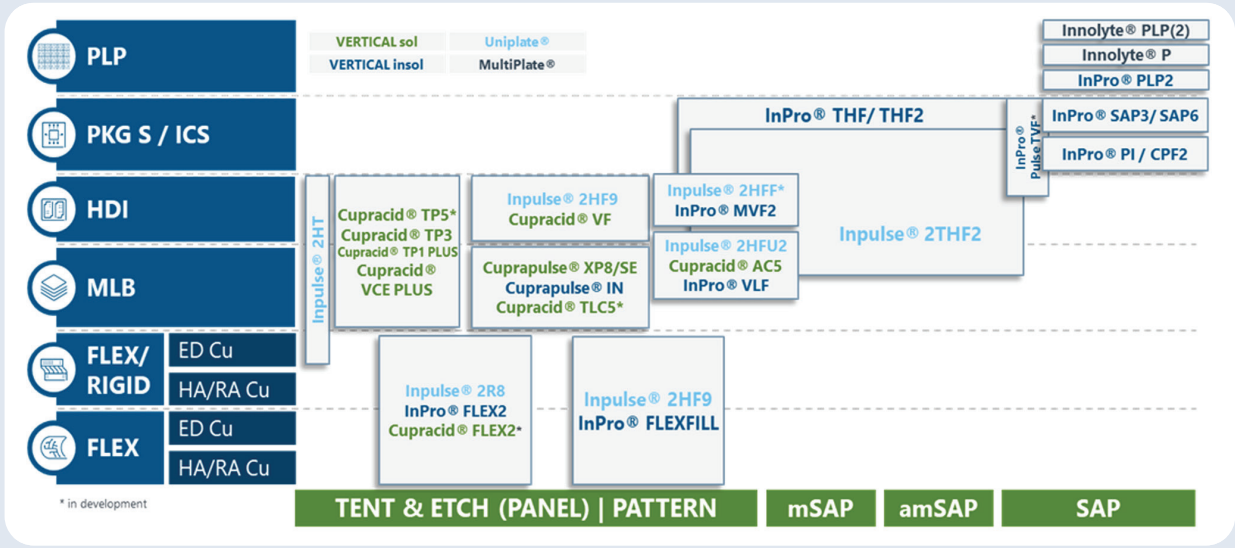


Figure 40. MKS ECD Cu products for advanced HDI and ICS manufacturing.

The process requirements of different applications vary with device parameters such as line and space requirements, plated uniformity, conformal plating or via filling, physical properties of the deposited metal, etc. Also, the type of plating equipment determines the suitability of the plating process; different solutions are necessary for plating with soluble or insoluble anodes, with air agitation or eductor agitation, and with DC or reverse pulse plating. All these factors need to be considered to find the optimal plating process for a given application.

This chapter explores the fundamental principles, processes, and applications of electrochemical deposition, highlighting its role in various sectors and reviews some recent advances in the field.

4.7.1 Electroplating Pre-treatment

Pre-treatments are used to ensure a controlled and uniform nucleation, coalescence, and crystal growth of the metal on the conductive layer (usually electroless copper). Pre-treatment processes must meet the following criteria:

1. Removal of impurities like particles, dust, and fingerprints by solubilization
2. Creation of an oxide-free surface on the conductive layer that provides the best adhesion with ECD metal deposition
3. Removal of any foreign process chemical residues from electroless copper or dry film processing
4. Wetting of surfaces and vias for void- and inclusion-free plating

Any pre-treatment methodology must consider the constant reduction in copper traces and the associated adhesion problems of the ever-narrower dry film pattern.

Water-based acid cleaners contain one or more inorganic or organic acids that will dissolve the copper oxide on electroless copper surfaces to produce the Cu^{2+} salts that can be rinsed away. As well, alkaline residues from pre-processes (electroless Cu, dry film development) are neutralized in an acid cleaner. Solvents, organic acids, and surfactants are all used to remove foreign impurities from the substrate surface. Surfactants encapsulate impurities in micelles, removing them from the substrate and then retaining them in solution. The strength of adsorption of the surfactant on the conductive layer of the substrate (usually electroless Cu) is an important consideration when choosing a surfactant. While the adsorption must be strong enough to produce efficient encapsulation of impurities, it must be weak enough to allow easy removal with water, especially from vias, to avoid cleaner residues on the metallic interfaces. The best rinsing result of cleaned substrates is achieved using mineralized rather than fully demineralized water.

4.7.2 MKS Products for Electroplating Pre-treatment

The cleaners from the CupraPro® series are particularly suitable for optimum conditioning and wetting of the smallest vias and the removal of foreign contamination from the substrate. Special products are available depending on the application conditions, e.g., high flow or short treatment times.

4.7.3 Direct Current vs. Reverse Pulse Plating

The differences between the mechanisms of reverse pulse plating (RP) and direct current (DC) plating primarily revolve around how the current flows and its effects on the electroplating process. The detailed mechanisms of these two electroplating techniques are:

DC Plating Mechanism

1. **Constant Current Flow:** In DC plating, there is a constant and unidirectional current flow from the anode (positively charged electrode) to the cathode (negatively charged electrode).
2. **Ion Migration:** Metal ions are dissolved in the electrolyte bath and are attracted to the cathode. The continuous flow of current ensures a steady supply of metal ions to the cathode surface.
3. **Metal Deposition:** At the cathode, metal ions gain electrons and are reduced, forming a solid metal layer that adheres to the substrate's surface. The thickness and quality of the deposit depend on factors like current density, plating time, bath chemistry, plating parameters such as convection, temperature and plating equipment used.

Reverse Pulse Plating Mechanism

1. **Reversal of Current:** In reverse pulse plating, the direction of the current periodically reverses. It alternates between flowing from the anode to the cathode and then from the cathode to the anode in a controlled manner.
2. **Ion Redistribution:** When the current direction is reversed, metal ions in the electrolyte migrate back toward the anode. This redistribution helps prevent over plating in certain areas and ensures a more even distribution of ions across the substrate.
3. **Metal Deposition Control:** The intermittent reversal of current provides precise control over the plating process. It allows for further fine adjustments to the plating parameters, leading to plating performance improvements where DC plating is showing limitations.

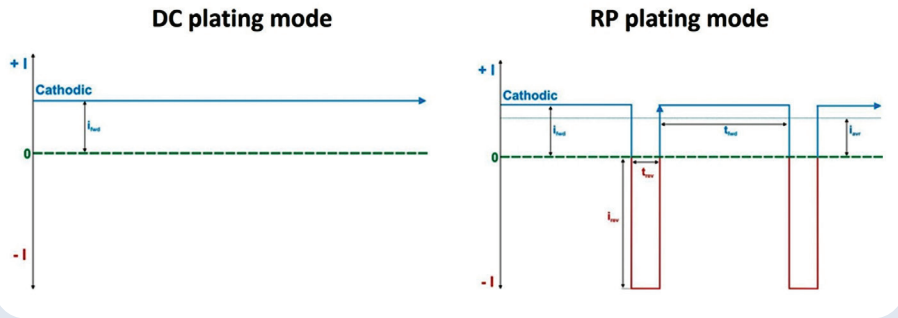


Figure 41. Current diagrams of Direct Current (DC) versus Reverse Pulse (RP) plating concept.

In summary, the main difference in the mechanism between DC plating and reverse pulse plating is the direction of current flow and its control (Figure 41). DC plating relies on a continuous, unidirectional current. In contrast, reverse pulse plating alternates the current direction, allowing for better control over the plating process.

Historically, PCB manufacturers have used direct current for electrolytic copper plating of through holes, copper tracks and blind micro vias. Electroplated copper deposits, depending on the additive formulation used, have a shiny surface appearance combined with a good levelling performance in through holes and BMVs.

With increasing PCB complexity such as higher layer count, smaller hole diameter and smaller line and space structures, DC plating suffers with regards to throwing power (minimum thickness in high aspect ratio holes), surface distribution and too high surface thickness of plated deposits. Most of the issues experienced with use of direct current are solved when reverse pulse current is applied (Figure 42). Furthermore, due to the market introduction of more advanced pulse rectifiers combined with adapted electrolyte formulations, reverse pulse plating has become even more popular in recent years. These new,

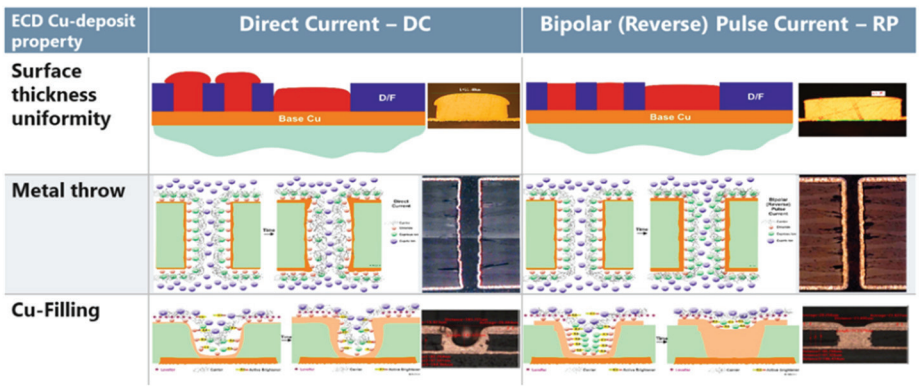


Figure 42. ECD Cu process performance comparison DC vs. RP.

programmable rectifiers allow the use of more complex pulse wave forms which are necessary to meet the requirements of advanced technologies like trough hole filling, copper pillar plating and blind micro via filling with best surface thickness uniformity.

Reverse pulse electroplating offers several advantages and drawbacks, depending on the specific application and requirements. Key advantages and drawbacks of reverse pulse plating include:

Advantages:

1. **Improved Plating Quality:** Reverse pulse plating provides better control over the metal deposition process, resulting in a higher-quality plated surface. This technique reduces defects such as uneven thickness, void occurrences, low throwing power, and poor copper purity.
2. **Uniform Deposition:** The periodic reversal of current helps to distribute metal ions evenly across the substrate, leading to more uniform plating thickness and a consistent finish.
3. **Improved Cost of Ownership:** By rule of thumb, the plating time can be reduced by almost 60% while retaining the same or better overall plating performance. This is in direct comparison to standard DC plating.

Drawbacks:

1. **Complexity:** Reverse pulse plating requires more sophisticated equipment and control systems compared to standard DC plating. This can increase the initial setup and operational costs.
2. **Operator Skill:** Skilled operators are needed to set up and maintain the reverse pulse plating process effectively, as well as to troubleshoot any issues that may arise during operation.
3. **Initial Investment:** Implementing reverse pulse plating may require an initial investment in specialized equipment and training, which may not be justified for smaller-scale or cost-sensitive projects.

In summary, reverse pulse plating offers advantages such as improved plating quality, uniform deposition, and improved cost of ownership. However, it comes with the drawbacks of increased complexity, the need for skilled operators, and higher initial costs. The decision to use reverse pulse plating is based on the specific requirements and quality standards of the application in question.

4.7.4 Copper Filling of Blind Micro Vias

Electrolytic copper deposition processes for the filling of BMVs must successfully treat several different aspect ratios and volumes. These processes fall into three main categories: (a) normal deposition, (b) conformal deposition and (c) bottom-up filling (Figure 43) [20]. Categories (a) and (b) are non-optimal processes that leave voids/inclusions or seams that represent a failure risk to the whole device (low reliability). Processes in category (c) are optimal, producing complete, void/inclusion-free copper filled vias.

The electrolyte used in electrolytic copper depositions for printed circuit board (PCB) and semiconductor fabrication are primarily aqueous sulfuric acid copper salt solutions with high solution conductivity. The typical composition of a copper electrolyte used in BMV filling contains Cu ions in a comparably high concentration (45-60 g/L). Sulfuric acid concentrations can also be an adjustable parameter that can be varied to optimize the homogeneous Cu thickness distribution over different structures and geometries on the substrate. As well, the presence of suitable organic additives helps to optimize the copper deposition in difficult features such as BMVs while simultaneously producing a reliable metal layer with excellent physical properties. Common compositions for copper electrolyte solutions for BMV filling contain three organic additives: Suppressor, Accelerator, and Inhibitor (Levellers).

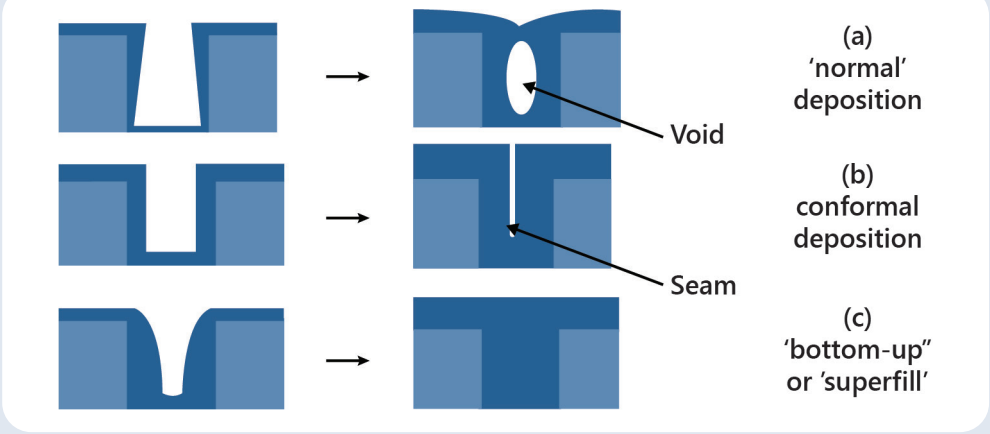


Figure 43. Growth types of BMVs by electrolytic metal deposition.

Figure 44A provides a schematic overview of the additives within a BMV. Figure 44B shows a cross-section of a filled BMV. In Figure 44A, the whole surface is covered with suppressor molecules, chloride, and copper ions. Due to differences in the local conditions between substrate surface and the bottom of the BMV, the electroless Cu surface inside the hole is covered with accelerator ("active" brightener) molecules. The copper deposition rate is therefore relatively high at the bottom. As plating proceeds, the depth of the BMV recess decreases, reducing this effect. Since the edges at the hole opening have very high current densities (Figure 45), inhibitor molecules are concentrated in these areas, reducing deposition rates and avoiding overgrowth (formation of inclusions, Category (a) in Figure 43). As the result, a perfectly filled BMV forms as illustrated in Figure 44B.

Suppressors are water-soluble polymeric compounds such as high molecular weight polyglycols. They reduce the surface tension of the electrolyte solution and form a stable diffusion layer at the copper/electrolyte interface that can act as a diffusion barrier to Cu ions that can inhibit or suppress the copper reduction and deposition [21] [22] [23] [24].

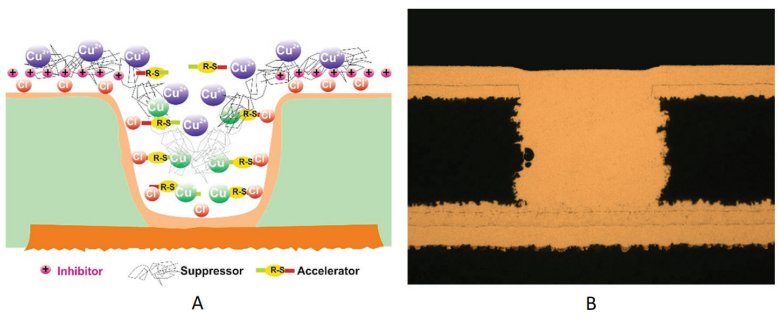


Figure 44. (A) Simplified overview of the arrangement of all additives inside a BMV during electrolytic plating. (B) Cross-section picture of a well filled BMV.

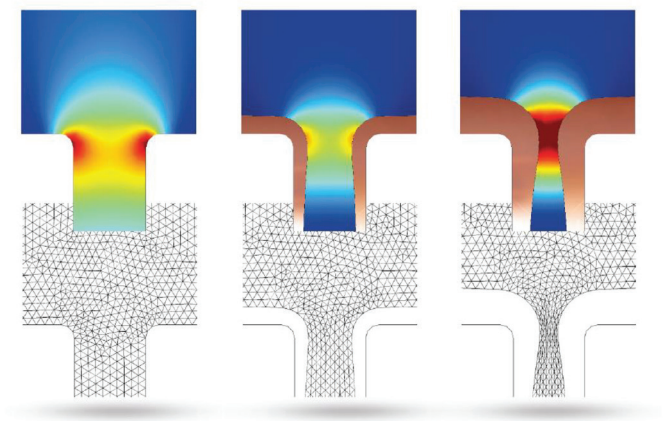


Figure 45. Current density profile for copper electroplating at a through hole shown for visual reference [41].

Accelerators, also known as brighteners, are a class of organic compounds for electrolytic Cu plating, that bind metal ions and catalyse their deposition onto the cathode surface. Accelerators lower the energy (potential) needed to reduce cuprous ions (Cu^{+}) to metallic copper (Cu^{0}), accelerating the metal deposition.

Levellers/Inhibitors increase the energy (potential) needed for the copper reduction reaction, slowing the rate of copper deposition. Most levellers have N-containing cationic functional groups (e.g., amines) that are protonated in the strongly acidic electrolyte. The effect of levellers is based on the strong adsorption of the charged molecules on the cathode surface. The higher the local current density, the higher their local inhibiting effect—at low current density areas the effect is negligible. This effect increases the deposition rate in recesses such as BMVs and decreases the deposition rate on protrusions (levelling).

In order to enable BMV filling without inclusions, the concentrations of the different process additives (especially of the inhibitor molecules) must be optimized, along with other process parameters such as solution agitation, temperature, and current density. Since all influencing factors interact strongly, the optimization of copper deposition rates over different features (e.g., board surface, BMV opening and BMV bottom) is very challenging.

ECD Cu processes for BMV filling should be optimized for uniformity, void-free filling (Figure 46), low surface roughness, copper trace line shape, and low copper thickness on the surface. Process improvements may also target reducing defects like seam voids or interface failures. Electrolytes usually have high concentrations of copper, and low concentrations of acid (about 50 g/L sulfuric acid) to enable rapid deposition and via filling. The concentrations of additives such as accelerators, suppressors, and levellers are optimized to produce the best physical properties, surface copper thickness, plated copper distribution variation, and yields.

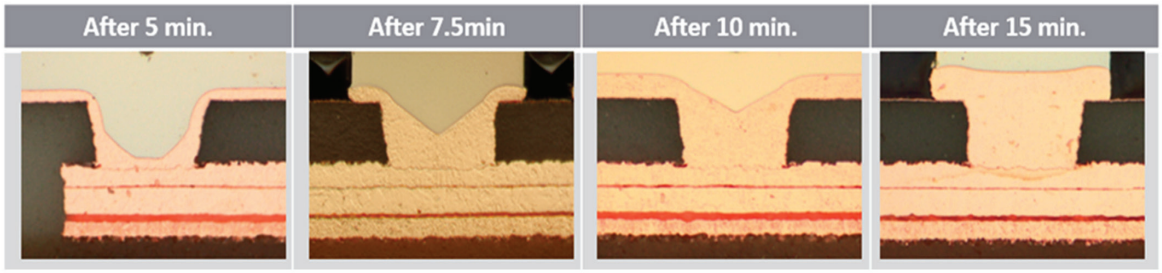


Figure 46. ECD Cu deposition observation in via by plating time (Source: InPro® SAP3).

4.7.5 MKS Products for Blind Micro Via Filling

BMVs in advanced HDI can be filled with copper using the InPro® MVF process series with minimal recess.

The process series InPro® SAP is characterized especially in ICS applications by unsurpassed surface distribution, rectangular line shape and excellent Blind Micro Via copper filling with lowest recess in pattern plating mode.

4.7.6 Through Via Filling

Filling Through Vias (TV) with solid copper, like filling of blind micro vias, is an essential step in manufacturing advanced printed circuit boards and IC substrates. The main applications for TV filling are in establishing reliable metallization in the core layers as well as improving thermal management. Recently, filling Through Glass Vias (TGV) is gaining attention due to potential use of glass cores in IC substrate manufacturing or glass interposer as an advanced packaging solution.

One of the main targets in TV filling processes is void-free filling, leading to defect-free copper deposition inside through vias. Other specifications for TV filling include plated copper thickness on the surface, overall plating time, and the quality of the crystal structure in the deposit. Depending on the specific targets, different approaches can be used for through via filling.

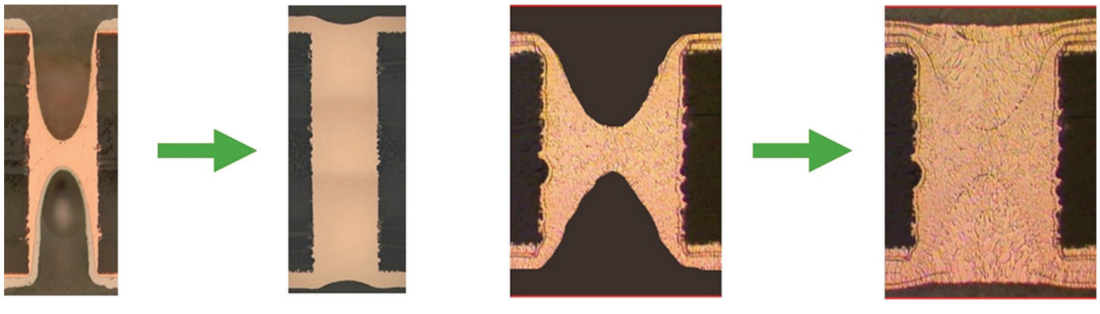


Figure 47. Bridge-plating and through via copper filling by specific RP concepts.

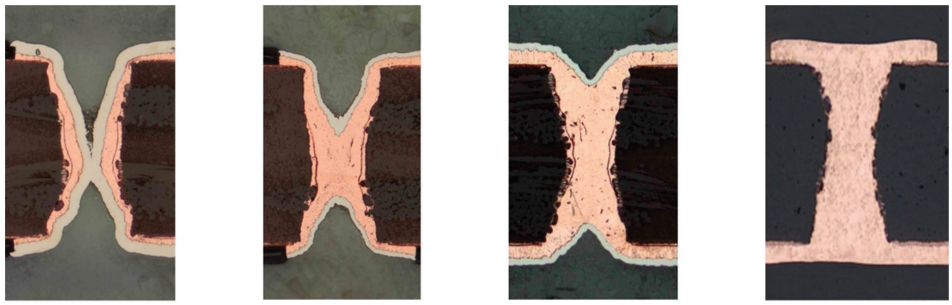


Figure 48. Step-by-step through via filling by electrolytic copper deposition, here with InPro® Pulse TVF series process in a laser-drilled through via as an example.

In all these cases, when symmetrical plating arrangement is used, copper deposition must happen in the center of through vias first, resulting in a bridge in order to ensure void free filling. As the copper deposition proceeds on both sides of the bridge, the remaining blind vias are continuously filled, ultimately resulting in no remaining recess on both sides of the substrate.

In some cases, it may be possible to complete through via filling processes in the same electrolyte and with the same process parameters. However, in order to achieve the best through via filling result, process parameters (current density, pulse form, agitation) and even electrolyte can be varied in the course of the through via filling process.

Through constant development of through via filling processes for effective filling of through via structures, more and more challenging dimensions and layouts can be achieved (Figure 49).

4.7.7 MKS Products for Through Via Filling

For less demanding aspect ratios (up to 2:1), smaller TV dimensions (panel thickness up to 0.2mm), and easier TV shapes (hour-glass shaped laser-drilled through vias) DC Cu electrodeposition processes can be used, for example InPro® THF series.

To ensure void-free filling, especially for higher aspect ratios (up to 4:1) as well as for larger through vias and/or other shapes (mechanically drilled through vias), horizontal reverse pulse plating processes of Inpulse® 2THF series are recommended.

In order to address advanced through via filling requirements, especially for pattern plating applications, vertical reverse pulse plating processes are processes of choice being developed (InPro® Pulse TVF-series).

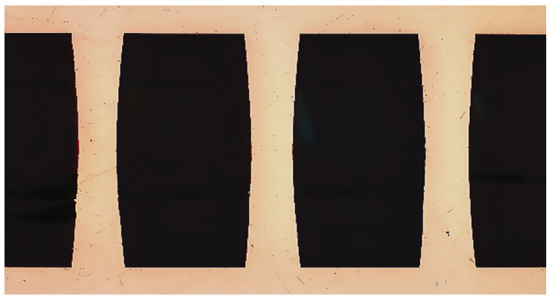


Figure 49. State-of-the-art high aspect ratio through glass via filling result with Innolyte® THF series ECD Cu process.

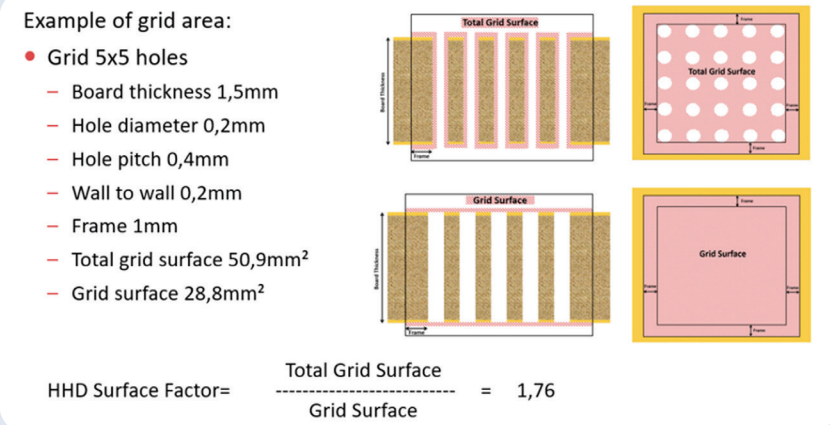


Figure 50. Calculation HHD surface factor (total grid surface area).

4.7.8 High Hole Density (conformal) - Reverse Pulse

Printed circuit board applications such as FCBGA require specific plating techniques to achieve good copper plating distribution in high hole density areas. Some FCBGA applications such as those for CPU and GPU are moving to higher core thicknesses and denser through hole areas in the printed circuit board. The main driving force for higher panel thickness is the reduction of panel warpage while for more dense through hole areas it is heat distribution of the components.

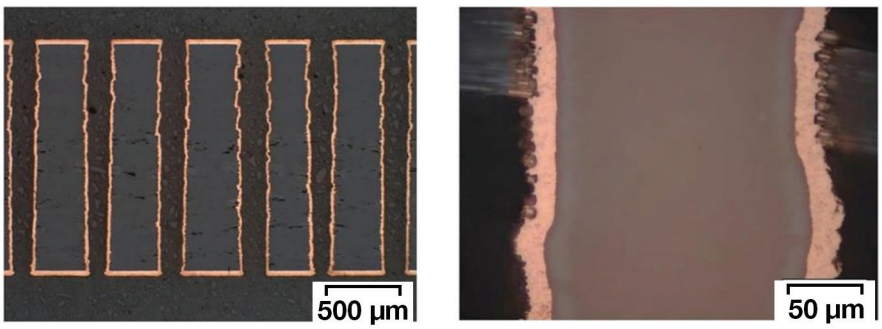


Figure 51. HHD plating result with ECD Cu.

High hole density (HHD) areas as shown in Figure 51 have a much higher surface area as compared to the plain/ground areas on the printed circuit board. The increased surface can be calculated as shown in Figure 50. This calculation yields a factor that can be used to calculate the area increase in the through hole dense area. In the example shown, the surface area is increased by a factor of 1.76. The increase of surface area impacts the copper plating thickness. In the example shown, the plating thickness in the high hole density area is reduced by a factor of 1.76. The market is trending towards higher HHD surface factors on printed circuit board designs and this is challenging the copper plating distribution on those features.

The copper electrolytes used in the plating equipment must be adjusted to improve the copper distribution. This can be done by selecting the optimal organic suppressors, brighteners and levellers and adjusting their ratios. Also, the use of reverse pulse plating can provide a key improvement, depending on the chemistry used and the values of the forward and reverse pulse current density and pulse time ratio. As well, the physical parameters like electrolyte flow and temperature must be optimized.

Another factor is the concentration of inorganic components such as copper and sulfuric acid. Lower copper and higher sulfuric acid concentrations will improve macro distribution of the copper due to higher copper plating polarization and better electrical conductivity of the plating solution. The quality of the copper deposit is also as important as the copper surface distribution. In low current density areas, the copper deposit must have a polygonal oriented grain structure to ensure the highest reliability. Plating defects like copper folding must be avoided.

4.7.9 Pillar Plating

A key driver for copper pillar or "copper post" technology (Figure 52) is the improved reliability offered by greater control of the joint diameter and standoff height. Furthermore, copper pillar technology also enables further miniaturization. Plating copper pillars enables the creation of finer-pitch joints with smaller bump diameter as compared with traditional bonding processes. In traditional solder bump design (C4FC), the solder forms the entire electrical and mechanical connection between the die and the package. Since the solder melts during the reflow process, the interconnect takes a spherical shape, but the dimensions, both diameter and height, are uncontrolled. Copper pillar technology provides the opportunity to create a cylindrical joint with more control over the diameter and standoff height.

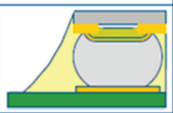
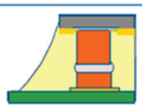
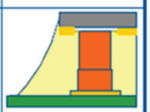
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level

Figure 52. Examples for bonding technologies and related pillar build up.
(Source: Bonding Technologies: Minsuk Suh, Sematech)

Copper Bump / Copper Post with Solder Cap

Specifications:

- Copper bump diameters = 20-130 µm; bump pitch ≥40 µm; and bump height = 7-30 µm.

The main requirements and challenges of the electrolytic plating processes (Figure 53) are:

Copper plating process:

- Bump height uniformity within the unit to improve solder joint reliability
- Filling (Levelling) performance of the copper plating process to achieve best bump shape with lowest bump height
- Plating of high purity copper with lowest internal stress

Nickel plating as barrier layer to prevent copper migration into the solder:

- Failure free deposition on copper pillar
- Best thickness uniformity
- Cleanliness of plated Ni deposit to prevent internal stress

Solder Cap:

- Purity of solder alloy or pure tin

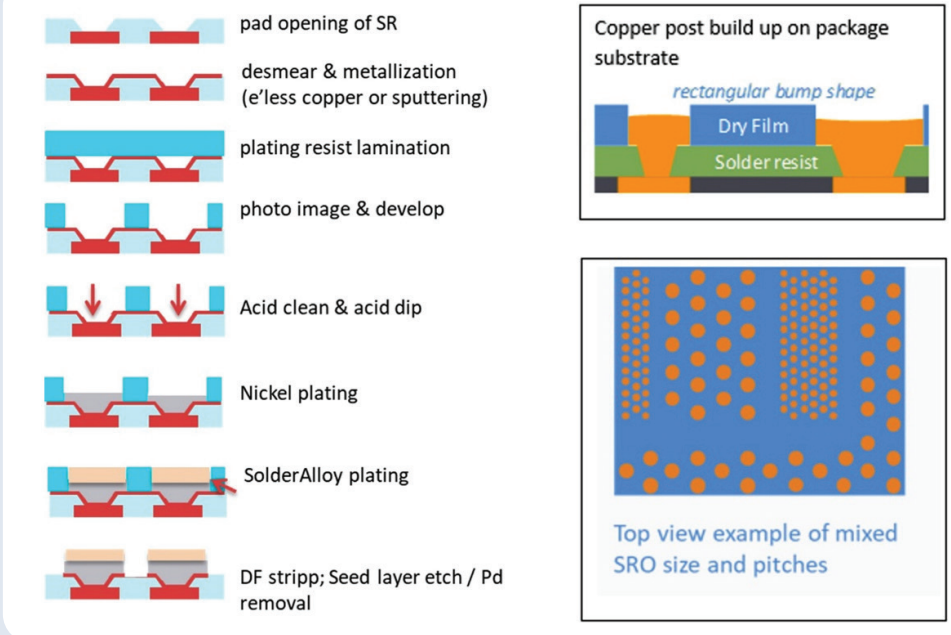


Figure 53. Process sequence copper pillar with solder cap.

- Uniformity of metal composition in case of alloy plating
- No micro or process voids after reflow/ soldering are allowed

Tall Pillar

''Tall Pillars" (Figure 54) are a design concept that compensates for mismatches in the Coefficient of Thermal Expansion (CTE) and improves the reliability of the final package.

Specifications:

- Bump diameter = 40-200 µm; bump pitch ≥60 µm; and bump height = 30-200 µm

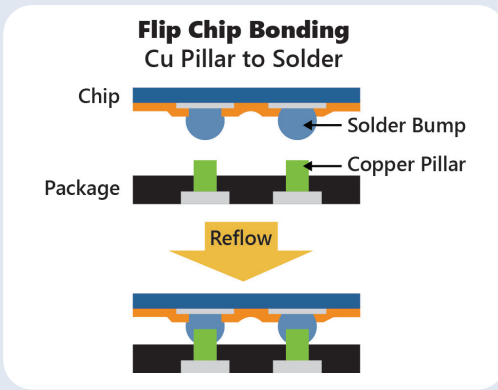


Figure 54. Tall copper pillar application.

The main requirements and challenges of the electrolytic plating processes for "tall copper pillar" technology are:

- Bump height uniformity within the unit to improve solder joint reliability
- Plating speeds up to 20 ASD (Amperes per Square Decimeter) have to be applied to reduce the plating time and thereby the process cost
- Plating of high purity copper with lowest internal stress to overcome CTE mismatch
- Superior pillar planarity (super conformal bottom-up plating)

Each individual process step for each pillar type requires process chemicals with corresponding properties. Electrolyte composition along with other parameters must be adjusted based on the requirements of specific applications.

4.7.10 MKS Products for Pillar Plating

Copper pillars of various diameters and heights can be electrolytically deposited with the InPro® PI and CPF series with the best uniformity in a wide variety of designs.

4.7.11 ECD Cu – Physical Properties and Reliability

Electrodeposited copper exhibits high purity, comparable with pure elemental copper. The main difference between these two forms is that the deposited form is polycrystalline with the size of the copper crystals typically 2-6 µm. The mechanical and physical properties of the copper layer are strongly influenced by the organic additives of the ECD Cu process which can produce various changes in the atomic lattice described in the following section.

4.7.11.1 Electrical and Thermal Conductivity

Copper's high electrical and thermal conductivity is exceeded only by silver, making it an excellent and inexpensive coating for products such as printed circuit boards. For this reason, it replaced aluminum in semiconductor interconnect technology after the late 1990s. In addition to the crystal size and irregularities in the atomic lattice, the purity of the copper deposit is particularly important for good conductivity (Table 3).

Cu Type	Electrical Resisitivity µW*cm @ 293.2 K (20°C)	Thermal Conductivity W/K*m @ 293.2 K (h20°C)	Condition of Copper
Literature Value	>1.68	>400	• 99.95% Cu • Fully annealed • ~100 µm grain size • Polyhedron grain shape
ECD Bright Copper	1.1 – 1.9	>375	• 99.999% Cu – ECD Bright Copper • Thermal anneal > 1 hr @ 230°C • ~5 µm grain size • Polyhedron grain shape

Table 3. Electrical resistivity of pure Copper vs. ECD Cu.

4.7.11.2 Elongation, Tensile Strength and Toughness

The elongation of most electroplated copper deposits is greater than many other electroplated metals. This property helps substrates such as plastics to withstand thermal expansion without cracking their electro-deposited coatings. The copper must be of high purity (grain boundaries) and have a complex 3-dimensional structure (polyhedron) to achieve good elongation and high tensile strength. The combination of elongation and tensile strength is critical for the mechanical reliability and toughness of ECD copper. The influence of the leveler and brightener additives on tensile strength and ductility (or elongation) is illustrated in Figure 55.

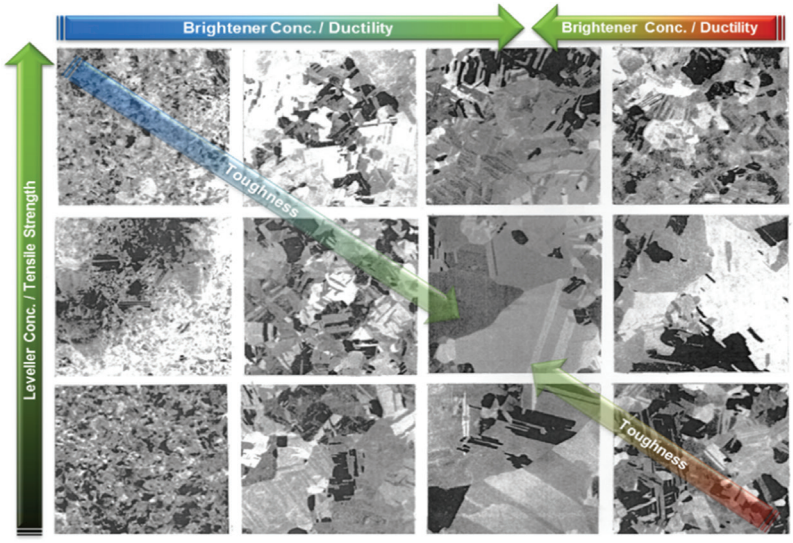


Figure 55. Elongation and tensile strength depending on the crystal structure, triggered by the organic ECD Cu additives.

4.7.12 Thickness Uniformity

The different factors affecting the surface distribution of the plated copper can be generally placed within three different categories:

1. **Ohmic Effects:** These are associated with ohmic losses mainly in the bulk of the electrolyte phase, but occasionally also significant in the electrodes and leads.
    a. After I-R drops in bulk phases and leads are considered, some I-R drop associated with electrode surfaces may persist.
    b. These are often caused by oxide films, which are generally poor electrical conductors.

Important problems that can be observed in through holes or BMVs:

    c. Solution resistance creates an ohmic overpotential gradient in such spaces.
    d. Ohmic effects can cause changes in the current density. These directly affect the plating thickness and need to be properly considered.

2. **Activation Effects:** These effects are associated with the different energy barriers for reactions and consequently, the activation energy for important reactions at the electrode.
    a. Low overpotential sought for primary cell reaction to minimize energy loss.
    b. High activation overpotential sought for suppressing competing reactions.

Activation energies are affected by the type of reactions taking place in the system and changing the reactants or using reaction additives allows us to control these activation effects.

1. **Concentration Effects:** These effects arise from mass transport limitations and are highly significant when the mass transport is slow for a comparatively faster reaction. This would eventually cause a lowering of the reactants or increase of the by-products in the diffusion layer (Figure 56). This is a highly undesirable effect for most practical applications as it causes a direct decrease in the efficiency of the system. The various types of mass transport in a system are diffusion, migration, and convection. For most commercial applications, we maintain some type of convection in the system using flow nozzles, air agitation, ultrasound vibration, etc. which increases the mass transport to the electrode and reduces concentration effects.

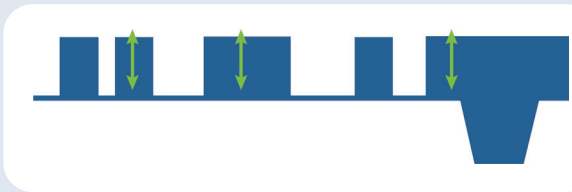


Figure 56. Example of typical measurement locations for copper thickness in unit which includes isolated and dense copper traces.

WiUD (Within Unit Distribution) is the uniformity in one unit on the full-sized production panel. Improvements in WiUD require the optimization of both the equipment set up and the chemical conditions in the deposition. Levelling agents are selectively adsorbed at locations with a high current density, such as feature hole edges.

For advanced packaging applications, line and space (L/S) requirements become more challenging, resulting in reduced copper thickness for several reasons:

1. **Electrical Performance:** The thickness of the copper layer directly affects the electrical performance of the substrate. A uniform plated copper thickness distribution ensures that the electrical current is distributed evenly throughout the substrate, reducing the risk of hotspots and improving overall electrical performance.

2. **Reliability:** A non-uniform plated copper thickness distribution can create stress and strain on the substrate. This can lead to cracking or other forms of damage over time and compromise the reliability of the substrate, potentially leading to premature failure of the device.

3. **Process Control:** Achieving a uniform plated copper thickness distribution is a critical process control parameter in the manufacturing of IC substrates. By monitoring and controlling the plating thickness distribution, manufacturers can ensure consistent and reliable production of IC substrates.

In summary, a uniform copper plating thickness distribution is essential for ensuring the electrical performance, reliability and consistant production of IC substrates.

4.7.13 Plating Equipment

Horizontal ECD Plating

As previously noted, (Chapter 4.5.8) horizontal equipment is used for the core layers in IC substrate manufacturing. Furthermore, it is widely applied for SLP application in the mSAP process. In mSAP processes, following via drilling, the PCB is run through desmear, electroless copper (0.3-0.5 µm), and finally thick electroplated copper (3.0 µm) build-up processes. The electroplating process is called flash copper plating. Each plating process, whether it is for conformal plating or for filling vias or through holes (Figure 57), has a unique process solution.

Horizontal equipment for electrolytic copper deposition clamps circuit boards from one side with several clamps and the circuit board acts as the cathode (negative electrode). The anode (positive electrode) is made of inert conductive material. The current is provided by an external power supply rectifier system. Before the panels enter the electrolytic plater, they must be aligned correctly for the clamp position and adjusted with uniform gap distance (distance from board to board in transport direction).

Vertical ECD Plating

In vertical equipment, panels are touched only at the "Keep Out Zone" (KOZ) during robotic loading, unloading and transport along the line. The advantage of not touching the panels at the product area means that dry-film or photoresist structures will not be damaged. This makes vertical tools the equipment of choice for pattern plating. Rack tools offer high flexibility of dwell times, vertical conveyorized plating tools have high throughput, and single panel tools are highly optimized for fine structures.

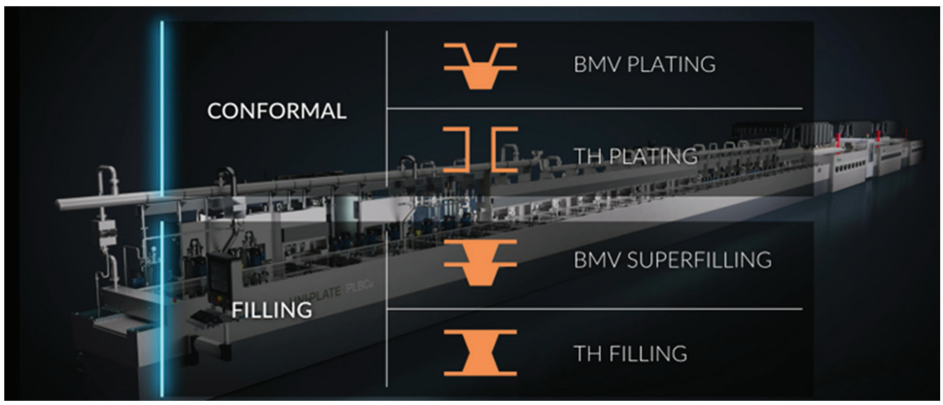


Figure 57. Types of electroplated copper processes.

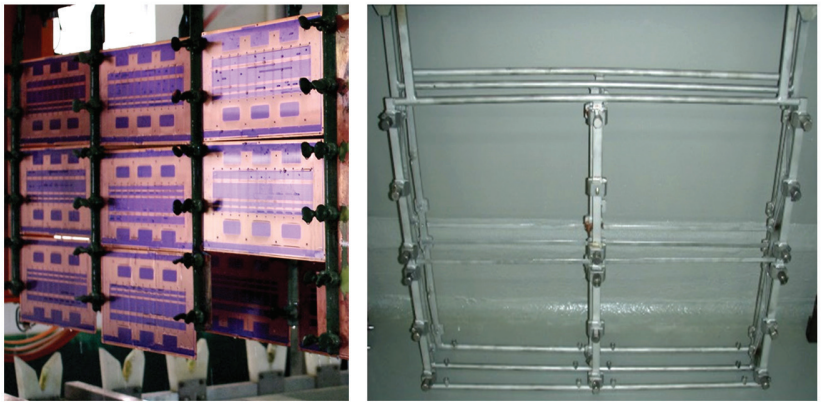


Figure 58. Rack type panel holder for vertical tools.
(Source left: Alibaba.com)

Vertical tools can use either direct fluid supply to each side of the panel using eductor nozzles or indirect supply by flooding the module from the bottom. The flow speed in direct supply systems can be adjusted to the process needs and results in a stronger solution exchange at the surface and in the holes. An indirect flow from bottom does not allow high solution speed, therefore it must be supported by additional devices, such as shear plates (paddles) or air agitation. The panels are normally placed in a carrier attached to a "flight bar" by the robot. They are arranged beside or above each other, so that each side of a panel is exposed to the anode. Depending on the stiffness of the panel and its warpage, one of two types of carriers may be used.

Rack Type:

The rack is an arrangement of vertical rods with a clamping system at the left and right of the panel (Figure 58). Panels are usually only mounted in one row with specific panel heights, but in rare cases they may be arranged over each other. The use of racks in the Advanced Packaging industry is decreasing.

Frame Type:

The most common mounting method for panels is a metal frame in which panels are clamped at the top and bottom using electrically conductive clamps (Figure 59). The frame is not coated and is used as active shielding. "Flight bars" are transported along the line by a hoist type of transporter, which lifts them from one tank to the next (Figure 60). Each module has a fixing point for the flight bar. In electrolytic Cu modules, the fixing points are also the connection for the current supply between panel/holder and the rectifier. Frequently, the fixing points are attached to an agitation device which moves the panel within the module to equalize any differences in solution flow and current distribution over the panel surface. Inert anodes are located on both sides of the module and connected to the rectifiers, which supply DC current. Copper for plating is supplied as dissolved CuO from a separate solution tank.

Each process step has its own module. Depending on the required throughput and dwell times of the process step, the number of modules per step can be adjusted. For high throughput several panels will be arranged in a row, resulting in wide modules. The process times of each process step can be individually adjusted without influencing the dwell times of other steps. This modular set-up makes this type of tool very flexible for different process needs, variable production, and small batch production.

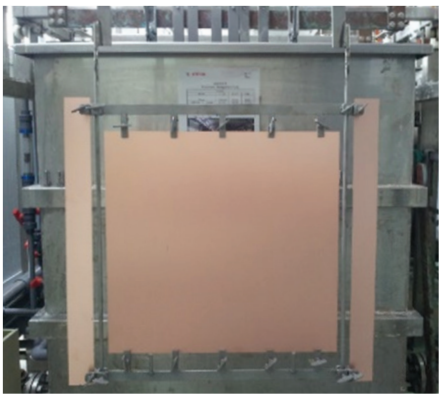


Figure 59. Frame type panel holder for vertical tools.

Figure 60. Gantry for transportation of racks along the line.

4.7.14 MKS Uniplate® Cu Plater

MKS supplies the Uniplate® Cu Plater line of horizontal plating equipment. With MKS' Uniplate Cu Plater (Figure 61), this task is carried out by an automatic handling device, the CGA (center gap adjustment) or with the TGA (turn gap adjustment). The TGA can turn the panel by 180° and with that change the clamping site of the panel in case further plating units will follow, further improving the Cu deposition uniformity (Figure 62).

For controlled and uniform copper deposition, it is important to consider the most fundamental process parameters. The current strength per area [A/m^2] influences the plating speed while the structure and position of the anodes influence the location and density of the electric field lines and the uniformity of the copper deposition. If the electric field lines are denser at certain points (sharp edges of the circuit board e.g., holes), then, with direct current, more copper is deposited at this point.

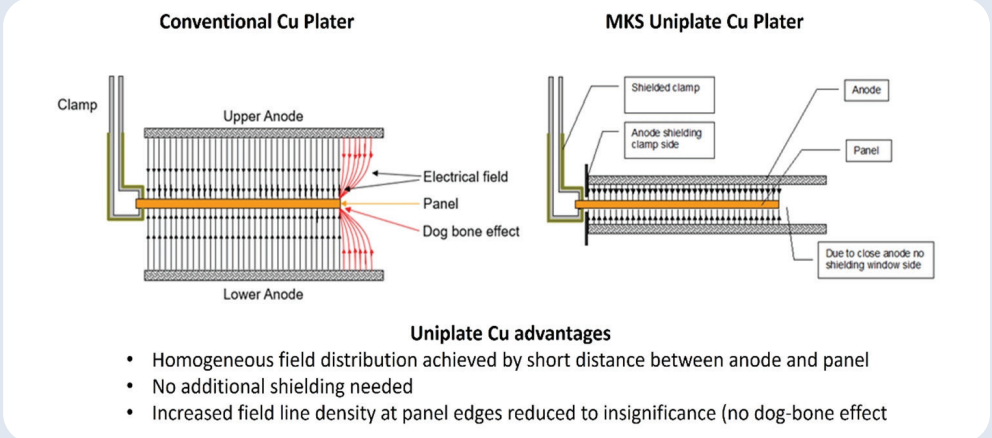


Figure 61. Uniplate® Cu Plater advantages.

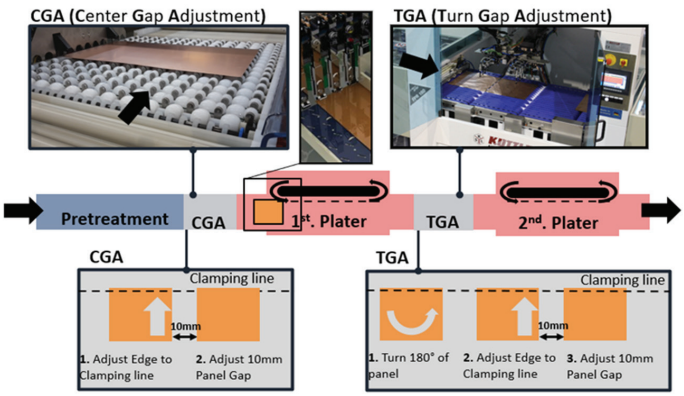


Figure 62. Automated panel handling in MKS Uniplate® Cu Plater.

The latter issue can be resolved using a technique known as bipolar pulse plating (also known as reverse pulse plating). In reverse pulse plating the current flow is reversed and amplified over a relatively short cycle time (Figure 63). By correctly switching the current and adjusting the level and duration of the current, copper is deposited more uniformly over flat surfaces and sharp edges.

Another important parameter is the chemical concentration, especially the metal ion concentration. MKS' horizontal Uniplate® Cu Platers use a Cu/Fe electrolyte in which an auxiliary system analyzes the concentration of Cu and Fe ions and, depending on the deviation, counteracts it by pumping the electrolyte through an auxiliary redox system. The automatic copper replenishment system maintains the concentration of Cu/Fe ions at an optimal level enabling consistent quality. A brief review of the chemistry associated with the Cu/Fe electrolyte used in Uniplate® Cu Platers can aid in understanding the advantages offered by the Cu/Fe electrolyte system.

The cathodic reaction during electrochemical deposition of copper is reduction of cupric ions to Cu metal:

$$\text{Cathode surface: } Cu^{2+} + 2e^{-} \rightarrow Cu^{0}$$

The anodic reaction depends on the electrolyte system and equipment used. In processes with soluble anodes, metallic copper is dissolved to replenish cupric ions in the electrolyte:

$$\text{Soluble anode surface: } Cu^{0} \rightarrow Cu^{2+} + 2e^{-}$$

In processes with insoluble, or dimensionally stable anodes (DSA) normally water is oxidized at the anode, resulting in oxygen evolution and an increase of acid concentration. Cupric ion replenishment takes place, as e.g., CuO or $CuCO_3$ is added at the same time reducing acid concentration back to its setpoint:

$$\text{Insoluble anode surface: } 6H_20 \rightarrow 4H_3O^{+} + O_2 + 4e^{-}$$

$$\text{Cupric ion replenishment A: } CuO + 2H_3O^{+} \rightarrow Cu^{2+} + 3H_2O$$

$$\text{Cupric ion replenishment B: } CuCO_3 + 2H_3O^{+} \rightarrow Cu^{2+} + 3H_2O + CO_2$$

While use of inert anodes is advantageous compared to soluble anodes, some drawbacks exist. These are mainly related to oxygen evolution, which leads to increased additive consumption, reduced

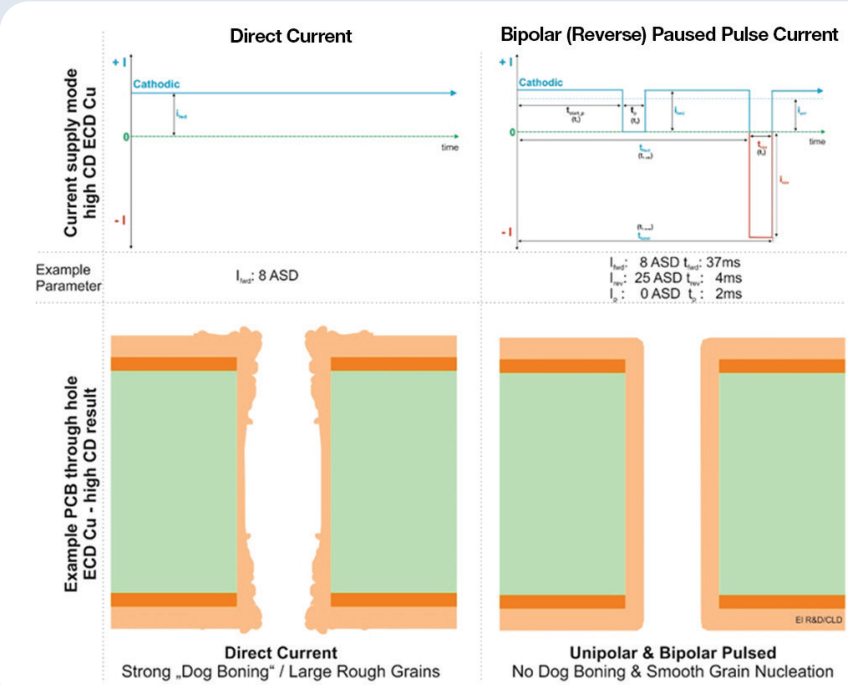


Figure 63. Application of reverse pulse plating ensures best copper quality with unmatched metal throw.

bath life due to accumulation of breakdown products, shorter anode lifetime, risk of surface defects due to anode coating particles in the electrolyte, and surface defects due to oxygen bubbles interfering with the plating process.

An elegant way to suppress oxygen evolution at inert anodes is to introduce an auxiliary redox system, which is based on ferrous and ferric ions (Fe^{2+}/Fe^{3+}) (Figure 64). On one hand side, ferrous ion oxidation takes place at the anode instead of oxygen evolution due to its more negative redox potential:

$$\text{Insoluble anode surface: } Fe^{2+} \rightarrow F^{3+} + e^{-}$$

Suppression of oxygen evolution mitigates most of the above-mentioned disadvantages of inert anodes. On the other hand side ferric ions replenish cupric ion in the electrolyte by dissolving metallic copper clippings in a dedicated unit:

$$Cu^{0} + 2Fe^{3+} \rightarrow Cu^{2+} + 2Fe^{2+}$$

This is an easy and cost-effective way to replenish cupric ions in the electrolyte that, in addition, allows for better impurity control compared to CuO and $CuCO_3$ sources.

Copper deposition at the cathode is accompanied by the parasitic reaction of ferric ion reduction to ferrous ions. As a result, current efficiency of the overall plating process is reduced. However, many plating processes benefit from lower copper deposit thickness due to this side reaction.

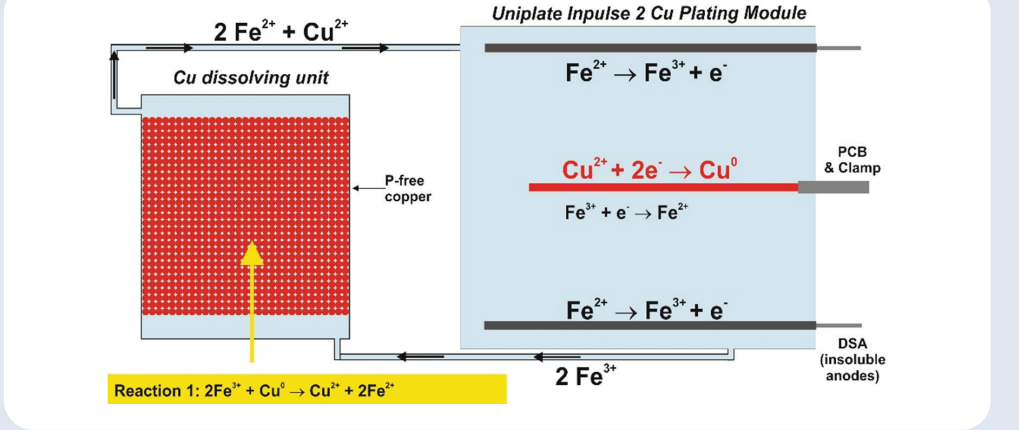


Figure 64. Electrochemical processes during electrolytic copper deposition using inert anodes and Fe redox system on a horizontal plater.

The iron redox system not only allows for mitigation of oxygen evolution at the anode, but also does not lead to negative effects such as contamination of the deposit. Due to a significant difference in redox potentials of the Fe^{3+}/Fe^{2+} and Cu^{2+}/Cu^{0} couples, no iron co-deposition takes place.

In summary, use of the Fe redox system in electrolytic copper deposition improves process stability and performance, without significant drawbacks.

4.7.15 MKS Products for Uniplate® Cu Plater

Uniplate® Cu systems (Figure 65) are specially designed for electrolytes which are replenished using the patented Iron RedOx Auxiliary system and used in reverse pulse (bipolar) mode.

All Inpulse® processes developed by MKS for conformal plating, micro via and through via filling can be used in this system.

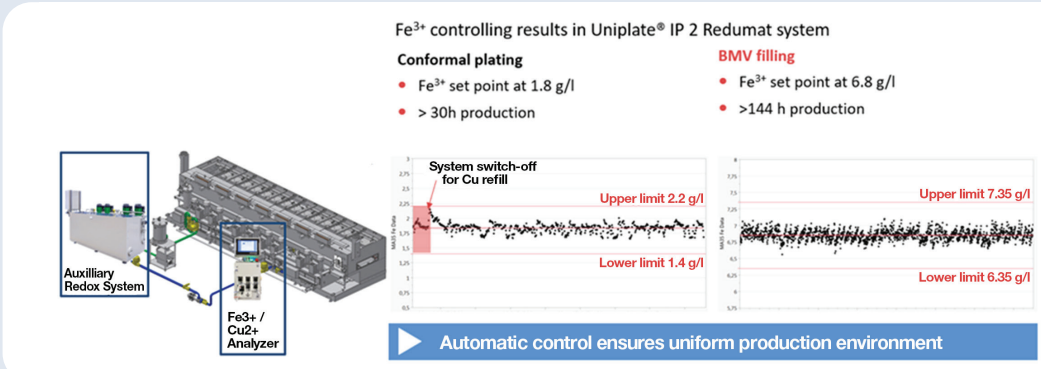


Figure 65. Process control in conformal plating and BMV fill results using the Uniplate® Cu Plater with auxilliary redox system.

4.7.16 MKS vPlate® Vertical Conveyorized Plating Tools

MKS offers the vPlate® Vertical Conveyorized Plating (VCP) tools for high volume production of touch sensitive products in advanced packaging applications (Figure 66). Module and panel orientation is parallel to transport direction. Thin panels are loaded to a jig while thicker panels are loaded to a top clamp hanger after which they are transported from module to module. Transportation occurs in an up/forward/down movement for pre- and post-treatment and continuously through the electrolytic Cu module. Modules in pre- and post-treatment are short modules for treating 1 to 5 panels simultaneously. They are optimized for process needs regarding solution flow, vibration or shock devices, air supply, temperature, or chamber material.

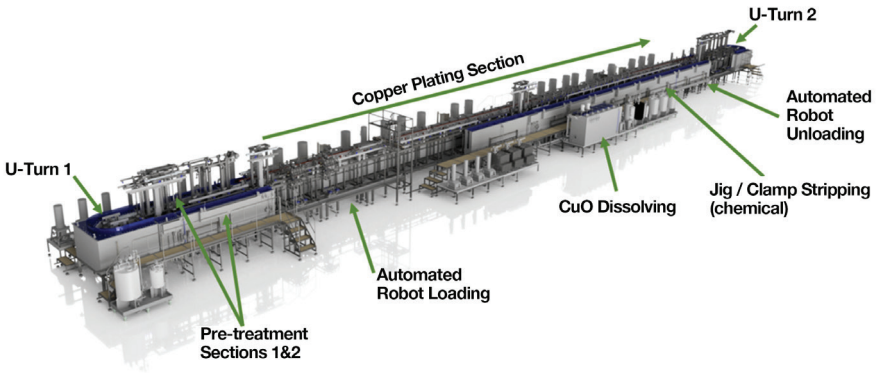


Figure 66. Typical set-up with MKS vPlate® VCP.

The plating chamber is a long module, easily reaching more than 30m, depending on the required plating time and throughput. The hangers are attached to a chain or belt that moves them slowly and continuously along the module. The hanger slides, with its contacts, along the cathode rail connecting the panel to the electrical circuit. Anodes are positioned on both sides of the module and connected to the rectifiers. In advanced packaging applications, anodes are mainly inert anodes, made from materials such as Ti that don't dissolve in the electrolyte solution. Copper is supplied as dissolved CuO from a separate solution tank. Both DC and pulse plating technologies can be applied, depending on the process needs. Benefits of the continuous transport used in vPlate VCP tools include:

- High consistency of within-panel and panel-to-panel performance, as every panel is treated the same.
- Clear tendency towards better uniformities - approximately 20% better compared to hoist type.
- Improved filling performance, as solution flow parameter can be better controlled which prevents spot issues like honeycomb effect (flow dependent copper crystallization leading to a visual imprint of the copper nozzle arrangement on the substrate surface)

VCPs constitute the majority of electrolytic Cu plating equipment used in the Advanced Packaging industry.

4.7.17 MKS Products for vPlate® VCP Plater

As an advanced electrolytic plating system, all ECD Cu processes with insoluble anodes (DSA) and CuO replenishment can be used with this VCP system. All relevant processes of the InPro® family developed by MKS for conformal plating, micro via and through via filling are optimized for use in vPlate® systems.

4.7.18 Single Panel Tools

Single Panel tools handle and treat each panel separately in a vertical panel orientation. After taking a panel from a hand-over station or from load ports, the panel is fixed in a substrate holder. A transportation system moves these holders from module to module along the line in a vertical mode. Process modules are arranged in a row as in vertical hoist type equipment. One panel per module allows the process parameters for solution flow, current density and/or application of shielding to be optimized to the panel. Single panel systems can achieve plating uniformities of 6% or better.

Two types of flow solutions can be used in Single Panel tools:

1. **Fluid Agitation by Paddles (shear plates):** In these tools the fresh chemicals are supplied from bottom at lower speed. Shear plates are oscillated back and forth at high speed, producing strong turbulence and therefore a better solution exchange at the panel surface. In these tools shielding can be applied to optimize electrical current flow.

2. **Direct Fluid Supply to the Panel:** The fluid flows through the anodes directly to the panel. It generates a strong flow and therefore a high solution exchange rate, ensuring fresh chemicals at the plating surface. This method of solution supply is realized by MKS' MultiPlate® Single Panel tool.

High solution exchange, as in MultiPlate® tools, enables current densities of up to 5ASD for fine line/spaces pattern plating, such as RDL plating, or even more than 20ASD for pillar plating.

Particle load is minimized by the combination of fine particle filtration in the tool and housing the complete system in a clean room with controlled conditions compliant with ISO 5. This is important for guaranteeing high yields in pattern plating of fine line/spaces such as RDL plating.

4.7.19 MKS Products for MultiPlate® Single Panel Tool

The Innolyte® product range covers all panel level package (PLP) applications in electrolytic copper plating. The copper plating processes are characterized by the best metal distribution combined with unparalleled process stability.

4.8 Circuitization

Circuitization describes the process of creating the actual circuitry on the IC-substrate. In Chapter 3.2 the most commonly used circuitization technologies were introduced.

4.8.1 Dry Film Pre-treatment

Dry film is used as a plating resist in most circuitization technologies (Chapter 4.6.1). When the copper seed layer is thicker than 1 µm, chemical roughening of the copper surface by mild etching is often permitted. Dry film already contains adhesion promotors for chemical adhesion; however, mild roughening of the copper surface promotes much stronger adhesion.

4.8.2 MKS Products for Dry Film Pre-treatment

The CupraEtch® DF 8000 process is an innovative low etch depth cupric chloride based micro etchant as pre-treatment process for superior dry film adhesion. It consists of a three-step process (Figure 67) and is applied in horizontal spray equipment for homogeneous surface treatment and high throughput. CupraEtch® DF 8000 is an intergranular etching (IGE) system employing a modified cupric chloride micro etchant, providing optimized surface roughness (Figure 68) for best dry film adhesion for a wide variety of dry films.

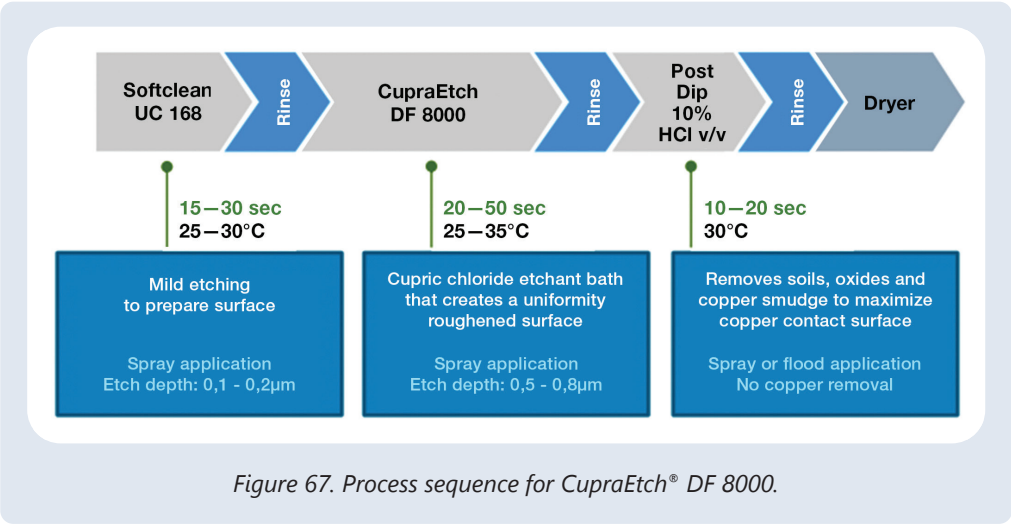


Figure 67. Process sequence for CupraEtch® DF 8000.

As the name implies, IGE systems predominately attack the grain boundaries and not the surface of the copper crystals. For this reason, the copper quality and type have a major impact on the performance of IGE systems. Ideally, copper crystal size distribution should be homogeneous since small crystals are more rapidly etched by the IGE systems than larger crystals. This is often noticed visually by variations in the reflectivity and surface color.

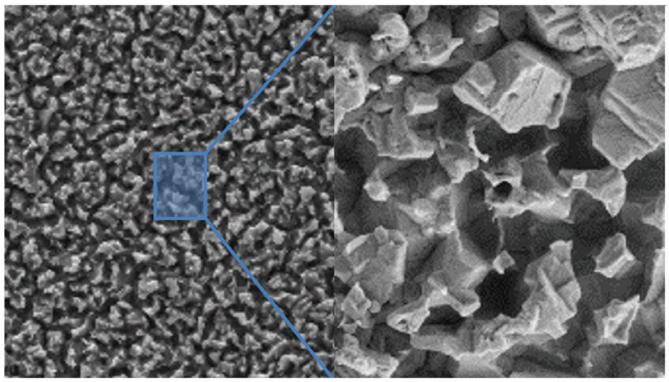


Figure 68. CupraEtch® DF 8000 roughened copper surface.

4.8.3 Dry Film Removal

The ultra-fine circuitry of the IC substrate is created by electrolytic copper plating of the areas not protected by the dry film. After the copper has been plated, the dry film must be removed to create the circuitry. This is done using dry film strippers. Normal HDI and IC substrate dry film strippers are either hydroxide-based, amine-based, or a mixture of both. Compared to hydroxide-based strippers, amine strippers have the advantage that the dry film breaks apart into small pieces that can be easily filtered out of the stripper solution. Hydroxide-based strippers remove the dry film in large sheets that can stick to the equipment or, in the worst case, to the circuit boards. Furthermore, the strip speed of amine strippers is considerably faster than that of hydroxide-based strippers. These strippers also contain an anti-tarnish package to prevent Cu oxidation or Cu dissolution. IC substrate strippers for fine lines prevent swelling of the dry film which eliminates residual dry film trapped in the spaces of the fine line structures.

4.8.4 MKS Products for Dry Film Removal

The standard dry film strippers commonly used for HDI application are not suitable for IC substrate manufacturing. Due to the fine line circuitry, there is not enough space between the copper tracks to allow the dry film to swell, break apart, and be washed away. Rather, swelling of the dry film between fine copper tracks can easily lead to locked-in dry film residue blocking the space between tracks. Therefore, a different approach is needed. Dry film strippers for IC substrate manufacturing contain ingredients which diffuse much more rapidly into the dry film and attack the interface between copper and dry film. The diffusion into the dry film and the lifting occurs much faster than the swelling so that the dry film is already outside the plated features before swelling and the subsequent break-up into smaller flakes occurs. In addition, any remaining micro residues of dry film are dissolved by the special IC substrate resist strippers, producing complete and residue free stripping.

MKS supplies specially formulated ResistStrip® IC, formulated to work as described in the previous paragraph, to meet the demands of ultra-fine line dry film stripping in the manufacturing of IC substrates. The single process step is suited to all types of stripping equipment with either “dashpot“ or bulk storage-style replenishment systems. Compared to amine systems, ResistStrip® IC significantly reduces waste volumes.

The even and rapid strip rate enables the highest throughput. ResistStrip® IC offers the following features and benefits:

- Minimal swelling of resists to ensure maximum stripping without entrapment
- Minimal attack on copper surfaces due to the use of an integrated inhibitor package
- Two highly concentrated stripper solutions for easier handling
- Suitable for use with most alkali-soluble photoresists
- For use in conveyorized spray equipment

The ResistStrip® IC series of strippers directly attacks the copper-dry film interface, lifting the dry film out of even very narrow plated copper channels, with minimal attack of the copper. Even partially over plated dry film can be successfully stripped using the ResistStrip® IC series. Complete stripping is easily verified using fluorescence microscopy, in which dry film residue will fluoresce as shown in the comparison in Figure 69. Even high-quality amine-based resist strippers are not able to fully remove all dry film in ultra-fine line circuitry. Especially, entrapped or over plated dry film (F POR side) will not be removed. Only the ResistStrip® IC series is able to remove the dry film quickly and completely, even in the presence of over plating.

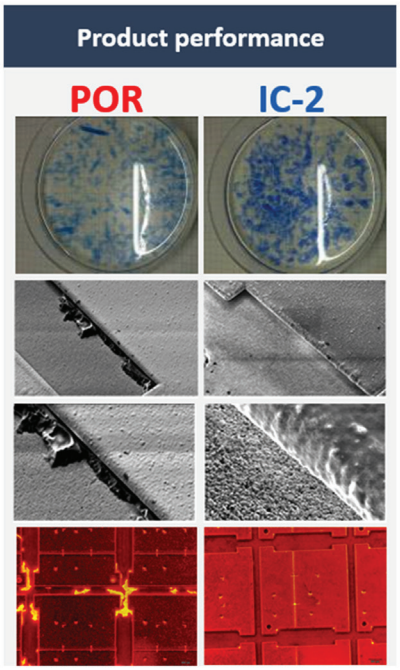


Figure 69. Performance comparison of amine strippers vs. the ResistStrip IC series.

4.8.5 Copper Seed Layer and Palladium Removal

The continuing move to greater miniaturization is forcing IC manufacturers to increase the density of interconnects by using ever finer conductor lines and spaces. Advanced manufacturing technologies such as Semi-Additive-Processing (SAP) and advanced Modified-Semi-Additive-Processing (aMSAP) have been developed and implemented to meet the requirements of this increased density. SAP as well as aMSAP processes are based on pattern plating of the desired circuitry on a thin conductive copper seed layer followed by removal of the seed layer using so called flash/differential etching solutions.

Differential etchants are based on sulfuric acid/hydrogen peroxide solutions containing different organic additives. The main advantage of this type of etchant is its uniform and fluid-independent etch attack. However, these etchants exhibit several drawbacks. Etching processes employing these solutions must run in feed and bleed mode to maintain a stable copper content and to replenish the consumed oxidizer. This results in the generation of considerable amounts of chemical waste that require costly waste treatment. As well, this etchant type is known to undercut the conductor tracks (by up to several micrometers), and this impacts the mechanical stability and interfacial integrity of the conductors, especially fine line conductors (track width <10 µm).

As the industry continues to evolve and push the limits of technology, traditional differential etching processes are struggling to keep up with shrinking line and space dimensions. In particular, conventional etching processes exhibit excessive roughness and/or copper removal at the trace. As well, residual palladium in the differentially etched open spaces in SAP-produced IC substrates can produce isolation defects and therefore need to be removed. Two types of palladium catalysts are in general use: colloidal and ionic. Cyanide-based solutions are often used to remove the palladium layer, with immersion times of 30 minutes required for complete removal. There is a pressing need to increase yield while minimizing operational costs and reducing environmental impact through minimized wastewater expenses.

4.8.6 MKS Products for Copper Seed Layer and Palladium Removal

The copper seed layer can be removed using a differential etching process such as MKS' EcoFlash® S 300 process. EcoFlash® S300 is a modified iron etchant that uses ferric sulfate as the oxidizing agent. Figure 70 shows the chemical oxidation of copper using ferric ions. Two mole Fe (III) ions are reduced to Fe (II] ions to etch one mole of copper. Fe (II) ions can be re-generated to Fe (III) either electrolytically using an electrolytic regeneration system or, more easily, by the addition of hydrogen peroxide.

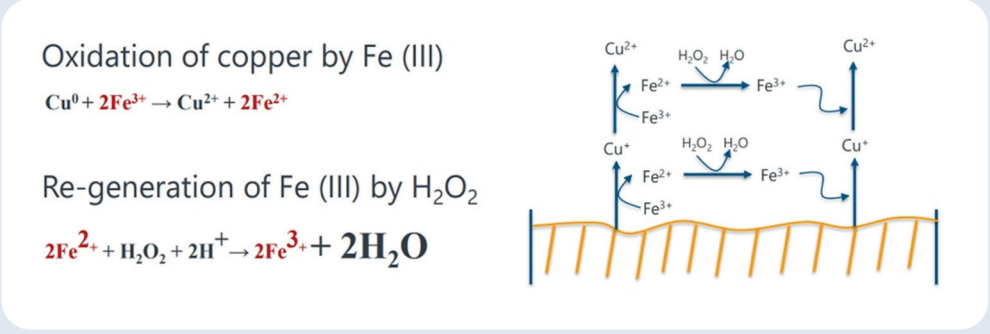


Figure 70. Etching and regeneration using ferric sulfate.

The EcoFlash® S 300 process was developed to ensure minimal attack and undercut of the plated circuitry. It ensures no undercut for sub-2/2 µm, low surface roughness, minimized Line Width Reduction, and optimal (rectangular) track shape. EcoFlash® S 300 causes no undercut of the copper tracks, does not cause roughening of the copper surface, and thus has no negative impact on track shape and signal integrity. Special additives were developed to ensure that the seed layer is etched away without causing unwanted change in the copper track shape. EcoFlash® 300 employs these special additives to ensure a higher etch rate at the bottom of the tracks and to avoid trapezoidal etching of the copper tracks. This results in an optimal track shape. EcoFlash® S 300 is used successfully for Embedded Trace Substrates (ETS) as shown in Chapter 3.4.3.

Alternatively, PallaStrip® IC cyanide-free palladium stripper is suitable for the removal of palladium-containing seed layers. The removal of any seed layer is critical in fine line applications as they can lead to uncontrolled deposition during subsequent plating operations. PallaStrip® IC offers a simple and easy process solution without the use of any harmful cyanide components, giving the most efficient removal of palladium catalyst deposits with minimal copper removal.

4.8.7 Bonding

Following the creation of circuitry and depending on the design, the next layer can be either a build-up film as described in Chapter 3.2 or a solder mask. Due to the ultra-fine line geometry of the IC substrates, the standard etching systems are not used. The standard etching systems with an etch depth of up to 1 µm would reduce the width of the copper circuitry too much, considering that SAP circuitry is in the range of only 5 µm wide. Also, highly roughening the tracks will have a detrimental impact on the signal integrity for high frequency applications. For IC substrate manufacturing, special processes for bonding of build-up film as well for solder mask need to be used.

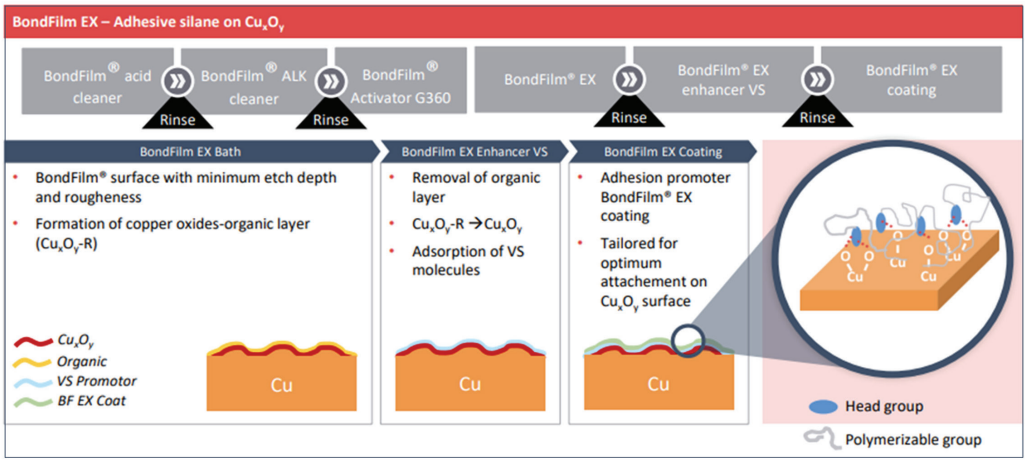


Figure 71. Process sequence for BondFilm® EX-S2.

4.8.8 MKS Products for Bonding

The MKS BondFilm® EX-S2 process was developed as an answer to the following technology challenges:

- Smooth copper interface desired for high frequency applications
- Excellent adhesion and thermal reliability
- Excellent material compatibility

BondFilm® EX-S2 is a very mild etching process combined with a chemical adhesion promotor as shown in Figure 71.

In contrast to conventional Oxide Replacement (OR) processes, MKS BondFilm® EX-S2 provides excellent adhesion and thermal reliability on high performance materials while producing low roughness and thereby providing a significant high frequency signal loss improvement. The low roughness is seen in cross-section imaging (Figure 72) and can be quantified by Atomic Force Microscopy (AFM) roughness measurements (Figure 73).

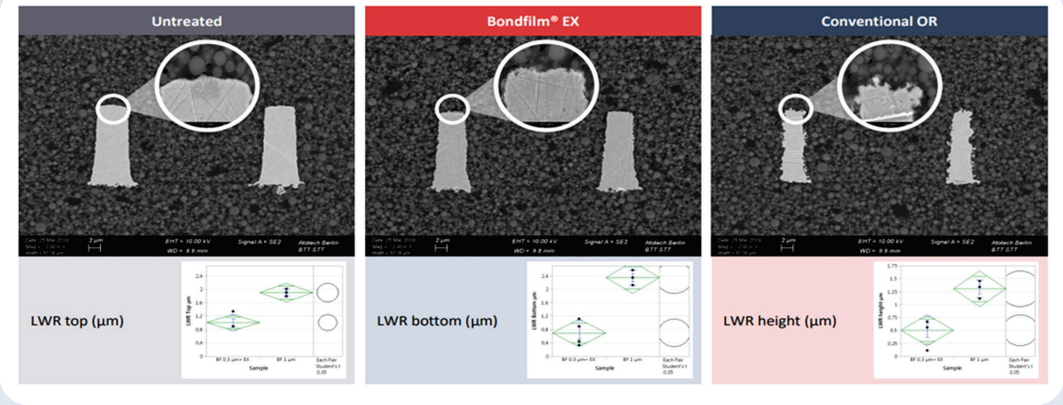


Figure 72. Comparison BondFilm® EX-S2 to conventional oxide replacement.

For ultra-fine line circuitry and high frequency applications, a completely non-etching process like the MKS NovaBond™ EX-S2 must be used (Figure 74). NovaBond™ EX-S2 does not roughen the copper by etching. Instead, nanoscale pitting is produced that provides mechanical anchoring for optimal adhesion performance. The specially formulated organic adhesion promoter acts as a chemical bonding bridge between the copper and the dielectric material. NovaBond™ EX-S2 does not reduce the track height or width, it creates a nano-roughness in the copper surface and, in combination with a special patented silane chemical adhesion promotor, ensures high frequency signal integrity (SI), thermal reliability, and high bonding strength.

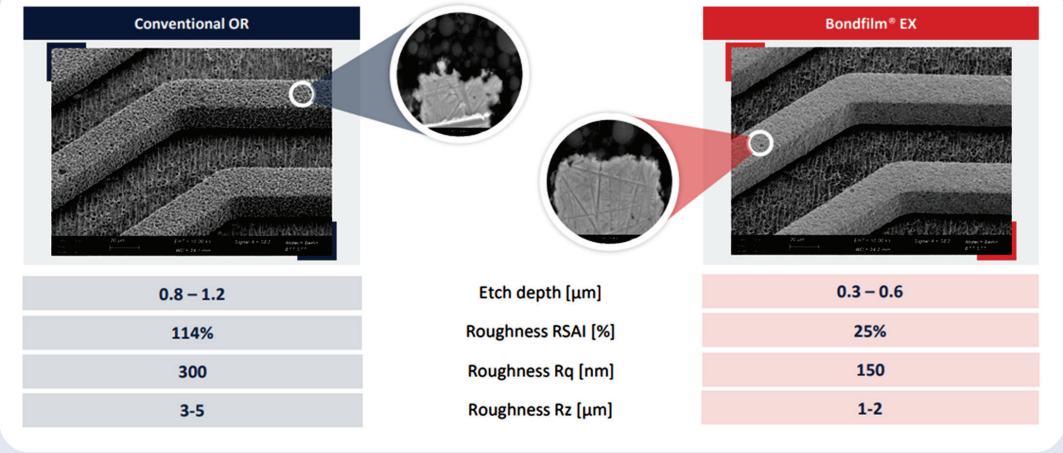


Figure 73. Comparison of surface roughness by AFM.

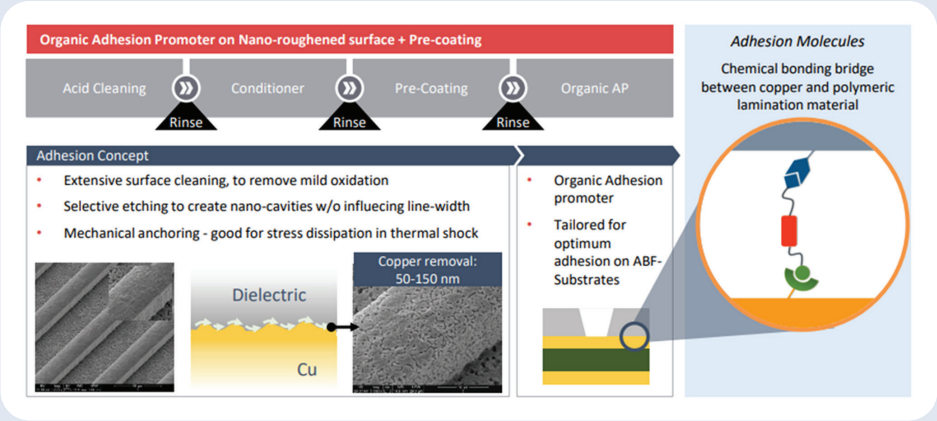


Figure 74. Process sequence of NovaBond™ EX-S2.

4.9 Final Finishing

4.9.1 Why is a Final Finish Needed?

A final finish protects the copper surface on the PCB or package substrate. Copper oxidize, a protective coating, is required that prevents surface oxidation, maintains the solderability of the surface, and allows effective wire bonding to the copper. Various final finishes are available, all of which exhibit specific benefits and limitations. The choice depends on the requirements of the final application and is always a compromise between performance, material properties, and cost. No final finish can fulfill all expectations. Table 4 provides an overview of the most-used final finishes and their key properties and capabilities.

■ = very good
▲ = good
● = sufficient
▼ = limited
◆ = not possible

Atotech Process Name		Aurotech® CNN Aurotec® Plus	Aurotech® HP EPAG	PallaBond® 2,	Universal ASF II Universal Finish SB	Universal ASF® Aurotech® PEP Process	Aurotron B100 Process	Aurotron H200	Stannatech®	OS-Tech® OS-Tech® SIT2			
	Finish type	ENIG Med-Phos.	ENIG High-Phos	EPAG	ENEPIG	ENEPIG	E'lytic Ni/ Au Softgold	E…/ Au Hard-gold	Immersion Sn	Immersion Ag	HT-OSP	HASL
	Phosphorous content Pd-layer	-	-	Pure Pd	Pure Pd	PdP 4-6%	-	-	-	-	-	-
	Typical Thickness [µm]	Ni: 5 Au: 0.07	Ni: 5 Au: 0.04	Pd: 0.1 Au: 0.1	Ni: 5 Pd: 0.1 Au: 0.06	Ni: 5 Pd: 0.1 Au: 0.06	Ni: 7 Au: 0.1-0.5	Ni: 7 Au: 0.3-1	Sn: 1	Ag: 0.3	OSP: 0.25	Sn: 1 – 40
Soldering	Multiple soldering (more than 3 soldering steps)	■	■	■	■	■	■	■	▲	▲	●	■
	Solder spread eutectic solder	■	■	■	■	■	■	■	■	■	▲	■
	Solder spread LF solder	■	▲	■	■	■	■	■	▲	▲	▲	■
	Solder joint reliability eutectic solder	■	■	■	▲	▲	●	●	■	■	■	■
	Solder joint reliability LF solder	▲	▲	■	■	■	●	●	■	■	■	■
Wire bonding	Al-Wire	■	■	■	■	■	●	◆	◆	▼	◆	◆
	Au-Wire	▼	●	■	■	■	■	◆	◆	▼	◆	◆
	Pure Cu-Wire	◆	◆	▲	●	▼	▲	◆	◆	▼	◆	◆
	Cu-Pd-Wire	◆	◆	■	▲	▲	▲	◆	◆	▼	◆	◆
Insertion contact area	For memory card slot	●	●	▼	●	●	▲	■	◆	◆	◆	◆
Key press contact area	For keypads	▲	■	■	■	■	Possible but not used	Possible but not used	◆	◆	◆	◆
Corrosion resistance	Environmental corrosion test (e.g. SO_2 gast test)	●	■	▲	▲	▲	■	■	■	▼	▼	■
Press fit	Pin insertion technology	●	●	▲	●	●	●	●	■	●	●	■
Planarity	For SMD	■	■	■	■	■	■	■	■	■	■	●
High frequency capability	HF applications	●	●	■	●	●	●	●	■	■	■	■
Shelf life	Shelf life before assembly [month]	≥12	≥12	≥12	≥12	≥12	≥12	≥12	12	6	12	≥12

Table 4. Types of final finishes and their key properties.

The requirements for final finish for packaging substrates can be quite different from those in standard PCB applications. The required final finish properties in package substrate applications are driven by decreasing feature size, solder joint reliability, wire bond ability (in certain cases), and process cost. The most common final finishes in package substrate applications are ENEPIG (Electroless Nickel/Electroless Palladium/Immersion Gold), ENIG (Electroless Nickel/Immersion Gold), ISn (Immersion tin) and OSP (Organic Solder Preservative). Internal market studies show that ENEPIG, ISn and OSP are used for more than 90% of the plated area with almost equal shares. ENEPIG, which uses the expensive precious metals palladium and gold as part of the layer, represents more than 90% of the market size by value (Figure 75).

OSP is the final finish that offers the lowest cost option for solderable surface protection. The process is simple, with no metal deposition and easy application. During the assembly process, a flux is used to remove the organic coating, and an intermetallic interphase is produced by the solder and copper which allows a ductile and reliable solder joint to be created. Due to the fine thickness of the organic layer, the protective properties of the coating are limited, and special care is required in handling and storage to avoid defects or scratches. As well, the organic coating cannot fully prevent copper oxidation and after long storage periods the solderability performance can deteriorate.

Immersion tin, ISn, provides highly reliable solder joints with copper. During the assembly process the tin is dissolved into the solder so that an intermetallic compound (IMC) with copper is formed. One of the benefits of ISn over OSP is improved corrosion resistance which produces a more robust final finish.

Compared to OSP and ISn, ENIG and ENEPIG offer the additional benefit of a wire bondable surface finish. While for ENIG this is limited to Al-wire, ENEPIG also allows Au-wire bonding. The additional palladium layer in the ENEPIG finish helps to reduce the brittleness of the solder joint which creates higher solder joint reliabilities.

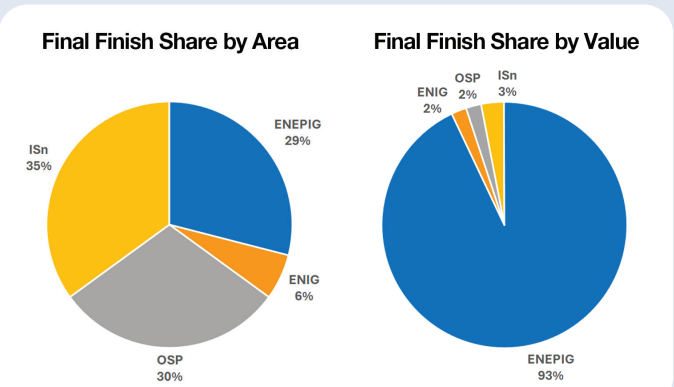


Figure 75. Market shares of different final finishes by area (left) and value (right) in the package substrate industry.

Novel final finishes such as Pd/Au or Au/Pd/Au that can be plated directly on copper have been introduced in the recent years and are gaining market acceptance in packaging applications. They combine the benefit of a solderable and wire bondable finish with a thin nickel-free layer that better accommodates shrinking lines and spaces. Another novel final finish is provided by the use of an autocatalytic tin plating process (ASn). In contrast to immersion tin plating, autocatalytic plating enables greater tin thicknesses and does not restrict tin deposition to plating on copper. Autocatalytic tin plating can be applied on different metals such as nickel or gold allowing the creation of completely new final finish systems.

4.9.2 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)

ENEPIG is one of the three most used final finishes for package substrates. It consists of a nickel, a palladium, and a gold layer in which the palladium layer can be either pure palladium (Pd) or a palladium-phosphorous (PdP) alloy. Metal layer thicknesses vary, with nickel between 4 µm and 8 µm, palladium between 0.03 and 0.1 µm, and gold between 0.05 to 0.1 µm. In ENEPIG as well as in ENIG the nickel acts as a diffusion barrier, preventing the diffusion of copper to the solder alloy which improves the reliability of the solder joints.

The palladium alternatives differ in layer structure and hardness. While pure Pd layers are crystalline, PdP layers are amorphous, with 490 Vickers Hardness, about twice that of pure Pd-layers (250 Vickers Hardness). The softer pure Pd-deposit can achieve slightly better wire bonding performance when combined with low gold thickness [38]. Conversely, the PdP layers exhibit better solder joint reliability in high-speed shear testing as higher total energy values can be achieved [26]. In package applications, it is important to consider wire bonding in decisions regarding which type of Pd-deposit to select for the final finish. Typically wire bonding is done using Au-wire or Cu/Pd-wire.

Important critical defects that are specific for package applications include skip plating on small pads, excessive plating on fine lines and spaces, and peeling of Ni or Pd/Au before or after the wire bonding process.

Compared to the standard PCB process, the ENEPIG process must be modified to provide a reliable and even deposit on small structures (Figure 76). The modifications include a dedicated pretreatment with an activation step that ensures even Pd-seeding and good solution exchange in small structures. The application of mechanical shock during the electroless nickel process is highly recommended for the removal of hydrogen gas bubbles from small structures. Post-dip solutions that are applied after the activation step to de-activate Pd-residues entrapped in small gaps or structures are also available. These prevent excessive nickel deposition in unwanted locations.

Peeling defects that are observed after wire bonding are, in most cases, caused by poor rinsing following the nickel-plating step or by poor copper cleanliness. A pretreatment process that produces a clean and smooth copper surface is recommended to prevent peeling of the nickel layer. Supplier recommendations for water purity and rinse criteria should be followed to ensure a good adhesion between the nickel layer and the Pd/Au layer.

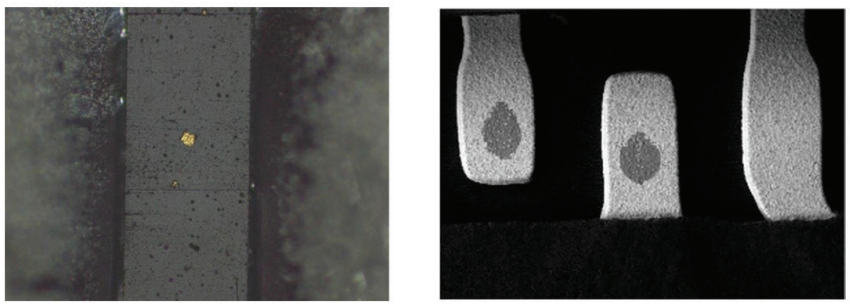


Figure 76. Images of excessive plating in the gap between copper tracks (left) and gold-peeling after wire bonding (right).

4.9.2.1 MKS Products for ENEPIG

MKS offers dedicated process solutions for ENEPIG with pure Pd as well as PdP-deposits on PCBs and package substrates. Aurotech® PEP is the PdP based ENEPIG for PCBs, while for the deposition of pure Pd-ENEIG Universal Finish Solderbond® offers state-of-the-art process solutions. It includes the latest Pd-electrolyte PD-Core® which exhibits an outstanding bath stability and lifetime going along with substantial cost saving potential by low Pd-concentration. In combination with the Aurotech® G-Bond series products for the autocatalytic-dominated deposition, they fulfill the latest industry demands of gold corrosion free deposits with excellent thickness distribution. For package substrates, Universal ASF® (PdP) and Universal ASF® II (Pure Pd) are available as specific process solutions fulfilling all requirements of the package substrate industry including the need for highest reliability and shrinking feature sizes.

4.9.3 Electroless Nickel/Immersion Gold (ENIG)

The lower cost of ENIG compared to ENEPIG (no palladium layer) makes it attractive as a final finish. As with ENEPIG, nickel acts as the barrier layer. However, due to the greater brittleness of the solder joints formed with ENIG and the stronger risk of hyper-corrosion, its use in package substrates is comparatively low.

ENIG layers typically consist of a nickel layer of 3-8 µm and a gold layer of 0.03 to 0.1 µm. ENIG layers are applied for soldering applications only. The gold process which is applied in ENIG or even ENEPIG plating can be characterized as three different processes:

1. **Immersion gold:** the process involves full immersion, and electrons are provided by the dissolution of nickel only (e.g.: MKS Aurotech® SF Plus).

2. **Mixed reaction gold (type 1):** the process employs an immersion reaction supported by additives with reducing properties (e.g.: MKS Aurotech® DC CH).

3. **Mixed reaction gold (type 2):** the gold electrolyte contains reducing agents and the process is a mixed reaction which starts with an immersion reaction and becomes autocatalytic as soon as the first gold seedings are plated (e.g.: MKS Aurotech® G-Bond series).

Mixed reaction gold electrolytes offer the benefit of reduced corrosion of the electroless nickel layer. With mixed reaction gold electrolytes having autocatalytic properties, corrosion-free ENIG layers can be deposited, and greater gold thicknesses can be achieved. In those cases, requiring thicker gold layers, the gold plating step is often referred to as AG, autocatalytic gold.

Typical defects encountered in ENIG plating include skip plating or excessive plating, similar to what is observed with ENEPIG. Countermeasures to prevent these defects are comparable to those used in ENEPIG: they focus on pretreatment to provide an even and homogeneous Pd-seeding during the activation step, an optional post-dip solution to remove/de-activate Pd-residues, and finally a tailored Nickel-plating solution with a good solution exchange and wetting properties in small features. Mechanical shock may also be applied to support the removal of entrapped hydrogen bubbles in small, high aspect ratio features.

4.9.3.1 MKS Products for ENIG

For ENIG plating, MKS offers a wide range of process solutions combined under the name of Aurotech® Plus. This includes specific cleaner and pretreatment solutions such as ProSelect® CT Plus as dedicated cleaner to prevent appearance defects caused by base material leach out, Coppertreat® 800 to provide a smooth and even copper surface, and Aurotech® ACT RE as low Pd-activator to ensure homogeneous Pd-seeding and prevent excessive plating. For Nickel-plating, Aurotech® NIC and Aurotech® NIC 2 are available for the defect free plating on PCBs and even on critical base materials used for high-speed applications. For gold deposition, either immersion dominated processes such as Aurotech® DC CH or Aurotech® AU Plus CH or autocatalytic dominated process such as Aurotech® G-Bond 2 or Aurotech® G-Bond 3 are available, ensuring fully corrosion free ENIG deposits.

4.9.4 Nickel-free Precious Metal Finishes: Electroless Palladium/Autocatalytic Gold (EPAG), Gold/Palladium/Gold, Direct Immersion Gold (DIG)

Nickel-plating can be incompatible with fine lines and spaces due to the nickel layer thickness of 4-6 µm. To overcome this limitation, nickel-free finishes have been introduced that are solderable and wire bondable. These finishes use palladium and/or gold directly on copper. The process flow requires activation steps that are tailored to the palladium deposition to prevent excessive attack of the copper track. Target thicknesses for the palladium and gold layers are 0.1 µm. These finishes are solderable and wire bondable and are capable for SIT (second image technology) as well. Owing to the lack of nickel as a barrier layer, these finishes have a potential risk of copper migration after long times or thermal storage. Good layer homogeneity is essential to provide reliable surface protection and therefore, an even appearance after aging or a hot water dip (60°C, 5 min) is required. This can be achieved by the application of dense palladium layers such as PD-Core®, that mitigate the copper migration and reduce the risk for

discoloration [27]. The palladium plating electrolytes used for EPAG or Au/Pd/Au deposits are electroless, with a reducing agent added to enable palladium deposition. Gold deposition typically employs a mixed reaction gold electrolyte. To prevent corrosive attack to the underlying copper, gold electrolytes with high autocatalytic properties are recommended. Nickel-free precious metal finishes show additional benefits in high frequency applications, as they have a negligible effect on the signal transmission.

4.9.4.1 MKS Products for EPAG

With PallaBond® 2, MKS offers a very versatile process solution for EPAG deposits as the palladium electrolyte as well as gold electrolyte can be used in EPAG, ENEPIG and ENIG plating. It includes the use of a versatile acidic cleaner ProSelect S8, a mild microetch SoftEtch and a dedicated activator step Activator HE which can be used for EPAG as well as for ENEPIG and ENIG. With the Pd-Electrolyte PD-Core®
a low Pd-content process is available which exhibits an outstanding bath stability and robustness to keep the handling as simple as possible.

4.9.5 Organic Solder Protection (OSP)

Organic solder preservative (OSP) is a non-metallic finish that consists of an organic layer based on benzimidazole derivates. OSP acts as a protective coating during the storage of the unassembled substrate. In the assembly process the organic coating is dissolved and removed using a flux and a solder joint and intermetallic phase is formed between the copper and the solder alloy. The copper surface remains solderable after OSP processing but does not provide a wire bondable surface. OSP processes are simple and quick and offer surface protection at low cost. As the solder joint is formed with copper directly, the solder joint reliability is high and high forces and solder joint ductility can be achieved. Nevertheless, the protective properties are limited when it comes to long-term storage or thermal exposure since the organic layer cannot fully protect the copper from oxidation. After several reflow cycles or thermal exposure, copper oxides can be formed, and this can impact the solder joint reliability of the substrate as shown in Figure 77, image of substrate after thermal aging for 4h at 160°C.

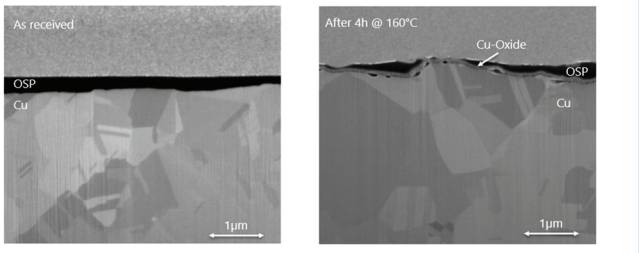


Figure 77. FIB cut of the organic coating before and after thermal aging.

OSP processing can be combined with ENIG or ENEPIG in Second Image Technology (SIT, Figure 78). In this process two different final finishes are applied on one substrate/PCB. In a first process step the copper tracks and pads which are supposed to be plated with OSP are covered with a dry film (SIT Mask). After that the panels are processed through the ENIG or ENEPIG process and the Nickel/Gold or Nickel/Palladium/Gold layer is applied, the dry film mask is stripped, and the panels are processed through the OSP line. In this process it is important that the organic coating is selectively deposited on the copper pads and does not interact with the ENIG or ENEPIG finish. Dedicated OSP electrolytes are available that ensure selective deposition and prevent excessive attack on the non-copper surfaces.

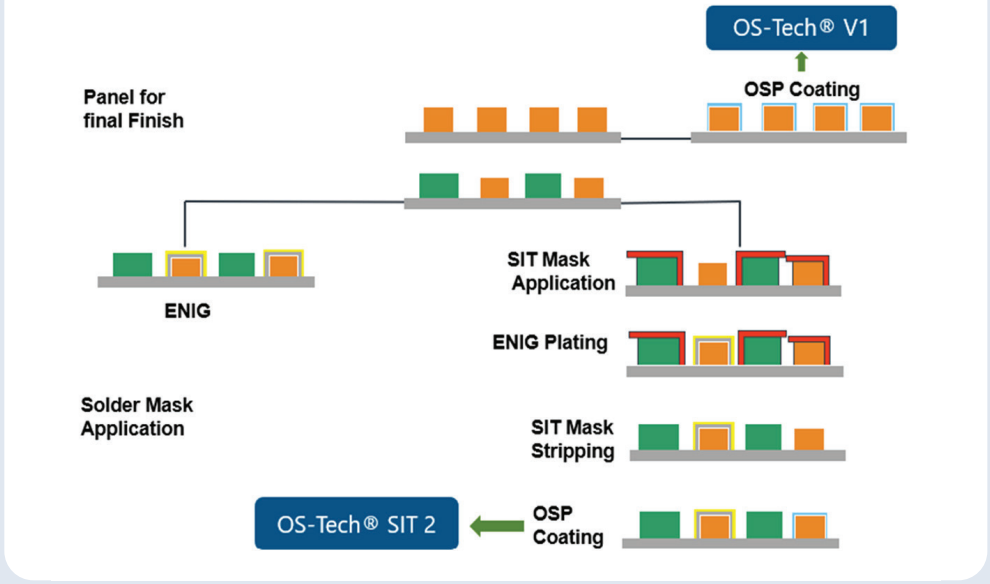


Figure 78. SIT Process sequence for ENIG and OSP on one substrate.

4.9.5.1 MKS Products for OSP

MKS offers two types of OSP processes: OS-Tech® and OS-Tech® SIT 2. While OS-Tech® is limited to the plating on copper only, OS-Tech® SIT 2 is capable for SIT processing as well and deposits selectively on copper even in the presence of ENIG or ENEPIG plated pads.

4.9.6 Immersion Tin (ISn)

Immersion tin is a mature final finish which has been used in the PCB industry for many years. ISn layers exhibit outstanding corrosion resistance that outperforms all other final finish types, and it is used extensively in the automotive industry. In the ISn process, tin is deposited by a replacement reaction where the electrons which are required for the tin deposition are provided by the dissolution of copper. Thiourea is added to the plating solution to lower the electrochemical potential of copper, allowing this exchange reaction to occur even though copper is more noble than tin. During assembly, a Cu6Sn5 and Cu3Sn intermetallic phase is formed between the copper and the solder alloy. After two reflow cycles, the free tin is mostly consumed, and only small islands of tin remain at the tin layer surface. The surface is covered by a few nanometers thick tin oxide layer. This produces reliable and ductile solder joints with the best solder joint reliability even after thermal aging. The achievable layer thickness is limited since the reaction slows down with increasing tin thickness. Typically, a thickness of 1.3 µm or higher is targeted for package applications.

High cleanliness and proper process control are mandatory for the creation of good solder joints and solder wetting performance of the tin layer. Contaminations that impact the solder joint or tin plating can have three root causes:

1. Contamination on copper caused by previous process steps such as the solder mask application. As an example, residue can remain from the developer if it is not replaced according to supplier recommendations.

2. Contaminants that are co-deposited during the tin plating process. These can be organic components that are leached into the plating solution from base material or solder mask. UV-treatment of the panel to allow complete cross linking of the organic components is recommended before the panel enters the tin plating process.

3. Contaminants that evaporate and re-deposit on the tin layer during the assembly process. To prevent this, proper solder mask application must follow the technical recommendations of the supplier as well as UV-treatment prior to tin plating.

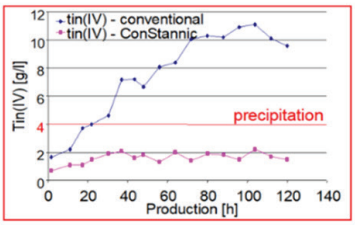
Most observable soldering defects in immersion tin layers, such as melting/non-melting of the tin surface after reflowing or missing bump defects, can be correlated with contamination during the plating process or the assembly. These defects can impact the stability of the tin oxide that leads to inhomogeneities that can cause oxide layer cracks during the assembly process. Such cracks can allow liquid tin to reach the surface producing an uneven appearance. Contaminants that are incorporated during the plating process can lead to uneven IMC formation which results in uneven solder wetting during assembly. Finally, any contaminants remaining on the copper surface before tin plating may inhibit tin deposition and lead to skip plating in single areas. To prevent contamination-related failures, copper cleanliness and rinsing are key criteria for the immersion tin plating process. For package applications, acceptable cleanliness can be achieved through automated control of the horizontal equipment and optimized flow and rinsing conditions in the plating and rinsing modules.

4.9.6.1 MKS Products for Immersion Tin

With Stannatech® 2000 MKS offers a market leading immersion tin process dominating the PCB as well as the package substrate market. Stannatech® 2000 is characterized by a high process robustness and final finish reliability and is widely accepted by all major OEMs in the related industries. With Stannatech® 2100 for PCB and Stannatech® IC for package substrates, two new processes are entering the market which exhibit a lower plating solution viscosity leading to improved rinsability with a reduced risk of soldering defects or missing bump failures. Additional post-treatment solutions such as Tin PostDip 2020 complete the latest full process portfolio.

4.9.7 Horizontal Immersion Tin Equipment

The MKS Horizon Stannatech product line is a high-volume manufacturing system for horizontal immersion tin processing. The systems for fluid exchange on the PCB or package substrate are process-specific, but have one thing in common, a patented feature that enables uniform fluid exchange across the entire PCB width. As a result, the entire surface is treated evenly. The main module, the Immersion Tin bath, uses auxiliary devices (ConStannic and Crystallizer – Figures 79, 80, 81) that automatically regenerate the bath chemistry to maintain constant process parameters. This results in higher yields while simultaneously minimizing the consumption of water, chemicals and energy.

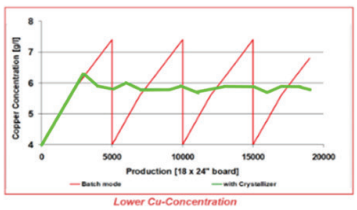


ConStannic:

Continuously reducing of Tin (IV):

- Reduce the amount of slurry in the modules
- Reduce the risk of EQ problems (uneven drive, blockages, etc.)
- Reduce the risk, which could affect the quality on
  - Appearance
  - Wettability
- Control the deposition speed of ImTin

Figure 79. ConStannic concept to prevent SnIV-precipitation.

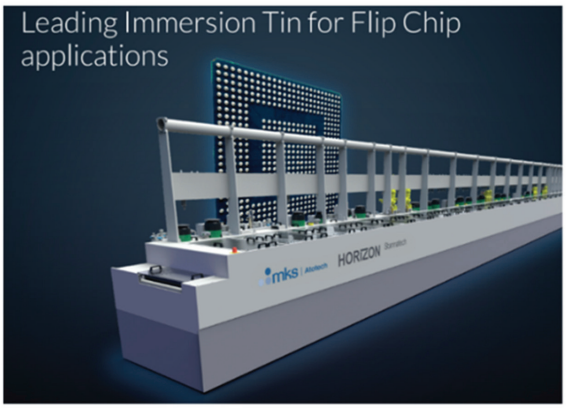


Crystallizer:

Continuously removing of Copper:

- Reduce the risk of rinsing problems in the first rinse after ImTin bathes caused by copper re-deposition, which could affect the quality on:
  - Appearance
  - Wettability
- Control the deposition speed of ImTin

Figure 80. Crystallizer concept to maintain constant copper content.



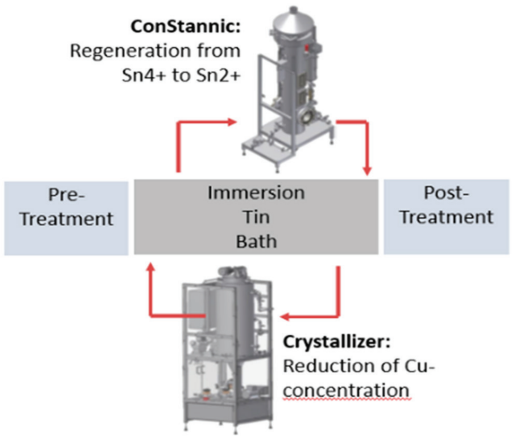


Figure 81. General concept of auxiliary equipment for constant process conditions.

Rinsing performance strongly impacts process success, especially in the post treatment area of the Immersion Tin Line. To deliver both effective rinsing performance and efficient material and energy use, the rinsing modules need to be designed for optimal and efficient use of rinse water in each rinsing cascade. Cascade rinsing technology achieves this goal by reducing the total consumption of water while maintaining the targeted rinsing dilution factor during the final rinsing step. The formula and table in Figure 82 shows that with a Quadruple Rinse, more than 50% of rinse water can be saved compared to a Triple Rinse configuration.

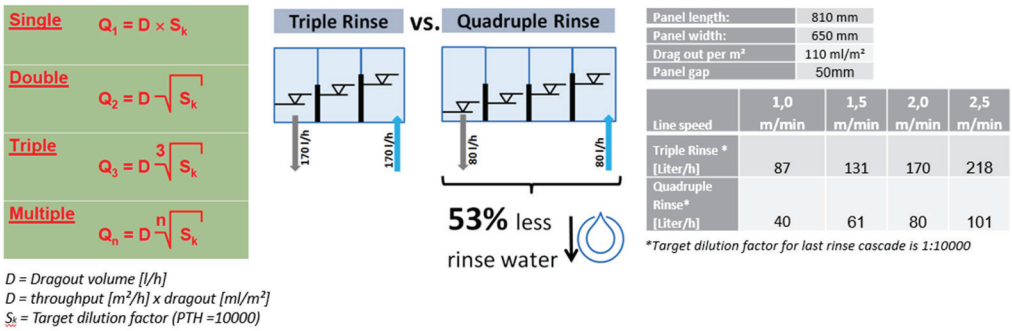


Figure 82. Water saving concept of quadruple rinsing.

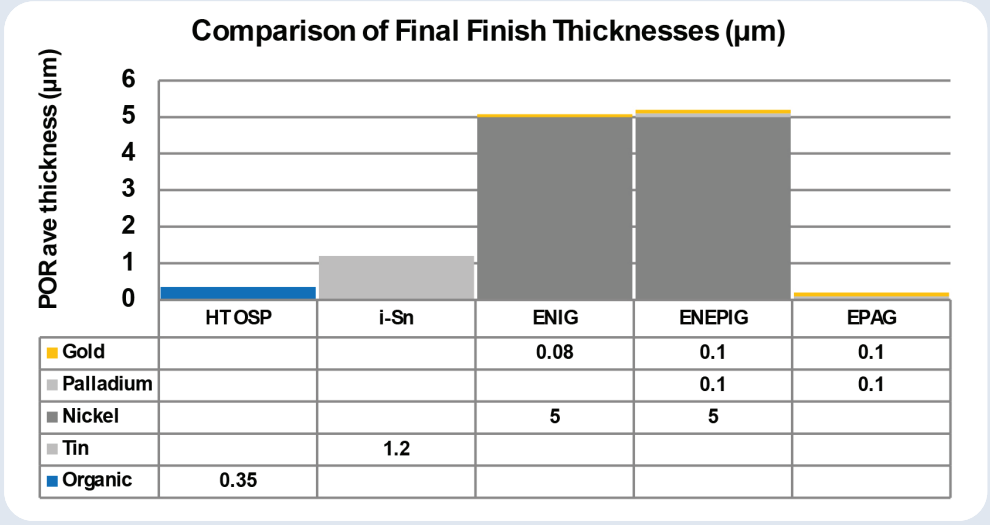
4.9.8 Requirements for Final Finishes in the Package Substrate Industry

The different design and scale of IC substrates means that the final finish must fulfill requirements well beyond those that are typical of printed circuit board applications:

- Decreasing structure sizes lead to the need for finer line and space capabilities
- High solder joint reliability with ductile and strong solder joint formation
- Good solder coverage, no missing solder or solder wetting defects
- Thermal resistance and good resistance towards harsh environment
- Capable for second image technology, a combination of two final finishes like ENIG or ENEPIG with OSP on one surface

Fine Lines and Spaces

With the decreasing pitch sizes and lines and space (L/S) in the substrate design, the fine line capability of the final finish becomes crucial. This includes the capability to deposit a finish on a fine structure with small lines and spaces without leading to shorts or excessive plating, and also to deposit the finish on pads or BGA structures with small pad diameters. While in the first case excessive plating of the deposit needs to be prevented, in the second case a good solution flow needs to be ensured to allow for an efficient solution/ion exchange at the plating interface. With respect to excessive plating, the fine line capability of the process is defined by two factors: a) the overall plating thickness of the deposit, and b) the risk for excessive plating in unwanted areas. The lowest gap loss is provided by those final finishes with an overall low coating thickness.



	HTOSP	i-Sn	ENIG	ENEPIG	EPAG
Gold			0.08	0.1	0.1
Palladium				0.1	0.1
Nickel			5	5	
Tin		1.2			
Organic	0.35				

Figure 83. Comparison of the final finishes with respect to thickness after Process of Record (POR) layer deposition.

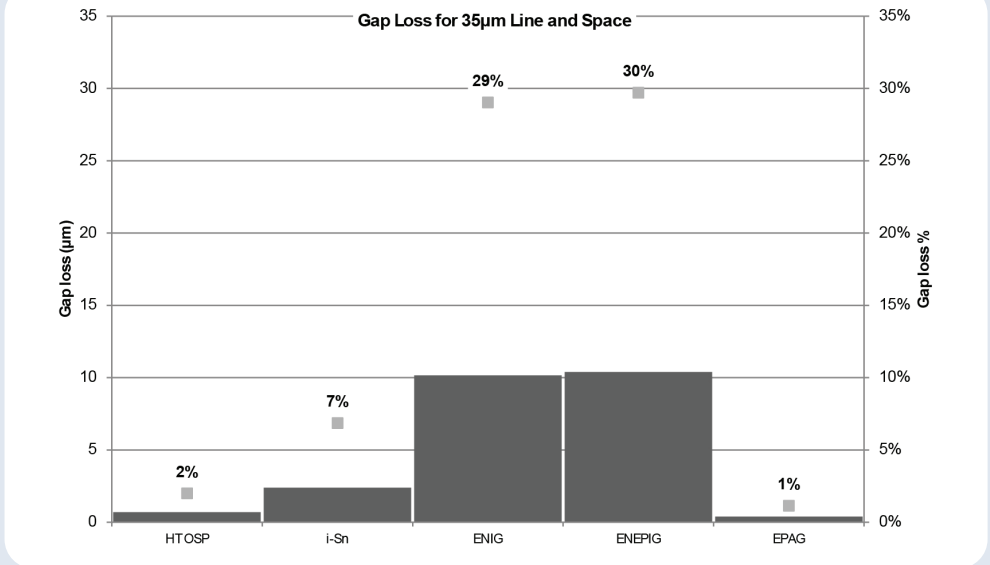


Figure 84. Gap losses of the finishes at typical layer thicknesses [25].

Figure 83 and Figure 84 visualize the comparison of the layer thickness of the different final finishes and the connected gap loss which affects the fine line capability. The lowest gap loss can be provided by EPAG and OSP which differ significantly in the assembly capability. While OSP offers only a protection layer that does not interact in the assembly process, with EPAG a solderable and bondable finish is available that protects the copper surface and at the same time interacts in the solder joint and wire bond connection.

With final finishes that contain nickel, the risk of excessive plating in fine lines and spaces is increased due to the higher layer thickness. For these processes the plating process can be modified by using additional additives or post dip solutions that remove or de-activate Pd-seeding in gaps or on base material, preventing nickel growth in these areas.

Solder Joint Reliability

The solder reliability of the surface finish is determined by the intermetallic phase formed between the surface and the solder alloy. Studies of solder joint reliability by high-speed shear testing show that surface finishes in which an intermetallic phase is formed with copper can achieve higher total energies compared to nickel-containing final finishes [28]. In High-Speed Shear testing, solder balls are attached to a ball grid array structure and sheared off at high speed. The shear force and total energy of the ball removal provides information on the solder joint reliability. The investigation of crack formation also provides information on the ductility of the solder joint, depending on whether the crack is located in the IMC or the solder ball. To evaluate the impact of thermal exposure during assembly and back-end processing in package substrate applications, final finishes were investigated under two different conditions:

- As-received - solder balls attached on the surface finish and reflowed
- Pre/post aged: plating→baking for 2h @ 175°C, 5 min DI-water @ 60°C→ball attachment →120h @ 60°C/60% RH, 5x reflow

The shear speed was adjusted to 0.9 m/s to achieve the widest possible spread across all possible fracture modes. In the as-received condition, the mean total energies of the solder joint are comparable for the final finishes that form the IMC directly with copper. When nickel is involved, the total energy is lowered. The palladium layer in ENEPIG finishes helps to maintain the solder joint strength, however, the strongest degradation of total energy is observed for ENIG layers. This situation changes in the aged condition. A significant drop in performance can be observed for the OSP coating that is mainly due to thermal pre-aging that accelerates copper oxide formation on the coated pad. Also, the nickel-containing finishes exhibit significant performance losses. ISn and EPAG are nickel-free solutions that can outperform all other finishes with regard to reliability of the solder joint. They provide the best energy values and most ductile fracture behavior in this direct comparison. Therefore ENEPIG, ISn and EPAG are the first choices in final finishing for package substrates.

Solder Wetting (Missing Bump and Melting/Non-Melting)

Another important aspect for soldering is the solder wetting performance which determines how well the liquid solder spreads on the pad surface. Possible failures are “non-wetting” or “de-wetting”. In the first case the solder does not spread on the surface while in the second case it contracts from the pad edges. Typical solder wetting defects in package substrate applications are the so-called “missing bump” effect or “melting/non-melting” that can be observed on e.g., ISn-plated substrates. Figure 85 shows the backend process flow after the immersion tin plating and the missing bump effect. This effect is related to the solder wettability of the immersion tin surface. A possible root cause for poor solder wetting of the tin surfaces is contaminations in or on the tin layer. This can be caused by:

- Poor copper cleanliness due to previous process steps causing defective immersion tin layer.
- Poor rinsing conditions in the immersion tin plating process leaving chemical residues in gaps.
- Poor cross-linking in the solder mask application causing volatile components to leach out during the plating process and co-deposit or evaporate during reflow.

All of these potential contamination issues can cause irregularities in the immersion tin layer that produce poor solder wetting performance.

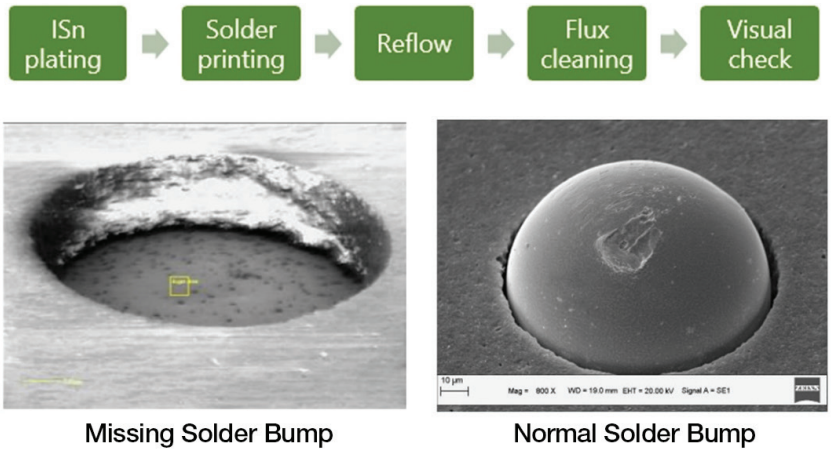


Figure 85. Process after ISn plating and missing bump effect.

Another related defect is the "melting/non melting" defect (Figure 86). This defect is defined as any dark or shiny areas on the tin surface following the reflow cycle. This effect is caused by inhomogeneities in the tin-oxide layer that are formed during the reflow process on the unassembled side. Potential contamination as described above leads to uneven formation of the tin-oxide layer, producing weak spots that crack during the reflow process allowing liquid tin to reach the surface [29].

To prevent the missing bump or the melting/non-melting defect, key focus must be put on good copper cleanliness, good rinsing performance in the plating line, low viscosity of the tin plating process, a good solder mask process, and additional UV-bump to ensure sufficient cross-linking of the organic components in the solder mask. This can be achieved by dedicated flooding devices in the horizontal equipment that ensure best fluid delivery and exchange.

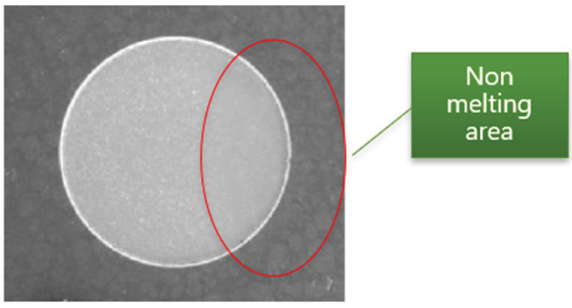


Figure 86. BGA-Pad coated with immersion tin showing melting/non melting defect.

4.9.9 Second Image Technology

In some cases, a combination of different final finishes makes sense to take advantage of the specific properties of the different layers. Typically, this process, also known as Second Image Technology (SIT), combines the OSP finish with ENIG or ENEPIG. SIT has special requirements for the individual plating processes involved. The typical process flow includes the process steps shown in Figure 87.

Figure 87. Process flow in SIT process.

ENIG and ENEPIG plating processes require compatibility of the SIT dry film so that the coating is not attacked by the electroless nickel, electroless palladium or the gold plating process. Once the dryfilm is removed, the OSP must be selectively deposited on copper only and not attack the ENIG or ENEPIG coated pads. Additionally, the deposition needs to be independent of the potential electrical connection of the copper pads to ENIG or ENEPIG plated pads as this connection can produce galvanic effects that impact the OSP deposition. Figure 88 shows the results of an electrochemical study in which a conventional OSP process (OS-Tech®) was compared to an OSP process for SIT applications (OS-Tech® SIT 2). The graph shows the current density measured on copper pads connected to ENIG plated pads when immersed to the OSP solution. To evaluate the impact of the Cu/ENIG area ratio on the deposition, different ratios were compared. The columns in blue represent the results for the conventional OS-Tech® while the orange columns show the results for the dedicated OSP for SIT plating. The graph clearly shows that a specific OSP solution is recommended to ensure a homogeneous deposit when combined with ENIG or ENEPIG coating.

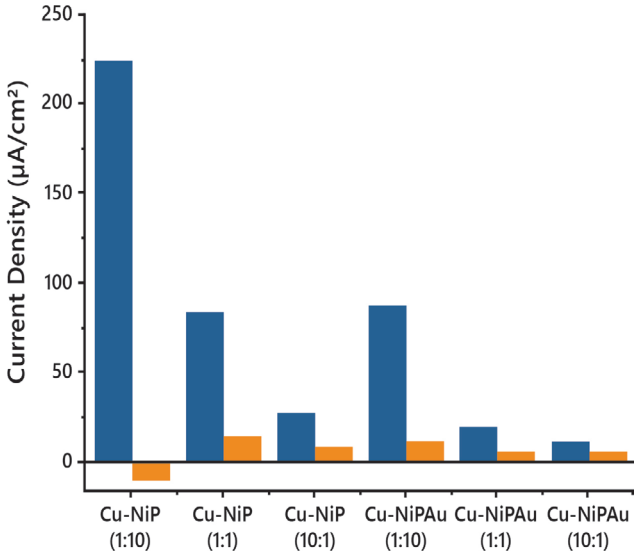


Figure 88. Electrochemical current density measurement to evaluate the galvanic effect in different OSP solutions (blue: standard OSP, orange: OSP for SIT applications).

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Chapter 5

Flip Chip Packaging and Assembly

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5.1 Introduction

Flip Chip (FC) is an advanced technology used to create Surface Mount Devices (SMDs) for Surface Mount Technology (SMT) assemblies that was developed to facilitate shorter power and signal trace lengths. It was introduced in the semiconductor industry around 1995. In FC technology (Figure 1 and Figure 2), the semiconductor chips are flipped so that the active side is bonded to an IC substrate interposer, or, in the case of COB (Chip on Board), as a Fan-In Wafer Level Chip Scale Package (FI-WLSCP) bonded directly to a Printed Circuit Board (PCB). Prior to the introduction of FC Technology, wire bonded SMDs (Figure 3) dominated SMT for active devices. FC Technology exists in parallel with wire bond technology and respective SMDs having ceramic, metal leadframe or organic laminate interposers. It has smaller package form factors (despite higher I/O counts) with I/O arranged in a matrix similar to the Ball Grid Array (BGA) of the package itself, but with much smaller bumps and finer pitches. Unlike bond wire, FC bumps have two functions: the electrical connection of the die pads to the substrate pads, replacing the bond wire; and the mechanical connection of the die to the substrate, replacing the adhesive materials or die backside soldering or sintering used in wire bond packages. FC technology is used for applications with different requirements in terms of electrical, thermal, and thermo-mechanical performance, form factor, integration capability, and cost. The drivers and reasons for developing FC technology are discussed in this chapter.

Figure 1. Flip Chip Package Outline (FCBGA). (Source: Amkor Technology Inc. ©2025)

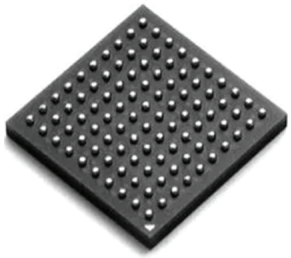


Figure 2. Flip Chip Package Outline (FI-WLCSP) [2].

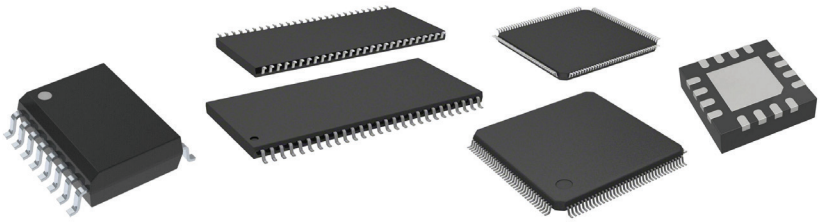


Figure 3. Wire bonded Surface Mount Devices with Gullwing-Leads and without leads. (SOIC – Small Outline Integrated Circuit, TSOP - Thin Small Outline Package, LQFP – Large Quad Flat Package, and TQFN – Thin Quad Flat No-Leads)

Chapter 8, Section 7 of the Heterogenous Integration Roadmap (HIR) states: "Flip Chip continues to grow across multiple package platforms as higher package pin counts and performance are needed (Table 1). Today's applications are driving unique ways of organizing advanced semiconductor system solutions. System on a Chip (SoC), once the preferred design layout option, has shifted towards best-in-class silicon to achieve optimal cost/performance. The alternative to SOC is to look for ways to heterogeneously integrate key portions of the design into a close side-by-side configuration that can leverage optimized silicon nodes for portions of the design. As part of heterogeneous integration, the interconnect of the die also becomes critical because the inductance of the lines, connecting each subsystem, can significantly impact performance. Interconnect pitch, size, metallurgy and even substrate technology can play a critical role in ensuring that a design can meet necessary high-performance standards. This section will concentrate on the key challenges and considerations for flip chip when looking at how best to leverage heterogeneous integration." [1]

Bn units	2022	2023	2024F	2028F	2023/ 2022	2024F/ 2023	CAAGR 2023-2028
Flip Chip QFN/MIS	5.8	6	6.5	7.2	3.4%	8.3%	3.7%
Flip Chip SiP on Laminate[1]	8.9	9.1	9.6	14.5	2.2%	5.5%	9.8%
Flip Chip CSP	6.5	5.6	6	8.5	-13.8%	7.1%	8.7%
3D Stacking HBM	0.02	0.04	0.08	0.2	66.7%	100.0%	35.2%
Flip Chip CSP for DRAM	8.9	8.5	10	12.5	-4.5%	17.6%	8.0%
FCBGA[2]	1.6	1.3	1.3	1.6	-20.4%	2.0%	5.2%
WLCSP	42.5	42.8	43.4	54.0	0.7%	1.4%	4.8%
FO-WLP/PLP[3]	1.3	1.4	1.5	1.7	7.2%	5.1%	4.6%
2.5D (Client Computing)	0.000	0.003	0.010	0.067	NA	296.2%	91.4%
2.5D (Server/Networking/ASIC)	0.003	0.005	0.010	0.019	63.3%	100.0%	30.4%
HD-FO[4]	0.003	0.003	0.005	0.029	14.3%	57.4%	53.6%
COF/COG	13.5	12.7	12.9	14.5	-5.9%	1.4%	2.7%
Subtotal Flip Chip	***89.0***	***87.4***	***91.3***	***114.9***	***-1.8%***	***4.4%***	***5.6%***
Subtotal Wire Bond	243.8	234.8	237.8	266.8	-3.7%	1.3%	2.6%
IC TOTAL	**332.8**	**322.2**	**329.0**	**381.7**	**-3.2%**	**2.1%**	**3.4%**

1. *RF PA, Connectivity, and Power*
2. *Excluding the FCBGA of HD-FO / 2.5D*
3. *Includes low density and mid-density Fan-Out Package*
4. *HD-FO: High-Density Fan-Out packaging, includes FO-MCM and FO with embedded bridge*

Table 1. Flip Chip IC Package Unit Growth (Source: Prismark 2023).

5.2 Major Parameters, Advantages and Disadvantages of Flip Chip

5.2.1 Parameters

The leading Outsourced Semiconductor Assembly and Test (OSAT) service provider of packaging, assembly and test solutions, ASE Group, describes this package type as follows:

"Flip Chip derived its name from the method of flipping over the chip to connect with the substrate or leadframe. Unlike conventional interconnection through wire bonding, flip chip uses solder or gold bumps. Therefore, the I/O pads can be distributed all over the surface of the chip and not only on the peripheral region. The chip size can be shrunk, and the circuit path optimized. Another advantage of Flip Chip is the absence of bonding wire reducing signal inductance." [2]

The major parameters of Flip Chip components for SMT assemblies (Figure 4) are:

- Underbump Metalization (UBM) pad size
- Bump pitch
- Stand off once assembled (determied by bump diameter)

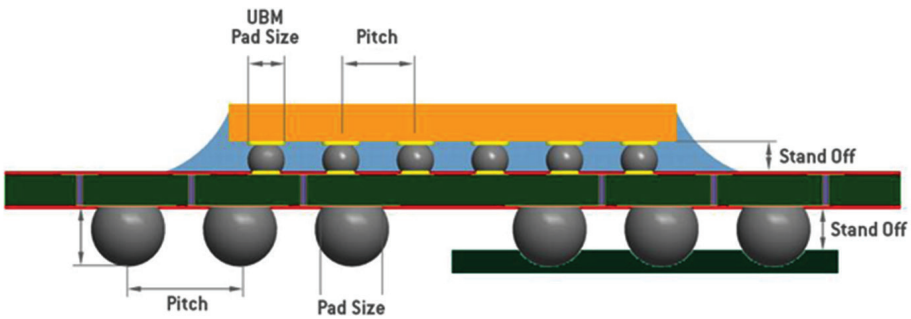


Figure 4. Cross section and basic parameters of Flip Chip on IC substrate [12].

Other parameters such as die size and thickness, which often define the need for underfill, are also important.

Wafer preparation, known as Wafer Bumping, is a critical process in Flip Chip packaging. Wafer bumping is an advanced packaging technique where, depending on required size and pitch, bumps, microbumps, or balls made of solder are formed and reflowed on the wafers before being diced into individual dies. For very small pitches and high I/O count, copper pillars (CuP) with SnAg caps are used. Those are typically processed in the wafer fab or in advanced wafer level packaging facilities of OSATs.

Some typical parameters of FC components for SMT assemblies are shown in Table 2. The number of I/O's can vary between around 16 (absolute minimum is 3-4) and 2,500 bumps, depending on die size and bump pitch. Mainly due to reliability reasons, package sizes which used to be relatively small

	I/O	Package Size (mm)	Substrate	Ball Pitch (mm)
Ceramic Chip Scale Packaging (CCSP)	16 - 200	4 x 4 - 14.0 x 22.0	2/4 Layer Laminate	0.8 - 1.00
Ceramic Flip Chip Ball Grid Array (CFCBGA) / Pin Grid Array (PGA)	< 1556	27 x 27 - 49.5 x 49.5	Ceramic	0.8 - 1.27
Flip Chip Ball Grid Array (FCBGA)	100 - 1521	27 x 27 - 40.0 x 40.0	2/4 Layer Laminate 4 -8 Layer Build-up	1.0 - 1.27
Hybrid Flip Chip Ball Grid Array (HFCBGA)	256 - 2401	12 x 12 - 52.5 x 52.5	4 -8 Layer Build-up	1.0 - 1.27

Table 2. FC capabilities of leading OSATs today [2].

(e.g., 4 mm x 4 mm) have increased in size, up to >50 mm x 50 mm, in the last two decades. This has been enabled by advances in bump alloys, pad designs, UBMs and underfill materials. An interposer can be an organic laminate substrate with different build-ups (e.g., 2/4 Layer or 4/8 Layer) or ceramic, depending on the FC package type.

Chips must be designed for FC assembly. A BEOL process in the wafer fab needs to provide FC pad locations and sizes in the last metal layer that are suitable for the later bumping and FC assembly processes. If this is not provided, a thin-film RDL and UBM can be applied on the chip surface to achieve the required FC bond pad layout (Chapter 6 – WLP processes). Unlike wire bond pads, which are typically located on the periphery or as bond pad rows in the center spine of a chip, FC bond pads are arranged as a fully or partially populated array on the complete or partial chip surface, depending on the design and functionality requirements.

If the active area of the die (circuitry and pads) is required on top of the assembled die, Through Silicon Vias (TSVs) can be applied to move the bump pads from the active side of the die to the backside. This needs to be done in Chip-Package co-design and processed in the wafer fab (via first and via middle). Only the via last process can be applied in the OSAT as well, but also needs design features in the chip that allow contacting the circuitries bond pads from the backside. This is different to the standard wafer manufacturing process with Backend of Line (BEOL) to be placed in the first metal layers processed during wafer manufacturing.

5.2.2 Advantages and Disadvantages

The replacement of bond wires by bumps has certain key advantages, but also some disadvantages.

5.2.2.1 Advantages

- Shorter assembly cycle time (die attach and electrical connections in one pick-and-place step)
- Batch processing of electrical interconnects for Flip Chip packages (e.g., bumps, copper pillars)
- Good electrical performance with lower package parasitics (mainly inductance and crosstalk)
- Shorter path between die and substrate improves the electrical performance
- Higher signal density possible
- Smaller package size (footprint and height) possible
- Higher I/O count and I/O density due to area array pad layout
- Direct thermal dissipation path through the bumps
- External heat sink can be directly added to the chip backside to remove the heat
- Absence of wire (and in some variants also molding) allows for lower package profiles
- Self-alignment of FC package bump pattern to corresponding substrate pad pattern

5.2.2.2 Disadvantages

- Requires wafer preparation process steps (e.g., UBM and bumping, RDL and bumping)
- Requires a more complicated wafer singulation process (bumps on the wafer surface)
- There are die size limitations due to CTE mismatch between silicon and IC substrate/PCB
- Thermo-mechanical bump or copper pillar reliability impacts electrical function
- To improve thermo-mechanical reliability, an additional underfill process might be needed
- Manufacturing yield and reliability issues are observed
    - Thermal cycling solder joint fatigue, especially if no underfill is used
    - Viscosity of underfill material changes with time, process results may vary
    - In fine-pitch bumping, solder flux gets trapped and is very hard to clean (corrosion, voids)
    - Visual verification of FC bump position and solder quality difficult, especially after board mounting (automotive requirement)
    - FC packages present test problems after board mounting with respect to solder joint integrity. Voids in the joints may lead to reliability issues in the field.

The double function of the bumps, being an electrical and mechanical connection at the same time, has an impact on reliability, especially for larger die sizes. The matrix arrangement of bumps on the die makes them sensitive to CTE mismatches between die and interposer where they must function as a stress buffer. A small delamination of a die attached by, e.g., adhesive, does not cause electrical failure. A broken

bump does. In contrast, the flexibility of wire bonds (spring effect as stress buffer) provide the capability to manage CTE mismatch between die and IC-substate/PCB. Wires can also compensate for inaccuracies in die placement or interposer manufacturing since they are placed sequentially one-by-one between die pad and substrate pad following their actual position.

To overcome these disadvantages, underfill processes (e.g., CUF – Capillary UnderFill) have been introduced that use specially developed underfill materials. The CUF process is sequential, time-consuming, and expensive. Therefore, OSATs usually try to avoid using CUF whenever possible and when agreed to by the customer, typically following proof of reliability for the respective application. If the component gets an encapsulation, an underfill is required to avoid air getting trapped under the die which can lead to pop-corn during temperature load or short circuits between bumps due to embedded moisture. Mold underfill (MUF) is a promising replacement for CUF in which mold compound is used for underfill during the encapsulation process. It is not sequential, occurring simultaneously with the encapsulation process for all dies on the interposer. The cost for MUF is high, however, as it requires fine-filler mold compound which is much more expensive than standard mold compounds.

5.3 Varients of Flip Chip Packages

5.3.1 Flip Chip CSP

FCCSP (Flip Chip Chip Scale Package) offers chip scale capacity for I/O counts around 200 or less. FCCSP provides better protection for chips and better solder joint reliability compared with direct chip attach (DCA) or chip on board (COB). FCCSP is superior to Known Good Die (KGD) in low-cost test and burn-in and has electrical performance comparable with KGD. FCCSP features a thin and small profile, and lightweight packages (Figure 5).

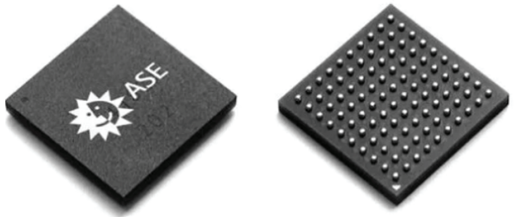


Figure 5. FCCSP by ASE.

Applications [2]:

- **Consumer:** Camcorders, Digital Cameras, DVDs
- **Computer:** Voltage Regulators, High-speed Memory, Card, PC Peripherals
- **Telecommunication:** Pagers, Cellular Handsets, GPS

FC in BGA package format is suitable for high-power and high-speed ICs requiring superb electrical and thermal enhancement.

Features [2]:

- **Thinner Profile:** Wafer thinning capability to support packages thinner than 1.0 mm.
- **Substrate:** 2-layer BT organic laminate substrate is used to reduce overall package cost.
- **Improved Performance:** Thin core (100um) substrate and via-on-pad design can be adopted.
- **Robust Structure:** Over-molded process can enhance throughput, first and second level reliability.
- **NSMD with OSP C4 Pad:** Low-cost solutions for electric interconnect between bump and substrate.

5.3.2 Flip Chip Ball Grid Array and Pin Grid Array

5.3.2.1 Flip Chip Ball Grid Array

In this discussion, we will differentiate FC with organic interposer-based BGA and FC ceramic interposer-based BGA (Figure 6).

FC Organic BGA (FCBGA) uses a laminate or build-up organic substrate and offers better electrical performance than wire-bond type BGA (WBBGA) packages, especially in high frequency applications.

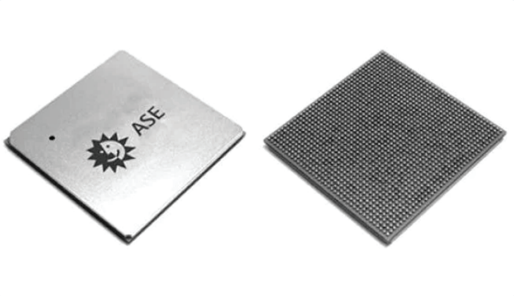


Figure 6. FCBGA by ASE.

FC Ceramic BGA (FCBGA) uses an alumina ceramic substrate and offers better moisture resistance, electrical insulating properties, and higher thermal conductivity than organic substrates.

FCBGA is used primarily for high-reliability commercial applications (e.g., CPU).

5.3.2.2 Flip Chip Pin Grid Array

FCPGA packages are used, for example, in Intel CPUs from the Pentium 3 onwards. The pin side, with the land side passives in the middle (Figure 7), is inserted into a socket when assembled to the PCB. The FC is attached upside-down to the top of the interposer laminate organic substrate, which consists of a very thick core layer with PTH (Plated Thru Hole) vias, and build-up layers on both pin side and FC side (Figure 8). This construction provides the greatest robustness for large FC dies such as CPUs.

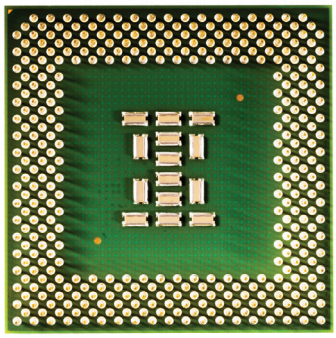


Figure 7. Pin side/Landing side view of a FCPGA package [13].

The die backside is exposed in the top of the package, providing an ideal interface for a heat slug that will be assembled on top of the package using TIM (Thermal Transfer Material). An active cooling element (e.g., fan) is directly attached to the heat slug allowing for very efficient cooling of the die. Heat Slug BGA (HSBGA) is suitable for high-power and high-speed ICs requiring superior electrical and thermal enhancement.

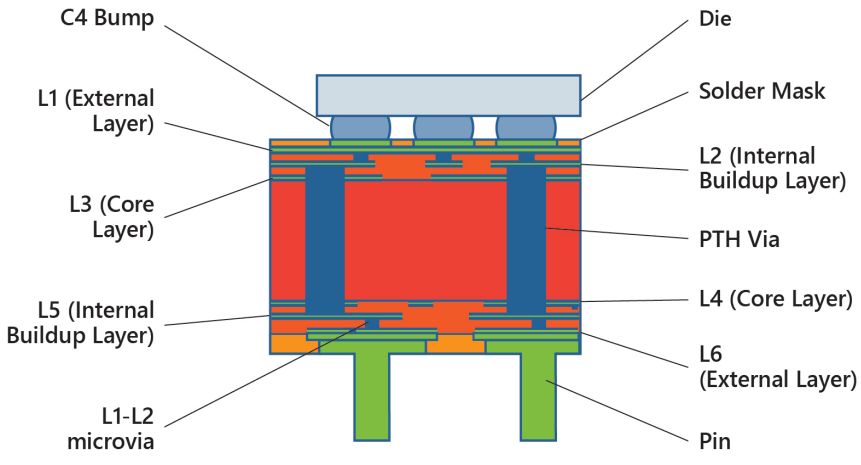


Figure 8. Cross-section of a FCPGA [13].

5.3.3 High Performance Flip Chip BGA (HFCBGA)

HFCBGA is a thermally enhanced FCBGA built by combining the package of FCBGA with heat spreader made of Cu, Al, or AlSiC. The heat spreader is used to extend the heat conduction area by connecting itself to the rear side of the silicon chip. This method desensitizes the performance deviation out of the chip size, lowers thermal resistance of junction-to-case (θjc) and enables the external heat sink or fan to work more effectively. HFCBGA can produce 6~8 watts of power dissipation under natural convection.

5.3.4 Applications [2]

- **Consumer:** Graphics/PC Chipsets, Server, High-end Applications, Microprocessor for PC and Server
- **Telecommunication:** Network Products (LAN), Switching, Transmission, Cellular Base Stations

5.3.5 Features [2]

- **Substrate:** 4-layer laminate, 4~12-layer build-up, ceramic, and PTFE substrates are available.
- **Thermal Lids:** Heat spreaders made of Cu with Ni plating, Aluminum, Ceramic, AlSiC.
- **Passive Component Attaching:** It can be placed on the top or bottom side of the package.
- **Ceramic BGA:** High Pb solder ball with eutectic solder paste improves board level reliability.

5.3.6 Process Flow and Variants

Flip Chip interconnect technology extends across multiple bump types and package platforms. Solder Bump, Copper Pillar and Gold stud have been the primary flip chip package interconnects but

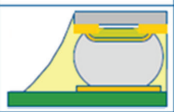
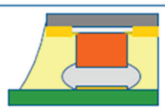
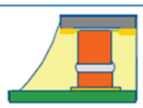
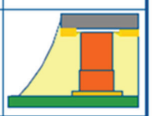
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	Cu
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level

Figure 9. Common Flip Chip Interconnect Options.
(Source: Bonding Technologies: Minsuk Suh, Sematech)

evolving interconnect options such as direct copper-to-copper interfaces using copper-to-copper bumps or copper nano-paste are being developed to help address pitch, electro-migration, and reliability issues. The choice of interconnect technology will depend on the bump pitch, power, speed/frequency requirements and die size. Figure 9 is a chart that shows the main types of flip chip interconnects. Figure 10 shows a comparison of FC assembly with bumps (b) and FC assembly with Copper Pillars (c) vs. the classical wire bond package. Both cases use a FC on IC-Substrate based construction, which, after encapsulation with mold compound, forms a BGA package with solder balls ready to be assembled on a PCB. Capillary underfill has been applied to both FC assemblies before encapsulation.

The flow chart in Figure 11 shows the generic FC process flow. Summarizing the three major process steps for TC packaging:

- Wafer Preparation
- Bonding on IC substrate
- Underfill

The result of the bump formation process is either standard FC solder bumps, fine-pitch bumps, microbumps, or copper pillar (CuP) bumps with SnAg cap, depending on the required I/O count and I/O pitch. The parameters that determine the bump size are shown in Figure 12. Special solutions for 10 µm bump sizes/20 µm bump pitches and below are SLID (Solid-Liquid InterDiffusion) bonding and the use of Indium bumps.

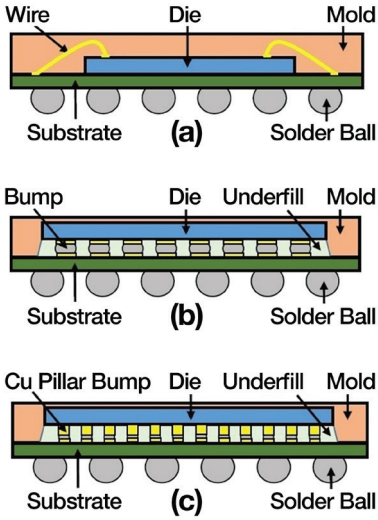


Figure 10. Flip Chip - Chip Scale Package Bonding Technology [4].

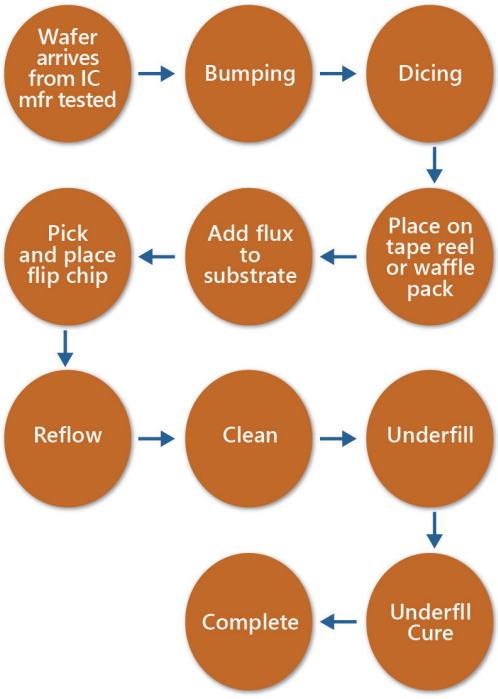


Figure 11. Flip Chip Process [17].

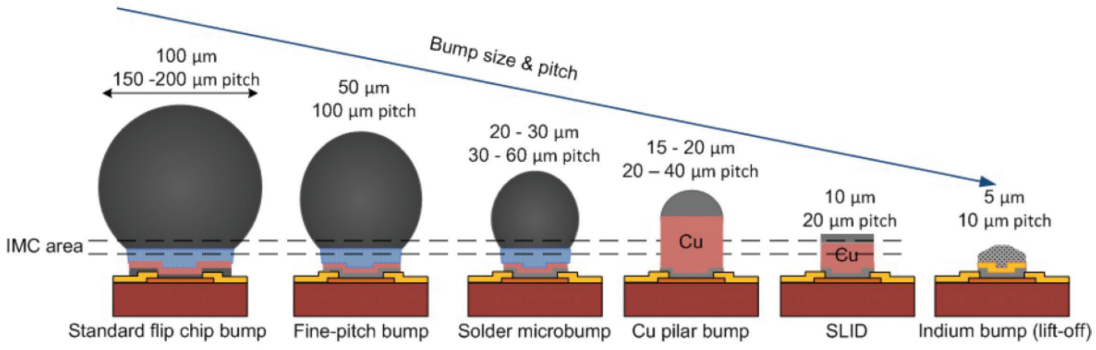


Figure 12. Evolution of bump size and pitch.
(Source: T. Tick and S. Vahanen)

5.3.7 MKS C4 and Microbump Products (also see Chapter 2.4.4)

- **Spherolyte Cu UF Series:** Basis for Cu pillars
- **Spherolyte Ni, Spherolyte NiFe and Spherolyte NiW:** Spherolyte Ni as a barrier and alloys like Spherolyte NiW, NiFe for improved barrier layers on Cu pillars
- **Spherolyte Sn Series, Spherolyte SnAg Series:** Solder deposit on the UBM or pillar

5.4 UBM and Solder Bumping

The typical construction of a standard FC solder bump is shown in the cross-section in Figure 13. The Al pad of the Si chip is accessed through a via in the passivation layer. This pad has had a physical vapor deposition (PVD/ Sputter) adhesion and a barrier/seed layer of nm thickness (Ti or TiW) applied. A wetting layer of thick Cu is applied over these layers in an electro-chemical deposition process (ECD) followed by a nm thick oxidation resistant layer to avoid Cu oxidation. The complete result is called Under Bump Metallization (UBM) on the chip pad. A flux applied before or with the solder transfer (paste printing or solder ball placement) will be used to break through this layer to allow good intermetallic phase (IMC) formation during the mass reflow process, important for low electrical interface resistance and good reliability. The UBM can also be applied in an electroless process setup. The main reasons for the application of the UBM with its different layers are:

- The die pad metallization in the BEOL is mostly Al which does not provide a solderable surface. It is neither wettable nor bondable by most solder materials. As well, the Al surface becomes oxidized when exposed to air and the oxide surface layer is an insulator.
- The nm thick sputtered adhesion layer adheres to the Al pad and the die passivation layer. It has a low contact resistance.
- The barrier layer acts as a diffusion barrier during the solder process.
- The wetting layer is needed to provide good wettability of the solder material that is used.

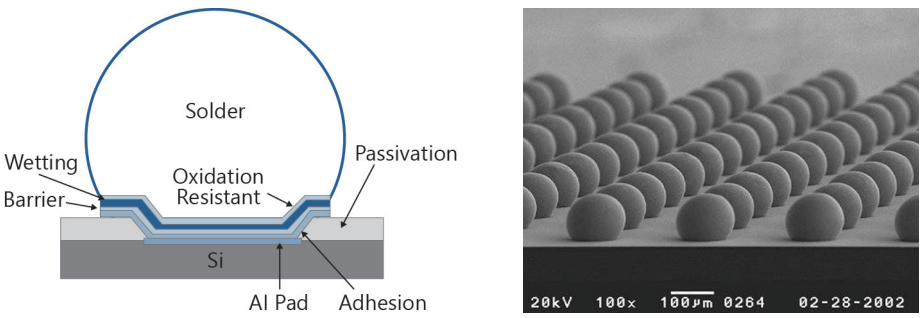


Figure 13. Standard FC Solder Bumps with ~100 µm diameter solder balls [15].

The types of solder bump formation techniques are:

- Evaporation
- Electroplating
- Printing of solder paste
- Placement of pre-formed bumps (solder balls)
- Stud bumping using wire bond technique
- Laser Assisted Bonding (LAB)

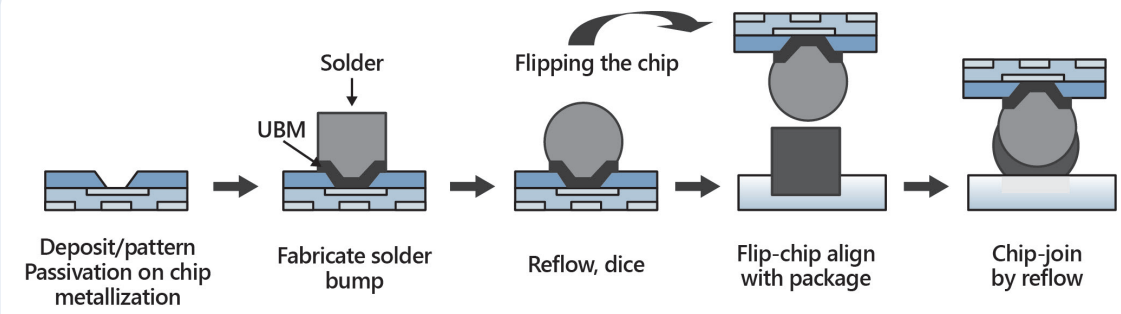


Figure 14. Example of a printed and reflowed solder bump for Standard FC and fine-pitch bumps.

The different bumping technologies produce bumps with different size, shape and spacing (pitch). Bump shape also depends on the die pad size, shape, and design (SMD: solder mask defined or NSMD: non-solder mask defined); solder components and their composition (alloy and dopants), cost, manufacturing time, equipment required, assembly temperature, and UBM. A careful selection is required to satisfy customer needs.

5.4.1 Evaporation Vacuum Reflow Bonding

The vacuum reflow (VR) bonding process (Figure 15) applies a temperature profile following the application of the selected solder materials. The profile defines the temperature rise rate, soak time, peak temperature, and total time of the reflow process. The process begins under a nitrogen atmosphere with vacuum applied during the peak temperature range. Cooling occurs under nitrogen. A reflow process forms the solder ball (Figure 15d) out of the truncated cone bump shape created by the evaporation of high Pb solder through mask. In a process variation (Figure 15e), an Sn cap can be deposited on the top surface of the truncated cone bump. Bonding under load (e.g., 0.18 N) can be useful in bump formation in some cases.

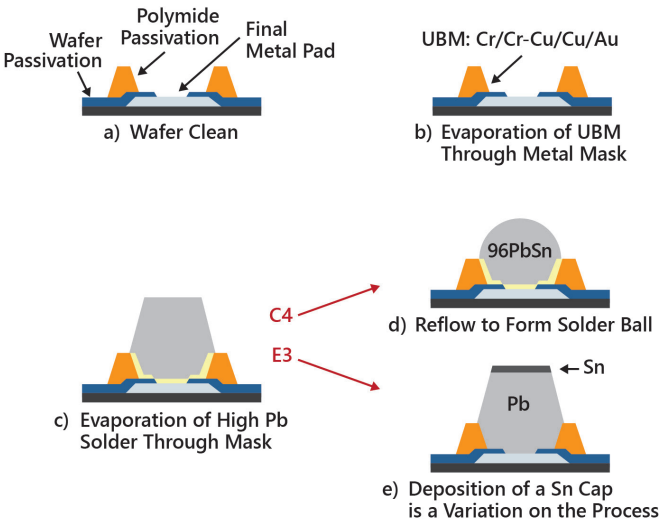


Figure 15. Evaporation Technique (Cr/Cr-Cu/Cu/Au UBM and 96PbSn lead-containing solder).

5.4.2 Electroplating Technique

Electrochemical Deposition – ECD, also called galvanic process, is most often used for lead-free solder materials (Figure 16). In the ECD process, a thick Cu layer is electroplated on top of the UBM. Due to overplating of the solder alloy over the edge of the mask, the formation of the bump results in a mushroom shaped bump. After removal of the mask and reflow process, the typical ball shape is achieved. An electroless plating technique is also available.

5.4.3 MKS RDL Products

- Spherolyte Cu UF series: For thick Cu layers
- Spherolyte SnAg: For reflow solder bumps (lead-free version) (Chapter 2)

5.4.4 Printing Technique

Solder alloy printing using a stencil and reflow process has become a mainstream method for high volume production of solder balls on UBM pads owing to its low cost (Figure 17). Alternatively, collective placement of pre-formed solder balls and reflow is another high-volume manufacturing method that applies a more accurately defined volume of solder alloy on the UBM pads.

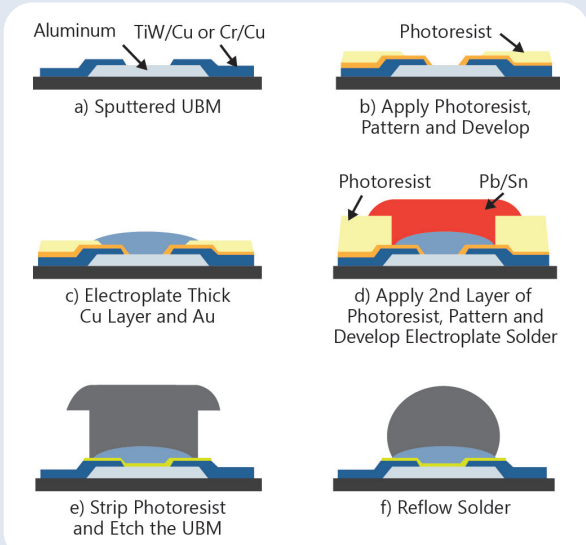


Figure 16. Electroplating Technique (with TiW/Cu or Cr/Cu UBM and 96PbSn lead-containing solder).

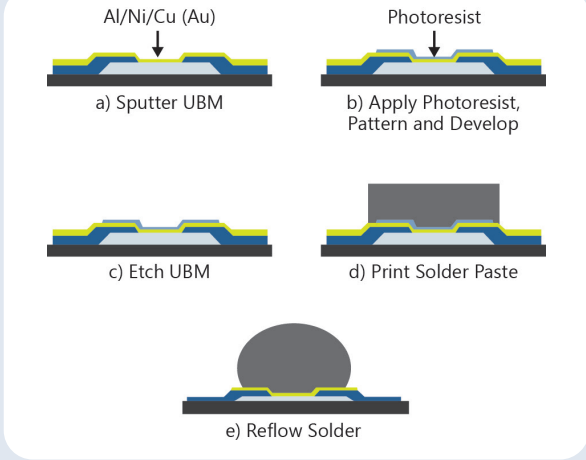


Figure 17. Printing Technique (with Al/Ni/Cu (Au) UBM and any kind of solder alloy available as solder paste).

5.4.5 Special Forms of Solder Bumping: Stud Bumping and Laser Assisted Bonding

Bumps can also be created using wire bond equipment, process, and bond wire (e.g., Au). This special form of bump creation, so-called stud bumping, uses the ball-wedge wire bond process. Mechanical force, heat and ultrasonic energy are used to form the ball (also called nail head) on the tip of the wire and to apply it to the Al bond pad. The wire is severed at the neck, creating a permanent and reliable conductive gold stud bump that penetrates the Al oxide to contact the underlying metal (Figure 18). The process is reserved for specialty applications since it cannot accommodate high volume manufacturing due to its sequential nature.

Laser-assisted bonding (LAB) is another interconnection. It uses laser energy to bond two surfaces of materials together (e.g., PacTech LaPlace). Single laser-assisted solder bump placement is also available (e.g., PacTech SB^2-Jet). These are fluxless and flexible and can produce different bump sizes and use different alloys on the same wafer. However, owing to its sequential nature, it has low throughput and is not used in high-volume manufacturing except for repair.

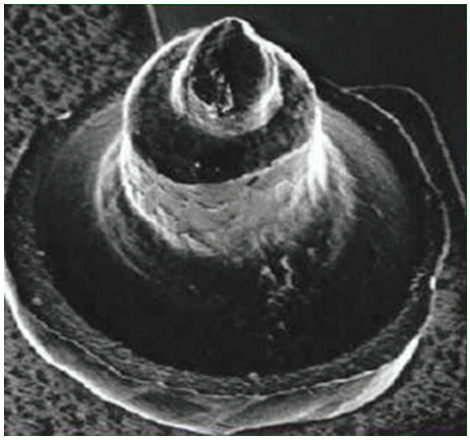


Figure 18. Stud Bump formed by wire bond process on Al bond pad without UBM.

5.5 Flip Chip Bonding – the FC Assembly Process

This section covers the assembly of the IC that has been prepared with FC interconnects onto an IC substrate. This is so-called first level or component level assembly. It consists of:

- Optional Land Pad Preparation on the IC substrate
- Pick and Flip and Place process
- Interconnect formation, either by mass solder reflow, adhesive curing, or by a thermocompression bonding (TCB) process that uses temperature and force. An alternative to the latter method is thermosonic bonding which uses ultrasonic energy.

After assembly, optional underfill and packaging (e.g., encapsulation) processes are applied. BGA balling of the IC substrate, marking, package singulation, inspection, laser marking, and packing in JEDEC-Tray or Tape and Reel are performed, so that the FC components can be fed to SMT line for assembly onto a PCB in the second-level or board-level assembly.

Figure 19 (academic view) and Figure 20 (industrial view) show the evolution of IC assembly technologies driven by the need for higher I/O density and smaller I/O pitches and bump sizes on the available die area. The receiving pads on the IC substrate may have pre-processed solder for high-volume manufacturing and for cost saving purposes. Flux-dipping of the bumps may be used to remove oxide on the pads and to promote wettability and solderability. The combination of pad design, bump pitch, and the solder depot of the microbump or the Cu-Pillar SnAg solder cap determine if extra solder is needed to ensure a complete, reliable, and low resistance interconnect.

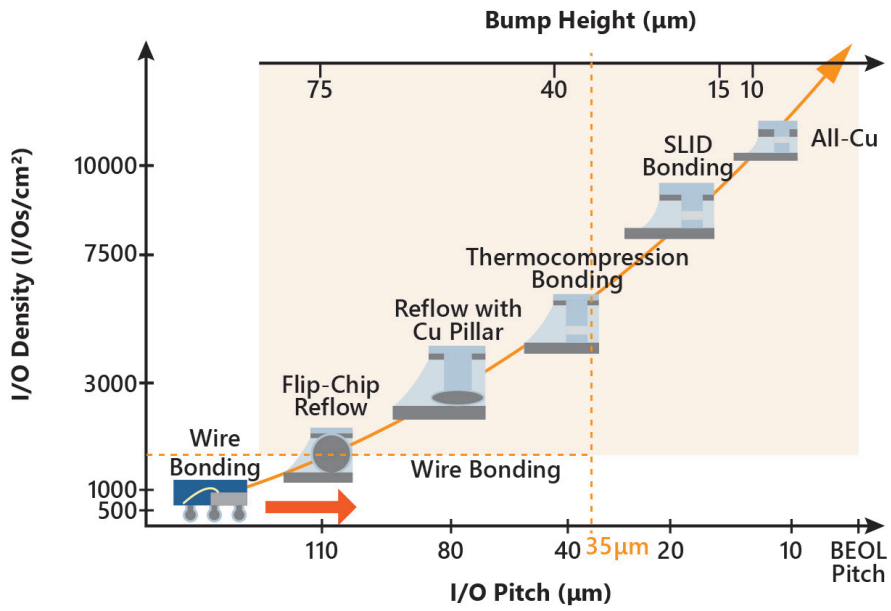


Figure 19. Evolution of IC Assembly Technologies [18].

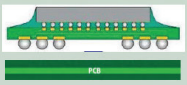
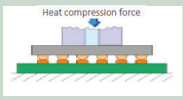
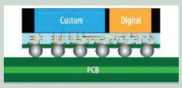
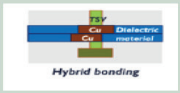
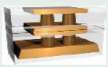
	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Architecture					
Contact Type	 Wire	 Solder ball or copper pillar	 Copper pillar	 RDL or copper pillar	 Copper to copper
Contact Density	 5-10/mm²	 25-400/mm²	 156-625/mm²	 500+/mm²	 10K-1MM/mm²
Substrate	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Accuracy	20-10µm	10-5µm	5-1µm	5-1µm	0.5-0.1µm
Energy/Bit	10pJ/bit	0.5pJ/bit	0.1pJ/bit	0.5pJ/bit	<.05pJ/bit

Figure 20. Overview on interconnect technologies evolution and driving parameters [10].

It is also possible to use a substrate with "solder-on-pad" provided by the IC substrate vendor. While difficult to source and costly, this is a suitable alternative for large chips with small diameter microbumps or Cu-Pillars with a SnAg solder cap and small pitch. Kyocera, for example, does something like this called "Solder Pre-Coat" [3].

More solder increases the reliability of the connection, especially for large chips with a large array of bumps, microbumps, or Copper-Pillars. However, for the aforementioned reasons and if solder printing on the substrate is not possible (due to either process flow or fine pitch/small pad design issues), only flux dipping of the FC is applied. A co-design of FC and substrate pad design is required to optimize the amount of solder. For FC placement on 2.5D interposer, in general only flux dipping is applied.

The following processes are available for FC attach to IC substrate:

- Reflow with bumps or microbumps (Chapter 2)
- Reflow with Cu-Pillars (Chapter 2)
- Adhesives, conductive, and non-conductive die attach films
- Thermocompression, and Thermosonic Bonding
- SLID and indium bump
- All Cu (D2D, D2W and W2W hybrid bonding without bumps)

Some of these processes are described below while reflow with bumps or microbumps and reflow with Cu-Pillars are described in Chapter 2.

The FC is assembled on the top side of the HDI (high density interconnect) IC substrate. The substrate has C4 bumps (BGA, package) with > 400 µm pitch on the bottom side, ready to be assembled to a standard PCB. If the FC pitch is ≥ 100 µm, Pick and Place using FC-DieBonders (e.g., BESI Datacon Evo 2200, 2200 plus and advanced, or Datacon 8800 FC QUANTUM) and mass reflow is used. A typical reflow profile for Sn-based leadfree solder alloys is shown in Figure 21. The same is used, with adjusted process parameters, for microbumps with FC pitch between ~ 100 µm and 50 µm. Below that pitch, and specifically for fine-pitch Cu-Pillar bumps, thermocompression bonding (TCB) on special thermocompression bonders are used.

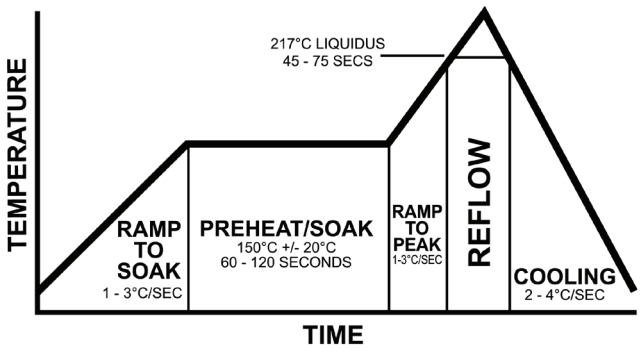


Figure 21. Typical solder profile for Sn-based leadfree solder alloys. (Source: https://en.wikipedia.org/wiki/Reflow_soldering)

FC may also be bonded on the top side of a 2.5D interposer (silicon, glass, or organic) with microbumps or Cu-Pillars (Figure 22). The interposer translates the fine pitch into a coarser pitch.

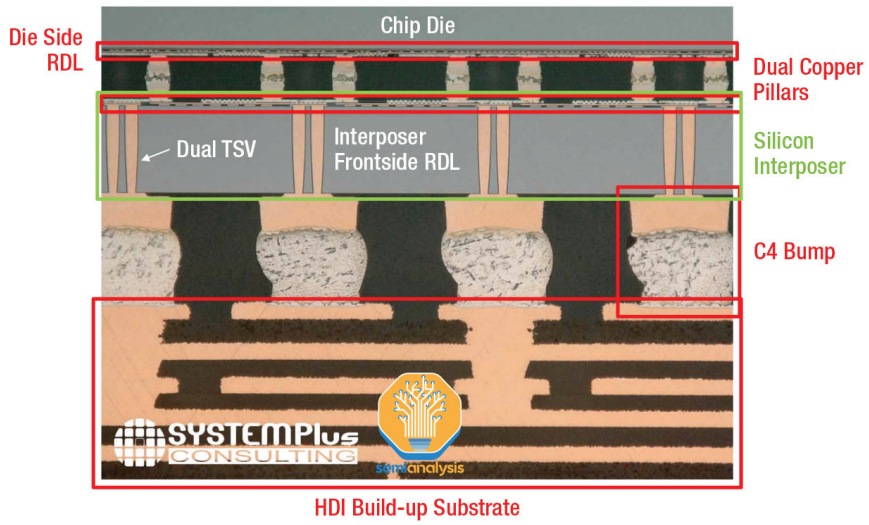


Figure 22. High Density Interconnect (HDI) build-up IC substrate cross-section (FC on 2.5D Si-Interposer with TSV). (Source: SystemPlus Consulting)

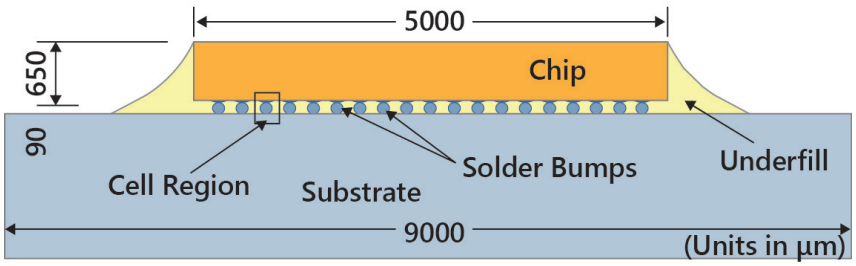


Figure 23. Example cross-section of an assembled FC on IC substrate.

In contrast to wire bonding, the soldered connections on the chip (solder bumps or Cu-Pillars) are placed directly on the bond pads of the IC substrate or 2.5D interposer to complete the circuit (Figure 23). Flux is used to clean the bond pads on the substrate (removal of native oxide of Cu pads or UBM) - if not Au plated - and to promote the wettability for soldering process. Flux can be applied to either the IC substrate pad directly or via "flux dipping" of the FC before die attach to the substrate. The bumped die with bumps is partially dipped into a flux bath, transferring the required amount of flux to the bond pads on the IC substrate. An underfill (CUF or MUF) can be applied to increase reliability. Encapsulation with epoxy (e.g., molding, dam and fill, glop top) protects the FC and increases robustness and reliability.

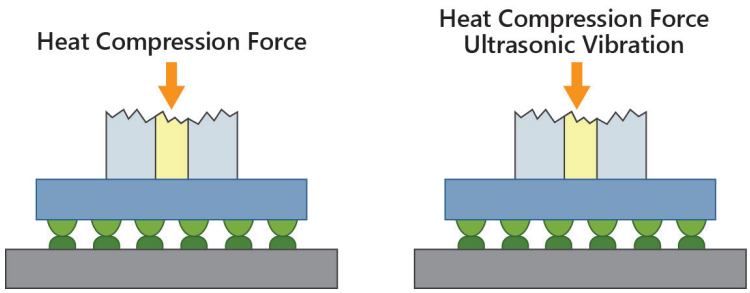


Figure 24. Concepts of Thermocompression Bonding (left) and Thermosonic Bonding (right).

5.5.1 Thermocompression and Thermosonic Bonding

Thermocompression Bonding (TCB) applies pre-conditioning, deposition, and bonding process steps. Bonding is a diffusion process that uses force (pressure joining), and heat (thermocompression welding or solid-state welding) as illustrated in Figure 24. Two metals, e.g., Au-Au, are brought into intimate contact by applying force and heat simultaneously. Interdiffusion of the two metals occurs by surface diffusion, grain boundary diffusion, and bulk diffusion. The bonding process takes place in either a vacuum or

forming gas environment, e.g., a nitrogen/hydrogen mixture. The parameters for the bonding process for most used bond metals are:

- Al: temperature 400 - 450°C, applied force above 70 kN, for 20 to 45 min
- Au: temperature 260 - 450°C, applied force above 40 kN, for 20 to 45 min
- Cu: temperature 380 - 450°C, applied force between 20 - 80 kN, for 20 to 60 min

The advantages of TCB include localized heating, rapid cooling, and a satisfactory level of hermeticity, while the drawbacks are the extensive preparation requirements and the need for deposition of Al and Cu.

In the case of thermosonic bonding, ultrasonic energy is applied to the bonding area, transferred from a pickup tool through the back surface of the chip. The main benefit of thermosonic bonding over thermocompression is the lower bonding temperature requirement and the shorter process time. The use of ultrasonic energy must be evaluated for each product, as excessive ultrasonic vibrations might produce damage in the chip.

5.5.2 Bonding with Isotropic and Anisotropic Adhesives

The use of adhesives to create electrical connections is a low-cost process that cannot be used for all applications but has value in some instances, especially if higher temperatures need to be avoided in the manufacturing process. Advantages are the ease of processing, low curing temperature, and elimination of the need to clean after the bonding process.

Isotropic conductive adhesive (Figure 25, top): pastes of epoxy and conductive particles, typically Ag, which assure conductivity in all directions.

Anisotropic conductive adhesive (Figure 25, bottom): Pastes of thermoplastics filled with metal coated polymer spheres that assure insulation in all directions before bonding and electrical conductivity in z-direction after bonding.

Similar principles are applied to conductive and non-conductive die attach films. Contact is made under pressure in z-direction, electrically connecting only the respective pairs of solder bumps and IC substrate pads, while the other areas stay insulated. The adhesives or films can function as an underfill at the same time.

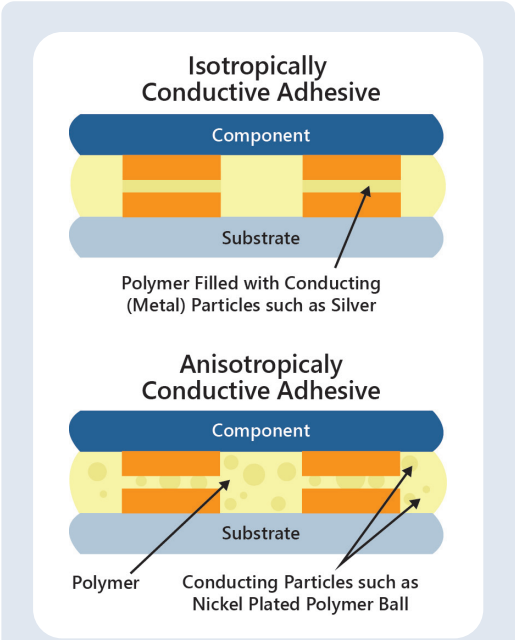


Figure 25. Isotropically and anisotropically conductive adhesives for low temperature FC bonding.

5.5.3 Flip Chip Underfill

Underfill material is a non-conductive adhesive that provides strength to the assembly by mechanically connecting the surface of the die with the surface of the IC substrate, taking part of the mechanical stress from the solder joints. It also protects the bumps from moisture and other environmental hazards. The underfill also helps to compensate for the CTE mismatch between Si (≈ 3 ppm/K) and typical FR-4 material used for IC-Substrates CTE (≈ 17 ppm/K). This thermal expansion mismatch creates a large strain on the solder joints.

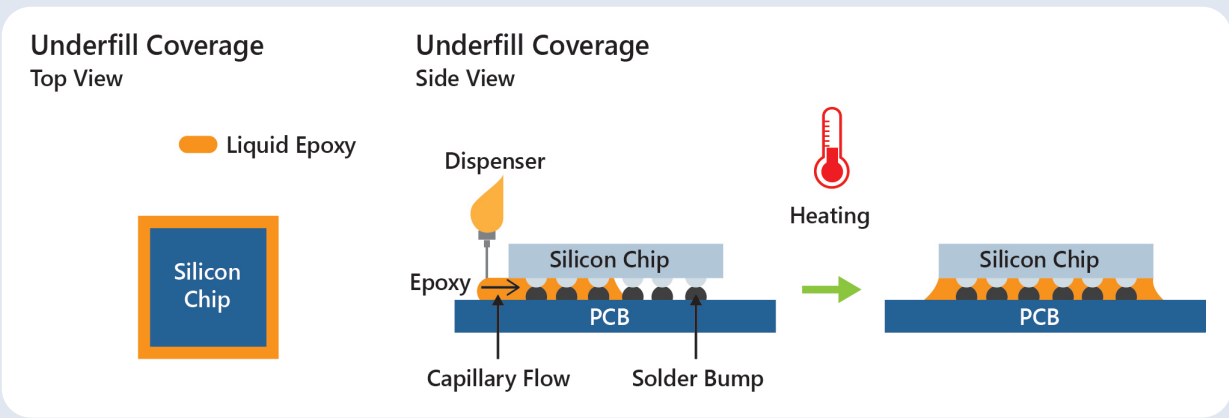


Figure 26. Underfill coverage and underfill process (here CUF on PCB assembly).

Underfill is typically a polymer or liquid epoxy that is applied just underneath the perimeter of the FC die assembled on the IC-Substate or 2.5D Interposer (Figure 26). The process can be capillary underfill (CUF) as a sequential process or molded underfill as a batch process. Underfill can be done only after the FC die has passed through a reflow, TCB, or another one of the bonding techniques described in the previous section. The IC substrate or 2.5D Interposer is heated during the underfill process so that the underfill is absorbed underneath the chip via capillary forces. Plasma cleaning and activation of the IC-Substrate can promote the flow, depending on critical factors like standoff, bump pitch and viscosity of the used underfill material.

Some of the challenges for underfill are:

- CUF is seen as a "dirty process" and it is the biggest throughput bottleneck.
- The need for underfill can become the showstopper for dense integration due to space requirements for the dispense needle around the die.
- Dispensing challenges include:
  - To achieve complete and void-free flow under the FC
  - Dispensing around closely packed FC
  - Avoiding damage and contamination of neighboring components
  - Control of flux residues

No-Flow Underfill (NFU) is a special type of underfill process that combines the solder reflow and underfill bonding processes into a single step. Liquid no-flow underfill is dispensed or film type is attached to the FC die or IC substrate prior to attaching the die to the IC substrate. This underfill material is then cured along with the solder reflow of the interconnect bumps, acting as a flux during the reflow process. This eliminates several process steps, including flux dispensing and cleaning, capillary flow, and one heating cycle, and results in greater production efficiency and potential cost reduction. Silica fillers cannot be used in the encapsulation material as they interfere with solder joint formation and produces higher thermal expansion of the underfill material which can lead to reliability problems. Research in this area focuses on process variations to enable the use of silica fillers or alternate fillers such as nano-silica powders that do not interfere with solder joint formation.

5.5.4 Emerging Technologies for Flip Chip Assembly

Continuous development is needed for FC assembly processes, driven by higher I/O counts, finer pitches, smaller bumps, larger dies, and lower stand-offs. Dense heterogeneous integration of multiple dies/chiplets in one FC package adds additional challenges. Some examples of emerging technologies are:

- Hybrid Bonding Cu-Cu (D2W, W2W)
- Improved TCB process
- Fast-flow snap-cure underfill (illustrated in Figure 27)
- Flux-less solder bumping
- Larger FC die and package sizes
- Test board and better acoustic image for voids

5.5.5 MKS Products (also see Chapter 2.4.9)

- Spherolyte Cu DB
- Everplate Cu 300 - two copper deposition processes for Cu-Cu bonding

These two processes follow different approaches to solve the same challenge of creating a seamless connection between two copper surfaces. Both systems need to be able to fill trenches and µ-vias and to enable copper crystal growth over the interface at temperatures not over 200°C.

Spherolyte Cu DB creates a very pure copper surface. The surface needs to be bonded very shortly after deposition since it tends to recrystallize to larger grain sizes that are less effective in producing Cu-to-Cu bonds.

Everplate Cu 300 solves the above limitation by depositing a fine-grained and doped copper layer. The doping stabilizes small crystallites which promote Cu-to-Cu bonding even after four weeks. The small surface grain structures only recrystallize to larger grains during thermal treatment in the bonding process.

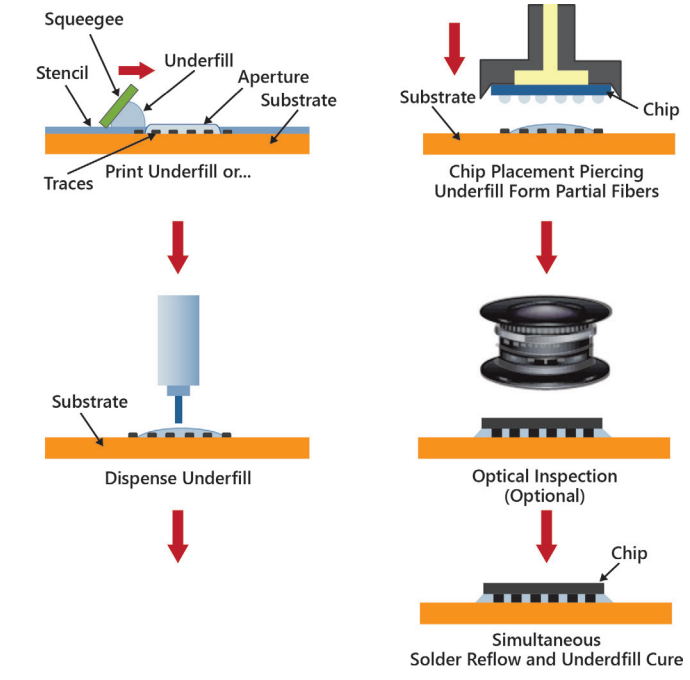


Figure 27. Fast-flow snap-cure process with new underfill materials.

5.6 Encapsulation, Molded Underfill and Solder Ball Attach

While encapsulation is optional and not required for electrical functionality of the FC components, it is strongly recommended for FC packaging. Encapsulation of the die and its electrical connection to the IC substrate protects the final component from environmental exposure and degradation. Once the assembly process is completed, the semiconductor die is firmly mounted and electrically connected to the IC substrate. In case of CUF or NFU, the underfill process must be completed prior to or during encapsulation when using mold underfill (MUF).

Additionally, the thermal expansion mismatch between the silicon die, the solder bumps, and the IC-Substrate must be accommodated. To compensate for this mismatch, in case of MUF, the encapsulation material (e.g., epoxy mold compound) must be deposited as an underfill to structurally couple the die with the IC substrate. This decreases the shear stress between the two and lowers the applied stress on the solder joints between the die and IC substrate. Different encapsulation methods (transfer molding, compression molding, Dam and Fill process, Glop Top process), and process formats are available for use.

Flip Chip Ball Grid Array (FCBGA) components (Figure 28) use PCB-like IC substrates (high layer count, high I/O count) and are encapsulated one-by-one using an epoxy molding process (e.g., Amkor - https://amkor.com/packaging/laminate/fcbga/). Flip Chip Chip Scale Package (FCCSP) components use thinner IC substrates (lower layer count, lower I/O count) and are encapsulated in high volume manufacturing by using a molding process of IC substrate in full strip or in mold cap format molding a matrix of components at the same time (e.g., Amkor - https://amkor.com/packaging/laminate/fccsp/).

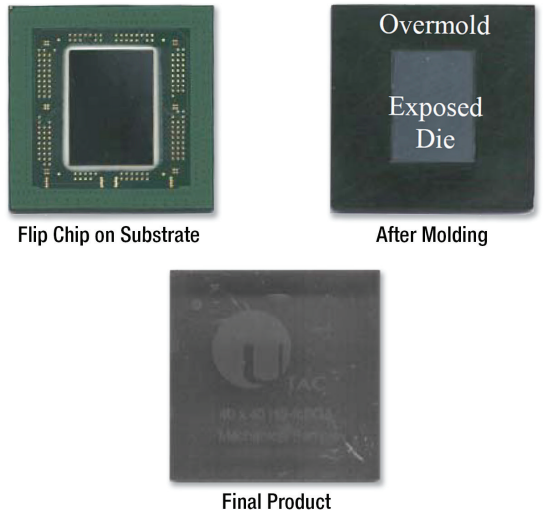


Figure 28. FCBGA package samples [16].

The complexity of packaged ICs and the associated advances in electronics, especially mobile and multi-die products, have placed additional requirements on encapsulation compounds, fine-tuning these complex material formulations for specific device applications and package form factors. Managing the mold cap and following component warpage after package singulation is one of the biggest challenges. Mold compound physical properties, die size, package design, and IC substrate type and finish all impact package reliability, board-level reliability, and product/system performance.

At the most basic level, encapsulation materials contain the following classes of raw materials:

- Organic resins
- Fillers (usually fine silica powder)
- Catalysts
- Curing agents
- Silane coupling agents
- Mold release materials
- Pigment or coloration (usually carbon black).

The additives include flame retardants, adhesion promoters, ion traps, and stress relievers. Typical resins include epoxy, polyurethane, silicone, and acrylic. After application, encapsulation materials must be cured using heat to cross-link and fully solidify the polymer resin. The cure cycle must be completed with care to ensure the formation of a void-free body that ensures protection, bonding to the substrate, and heat transfer. The primary source of void creation is absorbed moisture from the ambient environment. Voids can also be created by the release of volatile materials from the compound due to improper curing, most often, a too rapid heat ramp.

5.6.1 Encapsulation with Molded Underfill

Encapsulation and underfill can be simultaneously accomplished inside the mold tool by injecting the mold compound (transfer molding process is more suitable than compression molding due to the required flow underneath the FC die) into the mold cavity and applying heat to cure the mold compound. Heat is provided through the metal mold material, avoiding the need for an oven cure. Vacuum can be provided in the tool cavity to achieve better mold flow and void reduction, especially underneath the FC die. Figure 29 shows the impact of board vacuum on the mold flow front. This underfilling method is called Molded Underfill (MUF). It is suitable for high-volume production and provides better process control, at the expense of increased equipment and material cost, as fine-filler mold compound needs to be used; filler size depends on the standoff of the FC die over IC substrate. As a rule of thumb, standoff divided by three is the recommended filler size.

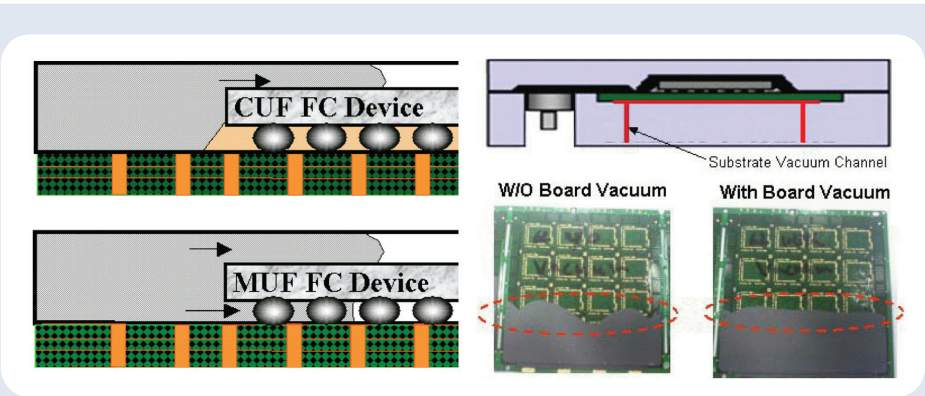


Figure 29. Left: Transfer Molding Encapsulation of assembled FC on IC substrate Right: Impact of vacuum usage in mold cavity on mold flow front [5].

Figure 30. BESI Fico AMS-LM Transfer Mold Machine with three stations (left), open mold chase with IC substrate (right). (Source: BE Semiconductor Industries N.V.)

Molding protects the FC die by encapsulating it in plastic. In line with the market trend toward SiP, exposed FC dies and more complex assemblies like multi-die molding, BESI developed the large IC-Substrate molding machine, the Fico AMS-LM (Figure 30). The Fico AMS-LM can manage substrates of up to 102 x 280 mm and all current single and dual sided packages. Large IC substrates allow a high board utilization and, in combination with deep vacuum, a unique clamping mechanism and high output that significantly improves the Fico AMS-LM performance and yield.

5.6.2 Solder Ball Attach for BGA Package

After encapsulation, the assembled and molded IC substrate will get its ball grid array (BGA) on the bottom side, the interconnect elements for second level assembly on PCB. The most common process used in high-volume manufacturing is placement of preformed solder bumps (solder balls) using solder ball attach (SBA) equipment. After applying flux by stencil printing or needle dipping and drop placing on the pads, the solder balls are picked and placed using needle transfer with vacuum method. The solder balls are "flying" on an air cushion in the ball tray when picked by the needles (complicated and expensive product specific tooling). Figure 31 shows an example of a solder ball attach machine from Shibuya Corporation in Japan.

Figure 31. Shibuya Solder Ball Mounter (SBM371). (Source: Shibuya Corporation)

Another less expensive process is using brushes that are moving solder balls applied to the surface of a product specific stencil into the holes of that stencil, which are placed over the pad positions on the IC substrate. This method is also used to place solder balls on wafers for Wafer Level Packaging. It is limited to minimum solder ball sizes around 75 µm. Equipment for this solder ball attach process is provided by companies such as Athlete.

5.7 Flip Chip Package Singulation

FC packages are singulated similarly to other die assemblies and packaged on IC substrates (e.g., Wire Bond BGA). Singulation is achieved using automatic mechanical blade dicing machines with high-speed circular diamond blades and precision robotic alignment (Figure 32). These machines are like those used for wafer dicing but with different dicing blade width and quality. Automated machines typically include blade preparation: cutting, cleaning, cooling with liquid, inspection, and sorting. The molded IC substrate can be fixed to a product-specific work holder or to an adhesive tape backing in a wafer film frame. The singulation saw has sufficient precision to cut the molded IC substrate material without completely cutting the tape, allowing the singulated components to be picked from the tape after dicing.

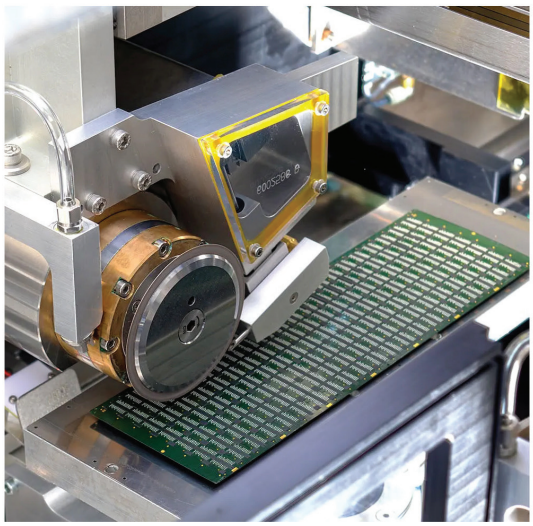


Figure 32. Package Singulation/ IC substrate Dicing Equipment. (Source: BE Semiconductor Industries N.V.)

5.8 Marking, Inspection, Electrical Test, and Packing

The final process steps for FC packaging are called Mark, Scan, and Pack (MSP) and, if required, a final component test. Component marking can be done much more efficiently at the molded IC substrate level before package singulation. The marking contains, depending on space available on the package, and smallest font allowed by the customer, information such as: trace code, order information, product code, date code, sort code, and company logo. Marking is only done on singulated, tested, and sorted components (typically in JEDEC-Trays) if a final electrical test of the singulated components is required and test results (e.g., sort code) impact the text and codes to be marked.

Marking is done by either printing or laser marking. In pad printing, a silicone rubber stamp pad is coated with white ink, and the ink is transferred to the surface of the package. The ink is then subjected to a cure cycle, commonly done with exposure to UV light. The silicone rubber needs to be manufactured for each new print pattern and is not flexible e.g., quick changes (date code, sort code, continuous numbering for traceability) are not feasible. It is relatively slow, expensive, and consumes much of the available print space. For these reasons, it is rarely done in high-volume manufacturing. It does, however, have the advantage of better readability — if font size is not too small — owing to good black/white contrast.

In laser marking, no direct contact with the package takes place. The laser's thermal effect is used to slightly ablate - typically 50 µm to 70 µm deep - the surface of the mold compound and leave a permanent mark. Laser marking is a very fast, flexible (because it is programmable), and cheap process. Its primary disadvantage is the low readability of laser markings due to very little contrast. Both variants, pad printing and laser marking, are accomplished in fully automated machinery.

After an automatic optical inspection (AOI) to ensure FC package quality (e.g., dimensions, solder ball count and position, solder ball size) the FC packages are dry-baked on a carrier to ensure that each package has the least possible amount of absorbed moisture when packaged for shipment to guarantee reliability when later mounted[1].

The FC packages can be packed in JEDEC-Trays, Tape & Reel (Figure 33) or Tubes.

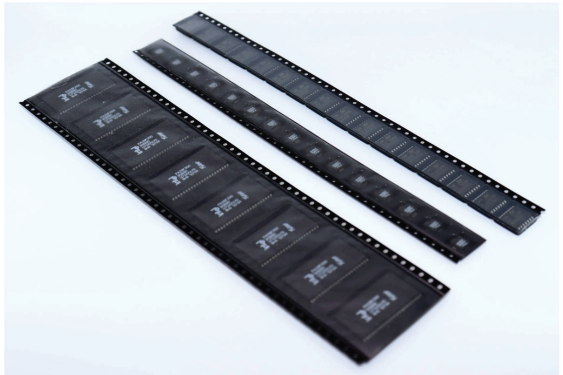


Figure 33. Tape & Reel (T&R) packing of packages to be fed in SMT component placement systems. (Source: Alltemated Inc.)

[1] *A part may be qualified for reliability to a 'Moisture Sensitivity Level' (MSL). For the least sensitive packages (MSL-1) baking and sealing is not required.*

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Chapter 6

Wafer Level Packaging

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6.1 Introduction

The performance of electronics systems, such as computers, displays, or smartphones to name just a few, is determined not only by the performance of its on-board silicon chips, but also by the performance of the entirety of peripheral silicon chips. Each chip needs a package enabling its integration within the system. The interconnection (e.g., wire, flip chip, or RDL) of the IC (device) to the package and, ultimately, of the packaged IC (component) to a printed circuit board (PCB), constitutes one such peripheral component that profoundly affects the performance of these systems. The design of the interconnection, the length of signal paths, and the materials employed in the interconnection and packaging interfaces all influence signal integrity and signal attenuation. This, in turn, impacts the overall performance of the electronic system. Note that general package functions are outlined in Chapter 1.

In standard chip packaging (Figure 1), the wafer is first tested (wafer probe) then ground to final wafer/die thickness (GBD – Grinding before Dicing) and singulated into separate dies using a method known as dicing. The option for Dicing before Grinding (DBG) also exists. In DBG the wafer is diced to a depth less than the wafer thickness and subsequent grinding separates the dies from the wafer. Wafers are thinned from their initial thickness (300 mm wafers come at 780 µm initial thickness, 200 mm wafers at 725 µm) to the target thickness by backside grinding. Different singulation technologies such as (supported) cleaving, mechanical blade dicing, laser dicing, or plasma dicing are used [1]. Prior to dicing, all dies are electrically tested and Known Good Die (KGD) are identified in electronic wafer maps. These KGD are then assembled to an interposer (e.g., leadframe or substrate), interconnected (e.g., by bond wire of flip chip bumps – Chapter 2.4), and packaged.

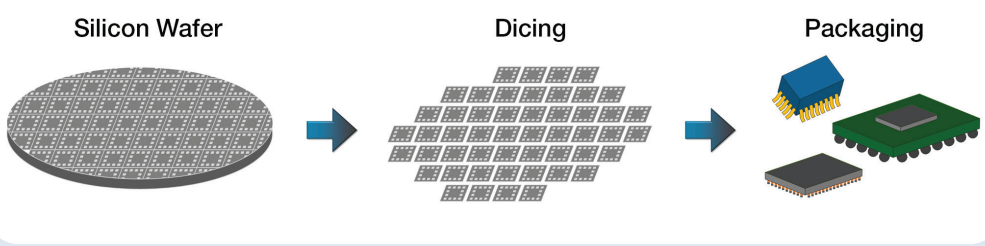

Figure 1. Process flow for standard packaging technologies [2].

In Wafer Level Packaging (WLP) a die is packaged while still in wafer form (round form). Wafer and Panel Level Packaging (WLP and PLP) technologies are newer, more advanced technologies that achieve significantly better electrical performance owing to their very short electrical connections, much lower package parasitics, and smaller form factor. No extra interposer (e.g., leadframe or substrate) is needed as the chip is the package that carries the routing as a re-distribution layer (RDL) and the interconnects as either fan-in (all contacts on the chip area) or fan-out (at least one contact outside the chip area). Figure 2 shows the 2D and 3D integration methods with and without classical separately manufactured interposers (e.g., ceramic, metal leadframe, organic substrate), where WLP (Fan-In and Fan-Out) and PLP (Fan-Out only) are highlighted as the "without IC substrate" category. The interposer is done on the chip (RDL) during batch processing while still in wafer or panel format.

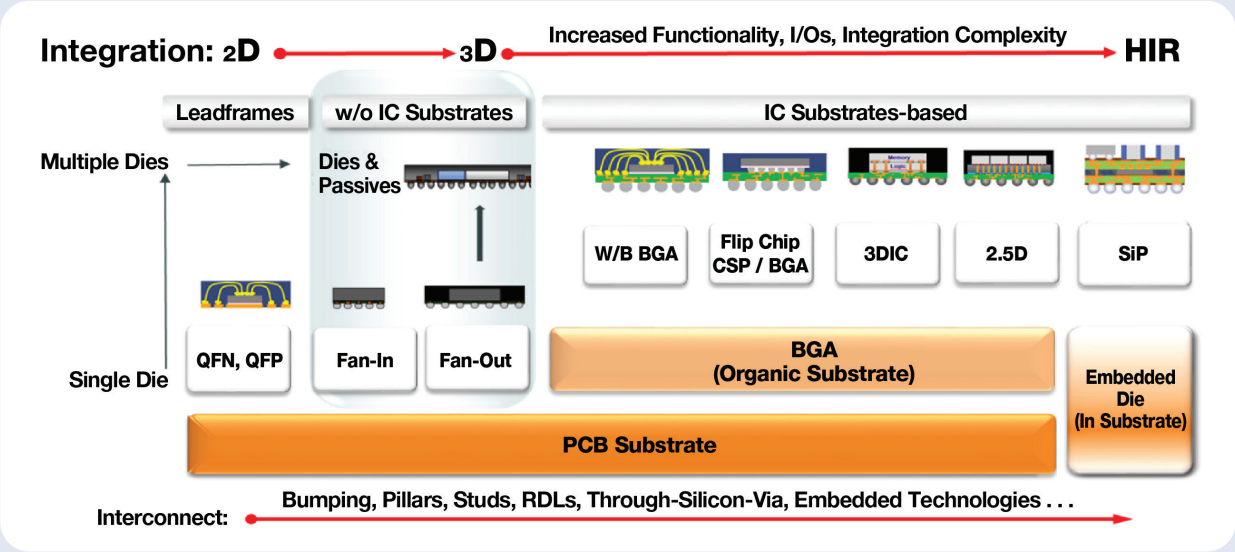

Figure 2. Overview of different packaging technologies and substrates [19].

6.2 Fan-In Wafer Level Packaging (WLP)

In Fan-In WLP (Figure 3), also called Wafer Level Chip Scale Packaging (WLCSP), the RDL interposer is produced at the wafer level prior to dicing (Figure 4) and the contact area for I/O is usually smaller than or equal to the die area. Fan-in results in a single die in a package – the die is the package and, in contrast to fan-out technology, both good and bad dies are processed. Figure 3 shows a comparison of a Fan-In WLP and a Fan-Out WLP. Whereas for fan-in technology the I/Os are placed at the chip area only, for fan-out technology the fan-out zone (region) around the chip provides additional space to redistribute and place a higher number of Input/ Outputs (I/Os) compared to fan-in.

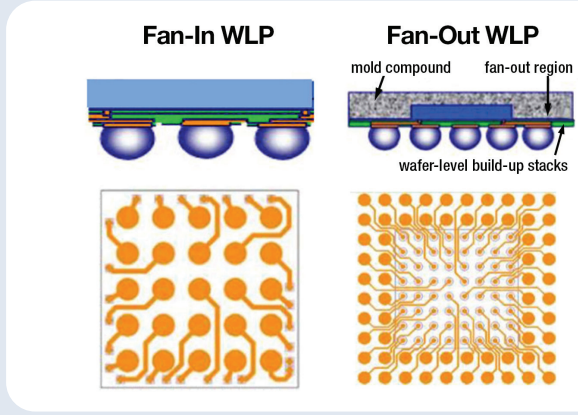

Figure 3. Fan-In vs. Fan-Out WLP and placement of I/Os [20].

Unlike with standard packaging technologies (Figure 1), routing of the electrical connections and interconnect processing for fan-in packaging is a batch process that is carried out with the wafer intact and in its original format (Figure 4). Bad chips are processed, sorted, and rejected after packaging and singulation. There are also so called "blind builds" in which no tests are performed, until all chips have been fully processed. The sorting and rejection of bad components is then done during final test of the packaged and singulated chip.

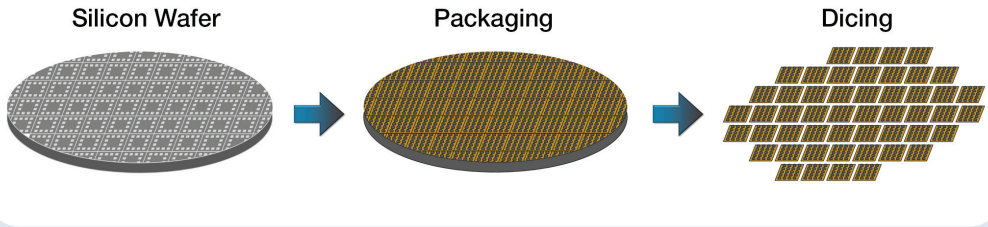

Figure 4. Process flow for Fan-In WLP [2].

- Main Market for Fan-In WLP: Mobile applications (90%) [2]
- Market Drivers and Capabilities for Fan-In WLP
  - Small footprint
  - Better electrical performance
  - Lower cost package
  - Thinner package
  - Lower thermal resistance

- Enabling Technologies
  - Wafer processing
  - Bumping
  - Thin film RDL

Fan-In WLP consists of a bare die with a redistribution layer and interconnect elements, typically bumps. The die sidewalls and backside are protected from the environment by wafer molding compound. WLP is the smallest package size possible, and the only package equal to the chip size (routing and interconnects on the chip area). WLP uses flip chip technology for mechanical and electrical interconnections to the IC substrate (bumps or Cu-Pillars). The different interconnect methods used are (Figure 5):

Direct Bumping: The I/O on the die are designed so that they are already at the bump position. The UBM is deposited directly on the wafer passivation without a compliant layer in between. Because of the strong interaction between the front-end process, the bumping process and the bump design, this construction has limited use. The die passivation (SiO_2, Ti_3N_4) also acts as an isolation layer for the packaging.

Repassivation: The I/O on the die are designed so that they are already at the bump position. A repassivation layer is added to provide improved board level reliability and to decouple the Under Bump Metallization (UBM) and bump from the die passivation. This avoids cracking of the die passivation during temperature cycling. A UBM is added to provide adhesion, function as a barrier layer, and ensure solder wetting.

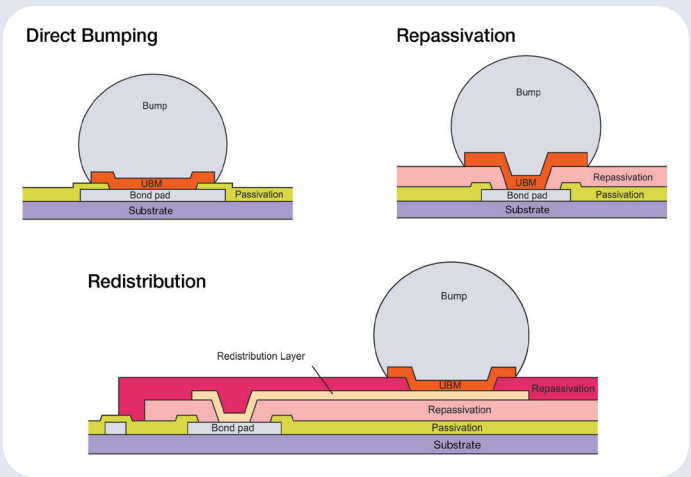

Figure 5. WLP interconnect technology [23].

Redistribution (RDL) (Chapters 2.4.3 and 6.4.1.6): I/O on the die are aligned with the corresponding bump locations with a redistribution layer, typically consisting of Cu. For one RDL (metal layer), two repassivation layers (so called "sandwich structure" – a metal layer between two passivation layers) are used. Each additional RDL (metal layer) normally requires one additional repassivation/passivation layer. In general, a redistribution design provides better board level reliability behavior than a direct bumping, repassivation design [3]. RDLs allow better distribution of I/Os over the chip area and can be used to generate wider pitches that are easier to process than fine pitches.

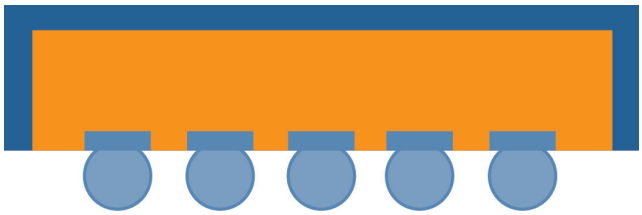

Figure 6. Cross-section of an eWLCSP with molded sidewall and backside protection. (Source: ESPAT-Consulting, 2019)

WLP may contain up to 21 thin-film layers (10 RDL metal layers and 11 passivation layers, with only metal layers counted, i.e., a 10L RDL has 10 metal and 11 passivation layers. Most WLP designs contain only 1-2 RDL layers, however, owing to problems with surface topology, the lack of planarization techniques, and the conformal behavior of liquid passivation layer materials[1]. Increased wafer warpage and processability also become more challenging with increased numbers of RDL layers owing to CTE mismatches between the materials in the RDL layers and the underlying silicon. Standard WLP designs provide no sidewall and backside protection. Such protection can be supplied by using a protective polymer coating in designs such as eWLCSP (embedded Wafer Level Chip Scale Packaging, Figure 6) which provide mechanical robustness and resistance to clipping, cracking, and handling damages [4].

[1] *S. Kröhnert, private communication*

6.3 Fan-Out Wafer Level Packaging

The constant demand for greater performance in electronic devices has led to the need for smaller, higher performing die, increased I/O counts, and ever smaller pitches on the die. The need for finer pitches necessitated the move from bumps to microbumps, then to Cu-Pillars to avoid the addition of more intervening layers to translate the small chip pad pitch to the much greater PCB assembly pitch. Fan-Out WLP, which provides additional space to place I/Os, enables the performance advantages of Fan-In WLP i.e., short connections and cost-effective packaging of smaller chips, at these much finer die pitches. The first Fan-Out WLP developed and produced in high volume – based on the idea of RCP (redistributed chip packaging) – was eWLB technology (embedded Wafer Level Ball grid array). eWLB uses a molded epoxy area around the die to provide not only sidewall and backside protection but also space for additional I/O placement. This is the so-called fan-out zone around the die.

Fan-Out Wafer Level Packaging can be considered as reconstitution plus redistribution (Figure 7). The designs employ a reconstituted mold compound wafer, produced on a temporary carrier in the assembly process. Prior to assembly, all die on the wafer are electrically tested and Known Good Die (KGD) are identified. After dicing and singulation, the KGD from the original device wafer are used to reconstitute a new fan-out wafer on the temporary carrier and this reconstituted wafer will be used in FOWLP processing.

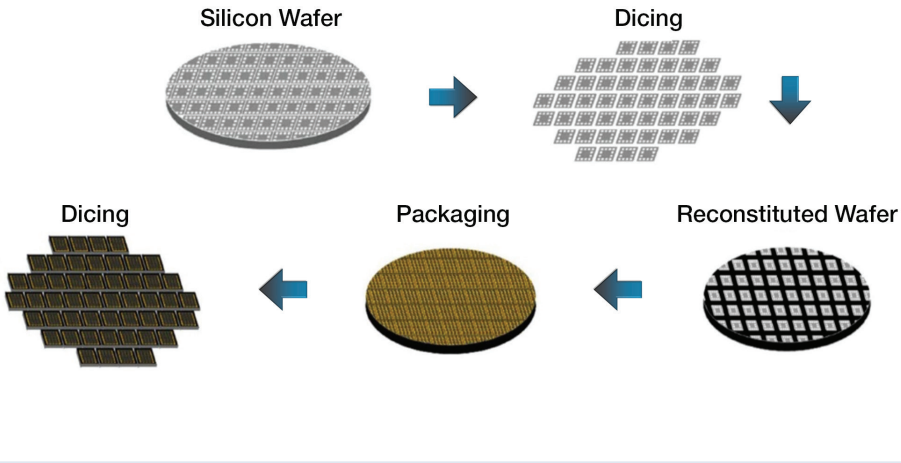

Figure 7. Process flow FOWLP [2].

FOWLP provides additional space for I/O placement by using molded area around the die for RDL and interconnects. In the die-first process flow, the carrier, with die, is overmolded with an epoxy compound and cured to produce what is known as a heterogeneous substrate or reconstituted wafer containing only KGD. The carrier is then released, the RDL fabricated and the bumps attached. The molded and bumped die are then singulated (Figure 8, left side). In RDL first designs (Figure 8, right side), the RDL is fabricated on the thermal release layer, followed by die attach, overmolding, and singulation. FOWLP provides additional space for I/O placement by using molded area for RDL and interconnects. The arrangement of the dies defines the additional space available for RDL and interconnects.

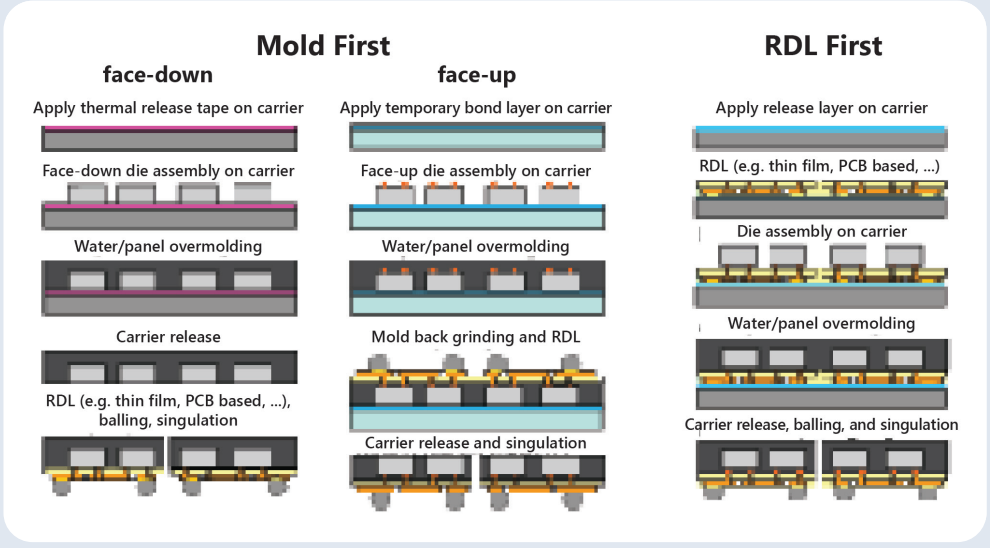

Figure 8. Process flow options for Fan-Out WLP. (Source: Fraunhofer IZM [18])

RDL layers that are fabricated on the reconstituted wafer provide more space (i.e., wider I/O pitch) for needed electrical interconnects (RDL) and contacts (Cu-Pillars or Bumps). Depending on the technology used, RDL structures can cross transition zones between silicon and the mold compound. The CTE mismatch between silicon and the mold compound can produce thermo-mechanical stress in the Fan-Out RDL structure during thermos-cycle tests and this stress can cause cracks in the RDL tracks. CTE mismatch can be addressed using several different FOWLP strategies that can improve reliability [5]. For example, die-first face-up technology can produce fully molded structures that help to increase the distance between thermo-mechanical stress areas and RDL copper tracks (Figure 8, Chapter 6.2.4). Additionally, the copper and the adhesion between copper and the polymer used can be adjusted to better withstand fatigue stress. This is especially true for the first RDL layer, where the buffer function of the dielectric and mold compound is not as pronounced. As I/O density increases, more RDL layers may be needed to distribute all contacts. The number of RDL layers depends on the application, with 2 - 8 RDL layers common [6]. The same challenges that are encountered with Fan-In WLP processing exist for Fan-Out WLP, with increases in wafer warpage with more layers and more complex topography being of particular concern. Typically, critical small L/S RDL layers are processed first and coarser layers with wider L/S are processed last, prior to bumping. The latter are less demanding in terms of surface flatness and wafer warpage.

As a result of SoC disintegration (Chapter 7), heterogeneous integration, System-in-Package (SiP), and chiplet technology are driving a trend to larger package size. Some roadmaps predict packages well over 120 mm x 120 mm (and larger) by 2026. This increase in package size is occurring in parallel with a move to finer pattern structures and greater miniaturization. This means that photolithography for RDL formation must use an i-line stepper and so-called stitching exposures. These steppers have a maximum exposure field (reticle) size of 52 mm x 68 mm and therefore larger package sizes require carefully aligned multiple exposures (stitching) as shown in Figure 9. This is especially important when going to single µm L/S structures. Stitching has been successfully demonstrated for 2µm L/S structures [7].

Different assembly strategies are used in FOWLP. Figure 10 shows an overview of the established FOWLP packaging types. FOWLP is divided into chip-first (w/assembly by embedding of chips from the tested FE wafer and RDL last) and chip-last (w/RDL first on carrier and flip chip assembly of bumped chips and encapsulation) technologies with chip-first technology further categorized into face-up (chip needs Cu-Pillars) and face-down (original chip as coming from tested FE wafer) assembly. Chip-last technology can also be classified as an advanced flip chip technology.

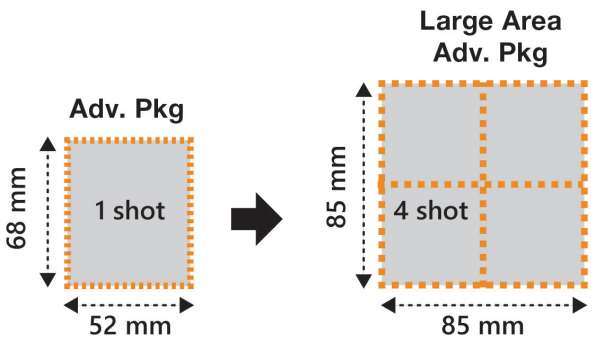

Figure 9. Stitching exposure.

The main markets for Fan-Out WLP include mobile Radio Frequency die (RF); Power Management Units (PMU); basis boards (BB (90%)); Low Density (LD) and Medium Density (MD) mobile application processors; Antenna in Package (AiP); High Density (HD) and Networking UHD (Ultra-High Density) interconnects [2].

- Market Drivers and Capabilities
  - Small footprint
  - Better electrical performance
  - Lower cost package
  - Thinner package
  - Lower thermal resistance
  - Larger package size
  - Improved reliability performance
  - PoP package capability
  - SiP package capability

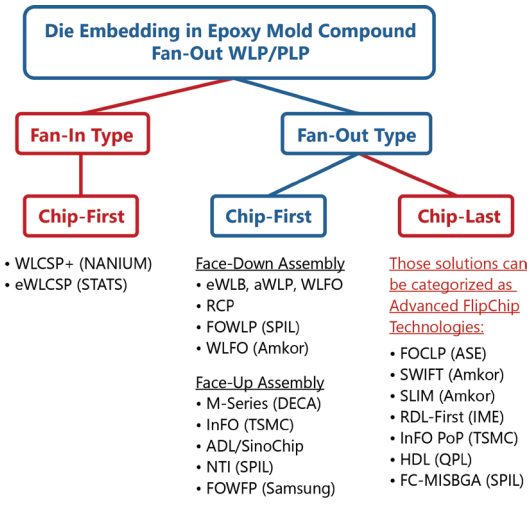

Figure 10. Overview of the different fan-out packaging types as well as assembly variations and examples. (Source: Steffen Kröhnert, NANIUM S.A., 2017)

- Enabling Technologies
  - Wafer processing
  - Bumping (in case of die-first, face-up, and die-last)
  - Thin-film RDL processing
  - Wafer molding (in case of die-first, face-down and face-up: die embedding, and creation of self-standing reconstituted wafer)
  - Low temperature cure RDL dielectric
  - Temporary bonding
  - Panel processing (for PLP only, not WLP)

6.3.1 FOWLP Technologies and Platforms

Chip-first, chip-last, and embedded die technologies are used to integrate dies into a package. In chip-first, the RDL is fabricated directly on the reconstituted wafer; chip-last technology attaches the die to a prefabricated RDL layer. Since chip-last technology requires a solder joint between the die and RDL (flip chip like), chip-first packages can be thinner than chip-last packages. One RDL (metal layer) requires two passivation layers and normally, each additional RDL (metal layer) uses one additional passivation layer. Thus, a 3L-RDL has 3 metal layers and, typically, 3+1 passivation layers. Very costly silicon chips may be attached to pre-tested RDL structures at the end of the packaging process to minimize scrap and the consequent added costs [8].

Before packaging, all chips are electrically tested at the wafer level. Bad chips are marked in an electronic wafer map and sorted out after singulation. In the singulation process, the wafer is first thinned using back-grinding techniques and then diced to yield the individual chips (Figure 11). The front side of the wafer is protected with tape during the backside grinding process. This avoids front side contamination and improves mechanical stability during the grinding process. Grinding is usually a two-step process that starts with a course grind for fast removal of the silicon (µm/min) and finishes with a fine grind and polish process that improves the surface finish. After thinning and cleaning, the back side of the wafer is taped and the front side tape is removed. Dicing and singulation is done from the front side. The wafer thickness for 200 and 300 mm diameter wafers is about 750 µm (to ensure mechanical stability and to avoid warping during thermal annealing process steps). Back-grinding (rough-grinding followed by fine-grinding) reduces the chip thickness to the desired value, typically 200-300 µm for current chips, (expectations for very thin packages are 50-75 µm). Different technologies can be used for dicing. Traditional mechanical saw dicing works

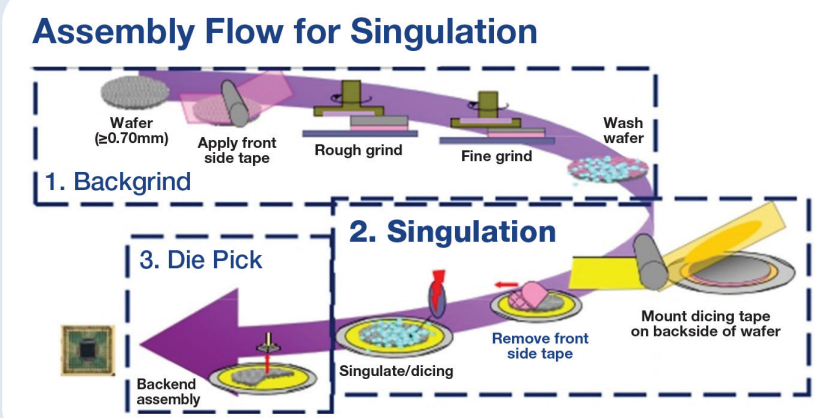

Figure 11. Process flow: chip thinning, singulation, and die pick [9].

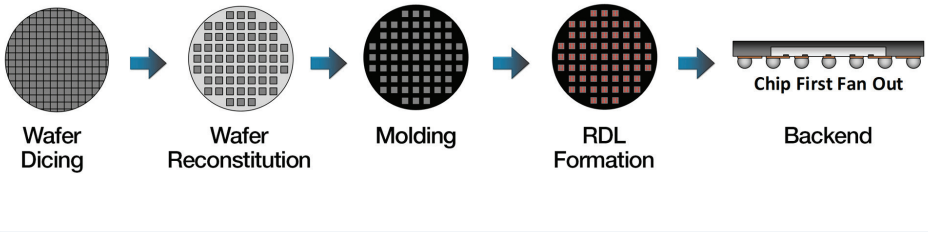

Figure 12. Process flow Chip-first technology [2].
In the case of Die-first, Face-down technology, the carrier is removed between molding and RDL formation to access the active area of the dies.

well for thick, unthinned wafers with multiple build-up layers. However, chip-out problems, water issues (galvanic corrosion), and particle contamination problems are encountered with mechanical sawing [1]. Laser grooving is used for Low-K and Ultra-Low-K wafer technologies (65 nm and below) to clean the metal structures from the kerf/dicing street, then typically mechanical blade dicing is used in mainstream applications (cost reasons). Different laser and plasma-dicing technologies are therefore used for thinner and smaller chip singulation [9].

6.3.2 Chip-first Face-down Technology

A chip-first face-down process starts with the assembly of KGD on an intermediate carrier wafer using a temporary adhesive tape (Figure 12). This is followed by over molding (embedding of the dies) and debonding of the molded wafer/panel from the intermediate carrier. The RDL, typically based on thin film technology, is built-up on the front side of the reconstituted wafer/panel (Figure 13). After redistribution, bumping is the last step, generating the interconnects. The package can be further thinned using an optional backside grinding (in the case of exposed Si backside, e.g., for cooling) and remold process. If the package has a mold backside, the final thickness can be achieved in the wafer mold process with no extra steps needed. For very thin package needs, mold backside grinding to expose the die and remold can be performed. As it is the last step in packaging, the individual chips are now laser marked and singulated, then subjected to a final electrical component test.

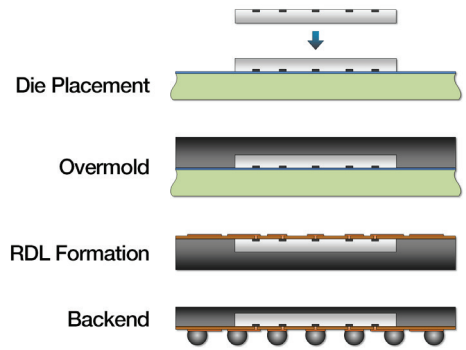

Figure 13. Process flow eWLB as example for Fan-out Die-first Face-down [2].

Chip-first face-down has the shortest interconnects with a direct plated via. This may lead to the best RF performance at high frequencies due to lower connection losses. A disadvantage is that the active chip area is relatively close to the solder, separated only by relative thin RDL layers. This can cause reliability issues (compared to chip-first face-up technology which has a mold layer as an additional buffer between the solder and active chip).

The price for the shortest connection—the challenge is the close coupling of very fine structures on active chips die with macro structure solder balls/bumps (reliability, CTE mismatch).

6.3.3 Chip-first Face-up Technology

The chip-first face-up approach (Figure 14, Figure 15) also starts with chip assembly on a carrier using a temporary adhesive tape. In contrast to die-first face-down, wafers cannot be used "as received" from the wafer fab. The die need to have copper bumps/ copper pillars and are placed face-up on the carrier. The copper bumps are fabricated at I/O locations on the native semiconductor wafer prior to the reconstitution process (which can have a "Fan-In RDL" already in place to save RDL layers in FO-Wafer processing). After molding (die embedding), a back grinding process is used to re-open access to the interconnects. The copper bumps provide current pathways through the mold from die surface. RDL built-up is done on the front side of the reconstituted wafer, providing electrical connection between the exposed copper bumps and the bump array of the WLP. After redistribution, bumping is the last step in generating the interconnects. Finally, the wafer/panel is diced for package singulation. After wafer release from the carrier, packages have bare die backsides. Optional grinding and overmold/remold or backside lamination improves the reliability of the package itself.

Advantage compared to die-first face-down:

- The active chip surface with very fine structures is decoupled from macro-structures solderball/ bumps. This yields better reliability, as Cu-Pillars function as a buffer for any CTE mismatch.

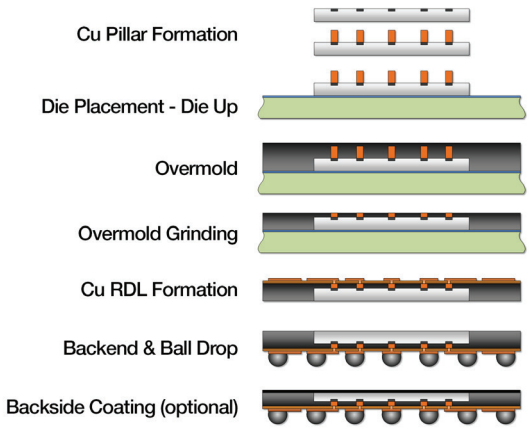

Figure 14. Chip-first Face-up technology [2].

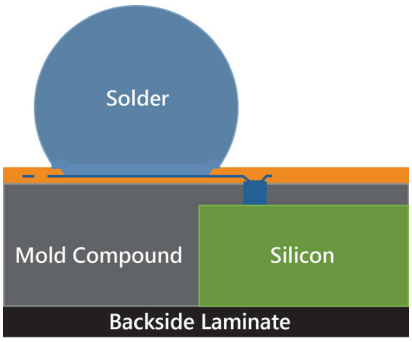

Figure 15. Chip-first Face-up technology detail [21]. Face-up needs a copper pillar in combination with a plated via and RDL.

6.3.4 Chip-last Technology (RDL-first) – "Advanced Flip Chip" Process Encapsulation

RDL-first (or chip-last) technology (Figure 16) is comparable to an advanced flip chip on substrate assembly. Bumping on the wafer level, before singulation and pick and place, is required. The RDL is applied first on an Si or glass carrier and the bumped dies are assembled by chip to wafer bonding on the RDL. This differs from chip-first face-down and chip-first face-up processes in that the RDL is not built up on the reconfigured wafer and is connected via solder bumps, as in flip chip technology. After pick and place and solder reflow, the chips are over molded. This kind of assembly technology can be used with very expensive chips/dies so that KGD and good RDLs can be combined to increase yield.

Difference as compared to die-first technologies:

- Higher accuracy, fine L/S and vias possible; no dies on defect package positions – if tested between repairability before encapsulation is possible.

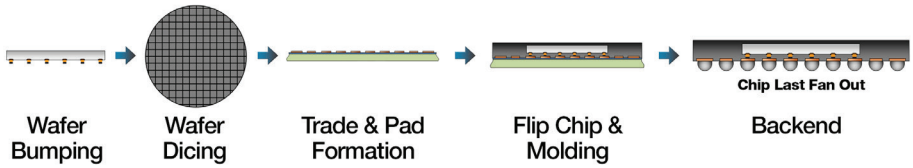

Figure 16. Die-last (RDL-first) technology [2].

Face-down and flip chip technology requires high-accuracy placement, unlike chip-first face-up technology (M-Series and InFO) in which adaptive patterning/LDI processing is used, allowing looser placement tolerance and the use of fast chip shooters. The solder joint structure in RDL first technoloy limits the pitch density and leads to usually thicker packages, as compared to chip-first technologies (Figure 12, Figure 17).

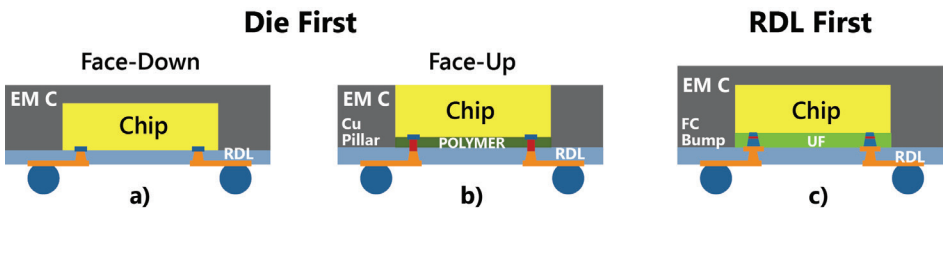

Figure 17. Build details for a) Die-first Face-down, b) Die-first Face-up, c) RDL first technology [14].

The different die integration technologies also result in different package structures. With chip face-down and chip-last technologies, the side walls and backside are protected by mold compound. With face-up technology, the backside of the chip is exposed and may need back side lamination protection.

6.3.5 Backside RDL

Backside RDL technology (BSRDL) can be used in both Fan-In and Fan-Out WLP. Through vias/ vertical contacts/3D are needed to electrically contact the back side for electrical connection. These vias are comparable to Through Silicon Vias, TSVs (Chapter 2.4.6), and are often labelled as Through Mold Vias TMVs (Fan-In: TSV; Fan-Out: TSV or TPV/TMV).

RDLs are patterned using a liquid photoresist mask with an insulating layer (lithography process: Coat, Expose, Develop), then have a PVD Ti or TiW barrier layer and a sputter copper seed layer deposited. This is followed by the electrochemical deposition of copper and mask etch or strip. The same process steps can be used to build up BSRDLs with the addition of through substrate vias for electrical connection (Figure 18). BSRDL for PLP is patterned using a patternable polyimide and sputtered adhesion layer/seed or dry film (ABF) photolithography and electroless Cu as seed. Laminated cladding can be used for layer build up and electroless copper for initial metallization as shown in reference [10]. BSRDL structures are usually larger than RDL since through-substrate vias require alignment to the front RDL that is processed on the mold compound.

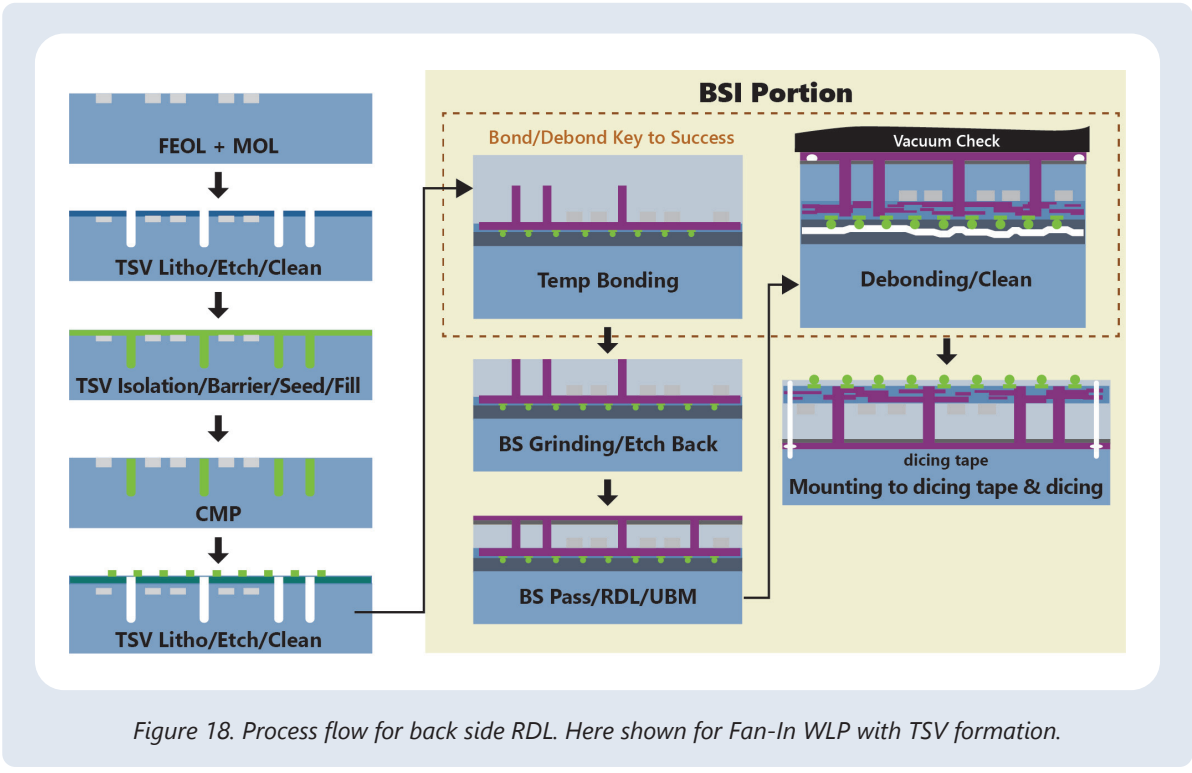

Figure 18. Process flow for back side RDL. Here shown for Fan-In WLP with TSV formation.

6.4 Fan-Out Panel Level Packaging (FOPLP)

Fan-Out Wafer Level Packaging (FOWLP) technology is evolving to accommodate heterogeneous integration (HI) and System-in-Package (SiP) that includes multiple die packaging, passive component integration in package, and redistribution layer or package-on-package approaches. The advent of HI has also produced a need to move to larger substrate formats. Rather than follow the wafer diameter roadmaps to 450 mm (which has been abandoned), panel level packaging has moved to a large rectangular panel as a cost-saving manufacturing format for FOWLP (Figure 19). Of course, switching substrates to a rectangular shape requires significant investment in a new, expensive, extra-large format processing line, and this is only commercially viable in high-volume production. The larger form factors possible with rectangular panels reduce costs and increase throughput through increased panel area (a 300 mm rectangular panel has 25% more surface area than a 300 mm round wafer, Figure 19) and through the elimination of device losses from edge effects. Panels range from 300 mm x 300 mm to 457 mm x 610 mm or 510 mm x 515 mm up to 600 mm x 600 mm or even larger [11] [12]. The Panel Level Packaging (PLP) Panel FOUP Task Force currently assumes two panel sizes: 510 mm × 515 mm and 600 mm × 600 mm, based on the SEMI 3D20 Standard [13].

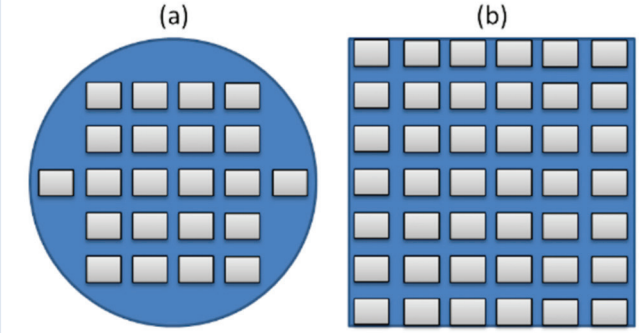

Figure 19. Fan-out packaging with wafer form (a) and panel form (b) [24].

The upscaling of technology from wafer scale to panel scale is not straight forward, requiring significant development or adaptation of materials, equipment, and processes. Carrier material selection requires consideration of not only the thermo-mechanical behavior of the material but also of properties such as weight and/or stability. Double sided adhesive tape in panel format is needed. Pick and place assembly on the carrier is a bottle neck for both wafer and panel level packaging owing to its sequential nature (most other processes are batch for both wafer and panel level technologies). Common practice is to cut the panel after RDL into smaller parts, matching the capability of the subsequent assembly equipment for bumping, marking and singulation [14]. Package manufacturers often use large panel format for the most critical and costly process, "RDL-Formation/Thin-Film Technology" only. Smaller panels (e.g., 300 mm x 300 mm, similar in size to 300 mm diameter wafer format) are used for process steps before and after. Existing equipment in the line also plays a role. Manufacturers try to avoid investment in panel equipment for those process steps where limited cost savings can be achieved by scaling up the manufacturing format.

The large area of PLP as compared with WLP places greater demands on the speed and accuracy of assembly processes. Lengthy process times on some equipment e.g., die pick and place on a panel (a sequential process) can take hours. Quality differences between first die placed (up to 4 hours previous) and last die placed need to be considered as a risk. Compression molding is typically used for chip embedding and to form the reconfigured wafer or panel, with liquid, granular and sheet type molding compounds available that all allow chip embedding (albeit with pros and cons in terms of cost, processability, and cleanroom compatibility). A large variety of lithography tools and dielectric material options exist for RDL formation. Material options such as photosensitive vs. non-photosensitive dielectrics,

liquid vs. dry-film materials, and positive vs. negative tone must all be considered. Lithographic tools that can process panel sized substrates may employ either mask-based technology (e.g., stepper technology) or maskless technology such as laser direct imaging (LDI). These technologies have different capabilities and strategies to overcome the challenges in die placement accuracy and die shift after molding. Also, solutions for grinding, balling and singulation are needed. Handling and especially automated handling solutions for molded large panels, including storage and transport, are needed. Many process flow options exist for different applications [11] [12].

The size of PLPs was the equivalent of 52 mm x 68 mm in 2024, and it is expected to grow to well over 100 mm x 100 mm after 2026. There are significant technical challenges for manufacturing as package sizes become larger. Thermal and mechanical stresses become significantly more important as package size is increased. In terms of manufacturing, the efficiency of use of the product area is decreased as package size increases. This means that the unused area when using wafers is greater than that when using panels. This increases the total unused substrate area, thereby increasing production costs. If a manufacturing platform moves from 300 mm wafer substrates to 600 mm panel substrates, the efficiency of use of the substrate area improves from 62% to 85% in 60 mm x 60 mm packages. Thus, PLP technology is a desirable option for large packages [7]. The manufacturing volume of a product must always be considered. For small and medium sized volumes and small packages, FOWLP might be a better solution than PLP. Also, panels are best suited for stable, high-volume processes, so orders having lots of only 2-3 panels are not recommended.

Manufacturers will need to run both wafer level packaging lines (for fan-in and fan-out) and panel packaging lines (fan-out only). These processes should run at or near capacity so as not to cannibalize each other. Otherwise, the potential cost benefit of large format panel processing is lost owing to the partially idle wafer level packaging line. Manufacturers need to dilute those costs to the products they produce.

Advantages for PLP technologies (Figure 20):

- Better area use
- Large package sizes
- Lower costs
- Higher throughput
- Positive environmental impact after setting up high volume production (safe base material and energy)

Challenges for PLP technologies:

- New tool park is needed (compared to existing wafer tool park)
- High volumes required to achieve the promised cost reduction and ROI
- WLP is more mature than PLP
- Higher throughput requires tight production planning to fill all production lines
- Die shift, edge effects
- Lengthy process times for pick and place (process window, stability)
- High value on one panel (significant yield impact if one panel does not yield or breaks, risk mitigation measures needed)
- Panel handling (size, weight)
- Panel warpage

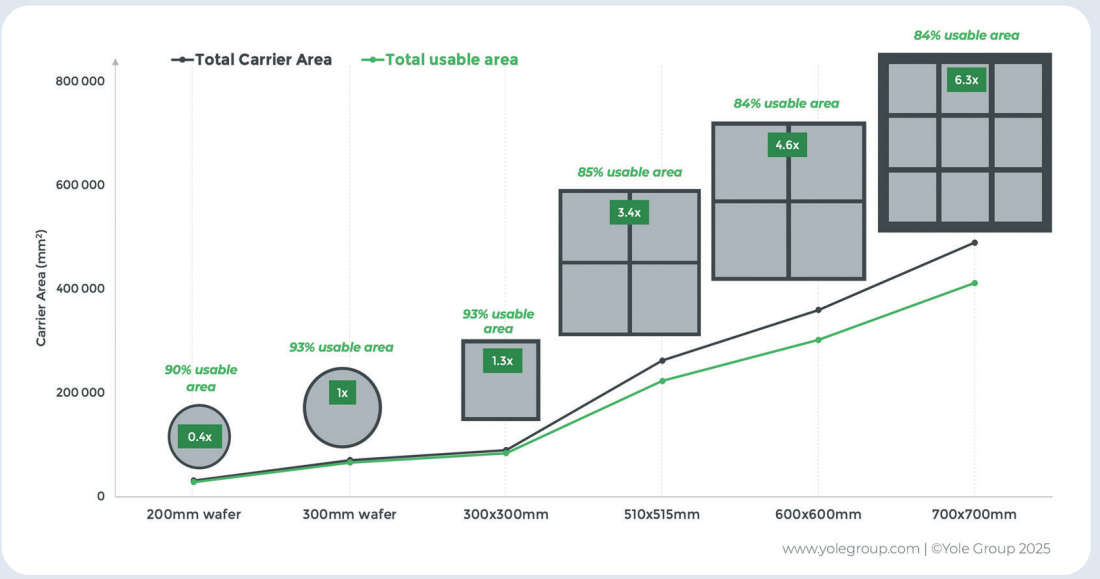

Figure 20. The benefits experienced in moving from wafer to panel processing [25].

The process steps involved in FOWLP and FOPLP are similar although the large panel areas can make process and materials challenges more difficult for PLP than for WLP. FOPLP requires specially adjusted materials, processes (e.g., spin coating of dielectric versus dry film), components, and tools that accommodate warpage issues, CTE mismatch, and shrink topics (chips may move during mold curing due to shrinkage of the mold compound). When chip shift is present, chip placement needs to be offset so that they are in the required position after molding. Algorithms have been developed that allow adjustment for chip shift for each new product. Furthermore, for multichip and SiP applications, different chip thickness might need to be accommodated [11].

6.4.1 Technologies, Materials, and Equipment Used for PLP and WLP Technology

6.4.1.1 Grinding Tape Lamination Process

Tape lamination is used during assembly, handling, and molding for the temporary attachment of components to a carrier. Typically, the tape is removed using a thermo-release mechanism (Thermo-release tape - TRT). Other release methods are mechanical peel off, chemical dissolution, and laser ablation. The tape lamination process is shown in Figure 21.

Material

TRT usually has a base layer with two sides having different adhesive behavior. The carrier-side adhesive has the property of thermal release. Thermal release often uses microscopic elastic capsules containing materials that show a liquid/gas phase transition at the desired release temperature. When heated, the capsules expand and push the carrier-side off the adhesive layer. The TRT stays on the die side and needs to be peeled off very carefully to avoid residues. Fully automated detaping tools with warpage correction are available for tape peel in which the tape is peeled at a 180° angle from the debonded, reconstituted wafer/panel [4].

Equipment

Backgrinding tape laminators

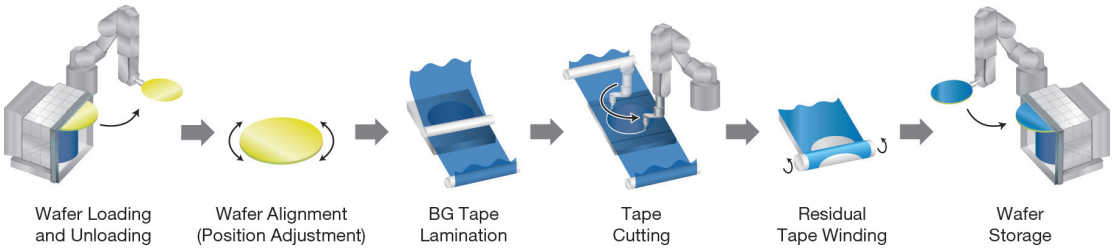

Figure 21. Release of new model back grinding tape laminator. (Source: LINTEC Corporation, www.lintec-global.com)

6.4.1.2 Wafer Backgrinding

The wafer backgrinding or wafer thinning process is a critical step in semiconductor manufacturing, as it reduces the wafer's thickness to improve the final device's performance and form factor. Thinner wafers allow for smaller, lighter, and more power-efficient devices and these are essential for applications such as smartphones, wearables, and other portable electronics. One of the primary methods for wafer thinning is backgrinding, which involves mechanically grinding the backside of the wafer to achieve the desired thickness [15].

Material

Material for grinding is made from different abrasive materials. The abrasive material used to thin the wafer is usually made of a thermal conductive material, such as:

- **Silicon carbide (SiC):** Very hard and sharp particles, SiC is an excellent choice for grinding silicon wafers. It combines a high material removal rate and excellent surface finish.
- **Diamond:** Hardest known material, giving best grinding performance, especially for hard and brittle materials like silicon. Diamond grinding wheels are often used for ultra-thin wafer grinding and applications that require high precision.

The conductive nature of the abrasive material and the carrier substrate are key factors in ensuring that the wafer is thinned to the desired thickness without damage or defects. Thermally conductive abrasive material helps to dissipate the heat generated by the grinding process and to prevent static buildup, which could damage the active features on the wafer. The wafer is typically mounted on a carrier substrate, which is conductive and helps ground the wafer during grinding.

Equipment

Special equipment is available for grinding, polishing and detaping in a single tool.

6.4.1.3 Temporary Carrier Attach

Three different classes of carrier materials are used for WLP/PLP technology: metal, glass, and polymer. The material of the carrier has significant influence on the die shift and warpage after debonding [11] [12].

Material

Metal carriers fabricated from material such as low-CTE steel are standard for FO processes. Advantages include temperature stability, mechanical stability, reusability over a long period of time. The primary disadvantage is the weight when dealing with larger panels.

A wide variety of glass carriers are available with CTEs that range between 3.3 and 12 ppm/K. Their primary disadvantage is the ease with which they may be broken. Laser debonding or UV release is only possible with glass carriers.

Polymer carriers may also be useful since the CTE of polymer materials can be widely adjusted. The disadvantage in this case lies with the limited temperature and mechanical stability of plastic carriers.

Equipment

Independent of the packaging technology employed (chip-first, chip-last), the first step is always the application of a release layer on the temporary carrier. For WLP the existing tool pack is used. For PLP separate equipment is needed (tape lamination process).

6.4.1.4 Assembly (Pick and Place) Process

The first step is to apply the thermos release tape to the carrier. This is followed by the placement of several fiducial dies that create a reference frame for all subsequent placement steps. The component assembly starts with optical recognition of these fiducials, followed by the assembly of components relative to these positions. Particle contamination needs to be avoided – panel level assembly requires ISO class 5 clean room conditions with tight control of temperature and relative humidity. The die shift needs to be considered and compensated with a suitable assembly strategy. For this, special assembling algorithms are developed for each new product compensating for e.g., CTE mismatch and mold shrink during curing [11] [12].

Material

Dies may be dissimilar materials and devices, including, passives, sensors, packaged devices, etc. They can be placed as a single die in package or in multiple die/SiP configurations.

Equipment

Modern chip shooters reach speeds of up to 150 kpcs/ hour on an area of 650 mm x 500 mm with an accuracy of ±41 µm @ 3δ. This is a large tolerance for FO processing. FOWLP on 300 mm reconstituted wafers, by comparison, uses flip chip die bonder placement tools that historically have had a typical tolerance of ±15 µm; these tools are currently moving to ±6 µm accuracy. Perhaps unsurprisingly, an examination of the specifications of different chip shooters shows a conflict between high speed and accuracy.

6.4.1.5 Compression Mold Process

Two different processes can be used for molding (Figure 22). Transfer molding is used for ball grid arrays and other lead technologies as well as for power applications. Compression molding is used for WLP and PLP processes to minimize the die shift caused by flow drag force in transfer molding processes. Compression molding is also used when there are restrictions due to residual stress and when there is a lack of packing caused by the high flow length and low mold cap thickness over a large forming area [16].

The compression molding process is critical for achieving reliable and efficient packaging in semiconductor devices. In the molding step, the tool is first evacuated to avoid bubbles or voids during processes then the molding compound is dispersed or distributed according to the compound type and the specific package needs. Granular and sheet molds need increased process temperatures to melt the mold material.

When dealing with large area cavities, compression molding process parameters (temperature, closing speed, and final pressure) need to be carefully balanced to ensure that the mold material spreads evenly and fills all gaps between the package components. Following the fill and spread phase, the EMC (epoxy mold compound) must be cured until the panel on the carrier is stable enough to be removed. Eighty percent of the mold material is cured in this mold cure phase and gelation of the EMC is obtained. Any chemical shrinkage during this part of the curing phase can stress the assembly and carrier, producing warpage. A post mold step completes the polymerization conversion of the mold materials. The last step after mold processing is release from the carrier.

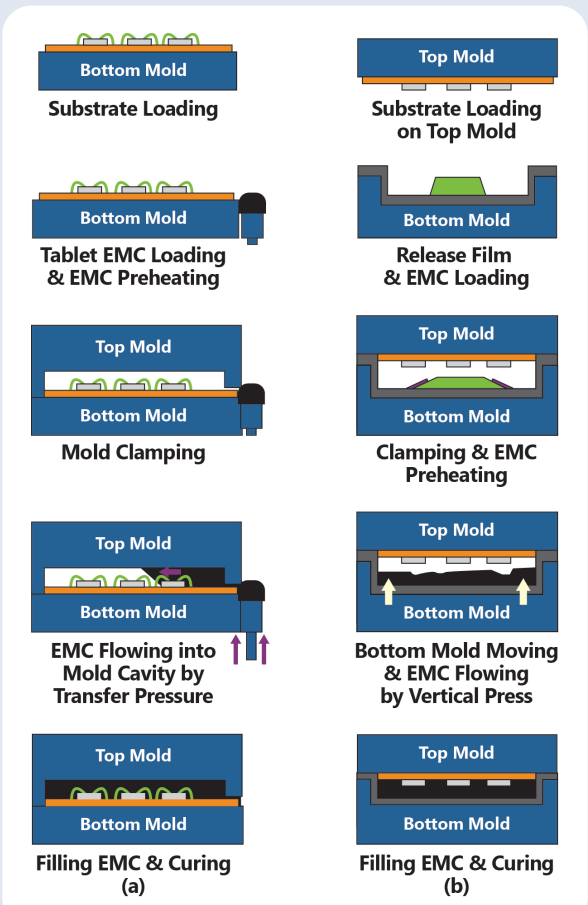

Figure 22. Transfer molding (a) and compression molding (b) process steps [16].

Material

Molding materials (epoxy mold compound EMC) can be liquid, granular, or sheets. For FOPLP liquid (paste-like) materials are often used owing to compatibility with clean room environments. Low extrusion temperatures allow the mold to cool faster, increasing throughput. The filler (SiO_2) content may be up to 90% to control CTE (range of 7 ppm/K) and mechanical stability/stiffness.

Equipment

Compression molding equipment usually works with liquid, sheets, and granular mold resins. The tools have 100% resin utilization (zero waste) and do not require a transfer mechanism (as needed for transfer molding). Heat sink technology is usually used to cool the caps faster and to increase throughput.

6.4.1.6 RDL-Stack Formation (See also Chapter 2.4.3)

An RDL reroutes the signal and power connections to the chip and connects it to the outer world. Since the feature dimensions in Advanced Packaging RDLs range between 5 µm and 0.5 µm L/S (line/space). This has been achieved primarily in die-last processing. For de-first processes, 20 µm, 15 µm, and 10 µm L/S appear to be mainstream owing primarily to via formation/catch pad size and via size limitations. Thin-film processes are used to generate the fine RDL metal structures. As the feature sizes get smaller, planarity (substrate warpage as well as inhomogeneity in stack build up) of the whole panel becomes more important during the stack build up.

Material

There are a variety of different dielectric materials and lithographic options for an RDL on a reconfigured panel:

- Material requirements for a good dielectric
  - Low cure temperature
  - Good mechanical properties
  - Heat resistance
  - Produces a good insulating dielectric layer
  - For certain high frequency applications, a very low dielectric constant material is needed
  - Large area coating ability
  - Precise fine patterning and simple blind via formation must be possible using photolithographic processes
- The selection of dielectric materials is limited due to mandatory low temperature curing.
  - Polyimide (PI) is an excellent choice since its curing temperature is typically 350°C.
  - "Low temp cure PI" (often PI/Polybenzoxazole (PBO) blends) can be cured between 160° and 180°C.
  - Photo-imageable dielectrics, PIDs, are PI/PBO photoresist materials that facilitate fine patterning.
    — PIDs can be used for either negative or positive resist, depending on their formulation and intended application. Whereas positive resists are often easier to process, negative resists allow higher resolutions and fine line widths [17].
- Due to the rectangular shape and size of the panels, spin coating is not the preferred method for application of the dielectric for PLP.
  - Dry film is a cost-effective alternative.

Coating Equipment

Spin coating equipment is used for round substrates and film lamination (dry film) equipment for panel shaped substrates. PCB equipment can be used for panel lamination.

Lithography Equipment (Coat-Expose-Develop)

- Stepper technology or laser direct imaging (LDI)
- Due to warpage and die shift laser direct imaging (LDI) usually gives better results with organic substrates.
- Die shift is compensated by adaptive patterning techniques.
  - Fast automated optical inspection is needed.
  - Layouts for LDI are automatically adapted to compensate misalignments.
  - LDI is a highly productive lithographic technique – 457 x 305 panel can be imaged within 1 min.

Metal Deposition and Etch

- Sputter technology (mainly used for WLP since an appropriate tool suite is available)
- Electroless plating as an alternative to sputtering (especially for panel processing)
- ECD (Electrochemical Deposited) copper plating
- Seed layer etch technology

Metal Deposition Equipment

Copper layer thickness for seed layers is between 50 and 300 nm. PVD is also the method of choice for dry metal depositions and for seed layer depositions where a very thin metal layer needs to be applied. Wet chemical electroless copper is an alternative method for seed layer deposition. These metal deposition methods require distinct equipment. PVD requires a high vacuum environment and, in some instances, plasma pretreatment. The equipment needed for electroless copper is much simpler, requiring just one heated wet chemical tank per process step (Chapter 4.5.5). With wafer substrates, ECD copper plating is performed in a fountain plating tool. Panels are ECD coated using wet chemical tanks with vertical positioning of the substrate (Chapter 4.7) .

Subsequent process steps are solder bumping (Chapter 2.4.2), marking, package singulation (laser) and electrical testing of the final package.

6.4.2 Reliability Testing of FOPLP

Typical tests to proof reliability of package:

- Thermal cycle test (-55 – 125°C, 15 min dwell, 1000 cycles)
- Pressure cooker test (121°C, 100% RH, 2 atm, 300 hours)
- High humidity storage test (85°C, 85% RH, 1000 hours)
- Elevated temperature storage test (125°C, 100% RH, 1000 hours)
- Drop test (1500G, 0.5 ms, 100 drops)
- Electrical testing
- Solder joint reliability test

6.5 MKS Product Solutions

6.5.1 ECD Equipment: Multiplate® and G-Plate® (WLP and PLP)

Single wafer/panel tools, such as Multiplate® or G-Plate®, handle and treat each substrate separately. Both tools can be used for packaging and IC substrate applications for the metallization of substrates of different sizes. Multiplate can handle 200 mm as well as 300 mm wafer or maximum 650 mm x 610 mm panel for the Multiplate panel version. G-Plate can handle a maximum 610 mm x 510 mm panel. After a substrate is transferred from a hand-over station or from load ports, it is fixed in a substrate holder. A transportation system then moves the holders/substrates from module to module along the line in a vertical mode.

Process modules are arranged in a row as with vertical hoist type equipment. Having one substrate in one module, process parameters such as solution flow, current density and/or application of shielding can be optimized for specific panels. Two kinds of ECD tools are in use, differentiated by the manner of chemical solution flow:

- Direct fluid supply to the panel (G-Plate)
  - The fluid flows through the anodes, directly to the panel. It generates a strong flow with a high solution exchange rate for fresh chemistry at the plating surface.
- Fluid agitation by paddles (shear plates) (Multiplate)
  - Fresh chemistry is supplied from the bottom of the tank at lower speed. Shear plates oscillate at high speed to produce strong turbulence and thereby a better solution exchange at the panel surface. In these tools shielding can be applied to optimize electrical current flow.

High solution exchange enables current densities of up to 5 ASD for fine line/spaces plating as with RDL plating, or more than 20 ASD for pillar plating. The high solution exchange rates and dedicated plating conditions allow single substrate systems to achieve near-perfect uniformities of 2% or better.

The complete ECD system is housed under clean room conditions compliant with ISO 5 for ambient particle control. Fine filtration of the plating solutions further minimizes the particle load within the process. For pattern plating of fine line/spaces, such as RDL plating, this is essential for the avoidance of shorts or similar defects and for the maintenance of high device yields.

6.5.2 ECD Chemicals: Spherolyte® Cu UF2/UF3, Spherolyte® Ni, and Spherolyte® SnAg

Fan-In (as well as Fan-Out) WLP requires galvanic copper plating of RDL, Pad, and Pillar structures. The main quality criterion for both processes is a good surface distribution of the deposited copper. Considering the missing planarization technology for RDL build up, this is of more interest since the number of RDLs is increasing.

MKS Spherolyte® Cu UF2 is a copper plating process that provides excellent coplanarity and feature shape. It requires a nickel layer between the copper and solder cap to avoid interface defects.

MKS Spherolyte® Cu UF3 exhibits excellent coplanarity as well but without the need for a nickel layer between the copper and solder, since the copper is designed to be compatible with the solder cap. No interface defects are obtained after reflow. Additionally, UF3 copper is made to withstand fatigue stress in RDL lines, which can occur during thermocycle tests of the package and therefore provides superior reliability results.

MKS Spherolyte® Ni is a sulfamate nickel process. Nickel acts as a diffusion barrier between the copper and solder (if needed). Unlike competing processes, the high-volume, manufacturing-proven Spherolyte® Ni process is an all-liquid additive process (important in a clean room environment). Even such important additives as sulfamic acid and boric acid are delivered into the process as solutions. Spherolyte® Ni has a wide operating window, with exceptional stability and ease of analysis and control, making it an optimal process for OSATs.

MKS Spherolyte® SnAg is a solder plating process. It is cost-effective and has been qualified for direct metal replenishment (up to 70% cost reduction compared to conventional replenishment). It produces outstanding uniformity especially for small solder deposits, where uniformity is key (good uniformity translates to a very even solder volume distribution). The process is robust and survives more than 200 Ah/l adding to the cost benefits. It produces a high purity deposit with low voiding tendency.

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Chapter 7

Integration in Packaging

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7.1 Monolithic Integration (System-on-Chip)

"Monolithic Integration" integrates different components on a single die to produce a System-on-Chip (SoC) that incorporates elements such as a Central Processing Unit (CPU), a Graphics Processing Unit (GPU), memory, etc. An example of an SoC incorporating different functionalities is shown in Figure 1. SoCs typically have low power consumption, high performance, and small area footprint which makes them ideal for use in mobile products such as smartphones, tablets, notebooks, and wearables. The high development and production costs associated with increased transistor miniaturization led to system development that employed alternative technologies, including System in Package (Chapter 7.3) and chiplets (Chapter 7.6). Additionally, increasing complexity requires a larger number of electronic components and this, in turn, results in larger die sizes. Yields drop significantly with increasing complexity and chip size (Figure 2).

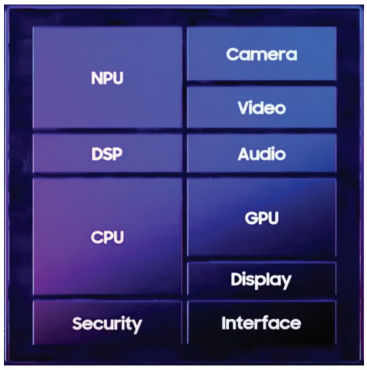

Figure 1. An example of monolithic integration used to form a SoC (Samsung's Exynos 990 5G processor) [13].

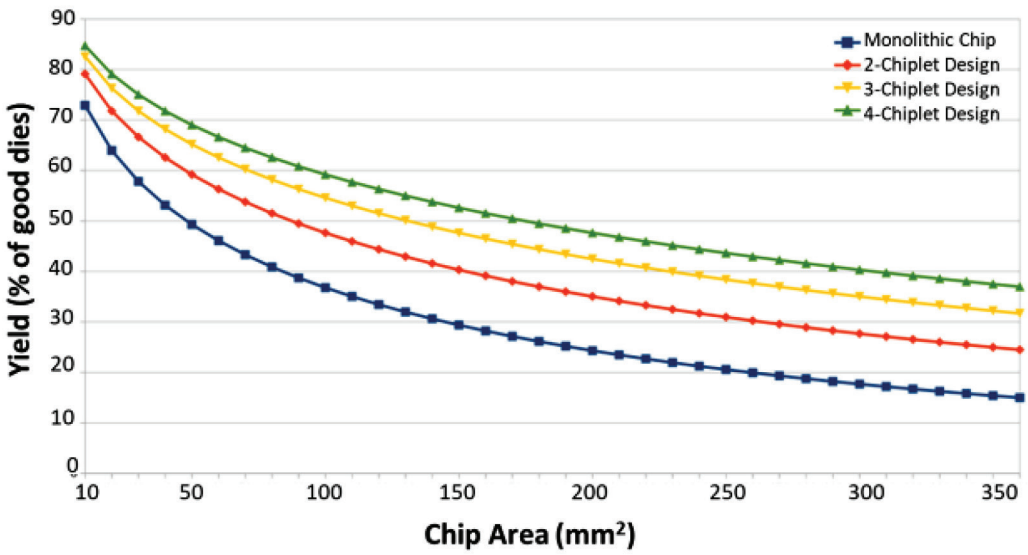

Figure 2. Yield vs. chip area for various chiplet designs of monolithic chips [14].

7.2 Die Stacking

7.2.1 3D IC Packaging and 3D IC Integration

3D integration comprises two main aspects: 3D IC packaging and 3D IC integration. Both involve the vertical stacking of chips; the key difference between them is that 3D IC integration uses through silicon vias (TSVs), but 3D IC packaging does not. Vertical die stacking is the process of mounting multiple chips on each other. Aside from space saving, die stacking results in better electrical performance and reduced power consumption due to a shorter routing of electrical signals through the interconnections and between circuits. A general requirement is that the stack must be thermally and mechanically stable on the substrate. At the same time, the resulting package must be as thin as possible, with die interconnections that are electrically reliable.

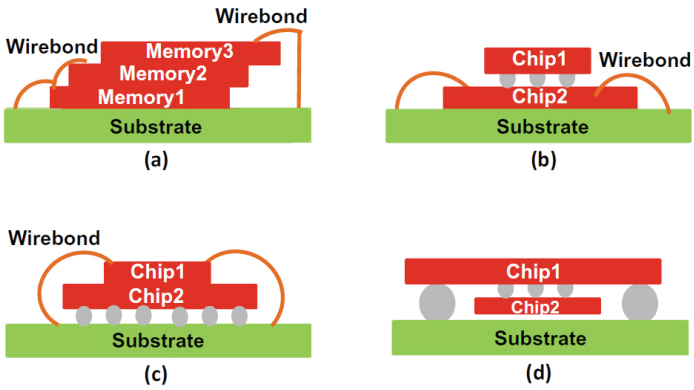

Figure 3. 3D IC packaging. (a) Memory chips stacked with wirebonds. (b) Face-to-face bonding with wirebonds to the substrate. (c) Back-to-back bonding with wirebonds to the substrate. (d) Face-to-face bonding with solder bump/ball to the substrate [14].

7.2.2 3D IC Packaging

Today's packaging technology includes several approaches of 3D IC packaging, some of which are illustrated in Figure 3. In Figure 3a memory chips are stacked and interconnected using wirebonds. A similar layout was applied in an eight-stack flash memory in Apple´s iPhone manufactured by Samsung (Figure 4). Figure 3b showcases two chips that are solder-bumped face-to-face via flip chip and in which the lower die is wirebonded to the substrate. Sony applied this type of design for a 5-chip stack in their Playstation (Figure 5). Two (DDR2) SDRAMs and a spacer die are stacked and interconnected using wirebonds. The 1 GB wide I/O

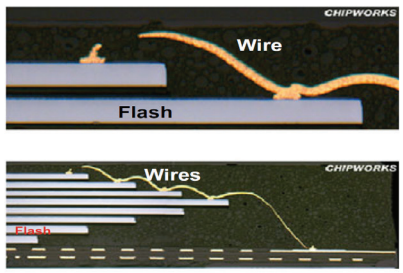

Figure 4. Eight flash memory chips stacked by Samsung for Apple´s iPhone [13] [14].

SDRAM and the processor are connected in a face-to-face solder bumped flip chip arrangement with wirebonding from the processor to the next level interconnect. Figure 3c displays back-to-back bonding. Here the bottom die is attached via solder bump flip chip to the substrate, while the top chip is connected using wirebonds. Intel used such a design for the modem chipset in iPhone XR (Figure 6). The graphic illustrates that the application processor (AP) is connected by solder bump flip chip onto a 3-layer embedded trace substrate (ETS). The DRAM is die-attached on the backside of the AP and interconnected with the ETS using wirebonds. This configuration demonstrates back-to-back bonding with wirebonds to the substrate. Another design, Figure 3d, illustrates two chips that are face-to-face solder bonded and in which the top (larger) chip connects to the substrate using solder balls.

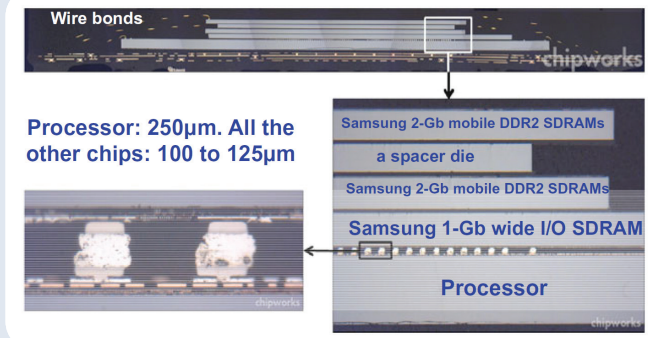

Figure 5. Sony´s Playstation CXD53135GG: 5-chip stacked (face-to-face with wirebond and solder bump flip chip) [1] [2].

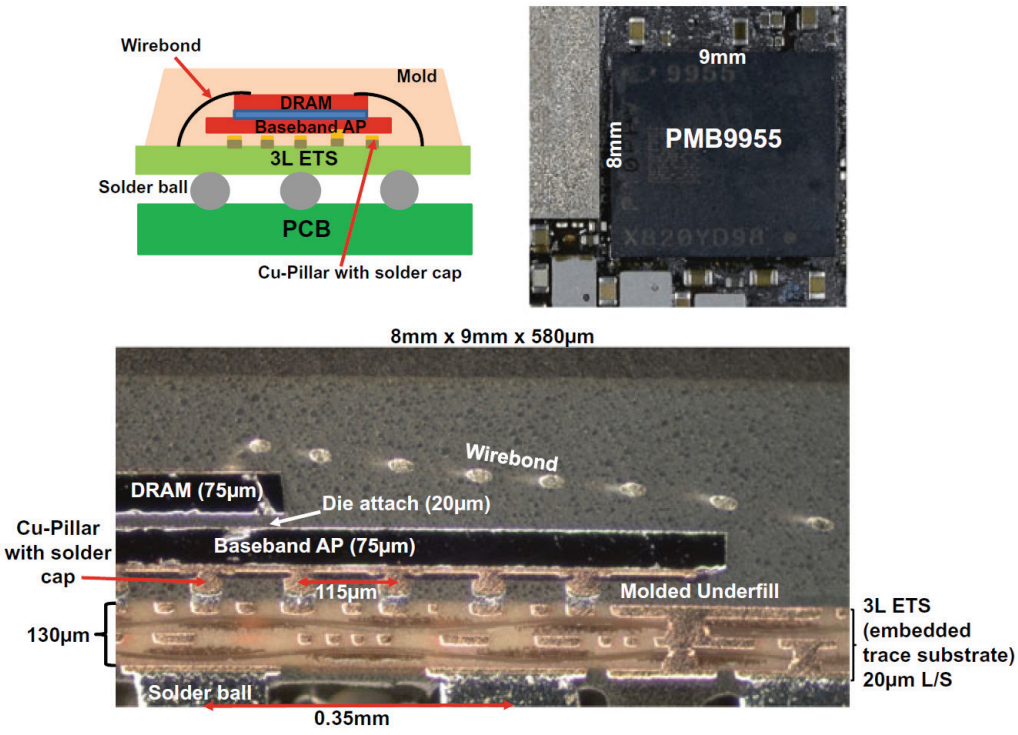

Figure 6. Intel's back-to-back bonding using wirebonds and solder bump flip chip [13] [14].

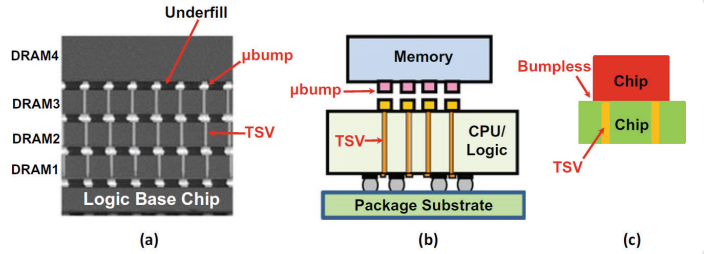

Figure 7. 3D IC integration: (a) Memory stacking with microbumps and TSVs. (b) Memory on logic with TSVs. (c) Bumpless hybrid bonding of chip-to-chip with TSVs [13] [14].

7.2.3 3D IC Integration

As previously mentioned, 3D IC integration is a concept that uses the vertical stacking of chips and through silicon vias (TSVs). Figure 7a shows the stacking of DRAMS and a base logic element with TSVs and microbumps. Figure 7b illustrates the attachment of a high bandwidth memory chip onto a logic chip with TSVs using microbumps. In Figure 7c another scenario is shown wherein a bumpless chip is bonded onto another bumpless chip by TSV and hybrid bonding. The decision of whether chips with TSVs are bonded using microbumps or the bumpless hybrid bonding method is determined by the pitch size between the pads. Figure 8 displays a comparison of chip stacking with TSVs which are either microbumped or hybrid bonded.

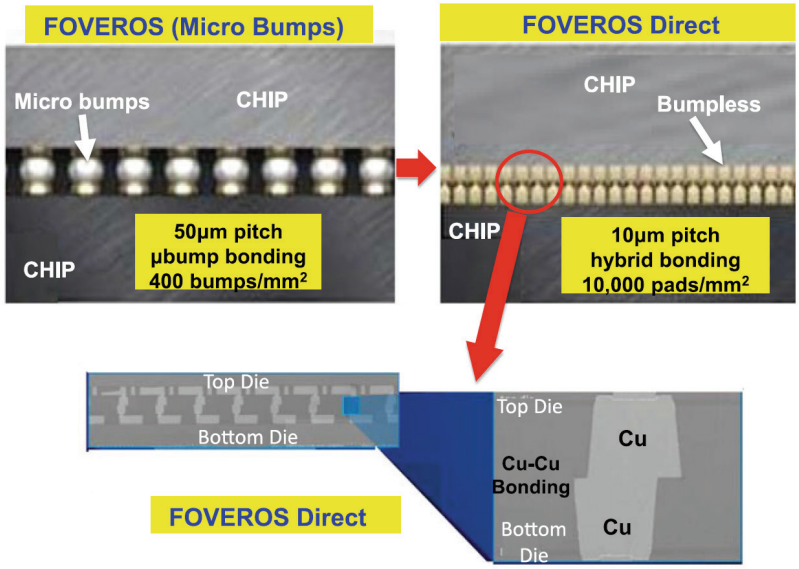

Figure 8. Chip stacking with TSV: (left) with microbumps; (right) bumpless (hybrid bonding) for Intel´s FOVEROS [13] [14].

7.3 System in Package

System in Package (SiP) has gained increasing importance as the fundamentals of physics have made reductions in transistor size more and more challenging. Advanced packaging technologies such as SiP have been identified as powerful design approaches that can maintain rapid progress in computational power. This shift is reflected by the term "More-than-Moore", a phrase that refers to a greater focus on increasing the functionality and efficiency of electronic systems through the integration of different functionalities in a single package (SiP) or a single die (SoC) rather than solely focusing on transistor scaling (Moore's Law).

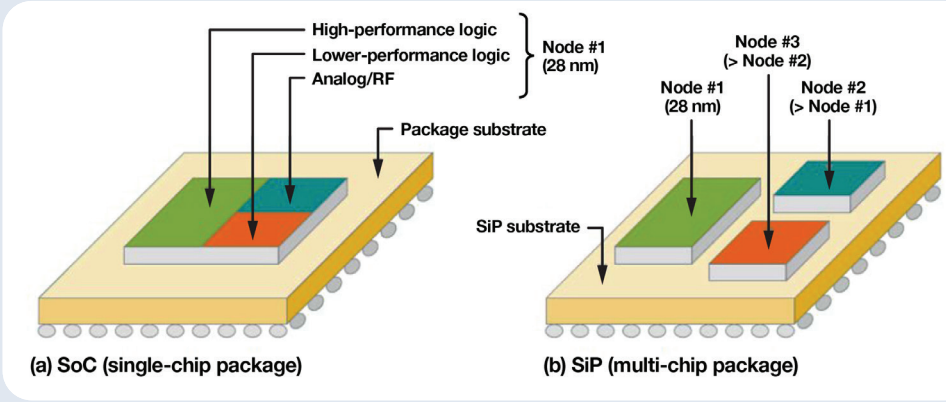

Figure 9. SoC vs. SiP.

SiP differs from System-on-Chip (SoC) in that it integrates diverse components in the same package instead of combining them on the same die. This means that multiple chips with different functionalities are included in a package rather than being integrated at the same level as with SoC. Each chip retains its individual functionality with a package consisting of e.g., processing units, memory modules, sensors, and other specialized components. Mounting of the different elements is carried out on a package substrate which provides both physical stability and electrical communication between the various units (Figure 9). SiP can be seen as the link between SoC and design at the PCB level, combining both the strengths and the challenges of each. Thus, we can distinguish three levels of integration: (level 1) integration on a chip (SoC), (level 2) integration in a package (SiP) and (level 3) integration on the PCB level (Figure 10). Each of these design strategies has its own characteristics (Table 1) [1]. All are employed in the fabrication of modern electronic devices.

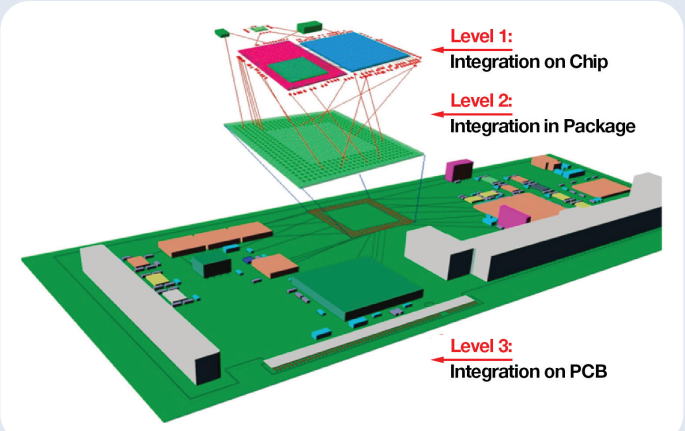

Figure 10. Levels of integration including integration on a chip (level 1), integration in a package (level 2) and integration on a PCB (level 3) [1].

Characteristic	SoC	SiP	PCB
Main Material	Semiconductor	Conductor Insulation	Conductor Insulation
Volume	Small	Medium	Large
Cost	High	Low	Low
Period	Long	Short	Short
Type	One Chip	Multiple Chips	Multiple Chips
Function	Simplification	Diversification	Diversification

Table 1. Characteristics of the three levels of electronic integration [1].

Increased performance, reductions in device size, and improvements in energy efficiency were all strong drivers for developments in SiP technologies. The modular design enables engineers to choose and combine the most efficient electronic elements available on the market and to integrate them in a single compact package. In contrast with SoC, the approach allows the use of chips and parts from different suppliers, each with their own specific and optimized characteristics and created by unique, perfected manufacturing techniques. This allows the designer to use a "best of breed" approach for the inclusion of different functionalities within the package. Moreover, costs and time-to-market can be reduced through the use of SiP since it can expedite the development process through the use of pre-existing, off-the-shelf components. Finally, scalability is another important advantage since new components are easily added or existing ones updated, without the need of redesigning the entire system.

Typical SiP build-ups are shown in Figure 11. Packages can include different elements, such as memory, microprocessors and microcontrollers, Application-Specific Integrated Circuits (ASICs), voltage regulators, power management ICs, analog/digital converters and passive components like resistors, capacitors, or inductors. As well, Radio Frequency (RF) components or sensors may be included. Improvements in miniaturization and electrical reliability can be achieved by mounting the chips on glass, ceramic or, most often, silicon interposers (Figure 11, left image).

Design options for SiPs may include side-by-side mounting, stacking or utilization of pre-packed ICs (e.g., by leadframes) (see Figure 12). Additionally, face-to-face (F2F) or POSSUM™ stacked configurations are possible in which two or more devices are assembled face-to-face and where a smaller die is nested within I/O-free areas of the larger die. As well, recessed and cavity substrates can be used that feature a

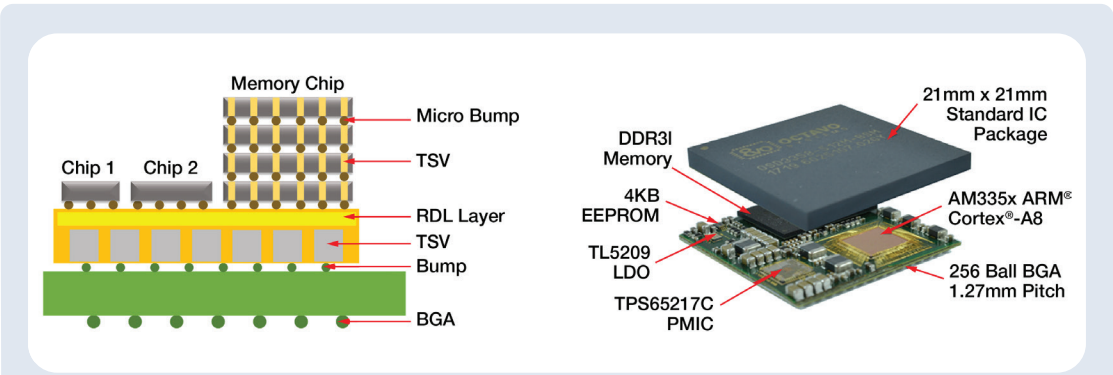

Figure 11. Typical SiP architectures [1] [15].

recessed area or cavity within its structure. These areas are designed to accommodate specific components, such as integrated circuits (ICs), microelectromechanical systems (MEMS), sensors, or other parts.

These different packaging techniques may be applied to produce increasingly complex 2.1D, 2.3D, 2.5D, and 3D architectures (Chapter 2.3) or in stacks of packages (Package-on-Package, PoP) (Chapter 7.4).

SiPs can use different interconnection types, including wire bonding and solder bumps. The latter are especially important for connecting a chip to the substrate in a flip chip configuration. Solder bumping provides advantages in terms of signal quality, power efficiency and flexibility compared to the traditional wire bonding approach.

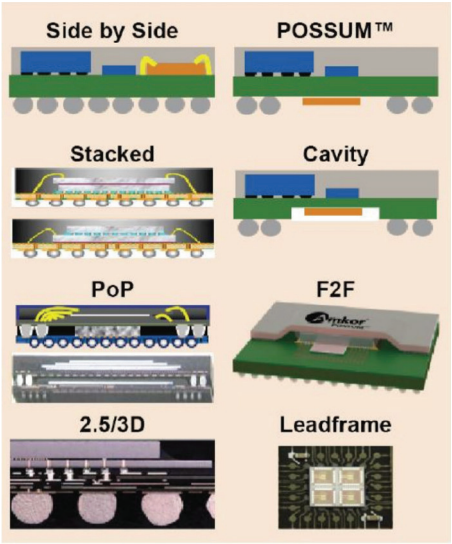

Figure 12. SiP module design options [16].

Designers have the option to increase the level of integration by using different architectures, such as Fan-Out Wafer Level Package (FOWLP) or Embedded Multi-chip Interconnect Bridge (EMIB). Another advanced package concept is the Double-Sided, Molded Ball Grid Array (DSMBGA) (Figure 13). It is commonly used in 5G network packaging, since it allows the effective implementation of digital, analog, and Radio Frequency (RF) functions. In DSMBGA designs, the strip milling molded underfill (MUF) method is used for top and bottom filling of the package. DSMBGA architectures allow molded assembly antenna tuner components as well as the implementation of front-end modules which may consist of a Low Noise Amplifier (LNA), a power amp, RF switches, RF filters and duplexes [2]. As the complexity of all advanced electronic systems increases, components within the system become vulnerable to Electromagnetic Interference (EMI) and must be appropriately shielded. EMI affects the functionality of all electronic technologies, and it is rapidly becoming a major functional and safety issue. Malfunctions caused by EMI in safety-related electronics can lead to serious safety risks for people or the environment as well as financial risks for manufacturers and service providers. Compartmental or conformal shielding elements are included to reduce the electromagnetic interference in all advanced packaging designs. Electromagnetic shielding reduces the electromagnetic fields present within a space by blocking the field using barriers made of conductive or magnetic materials. EMI shields isolate components, minimize crosstalk, and reduce EMI susceptibility without impacting system speed. To achieve good EMI shielding on integrated circuit (IC) assembly, manufacturers are switching from metal cans to other methods such as conductive painting, sputtering or Chemical Vapor Deposition (CVD) on top of molding resins as a consequence of further miniaturization of electronic devices [1]. MKS has developed RoHS and REACH compliant adhesion systems and electrolytic plated metal layers for molding resins, engineered plastics, and dielectrics to ensure proper Electromagnetic Shielding (EMS).

A variety of parameters must be considered in the design of SiPs if that design is to achieve and maintain the desired function of the device. Careful electromagnetic interference reduction is essential in the package design, not only for 5G modules, but also for other SiPs such as power modules. Undesired energy transfer to other components through coupling paths can cause severe problems. Parasitic effects can disturb the power integrity of a device producing a voltage drop and power supply noise. A reasonable panning of the device by optimizing component placement and interconnections, as well

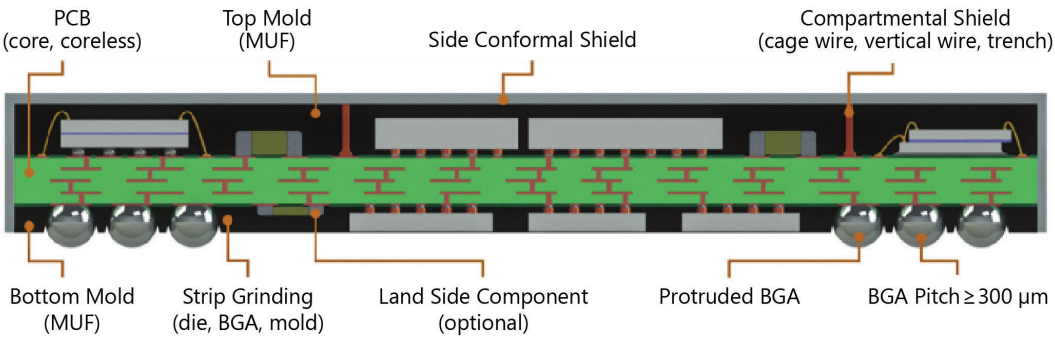

Figure 13. Schematic layout of the DSMBGA package [2].

as the usage of suitable materials with shielding and insulation properties can help to overcome such issues. Signal integrity problems can disturb signal transmission in cases where the transmission line impedance is discontinuous, resulting in reflection phenomena. Such effects can generally be overcome by impedance matching based on the choice of substrates with strong RF properties and low dielectric constants. The optimization of solder junctions in size and position is another key factor [1].

In addition to electrical properties, the SiP design must fulfill specific mechanical and thermal requirements to achieve reliability criteria for a given customer application. Effects like warpage, delamination, cracking, plastic deformation, or connectivity defects must be prevented over the whole lifetime of the device. Optimized locations of components and the utilization of suitable materials and production techniques can be effective tools in overcoming these challenges. Stress measurement methods based on X-ray diffraction, indentation, or curvature can be used to support the development of optimized packages. Thermal management also needs to be addressed in the SiP design since electrical energy is continuously converted into thermal energy due to the device's internal electrical resistivity. The use of materials with similar low coefficients of thermal expansion (CTEs) can help to protect the SiP from stress-derived defects. The incorporation of heat sinks and high thermal conductivity materials facilitates the transport of thermal energy to the outside of the package and thereby prevents overheating. The integration of Through Silicon Vias (TSVs) into a chip can also be considered in designing for thermal management, since their high thermal conductivity can help in transferring thermal energy. Thermal characterization of the SiP can be accomplished by simulation and measurement techniques like thermal imaging, finite-element analysis, phase-locked infrared thermal localization, X-ray scanning or the thermal resistance matrix method [1].

7.4 Package on Package

Package on package (PoP) is a technique for integrated circuit packaging that involves the vertical arrangement of separate logic and memory ball grid array (BGA) packages. This method stacks two or more packages on top of one another to get a lower profile. Figure 14 shows a sketch of the PoP design for Apple´s A9 application processor in an iPhone 6 Plus. In this example, the bottom package contains the logic and the top package, the memory. The logic has a C4 solder bumped flip chip on the bottom substrate. The stacked memory dies are wire bonded onto the top substrate and the top package is again solder bumped flip chip on the bottom package. The whole package is covered with a mold compound.

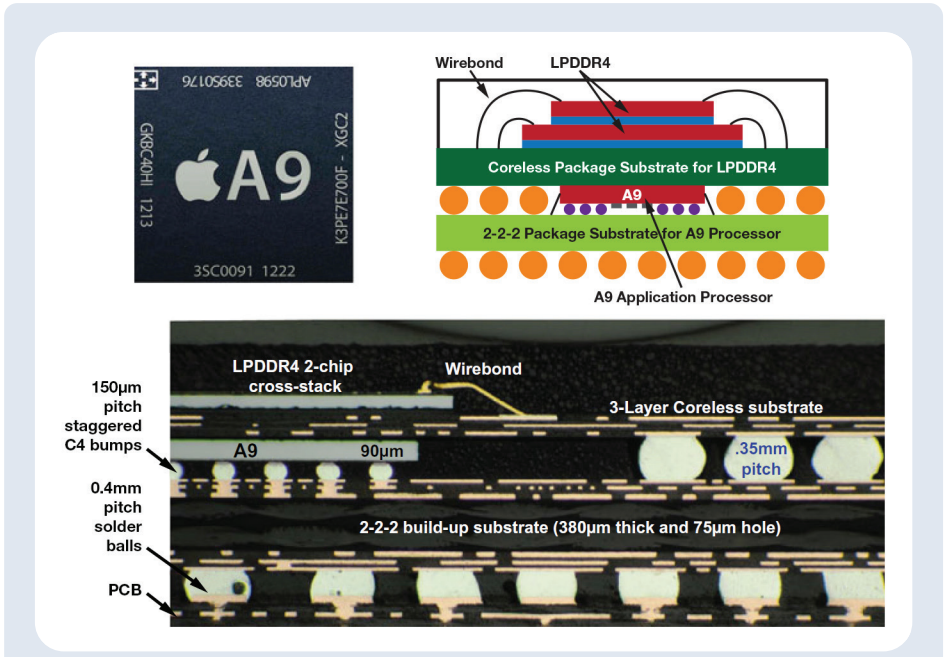

Figure 14. Apple´s A9 processor with PoP flip chip technology [13] [14].

There are various types of PoP configurations; one of the most innovative is TSMC´s Integrated Fan-Out (InFO) wafer level packaging technology. Figure 15 shows a PoP format with InFO technology applied for the bottom package. Fan-out technology was described in detail in Chapter 6. Key features of this technology are the elimination of the substrate and the mounting of the chip directly on the motherboard which allows a reduction in the package height. Figure 15 illustrates the A12 processor. It is mounted on an RDL (Fan-Out), and the top package is connected by through InFO vias (TIVs). The top package contains a conventional substrate with memories in a side-by-side configuration.

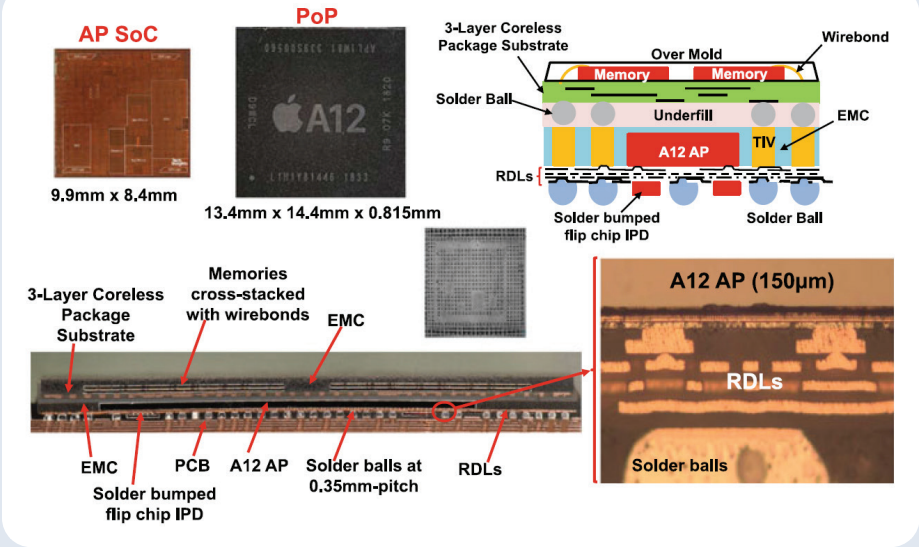

Figure 15. PoP with TSMC´s Integrated Fan-Out Wafer Level Packaging technology (InFO WLP) for Apple's A12 [13] [14] .

PoP assembly uses space more efficiently, as packages are stacked vertically, leading to a reduced footprint on the motherboard. This reduces the space requirement for PoP PCB assemblies allowing smartphones and other compact electronic devices to achieve higher levels of performance without increasing in size. Stacks with more than two packages are uncommon due to heat dissipation considerations. PoP employs a significantly smaller PCB area, nearly comparable to that of stacked-die packages, but shows some benefits over it. The main advantage of PoP is that the memory is decoupled from the logic. As a result, PoP offers all the benefits of conventional packaging techniques over stacked-die products such as separately testing of memory and logic, higher yield of "good packages", and increased logistical flexibility as memory and logic from different suppliers can be combined.

7.5 Heterogeneous Integration

Chapters 7.1 and 7.3 noted that advances in transistor integration into integrated circuits are slowing down due to physical limitations and increasing process costs. Deviations from Moore's law started to become obvious by the year 2010 and, by 2022, Jensen Huang, CEO of Nvidia stated: "Moore's law is dead" [3]. Nevertheless, in his 1965 paper Moore, ever the visionary, identified a "system focus" as a further key contributor to increasing the power of electronics devices [4].

Today, "Heterogeneous Integration" (HI) has emerged as a popular term that describes the integration of separately manufactured components, each with a characteristic functionality, into an electronics assembly. The concept involves building complex systems with great interconnectivity from smaller units, based on the utilization of a broad set of materials, manufacturing techniques and packaging strategies. Today, HI is a commonly applied tool to optimize the design of SiPs (Figure 16) [5].

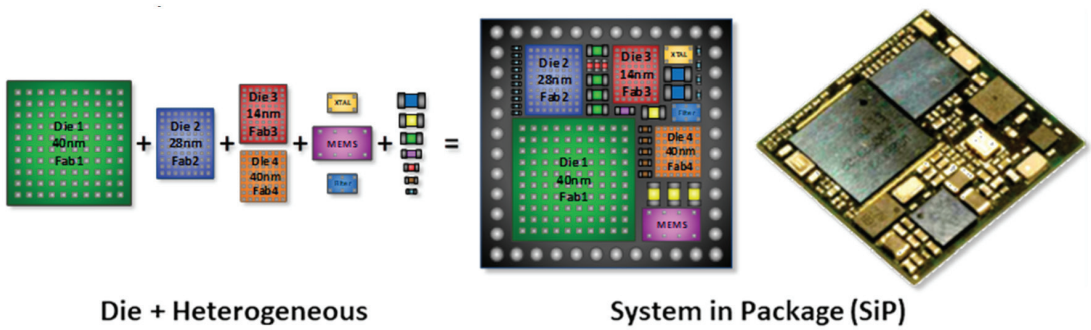

Figure 16. Heterogeneous Integration and its application in System in Package (SiP) [7].

The HI toolbox includes various bumping and interconnect standards, flex and mechanical assembly, 2.5D and 3D packaging, molding technologies, Wafer-Level Packaging (WLP), and different substrate and embedded technologies e.g., Semiconductor Embedded in Substrate (SESUB) or Embedded Active System Integration (a-EASI) (Figure 17). Additionally, shielding and HF-components, filters, sensors and actuators, power components, Micro-Electro-Mechanical Systems (MEMS) and optoelectronics should be mentioned in this context. A strongly emerging trend is the utilization of chiplets (Chapter 7.6).

HI may be more broadly defined as the link between chip fabrication and system integration. The Heterogeneous Integration Roadmap (HIR) views HI as "the integration of individually manufactured components into higher-level components to enhance functionality and improve overall operational characteristics" [6]. The concept and achievements of HI become apparent when one examines the progress in smartphone design in recent years. Modern phones are comprised of large sets of intricately interconnected components that are undergoing continual advancements in integration. These components include storage, RF modules or front-end modules (FEM), wireless modules, power management, and processing units (Figure 18). Additionally, the number of implemented sensors has continuously increased to strengthen the system's ability to interact with the user and the surrounding world. Cameras, accelerometers, gyroscopes, GPS, compass heading and microphones are typically incorporated, with most sensors being implemented as MEMS [7].

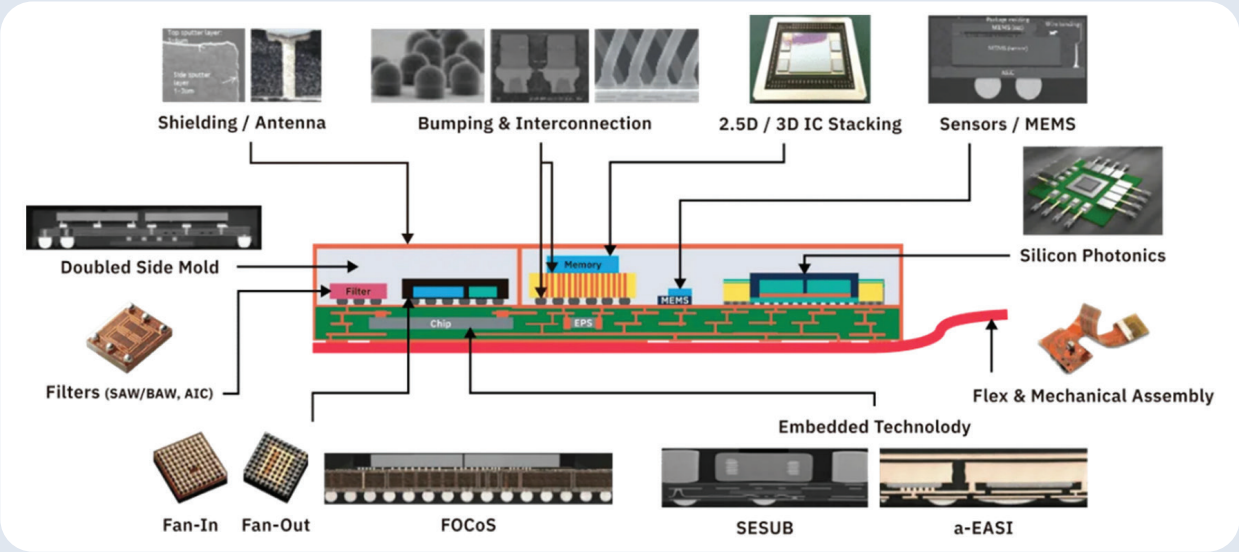

Figure 17. Technology building blocks for Heterogenous Integration.
(Source: ASE Global, https://ase.aseglobal.com/heterogeneous-integration/)

MEMS may be implemented as SoC solutions or, alternatively, as hybrid multi-chip solutions that use advanced packaging techniques. Such fabrication techniques represent an important area of HI. A 2D side-by-side integration of a MEMS and an IC is demonstrated in Figure 19. Interconnection is achieved by flip chip and wire bonding. The use of SiPs for MEMS integration led to a significantly reduced signal path length and more space-efficiency in comparison to PCB on-board approaches. Figure 20 illustrates

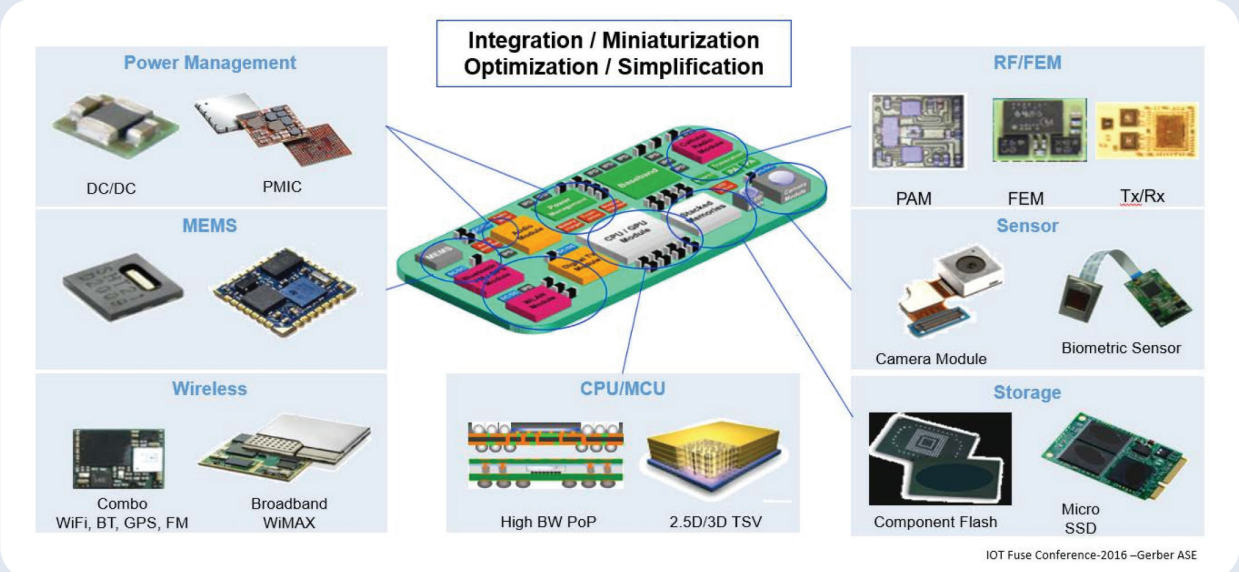

Figure 18. Common devices in a modern smartphone and their integration [7].

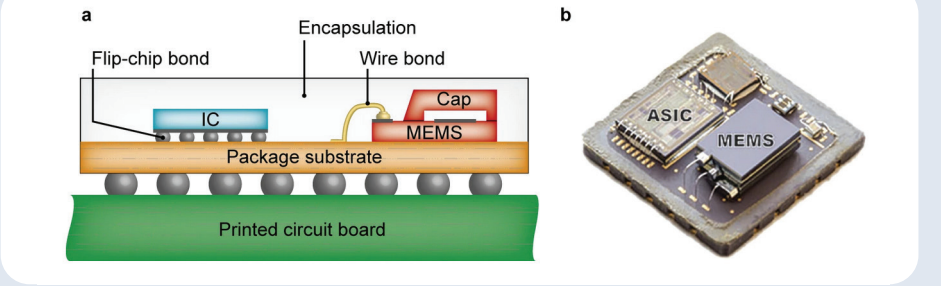

Figure 19. (a) 2D MEMS integration with IC and MEMS attached to a package substrate side-by-side. Flip chip and wire bonding are applied to create electrical interconnections. (b) STMicroelectronics LIS331DLH 3-axis accelerometer without encapsulant [8].

a package with 3D stacking of MEMS and IC. It is made of chips that are positioned on top of each other and interconnected via techniques like wire bond, through redistribution layers or via flip chip. The advantages of 3D stacking are increased compactness, shorter signal transduction pathways, and higher integration densities.

The utilization of a Chip Scale Package (CSP) for MEMS integration is shown in Figure 21. Here, MEMS and IC chips are encapsulated together with mounting space occupancy determined by the largest die. In the demonstrated package, the IC chip is attached to a larger, encapsulated MEMS device via face-to-face via flip chip bonding. This approach results in packages with dense functionality and interconnectivity. Vertical communication pathways are achieved by Through Silicon Vias (TSVs) or Through Glass Vias (TGVs) and solder balls [8].

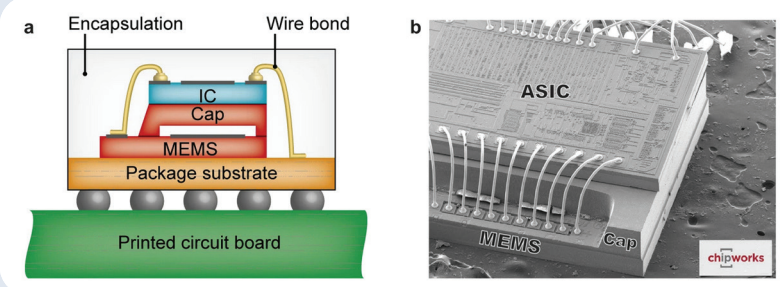

Figure 20. (a) SiP based MEMS integration using 3D stacking and wire bonded interconnects. (b) STMicroelectronics LIS331DLH 3-axis accelerometer without encapsulant [8].

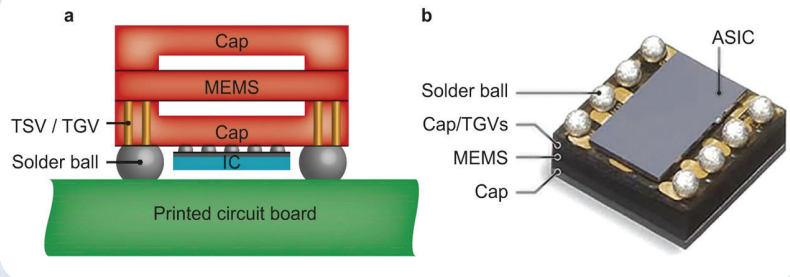

Figure 21. (a) Chip-scale package (CSP) in which MEMS and IC chips are connected via face-to-face flip chip bonding. (b) 3-Axis accelerometer (VTI, CMA 3000) based on chip-on-MEMS technology [8].

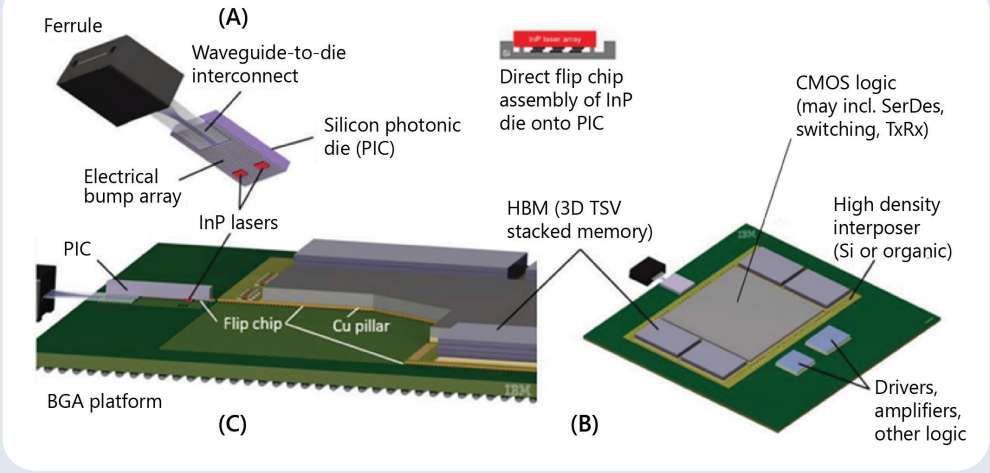

Figure 22. (A) PIC with laser die mounted by flip chip and edge-coupled waveguide. (B and C) HBM and logic mounted on a high-density interposer. (C) cut-away reveals copper pillar, BGA, flip chip architecture and optoelectronic interconnections [20].

Another field that is strongly shaped by HI is silicon photonics. Optoelectronic systems may contain processors, Application-Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), memory, passive components, and other functional elements in addition to the Photonic Integrated Circuit (PIC). Some units can be integrated into the photonic chip, whereas others must be part of the SiP. Figure 17 illustrates packaging concepts that can be utilized to integrate silicon photonic dies in an optoelectronic package. In such modules, the use of high-density interconnect (HDI) and advanced packaging techniques are preferred. A PIC equipped with waveguide array that enables effective photon transport into the die is shown in Figure 22A. Connection of the PIC to a BGA platform is via flip chip. In this build-up, the logic die and high-bandwidth memory (HBM) stacks are mounted directly onto a high-density interposer to optimize communications between logic, memory and PIC (Figure 22B and C). As an alternative to silicon interposers, organic HDI laminate materials can be used to lower costs [9].

Tohoku University has developed an optoelectronic chip module that can be utilized for signal-processing in an intelligent vehicle system. In its design, a 3D hybrid integration technology was applied, that allows the implementation of MEMS, photonics, CMOS Large-Scale Integration (LSI), Vertical Cavity Surface Emitting Laser (VCSEL), Photo Diode (PD), waveguides and memory (Figure 23). As the substrate, a silicon interposer equipped with microfluidic channels was used. Wireless transmission of data can take place via RF IC. Such multifunctional and compact sensor systems will find numerous applications in various fields and are a good example for the power of HI [10] [11].

HI is a versatile tool that can facilitate progress in a variety of fields and applications to yield unprecedented levels of performance. It holds the potential to shape the characteristics of future electronics and to be an important contributor in areas such as artificial intelligence (AI), 5G communication, consumer electronics and autonomous systems.

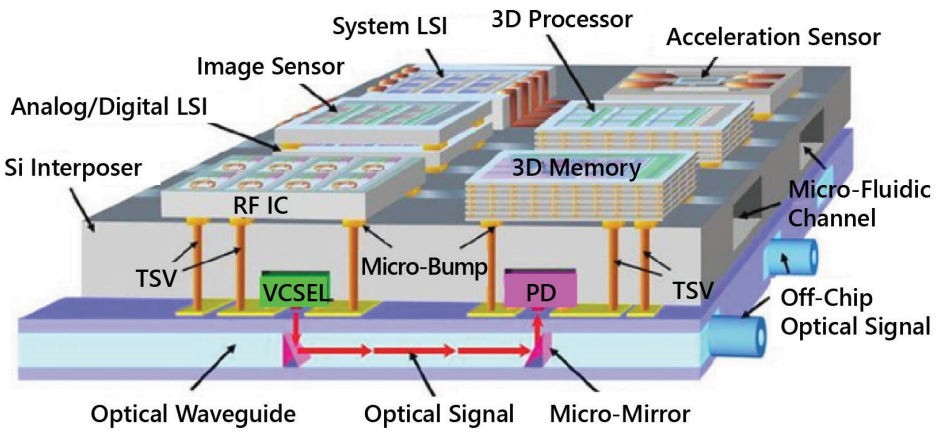

Figure 23. 3D heterogeneous integration allowing a smart sensor system that includes MEMS, sensors, and optoelectronics and can be used in an intelligent vehicle [10].

7.6 Chiplets

The market demand for faster and more powerful computing devices has historically progressed through the continued miniaturization of transistors and ICs. Simultaneously, however, dies often had to be larger to carry the huge number of transistors needed by modern computing devices. This increasing complexity of semiconductor manufacturing led to yield issues in the traditional SoC approach, as was discussed in Chapter 7.1. Splitting the functional units of a monolithic die into different single dies that can then be connected via a substrate evolved as a successful way to compensate for decreasing yields and increasing production costs (Figure 24). Over time the name "chiplets" emerged to describe dies having specific functionalities, often controlled by an I/O controller, that are resident on a substrate. Multiple dies that can be assembled onto a common substrate are denoted as Multi-Chip Module (MCM). Integration methods have been developed that allow efficient communication between these individual units. Advanced packaging technologies may be applied to integrate the components and to obtain an SiP (Chapter 7.3) or heterogeneous integration (Chapter 7.5). In this context, a variety of packaging technologies facilitate the necessary integration densities. Advanced interconnection architectures allow efficient communication between the chiplets with fast data transfer rates. Silicon interposers are often used as ideal substrates. Alternatively, Intel´s embedded multi-die interconnect bridge (Chapter 2.3.4) constitutes an economic way to integrate chiplets in a high-density framework directly onto an organic substrate. The bridge consists of silicon and is embedded into the organic substrate and can connect two neighboring dies (Figure 25).

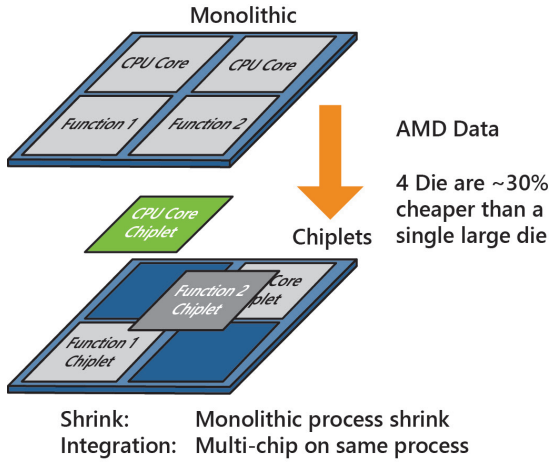

Figure 24. Schematic comparison of monolithic SoC and chiplets [18]. (Source: Open Compute Project)

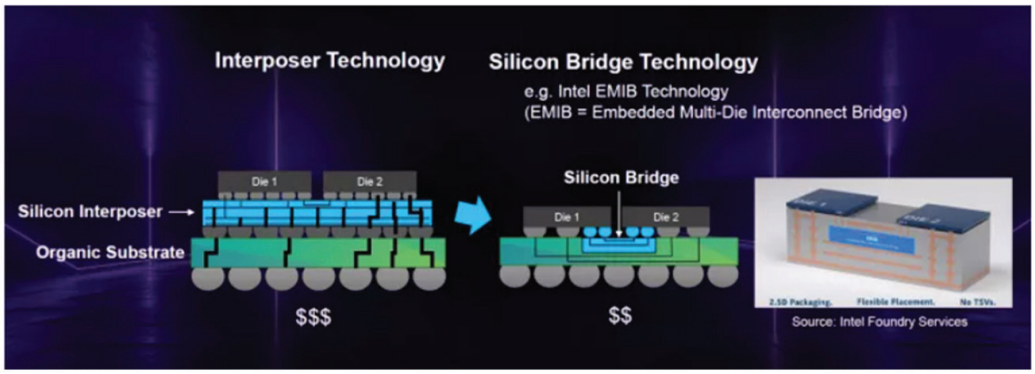

Figure 25. Schematic connection of dies via a silicon interposer or an embedded silicon bridge [19].

The chiplet approach offers numerous advantages over a SoC design, including the possibility to test every (smaller and cheaper) IC sub-unit with respect to its specified functionality. This fragmentation results in reduced production costs and higher overall production efficiency (Figure 2). Furthermore, the use of chiplets provides the opportunity to re-use successful die designs of previous ICs and, thereby, reduce R&D cost and time-to-market. Engineers have the option to combine and match dies from different suppliers, which can accelerate the optimization of each product in which specific chiplets have been tailored for specific tasks. In this context, IP protection and licensing of designs will become an additional and significant driver for the chiplet approach. Furthermore, chiplet integration allows different manufacturing processes of dies within the same package. The utilization of the most suitable fabrication technology for each die can reduce risks and simplify production. All these factors combine to yield a high flexibility in IC design and manufacturing from which the semiconductor industry strongly benefits. In recent years, the chiplet market has emerged and is rapidly growing. The Global Chiplets Market was valued at USD 5.3 Billion in 2024, and is expected to reach USD 42.8 Billion by 2029, rising at a CAGR of 41.90% [12].

The establishment of worldwide chiplet interface standards remains a major industry challenge that must be overcome. Such standards are necessary for exchangeability of dies designed by different companies. They are thus important cornerstones for the continued development of the chiplet market. Currently, Intel is working on a die-to-die interface standard UCIe (Universal Chiplet Interconnect express), which allows for an open ecosystem of chiplets from different manufacturers that are designed to cooperate in a multi-die system. Other consortia such as Bunch of Wires (BoW), OpenHBI, and OIF XSR are working on similar approaches. Standards for production will also have to be established, as will mounting and testing methods and capacities. IC planning will increasingly deal at the system level, requiring the co-design of the IC and housing. Furthermore, packaging technologies will have to adapt to the implementation of chiplets in SiPs.

In summary, chiplets have a high potential to strongly shape the future of the semiconductor industry as the modular approach provides valuable benefits in terms of design flexibility, performance, cost and shortening of development cycles.

7.7 MKS Products

MKS product offerings support the field of Advanced Packaging for various packaging architectures from 2.XD to 3.XD, including interposer types and interconnect technologies, as detailed in Chapter 2. Solutions for IC substrate manufacturing like via drilling, metallization, patterning, metal deposition, circuitization, and final finishing, are discussed in Chapter 4. Chapter 5 addresses MKS product offerings for flip chip packaging and emerging technologies for Flip Chip assembly. Chapter 6 covers Fan-In and Fan-Out Wafer and Panel Level Packaging, which require galvanic copper plating of RDL, Pad, and Pillar structures.

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Glossary

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5G	Fifth Generation Technology Standard for Cellular Communications
ABF	Ajinomoto's Build-up Film
AI	Artificial Intelligence
AiP	Antenna in Package
BGA	Ball Grid Array
C2	Chip Connection
C4	Controlled Collapse Chip Connection
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization
CoWoS	Chip-on-Wafer-on-Substrate
CPU	Central Processor Unit
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
D2W	Die to Wafer
DBHI	Direct Bonded Heterogeneous Integration
DIP	Dual In-line Package
EDA	Electronic Design Automation
eHDF	Embedded High Density Film
EMI/EMC	Electromagnetic Interference/Electromagnetic Compatibility
EMIB	Embedded Multi-Die Interconnect Bridge
ESD	Electrostatic Discharge
F2B	Face to Back
F2F	Face to Face
FC	Flip Chip
FCBGA	Flip Chip Ball Grid Array
FEM	Front End Module
FEOL	Front End Of Line
FIWLP	Fan-In Wafer Level Package
FLI	First Level Interconnect

FO	Fan-Out
FOCoS	Fan-Out Chip on Substrate
FOEB	Fan-Out Embedded Bridge
FO-EB	Fan-Out – Elevated Bridge
FOWLP	Fan-Out Wafer Level Package
Gbps	Gigabits per second
GPU	Graphics Processor Unit
HBM	High Bandwidth Memory
HDI	High Density Interconnect
HI	Heterogeneous Integration
Hi-Rel	High Reliability
HPC	High Performance Computing
HTCC	High Temperature Co-fired Ceramic
HVM	High Volume Manufacturing
IC	Integrated Circuit
IDM	Integrated Device Manufacturer
IEEE	Institute of Electrical Electronics Engineers
InFO	Integrated Fan-Out
InFO_AiP	Integrated Fan-Out Antenna in Package
InFO-LSI	Integrated Fan-Out Local Silicon Interconnect
I/O	Input/Output
IoT	Internet of Things
IRDS	International Roadmap for Devices and Systems
iTHOP	Integrated Thin Film Organic Package
ITRS	International Technology Roadmap for Semiconductors
KGD	Known Good Die
LGA	Land Grid Array
LFCSP	Lead Frame Chip Scale Package
L/S	Line/Space
LSI	Local Silicon Interconnect

LTCC	Low Temperature Co-fired Ceramic
MCM	Multi Chip Module
MM	More Moore
mSAP	Modified Semi-Additive Process
MSL	Moisture Sensitivity Level
MtM	More than Moore
NTRS	National Technology Roadmap for Semiconductors
OSAT	Outsourced Assembly and Test
PA	Power Amplifier
PCB	Printed Circuit Board
PGA	Pin Grid Array
PLCC	Plastic Leaded Chip Carrier
PoP	Package on Package
PQFP	Plastic Quad Flat Pack
PVD	Physical Vapor Deposition
QFN	Quad Flat Pack No Leads
QFP	Quad Flat Pack
RDL	Redistribution Layer
R/oS	RDL/Organic Substrate
RF	Radio Frequency
SAP	Semi Additive Process
SI	Signal Integrity
SiP	System-in-Package
SL-PCB	Substrate-Like Printed Circuit Board
SMT	Surface Mount Technology
SoC	System-on-Chip
SoIC	System on Integrated Circuit
SOIC	Small Outline Integrated Circuit
SOP	Small Outline Package
SRC	Semiconductor Research Corporation

SRC-MAPT	SRC Microelectronics and Advanced Packaging Technology Roadmap
SWaP-C	Size/Weight and Power Consumption and Cost
TCB	Thermal Compression Bonding
TMV	Through Mold Via
TSV	Through Silicon Via
TxV	Through Glass Via
UBM	Under Bump Metallization
uFOS	Ultra Fine Pitch Organic Substrate
W2W	Wafer to Wafer
WB	Wire Bonding
WLCSP	Wafer Level Chip Scale Package
WLP	Wafer Level Packaging

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